PRODUCT BRIEF

Intel® Cyclone® 10 GX FPGAs

2X Higher Performance at Up to Half the Cost[1]

Intel's Cyclone® 10 GX FPGAs are an optimized for high-performance applications in the low-end FPGA market segment.

Intel Cyclone 10 GX Advantages

- High-performance core fabric to support complex designs requiring complex intellectual property (IP) blocks
- 2X core performance over previous generations of Cyclone devices
- 1.4 Gbps LVDS I/O
- 1.866 Gbps DDR3/L EMIF support
- 12.5 Gbps transceivers
- Up to 134 GFLOPs of hardened IEEE 754 compliant single-precision floating-point digital signal processing (DSP) throughput
- Automotive, Industrial, and Extended Commercial grade devices
- Complementary optimized and validated Intel® Enpirion® power solutions

Synergy with Intel CPUs

- **High-level design flow** – OpenCL™ support enables software engineers to easily access the high performance offered by Intel FPGAs
- **Solutions** – Common IP cores and joint development platforms for maximum synergy with Intel CPUs and FPGAs

Intel Cyclone 10 GX Target Markets

These capabilities make the Intel Cyclone 10 GX devices ideal for solving the design challenges in next generation systems, in high-end Industrial, Automotive, and Pro-Av systems including computing, storage, military, medical, and test & measurement.

Notes:
1. When compared to previous generation Cyclone FPGAs list price.
2. OpenCL and the OpenCL logo are trademarks of Apple Inc., and used by permission by Khronos.

Intel Cyclone 10 GX FPGAs Product Table

PRODUCT LINE		10CX085	10CX105	10CX150	10CX220
Resources	Logic elements (LEs)[1]	85,000	104,000	150,000	220,000
	Adaptive logic modules (ALMs)	31,000	38,000	54,770	80,330
	ALM registers	124,000	152,000	219,080	321,320
	M20K memory blocks	291	382	475	587
	M20K memory size (Kb)	5,820	7,640	9,500	11,740
	MLAB memory size (Kb)	653	799	1,152	1,690
	Variable-precision DSP blocks	84	125	156	192
	18 x 19 multipliers	168	250	312	384
	Peak fixed-point peformance (GMACS)[2]	151	225	281	346
	Peak floating-point performance (GFLOPS)[3]	59	88	109	134
I/O and Architectural Features	Global clock networks	32	32	32	32
	Regional clocks	8	8	8	8
	Maximum user I/O pins	192	284	284	284
	Maximum LVDS pairs 1.4 Gbps (RX or TX)	72	118	118	118
	Maximum transceiver count (12.5 Gbps)	6	12	12	12
	Maximum 3V I/O pins	48	48	48	48
	PCI Express* (PCIe*) hard IP blocks (Gen 2 x4)[4]	1	1	1	1
	Memory devices supported	DDR3, DDR3L, LPDDR3			
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, 3V I/O Count, LVDS Pairs, Total Transceiver count[5]					
U484 pin (19 mm x 19 mm, 0.8 mm pitch)		188, 48, 70, 6	188, 48, 70, 6	188, 48, 70, 6	188, 48, 70, 6
F672 pin (27 mm x 27 mm, 1.0 mm pitch)		192, 48, 72, 6	236, 48, 94, 10	236, 48, 94, 10	236, 48, 94, 10
F780 pin (29 mm x 29 mm, 1.0 mm pitch)			284, 48, 118, 12	284, 48, 118, 12	284, 48, 118, 12

Notes:
1. LE counts valid in comparing across Intel devices, and are conservative vs. competing FPGAs.
2. Fixed-point performance assumes the use of pre-adder.
3. Floating-point performance is IEEE-754 compliant single-precision.
4. Hard PCIe IP core x2 in U484 package
5. Each LVDS pair can be configured as either a differential input or differential output.
6. A subset of pins for each package are used for high-voltage 3.0 V and 2.5 V interfaces.
7. All data is correct at the time of printing and may be subject to change without prior notice. For the latest information, please visit www.altera.com.

284,48,118,12 Numbers indicate GPIO count, 3V I/O count, LVDS pairs, total transceiver count.

Indicates pin migration path.

For more information, visit www.altera.com/cyclone10gx.

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