Revision 1.0.0
PCN Issue Date: 05/28/2021

# PROCESS CHANGE NOTIFICATION

# PCN2124

## Intel MAX® 10 WLCSP RDL/Bump Site Transfer and Package Appearance Change

## Change Description:

Intel® is announcing a change to the RDL/Bump site and package appearance on selected Intel MAX® 10 products in Wafer Level Chip Scale Package (WLCSP). The change will not impact fit, function, quality and reliability, and the post-change products will meet existing electrical and mechanical specifications.

Table 1: Change Details

| | Change From | Change To |
|---|---|---|
| RDL and Bump Site/Location | **Site:** Taiwan Semiconductor Manufacturing Company (TSMC)<br><br>**Location:** No. 6, Li-Hsin Rd. 6th HsinChu Science Park HsinChu, Taiwan | **Site:** Advanced Semiconductor Engineering, Inc (ASEK)<br><br>**Location:** 26, Chin 3rd Rd., Nanzih Dist, Kaohsiung, 811, Taiwan |
| Package Construction & Appearance | WLCSP- UFI (UBM-free Interconnect) solution<br><br>Black mold compound with exposed top side of solder balls | Standard WLCSP<br><br>Design pattern on the active area and entire solder balls are visible. |
| Package Outline Drawing (POD) | Only A1 & A2 dimensions have changed, overall A (height) is the same. See table 3 below. | |

Table 2: Package Appearance

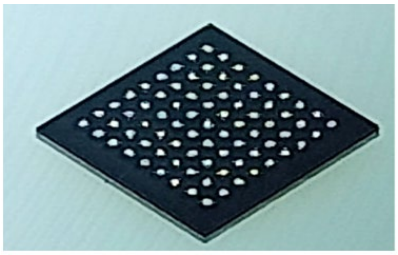
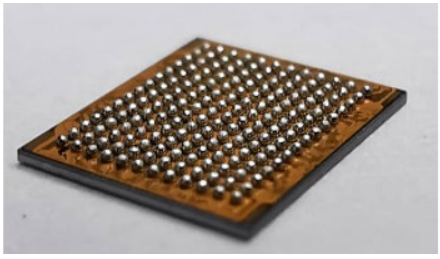
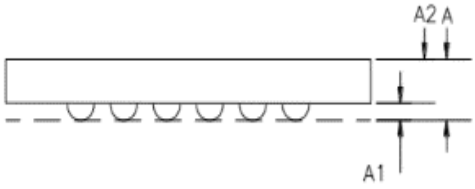
| From: UFI (TSMC) | To: WLCSP(ASEK) |
|---|---|
|  Top View |  Top View |
|  Bottom View |  Bottom View |

Table 3: Package Outline Drawing (POD)

| | Existing POD (Change From) | POD after Change (Change To) | Comments/ Notes |
|---|---|---|---|
| A(Nom) | 0.46 mm | 0.46mm | No change |
| A1 (Nom) | 0.13 mm | 0.20 mm | |
| A2 (Nom) | 0.33 mm | 0.26 mm | |
| D | 10M08 = 4.496 mm BSC<br>10M02 = 3.396 mm BSC | 10M08 = 4.496 mm BSC<br>10M02 = 3.396 mm BSC | No Change |
| E | 10M08 = 4.377 mm BSC<br>10M02 = 3.466 mm BSC | 10M08 = 4.377 mm BSC<br>10M02 = 3.466 mm BSC | No Change |
|  | | | |

## Products Affected:

Table 4

| Product Family | Part Number |
|---|---|
| MAX 10 | 10M02DCV36C7G |
| | 10M02DCV36I7G |
| | 10M02DCV36C8G |
| | 10M08DCV81C7G |
| | 10M08DFV81I7G |
| | 10M08DFV81C7G |
| | 10M08DFV81C8G |
| | 10M08DCV81C8G |
| | 10M08DCV81I7G |

## Recommended Action

Customers are requested to:

1. Acknowledge receipt of this notification.
2. Review and inform us, at the earliest convenience, of any questions or concerns regarding this change.

Please refer to the "Product Transition Dates" for the key milestones.

Upon implementation, Intel will ship either pre-change or post-change materials.

## Product Transition Dates:

Customers are requested to take note of the key dates shown in the table below.

Table 5: Key Dates

| *Milestone* | *Date* |
|---|---|
| Last date to acknowledge receipt of this notification[1] | July 12, 2021 |
| Earliest change implementation | November 1, 2021 |

Note 1: J-STD-046, section 3.2.3.1b, stipulates that lack of acknowledgement of the PCN within 30 days constitutes acceptance of the change.

## Reason for Change:

Supply continuity since existing site has discontinued UFI (UBM-free Interconnect) packaging.

## Impact and Benefit of Change:

There is no impact to fit, function, quality, and reliability of the product. The products will meet existing electrical and mechanical specifications.

## Qualification Data:

Qualification testing was performed to further evaluate the quality and reliability performance of ASEK for the products specific to this PCN.

### Table 6A: Component Level Reliability Test Data

- All tests passed with zero failures

| Test | Time point | Conditions | Sample Size | Lots# H3417 | Lots# H3418 | Lots# H3419 |
|---|---|---|---|---|---|---|
| Unbiased Highly Accelerated Stress Test (uHAST) | 192hrs | 130°C / 85%RH | 135 | 0/45 | 0/45 | 0/45 |
| Highly Accelerated Stress Test (HAST) | 192hrs | 130°C / 85%RH with bias | 135 | 0/45 | 0/45 | 0/45 |
| Temperature Cycle Test (TCB) | 1200 Cycles | -55°C /125°C | 135 | 0/45 | 0/45 | 0/45 |
| High Temp Storage (Bake) | 1500hrs | 150°C | 135 | 0/45 | 0/45 | 0/45 |

Note 1: Preconditioning performed according to J-STD-020, MSL 1@ 260C reflow
Note 2: Qualification testing and sample size based on standard J-STD-020 requirements

Table 6B: Board Level Reliability Test Data

| Test | Condition | Sample Size (Units) | Results |
|---|---|---|---|
| Temp Cycle (reference to IPC-9701) | TCT -40/125°C (1100cycles) | 35 | Pass |
| Drop test (reference to JESD22-B111) | Condition B (1500G,0.5ms) 30 drops | 30 | Pass |
| Bend test (reference to JESD22-B113) | 200K cycles | 30 | Pass |

## Contact

For more information, please contact Sales in your region, or submit a Service Request at the My Intel support page.

## Customer Notifications Subscription

Customers that have subscribed to Intel Programmable solutions Group (PSG) customer notification mailing list will receive the PCN document automatically via email.

If you would like to receive customer notifications by email, please subscribe to our customer notification mailing list at:
https://www.intel.com/content/www/us/en/programmable/my-intel/mal-emailsub/technical-updates.html

*Intel references J-STD-046 guidelines for PCN.*
*In accordance with J-STD-046, this change is deemed acceptable to the customer if no acknowledgement is received within 30 days from date of notification.*

## Revision History

| Date | Rev | Description |
|---|---|---|
| 05/28/2021 | 1.0.0 | Initial Release |