

PROCESS CHANGE NOTIFICATION PCN0701 EPCS16SI16N Process Change

Change Description

Altera's EPCS16SI16N Serial Configuration Device will be transitioned to a 0.11-micron process from the current 0.15-micron process. The functionality and AC/DC parameters described in the Serial Configuration Devices Data Sheet chapter of the Altera® Configuration Handbook will remain unchanged.

The device qualification data is in Appendix 1 of this document. The device characterization data is available upon request.

Reason for Change

The change is being made to ensure long-term customer support by increasing production capacity and reducing lead times.

Products Affected

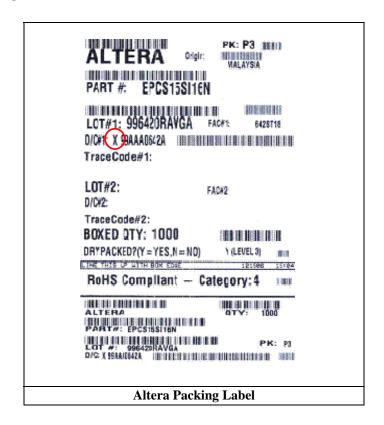
EPCS16SI16N

Product Traceability and Transition Date

Altera will begin the transition to the 0.11-micron process for EPCS16SI16N devices on April 16, 2007. After this date, customers may receive devices from either the 0.15-micron, or 0.11-micron processes.

The EPCS16SI16N devices with 0.11-micron process will be identifiable from the barcode label on the shipping boxes as shown in Figure 1. For 0.11-micron process devices, the numeral 4 will appear in the date code field, instead of the letter X shown circled in red in Figure 1.

Figure 1. Shipping Box Barcode Label



Process	Date Code Prefix
0.15 μm	X
0.11 μm	4

Contacts

For more information on this process change notification, please contact Altera Customer Quality support at customer-quality@altera.com.

In accordance with JESD46-B, this change is deemed acceptable to the customer if no acknowledgement is received within 30 days from this notification.

Revision History

[Rev	Date Released	Description of Change	
ſ	0	12-Jan-07	Initial Release	

Appendix 1 – EPCS16SI16N Qualification Data (Page 1 of 2)

Sub- group	Test Procedure	Method	Test Conditions	Lot 1	Lot 2	Lot 3
1	High Temperature Operating Life	JEDEC-JESD22 A108	150°C, 4.2V - 504 hrs - 1,008 hrs	0/80 0/80	0/80 0/80	0/80 0/80
2	Low Temperature Operating Life	Mil Std 883 Method 1005			_	_
3	High Temperature Bake	JEDEC-JESD22 A103	200°C - 504 hrs - 1,008 hrs	0/80 0/80	0/80 0/80	0/80 0/80
4	Erase/Write Cycles and Bake	Internal	10,000 E/W cycles + Bake 200°C, 48 hrs	0/80	0/80	0/80
5	Electrostatic Discharge	JEDEC-JESD22- A114	Human body model: $1.5 k\Omega$ 100pF Machine Model: $0 k\Omega$ 200pF	> 2,000V > 200V	> 2,000V > 200V	> 2,000V > 200V
6	Latch-Up	Jedec EIA/JESD78	at 150°C, Class A, Level II	Pass	Pass	Pass

Appendix 1 – EPCS16SI16N Qualification Data (Page 2 of 2)

Sub- group	Test Procedure	Method	Test Conditions	Lot 1
1	Preconditioning	AEC - Q100 - J-STD-020	Level 3	0/345
2	High Temperature Bake	AEC - Q100 - JA 103	150°C - 504 hrs - 1,008 hrs	0/80 ⁽¹⁾ 0/80 ⁽¹⁾
3	Temperature Cycling	AEC - Q100 - JA 104	-65 / +150°C - 500 cycles - 1,000 cycles	0/80 0/80
4	Pressure Pot	AEC - Q100 - JA 102	121°C, 2Atm, 100%RH - 96 hrs - 168 hrs	0/80 0/80
5	Thermal Shocks	Jedec-A106B	–55 / +125°C 200 shocks	0/25
6	Temperature and Humidity Biased	AEC - Q100 - JA 101	85°C, 85%RH, 3.6V - 504 hrs - 1,008 hrs	0/80 0/80
7	Electrostatic Discharge	AEC - Q100 - 011	Charge Device Model (Field Induced Charge CDM)	_

^{1.} Results not available at this time.