Revision 1.0.0
ADV Issue Date: 03/12/2021

CUSTOMER ADVISORY
ADV2107
Intel® Stratix® 10 Device L/H Tile PCIe Update

Description:

Intel® is notifying customers of an important update to Intel® Stratix® 10 device L and H-Tile using Intel Stratix 10 Hard IP for PCI Express*. Refer to Table 1 for details and link to KDB article with recommendations and further actions.

Table 1

Update Details	Impacted software versions	KDB Article
• Host system receives corrupted data without LCRC error or Completion Time Out error on a PCIe* Gen 3 x16 link that uses the Intel Stratix 10 Hard IP for PCI Express* in Intel Stratix 10 L-Tile and H-Tile devices. • IP impacted are Avalon-MM Stratix 10 Hard IP for PCI Express, and Avalon-ST Stratix 10 Hard IP for PCI Express • Permanent fix implemented in Intel® Quartus® Prime Pro ver 20.4 and above.	All Intel Quartus Prime Pro versions prior to 20.4	Why does the host system receive corrupted data without LCRC error or Completion Time Out error on a PCIe* Gen 3 x16 link that uses the Intel® Stratix® 10 Hard IP for PCI Express* in the Intel® Stratix® 10 L-Tile and H-Tile devices ?

Products Affected:

All Intel Stratix 10 GX, Intel Stratix 10 MX, Intel Stratix 10 SX, Intel Stratix 10 TX, Intel Stratix 10 NX Devices.

The list of affected part numbers (OPNs) can be downloaded in Excel form:
https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/adv2107-opn-list.xlsx

Change Implementation:

The permanent fix for the issue described in this customer advisory is available now. Refer to the relevant KDB link in Table 1.

Contact:

For more information, please contact your local Sales representative, or submit a question or request at the My Intel support page, log-in via:
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Revision History

Date	Rev	Description
03/12/2021	1.0.0	Initial Release