Revision 1.0.0
ADV Issue Date: 01/15/2021

CUSTOMER ADVISORY

ADV2101

Intel® Stratix® 10 Device Datasheet Update

Description:

Intel® is notifying customers of datasheet document updates for Intel Stratix 10 devices.

Following is a summary of the important changes made to the Intel Stratix 10 device datasheet:

- Updated the following tables under 'Transceiver Performance for Intel Stratix 10 DX P-Tile Devices': Table 73 (P-Tile PLLA Performance), Table 74 (P-Tile PLLB Performance), Table 75 (P-Tile Reference Clock Specifications), Table 76 (P-Tile Transmitter Specifications).

- Updated Common Mode Voltage (V_{CM}) [when Internal AC Coupling is used], and Absolute Voltage Maximum (V_{MAX}) [when Internal AC Coupling is used] values in Table 71 (E-Tile Receiver Specifications).

- Updated HBM2 DRAM IP support to include new Intel Stratix 10 device families.

Here is the complete list of updates to the Intel Stratix 10 device datasheet:

- Added Intel Stratix 10 NX and DX 2100 devices in the following sections:
  - Absolute Maximum Ratings for Intel Stratix 10 Devices table
  - Recommended Operating Conditions for Intel Stratix 10 Devices table
  - Performance Specifications of the HBM2 Interface in Intel Stratix 10 MX, NX, and SD 2100 Devices table
  - HBM2 Interface Performance section
- Updated the E-Tile Receiver Specifications table.
  - Updated the Absolute V_{MAX} and V_{CM} specifications.

    - Updated the note to V_{CM}.
    - Added note to Absolute V_{MAX} and V_{ID} (diff p-p).
- Updated the P-Tile PLLA Performance table.
    - Added PLL bandwidth (BWTX-PKG_PLL1) and PLL peaking (PKGTX-PLL1) specifications for PCIe 5.0 GT/s.
    - Updated PLL peaking (PKGTX-PLL2) specifications.
    - Added note on PLL bandwidth and PLL peaking.
- Updated the P-Tile PLLB Performance table.
    - Added PLL bandwidth (BWTX-PKG_PLL2) and PLL peaking (PKGTX-PLL2) specifications.
    - Added note on PLL bandwidth and PLL peaking.
    - Updated the spread-spectrum downspread, absolute V_{MAX}, and absolute V_{MIN} specifications in the P-Tile Reference Clock Specifications table.
    - Updated the differential peak-to-peak voltage for full swing specifications in the P-Tile Transmitter Specifications table.
    - Removed V_{ICM} (AC coupled) specifications from the P-Tile Receiver Specifications table.

    The history of changes is summarized in the Documentation Revision History table at the last section of the datasheet.

The Intel Stratix 10 device datasheet can be found here:
https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/stratix-10/s10_datasheet.pdf

Recommended Actions:

Customers are requested to take note of the changes and determine the impact on their designs.

For questions or support, please contact your local Field Applications Engineer (FAE), or submit a question or request at the My Intel support page, log-in via:
https://www.intel.com/content/www/us/en/my-intel/fpga-sign-in.html

Products Affected:

All Intel Stratix 10 devices

The list of affected part numbers (OPNs) can be downloaded in Excel form:
https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/adv2101-opn-list.xlsx

Reason for Change:

Addition and clarification of certain device specifications based on latest available data and characterization. There is no change to the Intel Stratix 10 device silicon and materials.

Change Implementation:

Table 1

Milestone	Availability
Availability of Intel Stratix 10 device datasheet update	Now

Contact:

For more information, please contact your local Field Applications Engineer (FAE), or submit a question or request at the My Intel support page, log-in via:
https://www.intel.com/content/www/us/en/my-intel/fpga-sign-in.html

Customer Notifications Subscription:

Customers that subscribe to the Intel FPGA customer notification mailing list will receive the notifications automatically via email.

If you would like to receive Intel FPGA customer notifications by email, you can register to the Intel FPGA program and set up your subscription at:
https://www.intel.com/content/www/us/en/programmable/my-intel/malemailsub/technical-updates.html

Revision History

Date	Rev	Description
01/15/2021	1.0.0	Initial Release