



CUSTOMER ADVISORY

ADV2034

Intel® Stratix® 10 Device Family Pin Connection Guidelines Update

Description:

Intel® is notifying customers of an important update to the Intel® Stratix® 10 Device Family Pin Connection Guidelines document.

Following are the major changes in the latest revision:

- Updated the regulator sharing for VCCM_WORD_ (BL, TL) from share to isolate in the Power Supply Sharing Guidelines for Intel Stratix 10 MX and DX parts
- Updated the notes for VCCM_WORD_ (BL, TL) in the Power Supply Sharing Guidelines tables for Intel Stratix 10 MX and DX parts
- Updated the notes for VCCIO_SDM, VCCIO, and VCCIO3V in the Power Supply Sharing Guidelines tables for the Intel Stratix 10 MX, DX and TX parts
- Removed the notes for VCCIO, and VCCIO3V in the example Power Supply Sharing Guidelines figures for the Intel Stratix 10 MX and TX parts

Please refer to the revision history of the Intel Stratix 10 Pin Connection Guideline for the complete list of changes:

Link: <https://www.intel.com/content/www/us/en/programmable/documentation/lod1484643014646.html>

Recommended Actions:

Customers are requested to take note of the changes and ensure that they are following the updated pin connection guidelines.

For questions or support, please contact your local Field Applications Engineer (FAE), or submit a question or request at the My Intel support page, log-in via:

<https://www.intel.com/content/www/us/en/my-intel/fpga-sign-in.html>

Products Affected:

All Intel Stratix 10 devices.

The list of affected part numbers (OPNs) can be downloaded in Excel form:

<https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/adv2034-opn-list.xlsx>

Change Implementation:

Table 1

Milestone	Availability
Availability of Intel® Stratix® 10 Device Family Pin Connection Guidelines Update	Now

Contact:

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Customer Notifications Subscription:

Customers that subscribe to the Intel FPGA customer notification mailing list will receive the notifications automatically via email.

If you would like to receive Intel FPGA customer notifications by email, you can register to the Intel FPGA program and set up your subscription at:

<https://www.intel.com/content/www/us/en/programmable/my-intel/malemailsub/technical-updates.html>

Revision History

Date	Rev	Description
10/30/2020	1.0.0	Initial Release

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