



# CUSTOMER ADVISORY

## ADV2004

### Intel® Cyclone® 10 Device EDCRC and Partial Reconfiguration Update

#### Description:

Intel® is notifying customers of potential problems in selected Intel Cyclone® 10 devices when Error Detection Cyclic Redundancy Check (EDCRC) is On or Partial Reconfiguration (PR) is used.

Failure signature: Unexpected output from Flipflop/DSP/M20k/LUTRAM when EDCRC or PR is used. The problems will not occur if EDCRC or PR is turned-off.

**Table 1**

<b>Cause 1:</b>	<b>Recommended Action:</b>
Functional failure if clock components (Flipflop/DSP/M20k/LUTRAM) are placed in LAB row Y59, with EDCRC On or PR enabled.	Implement software fix in Intel Quartus® Prime software. For more details on the software fix refer to the following Knowledge Database via this link: <a href="https://www.intel.com/content/altera-www/global/en_us/index/support/support-resources/knowledge-base/component/2019/is-there-a-problem-with-intel--fpga-when-flipflop-dsp-m20k-lutra.html">https://www.intel.com/content/altera-www/global/en_us/index/support/support-resources/knowledge-base/component/2019/is-there-a-problem-with-intel--fpga-when-flipflop-dsp-m20k-lutra.html</a>
<b>Cause 2:</b>	<b>Recommended Action:</b>
Functional failure if clock components (Flipflop/DSP/M20k/LUTRAM) are placed in a random LAB row, with EDCRC On or PR enabled. This is	The optimized VCCHG value will be implemented on parts with datecode 2025 (Year 2020; WW25) and onwards.  For parts before datecode 2025(Year 2020; WW25), there is no action required. Customer

caused by unoptimized internal voltage VCCHG value in test.	failure rate has been assessed to be very low (~20dppm).
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For questions or support, please contact your local Field Applications Engineer (FAE) or submit a service request in the [My Intel](#) support page.

### Products Affected:

All part numbers for the device densities listed below per product family.

Product Family	Device Density
Cyclone 10 GX	GX085/GX105/GX150/GX220

The list of affected part numbers (OPNs) can be downloaded in Excel form:

<https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/adv2004-opn-list.xlsx>

### Reason for Change:

Due to potential problems discovered in selected Intel Cyclone 10 devices using the EDCRC/PR feature, the above update was needed to help customers mitigate it. There is no change to the Intel Cyclone 10 device silicon and materials.

### Change Implementation:

Milestone	Availability
Availability of error message in Intel Quartus Prime software version 18.1.1 and above, if EDCRC and/or PR usage is detected without implementing software fix. Refer to the following KDB link for more details on the error message. <a href="https://www.intel.com/content/altera-www/global/en_us/index/support/support-resources/knowledge-base/component/2019/is-there-a-problem-with-intel--fpga-when-flipflop-dsp-m20k-lutra.html">https://www.intel.com/content/altera-www/global/en_us/index/support/support-resources/knowledge-base/component/2019/is-there-a-problem-with-intel--fpga-when-flipflop-dsp-m20k-lutra.html</a>	Now
Availability of optimized internal voltage VCCHG fix in affected Intel Cyclone 10 devices	Refer Table 1: Cause 2

## Contact:

For more information, please contact your local Field Applications Engineer (FAE) or submit a Service Request at the [My Intel](#) support page.

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<https://www.intel.com/content/www/us/en/programmable/my-intel/mal-emailsub/technical-updates.html>

## Revision History:

Date	Rev	Description
01/10/2020	1.0.0	Initial Release

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