Revision 1.0.0
ADV Issue Date: 1/25/2019
Rev 1.1.0 Date: 4/26/2019

CUSTOMER ADVISORY

ADV1832

Datasheet Update for Arria®V Devices

This is not a new ADV issuance. This is an update to ADV1832; please see the revision history table for information specific to this update

Change Description:

Intel Programmable Solutions Group ("Intel PSG", formerly Altera) is notifying customers of a documentation update for Arria V devices. The minimum Data Hold time (t_{DH}) timing specification for Active Serial (AS) configuration scheme has been updated.

Table 1: Minimum t_{DH} Specification

Speed Grade	Change From	Change To[1]	
		Arria V GZ Devices	All Other Arria V Devices
-3	0ns	3.7ns	1.7ns
-4	0ns	3.9ns	2.0ns
-5	0ns	N/A	2.3ns
-6	0ns	N/A	2.6ns

Note 1: Applies to Commercial and Industrial grade

The t_{DH} spec is stipulated in Table1-68 and Table 2-58 of the datasheet. Please review the revision history for all other updates to the datasheet. The Arria V device datasheet can be found here:
https://www.intel.com/content/www/us/en/programmable/documentation/sam1421821250281.html

Recommended Action:

Customers should review their board design against the updated Arria V minimum t_{DH} spec, otherwise configuration may fail.

Customers can calculate the hold time required for Active Serial configuration scheme, as mentioned in the 'Evaluating Data Setup and Hold Timing Slack' section of AN822 to evaluate the hold time slack on the board. AN822 can be found here:

https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/an/an822.pdf

For any additional questions, please contact your local Field Applications Engineer (FAE) or submit a Service Request at the My Intel support page.

Products Affected:

All Arria V and Arria V SoC Devices

The list of affected OPNs can be downloaded in Excel form:
https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/pcn/adv1832-opn-list.xlsx

Reason for Change:

It is necessary to update the datasheet with the new minimum t_{DH} spec, as the previous spec was determined to be inaccurate. There is no change to the Arria V product silicon and materials.

Change Implementation

Table 2

Milestone	***Date***
Availability of Arria V Datasheet Update	Now

Contact

For more information, please contact your local Field Applications Engineer (FAE) or submit a Service Request at the My Intel support page.

Customer Notifications Subscription

Customers that have subscribed to Intel PSG's customer notification mailing list will receive the ADV document automatically via email.

If you would like to receive customer notifications by email, please subscribe to our customer notification mailing list at:
https://www.intel.com/content/www/us/en/programmable/my-intel/mal-emailsub/technical-updates.html

Revision History

Date	Rev	Description
01/25/2019	1.0.0	Initial Release
04/26/2019	1.1.0	Update Minimum t_{DH} Specification for All Other Arria V Devices (Table 1) • Speed Grade -5: Change from 2.6ns to 2.3ns • Speed Grade -6: Change from 3.4ns to 2.6ns