

CUSTOMER ADVISORY ADV1007

ADDITIONAL BUMP LINE FOR ALTERA'S FLIPCHIP DEVICES

Change Description

Altera will be introducing TSMC BP-II (Tainan, Taiwan) as an additional bump line for Altera® devices. The bump attach process is currently performed at the TSMC BP-I (Hsinchu, Taiwan) location.

Recommended Action

No action is recommended as a result of this change. The equipment set used in BP-II is identical to the equipment used in BP-I.

This change does not affect the form, fit, or function as defined in Altera's Data Sheet and is backwards compatible with existing devices.

Reason for Change

This change is being implemented to improve manufacturing efficiency and to better support long-term demand for the affected products. This also supports Altera's supply-chain risk-mitigation strategy by establishing the capability to produce equivalent product from multiple qualified locations.

Products Affected

The additional BP-II bump line will be utilized for all Altera flip chip devices.

Product Traceability and Transition Dates

The additional bump line will become available at the end of December 2010. Customers may receive affected products beginning with a date-code marking of 1049 or later (See Figure 1). The 1049 date-code marking is the earliest date that the new material may be used for any of the affected products.

Figure 1: Date-code Marking



Altera Date-code Marking Format

A XβZαα**1049**T

Qualification Data

The reliability results below support the BP-II bump line qualification (See Table 1).

Table 1: Summary of Representative Qualification Data

| Product Family | Representative Product | Representative Packages | Qualification Test | Readout | Results |
|---|------------------------|-------------------------|--|----------|---------|
|  | EP1S80 | F1020 | High Temp Bake 150°C | 1000 hrs | 0/ 17 |
| | | | PCL 3 + Unbiased HAST 130°C / 85% RH | 96 hrs | 0/ 25 |
| | | | PCL 3 + Temp Cycle "B" (-55°C to 125°C) | 1000 cyc | 0/ 25 |
| | | | PCL 3 + Temp Humidity Bias (85°C/85%RH) | 1000 hrs | 0/ 25 |
| | | | Lifetest @ 125°C | 1000 hrs | 0/ 25 |
|  | EP3SL150 | F1152 | High Temp Bake 150°C | 1000 hrs | 0/ 23 |
| | | | PCL 3 + Unbiased HAST 130°C / 85% RH | 96 hrs | 0/ 25 |
| | | | PCL 3 + Temp Cycle "B" (-55°C to 125°C) | 1000 cyc | 0/ 25 |
| | | | PCL 3 + Temp Humidity Bias (85°C/85%RH) | 1000 hrs | 0/ 25 |
| | | | Lifetest @ 125°C | 1000 hrs | 0/ 25 |

Note: Pre Conditioning Level 3 performed @ 260°C

Contact

For more information, please contact Altera Technical Support by submitting a Service Request at Altera's [mySupport](#) website.

Customer Notifications Subscription

Customers that have subscribed to Altera's customer notification mailing list will receive updates automatically via email.

If you would like to receive customer notifications by e-mail, please subscribe to our customer notification mailing list at <https://www.altera.com/subscriptions/email/signup/eml-index.jsp>

Revision History

| Date | Rev | Description |
|------------|-------|---|
| 12/13/2010 | 1.0.0 | Initial Release |
| 01/07/2011 | 1.0.1 | Updated title. Changed "FPGA" to "FLIPCHIP" |

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