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1. Overview

This document describes the hardware features of the Stratix® V GT transceiver signal integrity development board, including the detailed pin-out and component reference information required to create custom FPGA designs that interface with all components of the board.

General Description

The Transceiver Signal Integrity Development Kit, Stratix V GT Edition, allows you to evaluate the performance of the Stratix V GT FPGA which is optimized for high-performance and high-bandwidth applications with integrated transceivers supporting backplane, chip-to-chip, and chip-to-module operation.

For more information on the following topics, refer to the respective documents:

- Setting up the development board and using the included software, refer to the Transceiver Signal Integrity Development Kit, Stratix V GT Edition User Guide.
- Stratix V device family, refer to the Stratix V Device Handbook.

Board Component Blocks

The Stratix V GT transceiver signal integrity development board provides a hardware platform for evaluating the performance and signal integrity features of the Altera® Stratix V GT device. The development board features the following major component blocks:

- Altera Stratix V GT FPGA (5SGTMC7K3F40C2) in a 1517-pin FineLine BGA package
  - 622,000 LEs
  - 234,720 adaptive logic modules (ALMs)
  - 50-Mbits (Mb) embedded memory
  - 512 18x18-bit multipliers
  - 36 transceivers (32 channels with 12.5 Gbps and four channels with 28 Gbps)
  - 174 LVDS transmit channels
  - 28 phase locked loops (PLLs)
  - 696 user I/Os
  - 850-mV core voltage
FPGA configuration circuitry
- MAX® II CPLD (EPM2210F256C3N) and flash Fast Passive Parallel (FPP) configuration
- MAX II CPLD (EPM570M100C4N) for on-board USB-Blaster™ to use with the Quartus® II Programmer
- JTAG header for external USB-Blaster
- Flash storage for two configuration images (factory and user)

On-Board clocking circuitry
- 625-MHz, 644.53125-MHz, 706.25-MHz, and 875-MHz programmable oscillators for the high-speed transceiver reference clocks
- 25/100/125/200 MHz jumper-selectable oscillator to the FPGA
- 50-MHz general-purpose oscillator to the FPGA
- One differential SMA clock input to the FPGA
- Four differential SMA clock input to the transceivers
- Spread spectrum clock input
- Four clock trigger outputs

Transceiver interfaces
- Four 25.78-Gbps TX/RX channels to MMPX connectors (for Stratix V GT FPGA only)
- Seven 12.5-Gbps TX/RX channels to SMA connectors
- One 12.5-Gbps TX/RX channel to SFP+ cage
- One 12.5-Gbps TX/RX channel to XFP cage
- Seven 12.5-Gbps TX/RX channels to Molex backplane connectors
- Seven 12.5-Gbps TX/RX channels to Amphenol backplane connectors
- Seven 12.5-Gbps TX/RX channels to Tyco backplane connectors

Memory devices
- One 1-Gbit (Gb) synchronous flash with a 16-bit data bus

Communication ports
- USB type-B connector
- Gigabit Ethernet port and RJ-45 jack
- LCD header

General user I/O
- Eight user LEDs
- Three configuration status LEDs (factory, user, error)
- Six Ethernet LEDs
- One 16-character × 2-line character LCD display
- Push button and DIP switches
  - One CPU reset push button
  - One configuration reset push button
  - Four general user push buttons
  - One 8-position user DIP switch
  - One 6-position MSEL control DIP switch
  - One 4-position frequency select and spread spectrum select DIP switch
  - One 4-position transceiver clock input select DIP switch
  - Two 4-position power sequence enable select DIP switches
  - One 4-position VCCRT_GXB/VCCA_GXB voltage select DIP switch
- Heat sink and fan
  - 40-mm heat sink and fan combo
  - One over-temperature warning indicator LED
- Power
  - 14-V – 20-V (laptop) DC input
  - One power-on LED
  - One on/off power slide switch
  - Power monitor and trim capability
  - Power sequence capability
- System Monitoring
  - Temperature—FPGA die
- Mechanical
  - 7.5” x 10.5” board dimension
Development Board Block Diagram

Figure 1–1 shows the block diagram of the Stratix V GT transceiver signal integrity development board.

Handling the Board

When handling the board, it is important to observe the following static discharge precaution:

CAUTION

Without proper anti-static handling, the board can be damaged. Therefore, use anti-static handling precautions when touching the board.

The Stratix V GT transceiver signal integrity development board must be stored between –40°C and 100°C. The recommended operating temperature is between 0°C and 55°C.
2. Board Components

This chapter introduces all the important components on the Stratix V GT transceiver signal integrity development board. Figure 2–1 illustrates major component locations and Table 2–1 provides a brief description of all features of the board.

A complete set of schematics, a physical layout database, and GERBER files for the development board reside in the Stratix V GT development kit documents directory.

For information about powering up the board and installing the demo software, refer to the Transceiver Signal Integrity Development Kit, Stratix V GT Edition User Guide.

This chapter consists of the following sections:

- “Board Overview”
- “Featured Device: Stratix V GT FPGA” on page 2–6
- “MAX II CPLD System Controller” on page 2–9
- “Configuration, Status, and Setup Elements” on page 2–14
- “Clock Circuitry” on page 2–21
- “General User Input/Output” on page 2–28
- “Components and Interfaces” on page 2–32
- “Flash Memory” on page 2–36
- “Power Supply” on page 2–37
- “Statement of China-RoHS Compliance” on page 2–42
Board Overview

This section provides an overview of the Stratix V GT transceiver signal integrity development board, including an annotated board image and component descriptions. Figure 2–1 provides an overview of the development board features.

Figure 2–1. Overview of the Stratix V GT Transceiver Signal Integrity Development Board Features

Table 2–1 describes the components and lists their corresponding board references.

Table 2–1. Transceiver Signal Integrity Development Kit Components (Part 1 of 4)

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Featured Devices</td>
<td></td>
<td></td>
</tr>
<tr>
<td>U29</td>
<td>FPGA</td>
<td>Stratix V GT FPGA (5SGTMCG7K3F40C2), 1517-pin BGA.</td>
</tr>
<tr>
<td>U19</td>
<td>CPLD</td>
<td>MAX II CPLD (EPM2210F256C3N), 256-pin BGA.</td>
</tr>
<tr>
<td>Configuration, Status, and Setup Elements</td>
<td></td>
<td></td>
</tr>
<tr>
<td>S7 (pin 6-7)</td>
<td>MAX II bypass switch</td>
<td>Enables or disables the MAX II CPLD in the JTAG chain. The MAX II CPLD is disabled by default.</td>
</tr>
</tbody>
</table>
Table 2–1. Transceiver Signal Integrity Development Kit Components (Part 2 of 4)

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J28</td>
<td>Program select jumper</td>
<td>Toggles the program LEDs to select which FPGA image to load on power-up; 0 selects factory image and 1 selects user-defined image.</td>
</tr>
<tr>
<td>S7</td>
<td>FPP configuration/MAX II bypass DIP switch</td>
<td>Select the configuration mode from the MAX II CPLD.</td>
</tr>
<tr>
<td>SW5</td>
<td>Spread spectrum clock settings DIP switch</td>
<td>Sets the spread spectrum output clock frequency and down-spread percentages.</td>
</tr>
<tr>
<td>SW2 (pin2-7)</td>
<td>VCCA_GXB voltage selection jumper</td>
<td>Selects $V_{CCA}$ voltage to the FPGA. When the jumper is set to close position, the $V_{CCA}$ voltage is 3.0 V (default). When set to open position, the $V_{CCA}$ voltage is 2.5 V.</td>
</tr>
<tr>
<td>SW2 (pin 1-8)</td>
<td>VCCRT voltage selection jumper</td>
<td>Selects $V_{CCRT}$ voltage to the FPGA. When the jumper is set to close position, the $V_{CCRT}$ voltage is 1.0 V (default). When set to open position, the $V_{CCRT}$ voltage is 0.85 V.</td>
</tr>
<tr>
<td>J26</td>
<td>Fan control jumper</td>
<td>Selects whether the fan is always on or the FPGA automatically controls the fan. To set it to its default setting of always on, connect jumper pin 2-3. Connect jumper pin 1-2 to set the fan in auto mode.</td>
</tr>
<tr>
<td>D7</td>
<td>Fan LED</td>
<td>Indicates an over-temperature condition in the FPGA and a fan should be attached to the FPGA and running.</td>
</tr>
<tr>
<td>D8</td>
<td>Load LED</td>
<td>Illuminates during embedded USB-Blaster data transfers.</td>
</tr>
<tr>
<td>D9</td>
<td>Error LED</td>
<td>Illuminates when the FPGA configuration from flash fails.</td>
</tr>
<tr>
<td>D3</td>
<td>Power LED</td>
<td>Illuminates when 14-V power is present.</td>
</tr>
<tr>
<td>D12-D17</td>
<td>Ethernet LEDs</td>
<td>Indicates the connection speed as well as transmit or receive activity.</td>
</tr>
</tbody>
</table>

**Clock Circuitry**

<table>
<thead>
<tr>
<th></th>
<th>Programmable oscillator</th>
<th>Feeds even-numbered REFCLKs on left side of the Stratix V GT device and trigger an output at board reference J81. The external input is available at board reference J79 and J80. The default frequency is 644.53125 MHz.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Y3</td>
<td>Programmable oscillator</td>
<td>Feeds odd-numbered REFCLKs on left side of the Stratix V GT device and trigger an output at board reference J85. The external input is available at board reference J83 and J84. The default frequency is 706.25 MHz.</td>
</tr>
<tr>
<td>Y4</td>
<td>Programmable oscillator</td>
<td>Feeds even-numbered REFCLKs on right side of the Stratix V GT device and trigger an output at board reference J88. The external input is available at board reference J86 and J87. The default frequency is 625 MHz.</td>
</tr>
<tr>
<td>Y5</td>
<td>Programmable oscillator</td>
<td>Feeds odd-numbered REFCLKs on right side of the Stratix V GT device and trigger an output at board reference J91. The external input is available at board reference J89 and J90. The default frequency is 875 MHz.</td>
</tr>
<tr>
<td>SW6</td>
<td>Transceiver clock input select DIP switch</td>
<td>Selects the SMA or oscillator as the clock input.</td>
</tr>
<tr>
<td>Y2</td>
<td>50-MHz oscillator</td>
<td>50.000-MHz crystal oscillator for general purpose logic.</td>
</tr>
<tr>
<td>X3</td>
<td>25/100/125/200-MHz core clock selectable oscillator</td>
<td>Selects the core clock frequency. The default frequency is 100 MHz.</td>
</tr>
<tr>
<td>SW5</td>
<td>Spread spectrum selection switch</td>
<td>Select either the core or spread spectrum clock. Pin 1-2 selects S0 and S1 while pin 3-4 selects SS0 and SS1.</td>
</tr>
<tr>
<td>J70 and J71</td>
<td>External core clock input</td>
<td>SMA external input at CLK10 p/n.</td>
</tr>
</tbody>
</table>
Table 2–1. Transceiver Signal Integrity Development Kit Components (Part 3 of 4)

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>J72 and J73</td>
<td>External core clock output</td>
<td>SMA external output at FPLL/IO4D.</td>
</tr>
</tbody>
</table>

**Transceiver Interfaces**

| J36, J39, J41, J46, J48, J53, J55, J57, J59, J61, J63, J65, J67, J69 | GXB transmit channel | Transceiver GXB transmit channels connected to SMA. |
| J35, J37, J38, J40, J42, J45, J47, J52, J54, J56, J58, J60, J62, J64, J66, J68 | GXB receive channel | Transceiver GXB receive channels connected to SMA. |
| J51              | Transceiver optical interface | Transceiver receive and transmit channel connected to the SFP+ module. |
| U25              | Transceiver optical interface | Transceiver receive and transmit channel connected to the XFP module. |

**Transceiver Interfaces – Backplane Connectors**


**Transceiver Interfaces – Stratix V GT**

| J94, J96, J98, J100, J102, J104, J106, J108 | Advanced transceiver interface | Transceiver GTB receive channels connected to the MMPX connectors. |
| J95, J97, J99, J101, J103, J105, J107, J109 | Advanced transceiver interface | Transceiver GTB transmit channels connected to the MMPX connectors. |
| J110, J111, J112, J113 | Transceiver test trace | Transceiver GTB receive and transmit channels connected to the MMPX connectors with an eight inch test trace. |

**General User Input and Output**

| D18-D25 | User LEDs | 8 user LEDs. Illuminates when driven low. |
| SW4     | User DIP switch | Octal user DIP switch. When the switch is in the open position, a logic 0 is selected. |
| S5      | Configuration reset push button | The default reset for the MAX II CPLD System Controller. |
| S6      | CPU reset push button | The default reset for the FPGA logic. |
| S1-S4   | General user push buttons | Four user push buttons. Driven low when pressed. |
| J30     | Character LCD header | A single 14-pin 0.1” pitch dual-row header which interfaces to the 16 character x 2 line LCD module. |
### Table 2–1. Transceiver Signal Integrity Development Kit Components (Part 4 of 4)

<table>
<thead>
<tr>
<th>Memory Devices</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>U21 Flash memory</td>
<td>Micron PC28F00AP30BF, 1-Gb CFI NOR flash memory.</td>
<td></td>
</tr>
<tr>
<td>U17 EEPROM</td>
<td>Microchip Technology Inc. 93LC468/SNG-ND, 64x16 EEPROM SO.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Communication Ports</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>J29 Gigabit Ethernet port</td>
<td>RJ-45 connector which provides a 10/100/1000 Ethernet connection through a Marvell 88E1111 PHY and the FPGA-based Altera Triple Speed Ethernet MAC MegaCore function in SGMII mode.</td>
<td></td>
</tr>
<tr>
<td>J93 JTAG header</td>
<td>Connects an Altera USB-Blaster dongle to program the FPGA and MAX II CPLD devices. The embedded USB-Blaster is disabled when you connect the USB-Blaster to the JTAG header.</td>
<td></td>
</tr>
<tr>
<td>CN1 USB Type-B connector</td>
<td>Connects a type-B USB cable to enable the JTAG embedded USB-Blaster to program the FPGA and MAX II CPLD devices.</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Power Supply</th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>J1 DC input jack</td>
<td>14-V – 20-V DC female input power jack. Accepts a 2.5-mm male center-positive barrel from 14-V DC power supply.</td>
<td></td>
</tr>
<tr>
<td>SW1 Power switch</td>
<td>Switch to power on/off the board.</td>
<td></td>
</tr>
<tr>
<td>J6 S5GX_VCC (0.85 V/0.9 V) banana jack</td>
<td>Banana jack for supplying external VCC power to the FPGA. Fuses F1 and F2 must be removed prior to supplying external power to this banana jack.</td>
<td></td>
</tr>
<tr>
<td>J12 VCCA_GXB (2.5 V/3.3 V) banana jack</td>
<td>Banana jack for supplying external VCCA power to the FPGA. Fuse F7 must be removed prior to supplying external power to this banana jack.</td>
<td></td>
</tr>
<tr>
<td>J9 VCCRT_GXB (0.85 V/1.0 V) banana jack</td>
<td>Banana jack for supplying external VCCRT power to the FPGA. Fuse F6 must be removed prior to supplying external power to this banana jack.</td>
<td></td>
</tr>
<tr>
<td>J15 VCCR_GTB (1.0 V) banana jack</td>
<td>Banana jack for supplying external VCCR power to the FPGA. Fuse F3 must be removed prior to supplying external power to this banana jack.</td>
<td></td>
</tr>
<tr>
<td>J21 VCCL_GTB (1.0 V) banana jack</td>
<td>Banana jack for supplying external VCCL power to the FPGA. Fuse F5 must be removed prior to supplying external power to this banana jack.</td>
<td></td>
</tr>
<tr>
<td>J18 VCCT_GTB (1.0 V) banana jack</td>
<td>Banana jack for supplying external VCCT power to the FPGA. Fuse F4 must be removed prior to supplying external power to this banana jack.</td>
<td></td>
</tr>
<tr>
<td>J3 Ground banana jack</td>
<td>Banana jack connected to ground.</td>
<td></td>
</tr>
<tr>
<td>U10 and U11 Power monitor devices</td>
<td>Linear Technology LTC2978, octal PMBus power supply monitor and controller.</td>
<td></td>
</tr>
</tbody>
</table>
Featured Device: Stratix V GT FPGA

The development board features the Stratix V GT 5SGTMC7K3F40C2 device (U29) in a 1517-pin FineLine BGA package.

For more information about the Stratix V device family, refer to the *Stratix V Device Handbook*.

Table 2–2 describes the features of the Stratix V GT 5SGTMC7K3F40C2 device.

**Table 2–2. Stratix V GT Device Features**

<table>
<thead>
<tr>
<th>ALMs</th>
<th>Equivalent LEs</th>
<th>Registers</th>
<th>M20K Blocks</th>
<th>MLAB Blocks (Mb)</th>
<th>18-bit × 18-bit Multipliers</th>
<th>PLLs</th>
<th>Transceiver Channels (12.5 Gbps)</th>
<th>Package Type</th>
</tr>
</thead>
<tbody>
<tr>
<td>234,720</td>
<td>622,000</td>
<td>939,000</td>
<td>2,560</td>
<td>7.16</td>
<td>512</td>
<td>28</td>
<td>36</td>
<td>1517-pin FineLine BGA</td>
</tr>
</tbody>
</table>

Table 2–3 lists the Stratix V GT component reference and manufacturing information.

**Table 2–3. Stratix V GT Component Reference and Manufacturing Information**

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturing Part Number</th>
<th>Manufacturer Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>U29</td>
<td>FPGA, Stratix V GT F1517, 622K LEs, lead-free</td>
<td>Altera Corporation</td>
<td>5SGTMC7K3F40C2</td>
<td><a href="http://www.altera.com">www.altera.com</a></td>
</tr>
</tbody>
</table>

I/O Resources

Table 2–4 summarizes the FPGA I/O usage by function on the Stratix V GT transceiver signal integrity development board.

**Table 2–4. Stratix V GT I/O Usage Summary (Part 1 of 3)**

<table>
<thead>
<tr>
<th>Function</th>
<th>I/O Type</th>
<th>I/O Count</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPGA Transceiver Clocks</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Programmable differential clock</td>
<td>LVDS input</td>
<td>4</td>
<td>Differential REFCLK input to feed the even-numbered channels on the left side of the Stratix V GT device.</td>
</tr>
<tr>
<td>Programmable differential clock</td>
<td>LVDS input</td>
<td>4</td>
<td>Differential REFCLK input to feed the odd-numbered channels on the left side of the Stratix V GT device.</td>
</tr>
<tr>
<td>Programmable differential clock</td>
<td>LVDS input</td>
<td>4</td>
<td>Differential REFCLK input to feed the even-numbered channels on the right side of the Stratix V GT device.</td>
</tr>
<tr>
<td>Programmable differential clock</td>
<td>LVDS input</td>
<td>4</td>
<td>Differential REFCLK input to feed the odd-numbered channels on the right side of the Stratix V GT device.</td>
</tr>
<tr>
<td>External differential clock inputs</td>
<td>LVDS input</td>
<td>4 pairs</td>
<td>Differential REFCLK input for one SMA pair per clock buffer.</td>
</tr>
<tr>
<td>FPGA Global Clocks</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>50-MHz clock</td>
<td>2.5-V CMOS input</td>
<td>1</td>
<td>Global clock input.</td>
</tr>
<tr>
<td>Spread Spectrum clock</td>
<td>2.5-V CMOS input</td>
<td>2</td>
<td>Differential global clock.</td>
</tr>
<tr>
<td>SMA differential clock input</td>
<td>LVDS input</td>
<td>2</td>
<td>Differential global clock.</td>
</tr>
</tbody>
</table>
### Temperature Monitor
- **Function**: Temperature sense diodes
- **Type**: Analog
- **Count**: 2
- **Description**: Stratix V GT internal sense diode.

### Power Monitor Devices
- **Function**: LTC2978 controller
- **Type**: 2.5-V CMOS
- **Count**: 24
- **Description**: Octal PMBus power supply monitor and controller.

### Temperature Measure
- **Function**: MAX1619 interface
- **Type**: 2.5V CMOS
- **Count**: 4
- **Description**: Die and ambient temperature sense.

### Fan
- **Function**: FAN_On
- **Type**: 2.5-V CMOS output
- **Count**: 1
- **Description**: Fan control
- **Function**: FAN_LED
- **Type**: 2.5-V CMOS output
- **Count**: 1
- **Description**: Fan LED

### USB-Blaster
- **Function**: JTAG USB-Blaster or JTAG header
- **Type**: 2.5-V CMOS
- **Count**: 4
- **Description**: Built-in USB-Blaster or JTAG 0.1-mm header for debugging

### FPP Configuration
- **Function**: FPGA Dclk
- **Type**: 2.5-V CMOS input
- **Count**: 1
- **Description**: FPP Dclk
- **Function**: FPGA D[15:0]
- **Type**: 2.5V CMOS
- **Count**: 16
- **Description**: FPP data bus
- **Function**: MSEL [4:0]
- **Type**: 2.5V CMOS
- **Count**: 5
- **Description**: Dedicated configuration pins
- **Function**: NCONFIG
- **Type**: 2.5V CMOS
- **Count**: 1
- **Description**: Dedicated configuration pins
- **Function**: NSTATUS
- **Type**: 2.5V CMOS
- **Count**: 1
- **Description**: Dedicated configuration pins
- **Function**: NCE
- **Type**: 2.5V CMOS
- **Count**: 1
- **Description**: Dedicated configuration pins
- **Function**: CONFIG_DONE
- **Type**: 2.5V CMOS
- **Count**: 1
- **Description**: Dedicated configuration pins

### Flash Memory
- **Function**: ADDR[26:1]
- **Type**: 1.8-V CMOS output
- **Count**: 26
- **Description**: Flash address bus
- **Function**: DATA[15:0]
- **Type**: 1.8-V CMOS input/output
- **Count**: 16
- **Description**: Flash data bus
- **Function**: FLASH_CEn
- **Type**: 1.8-V CMOS output
- **Count**: 1
- **Description**: Flash chip enable
- **Function**: FLASH_OEn
- **Type**: 1.8-V CMOS output
- **Count**: 1
- **Description**: Flash read strobe
- **Function**: FLASH_WEn
- **Type**: 1.8-V CMOS output
- **Count**: 1
- **Description**: Flash write strobe
- **Function**: FLASH_WAIT
- **Type**: 1.8-V CMOS input
- **Count**: 1
- **Description**: Flash ready or busy
- **Function**: FLASH_CLK
- **Type**: 1.8-V CMOS output
- **Count**: 1
- **Description**: Flash clock
- **Function**: FLASH_RSTn
- **Type**: 1.8-V CMOS output
- **Count**: 1
- **Description**: Flash reset
- **Function**: FLASH_ADVn
- **Type**: 1.8-V CMOS output
- **Count**: 1
- **Description**: Flash address valid
- **Function**: FLASH_WPn
- **Type**: 1.8-V CMOS output
- **Count**: 1
- **Description**: Flash write protect

### Reset
- **Function**: CPU_RESETn
- **Type**: 2.5-V CMOS input
- **Count**: 1
- **Description**: Nios® II CPU reset

### Switches, Buttons, LEDs
- **Function**: User push buttons
- **Type**: 2.5-V CMOS input
- **Count**: 4
- **Description**: 4 user push buttons
- **Function**: User DIP switches
- **Type**: 2.5-V CMOS input
- **Count**: 8
- **Description**: 8 user DIP switches
- **Function**: User LEDs
- **Type**: 2.5-V CMOS output
- **Count**: 8
- **Description**: 8 user LEDs (green)
<table>
<thead>
<tr>
<th>Function</th>
<th>I/O Type</th>
<th>I/O Count</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>LCD</strong></td>
<td>5.0-V LVTTL output</td>
<td>11</td>
<td>LCD</td>
</tr>
<tr>
<td><strong>Ethernet</strong></td>
<td>2.5-V CMOS output</td>
<td>4</td>
<td>Ethernet transmit RGMII data bus</td>
</tr>
<tr>
<td>TXD[3:0]</td>
<td>2.5-V CMOS output</td>
<td>1</td>
<td>Ethernet transmit enable</td>
</tr>
<tr>
<td>TXEN</td>
<td>2.5-V CMOS output</td>
<td>1</td>
<td>Ethernet transmit clock</td>
</tr>
<tr>
<td>RXD[3:0]</td>
<td>2.5-V CMOS input</td>
<td>4</td>
<td>Ethernet receive RGMII data bus</td>
</tr>
<tr>
<td>RXDV</td>
<td>2.5-V CMOS input</td>
<td>1</td>
<td>Receive data valid</td>
</tr>
<tr>
<td>RXCLK</td>
<td>2.5-V CMOS input</td>
<td>1</td>
<td>Receive clock</td>
</tr>
<tr>
<td>MDC</td>
<td>2.5-V CMOS input</td>
<td>1</td>
<td>Ethernet MII clock</td>
</tr>
<tr>
<td>MDIO</td>
<td>2.5-V CMOS inout</td>
<td>1</td>
<td>Ethernet MII data</td>
</tr>
<tr>
<td>ENET_SGMII_TXP/N</td>
<td>LVDS output</td>
<td>2</td>
<td>Ethernet SGMII transmit data positive/negative</td>
</tr>
<tr>
<td>ENET_SGMII_RXP/N</td>
<td>LVDS input</td>
<td>2</td>
<td>Ethernet SGMII receive data positive/negative</td>
</tr>
<tr>
<td><strong>Transceivers</strong></td>
<td>1.4-V PCML</td>
<td>16</td>
<td>Transceiver channel</td>
</tr>
<tr>
<td>28G channels to MMPX</td>
<td>1.4-V PCML</td>
<td>28</td>
<td>Transceiver channel</td>
</tr>
<tr>
<td>12.5G channels to Tyco backplane connector</td>
<td>1.4-V PCML</td>
<td>28</td>
<td>Transceiver channel</td>
</tr>
<tr>
<td>12.5G channels to Amphenol backplane connector</td>
<td>1.4-V PCML</td>
<td>28</td>
<td>Transceiver channel</td>
</tr>
<tr>
<td>12.5G channels to Molex backplane connector</td>
<td>1.4-V PCML</td>
<td>28</td>
<td>Transceiver channel</td>
</tr>
<tr>
<td>12.5G channels to SMA</td>
<td>1.4-V PCML</td>
<td>28</td>
<td>Transceiver channel</td>
</tr>
<tr>
<td>12.5G channels to a SFP+ cage</td>
<td>1.4-V PCML</td>
<td>4</td>
<td>Transceiver channel</td>
</tr>
<tr>
<td>12.5G channels to XFP cage</td>
<td>1.4-V PCML</td>
<td>4</td>
<td>Transceiver channel</td>
</tr>
<tr>
<td><strong>Spares</strong></td>
<td>2.5-V CMOS</td>
<td>8</td>
<td>Spare signals to the MAX II CPLD</td>
</tr>
<tr>
<td><strong>Device I/O Total:</strong></td>
<td></td>
<td>304</td>
<td></td>
</tr>
</tbody>
</table>

Table 2–4. Stratix V GT I/O Usage Summary (Part 3 of 3)
MAX II CPLD System Controller

The board utilizes the EPM2210F256C3N System Controller, an Altera MAX II CPLD, for the following purposes:

- FPGA configuration from flash memory
- Temperature monitoring
- Fan control
- Virtual JTAG interface for PC-based power and temperature GUI
- Control registers for clocks
- Control registers for remote system update
- Register with CPLD design revision and board information (read-only)

Figure 2–2 illustrates the MAX II CPLD System Controller's functionality and external circuit connections as a block diagram.

Table 2–5 lists the I/O signals present on the MAX II CPLD System Controller. The signal names and functions are relative to the MAX II device (U19).

Table 2–5. MAX II CPLD System Controller Device Pin-Out (Part 1 of 5)

<table>
<thead>
<tr>
<th>Schematic Signal Name</th>
<th>MAX II CPLD Pin Number</th>
<th>Stratix V GT Pin Number</th>
<th>I/O Standard</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>50MHZ_MAXLL_CLK</td>
<td>H5</td>
<td>—</td>
<td>2.5-V</td>
<td>50 MHz clock input</td>
</tr>
<tr>
<td>ALERTn</td>
<td>D2</td>
<td>E8</td>
<td>2.5-V</td>
<td>Temperature monitor alert</td>
</tr>
<tr>
<td>CONF_DONE</td>
<td>T13</td>
<td>AB12</td>
<td>2.5-V</td>
<td>Configuration done</td>
</tr>
<tr>
<td>CONFIG_D0</td>
<td>T11</td>
<td>AR33</td>
<td>2.5-V</td>
<td>Configuration data</td>
</tr>
<tr>
<td>CONFIG_D1</td>
<td>T10</td>
<td>AU32</td>
<td>2.5-V</td>
<td>Configuration data</td>
</tr>
</tbody>
</table>
### Table 2–5. MAX II CPLD System Controller Device Pin-Out (Part 2 of 5)

<table>
<thead>
<tr>
<th>Schematic Signal Name</th>
<th>MAX II CPLD Pin Number</th>
<th>Stratix V GT Pin Number</th>
<th>I/O Standard</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONFIG_D2</td>
<td>P12</td>
<td>AT32</td>
<td>2.5-V</td>
<td>Configuration data</td>
</tr>
<tr>
<td>CONFIG_D3</td>
<td>P11</td>
<td>AW32</td>
<td>2.5-V</td>
<td>Configuration data</td>
</tr>
<tr>
<td>CONFIG_D4</td>
<td>R11</td>
<td>AV32</td>
<td>2.5-V</td>
<td>Configuration data</td>
</tr>
<tr>
<td>CONFIG_D5</td>
<td>R10</td>
<td>AM32</td>
<td>2.5-V</td>
<td>Configuration data</td>
</tr>
<tr>
<td>CONFIG_D6</td>
<td>N12</td>
<td>AL31</td>
<td>2.5-V</td>
<td>Configuration data</td>
</tr>
<tr>
<td>CONFIG_D7</td>
<td>P10</td>
<td>AN32</td>
<td>2.5-V</td>
<td>Configuration data</td>
</tr>
<tr>
<td>CONFIG_D8</td>
<td>H4</td>
<td>AN31</td>
<td>2.5-V</td>
<td>Configuration data</td>
</tr>
<tr>
<td>CONFIG_D9</td>
<td>J4</td>
<td>AM31</td>
<td>2.5-V</td>
<td>Configuration data</td>
</tr>
<tr>
<td>CONFIG_D10</td>
<td>J3</td>
<td>AL30</td>
<td>2.5-V</td>
<td>Configuration data</td>
</tr>
<tr>
<td>CONFIG_D11</td>
<td>K2</td>
<td>AK30</td>
<td>2.5-V</td>
<td>Configuration data</td>
</tr>
<tr>
<td>CONFIG_D12</td>
<td>K5</td>
<td>AJ30</td>
<td>2.5-V</td>
<td>Configuration data</td>
</tr>
<tr>
<td>CONFIG_D13</td>
<td>K4</td>
<td>AJ29</td>
<td>2.5-V</td>
<td>Configuration data</td>
</tr>
<tr>
<td>CONFIG_D14</td>
<td>K3</td>
<td>AJ28</td>
<td>2.5-V</td>
<td>Configuration data</td>
</tr>
<tr>
<td>CONFIG_D15</td>
<td>L5</td>
<td>AM29</td>
<td>2.5-V</td>
<td>Configuration data</td>
</tr>
<tr>
<td>CONFIG_ERR</td>
<td>R9</td>
<td>—</td>
<td>2.5-V</td>
<td>Configuration error</td>
</tr>
<tr>
<td>DCLK</td>
<td>T8</td>
<td>U28</td>
<td>2.5-V</td>
<td>Configuration clock</td>
</tr>
<tr>
<td>ENET_RSTn</td>
<td>A15</td>
<td>AT6</td>
<td>2.5-V</td>
<td>Ethernet LED</td>
</tr>
<tr>
<td>F_AD1</td>
<td>M16</td>
<td>AE14</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD2</td>
<td>M15</td>
<td>AD14</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD3</td>
<td>M14</td>
<td>AC13</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD4</td>
<td>N16</td>
<td>AC12</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD5</td>
<td>N15</td>
<td>AG14</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD6</td>
<td>J16</td>
<td>AF14</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD7</td>
<td>N13</td>
<td>AD11</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD8</td>
<td>N14</td>
<td>AC11</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD9</td>
<td>C14</td>
<td>AF11</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD10</td>
<td>B12</td>
<td>AE11</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD11</td>
<td>F15</td>
<td>AE13</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD12</td>
<td>F16</td>
<td>AE12</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD13</td>
<td>D16</td>
<td>AJ14</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD14</td>
<td>A11</td>
<td>AH13</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD15</td>
<td>A12</td>
<td>AG13</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD16</td>
<td>B13</td>
<td>AF13</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD17</td>
<td>E15</td>
<td>AJ13</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD18</td>
<td>L14</td>
<td>AJ12</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD19</td>
<td>J15</td>
<td>AH12</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD20</td>
<td>D14</td>
<td>AG11</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD21</td>
<td>K14</td>
<td>AK12</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD22</td>
<td>D15</td>
<td>AK11</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
</tbody>
</table>
### Table 2–5. MAX II CPLD System Controller Device Pin-Out (Part 3 of 5)

<table>
<thead>
<tr>
<th>Schematic Signal Name</th>
<th>MAX II CPLD Pin Number</th>
<th>Stratix V GT Pin Number</th>
<th>I/O Standard</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F_AD23</td>
<td>A13</td>
<td>AL12</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD24</td>
<td>B14</td>
<td>AL11</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD25</td>
<td>C13</td>
<td>AM13</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_AD26</td>
<td>B16</td>
<td>AL13</td>
<td>2.5-V</td>
<td>Flash address bus</td>
</tr>
<tr>
<td>F_ADVn</td>
<td>P13</td>
<td>AP7</td>
<td>2.5-V</td>
<td>Flash address valid</td>
</tr>
<tr>
<td>F_BSYn</td>
<td>J14</td>
<td>AR7</td>
<td>2.5-V</td>
<td>Flash chip busy</td>
</tr>
<tr>
<td>F_CEEn</td>
<td>P14</td>
<td>AP9</td>
<td>2.5-V</td>
<td>Flash chip enable</td>
</tr>
<tr>
<td>F_CLK</td>
<td>R16</td>
<td>AN6</td>
<td>2.5-V</td>
<td>Flash clock</td>
</tr>
<tr>
<td>F_D0</td>
<td>L15</td>
<td>AN11</td>
<td>2.5-V</td>
<td>Flash data bus</td>
</tr>
<tr>
<td>F_D1</td>
<td>L16</td>
<td>AM11</td>
<td>2.5-V</td>
<td>Flash data bus</td>
</tr>
<tr>
<td>F_D2</td>
<td>K15</td>
<td>AP12</td>
<td>2.5-V</td>
<td>Flash data bus</td>
</tr>
<tr>
<td>F_D3</td>
<td>K16</td>
<td>AN12</td>
<td>2.5-V</td>
<td>Flash data bus</td>
</tr>
<tr>
<td>F_D4</td>
<td>H16</td>
<td>AN10</td>
<td>2.5-V</td>
<td>Flash data bus</td>
</tr>
<tr>
<td>F_D5</td>
<td>H15</td>
<td>AM10</td>
<td>2.5-V</td>
<td>Flash data bus</td>
</tr>
<tr>
<td>F_D6</td>
<td>G16</td>
<td>AR11</td>
<td>2.5-V</td>
<td>Flash data bus</td>
</tr>
<tr>
<td>F_D7</td>
<td>G15</td>
<td>AR10</td>
<td>2.5-V</td>
<td>Flash data bus</td>
</tr>
<tr>
<td>F_D8</td>
<td>M13</td>
<td>AT12</td>
<td>2.5-V</td>
<td>Flash data bus</td>
</tr>
<tr>
<td>F_D9</td>
<td>L13</td>
<td>AU13</td>
<td>2.5-V</td>
<td>Flash data bus</td>
</tr>
<tr>
<td>F_D10</td>
<td>J13</td>
<td>AU12</td>
<td>2.5-V</td>
<td>Flash data bus</td>
</tr>
<tr>
<td>F_D11</td>
<td>H13</td>
<td>AU11</td>
<td>2.5-V</td>
<td>Flash data bus</td>
</tr>
<tr>
<td>F_D12</td>
<td>G13</td>
<td>AT11</td>
<td>2.5-V</td>
<td>Flash data bus</td>
</tr>
<tr>
<td>F_D13</td>
<td>F13</td>
<td>AW13</td>
<td>2.5-V</td>
<td>Flash data bus</td>
</tr>
<tr>
<td>F_D14</td>
<td>F14</td>
<td>AV13</td>
<td>2.5-V</td>
<td>Flash data bus</td>
</tr>
<tr>
<td>F_D15</td>
<td>E14</td>
<td>AW11</td>
<td>2.5-V</td>
<td>Flash data bus</td>
</tr>
<tr>
<td>F_OEn</td>
<td>P15</td>
<td>AN9</td>
<td>2.5-V</td>
<td>Flash output enable</td>
</tr>
<tr>
<td>F_RSTn</td>
<td>H14</td>
<td>AL8</td>
<td>2.5-V</td>
<td>Flash reset</td>
</tr>
<tr>
<td>F_WEn</td>
<td>G14</td>
<td>AM8</td>
<td>2.5-V</td>
<td>Flash write enable</td>
</tr>
<tr>
<td>F_WFn</td>
<td>T12</td>
<td>AP6</td>
<td>2.5-V</td>
<td>Flash write protect</td>
</tr>
<tr>
<td>FACTORY_IMAGE</td>
<td>R8</td>
<td>—</td>
<td>2.5-V</td>
<td>Factory image for configuration</td>
</tr>
<tr>
<td>FAN_CTRL</td>
<td>E3</td>
<td>D6</td>
<td>2.5-V</td>
<td>Fan control</td>
</tr>
<tr>
<td>FAN_LED</td>
<td>C3</td>
<td>C6</td>
<td>2.5-V</td>
<td>Fan LED</td>
</tr>
<tr>
<td>INIT_DONE</td>
<td>R13</td>
<td>AN33</td>
<td>2.5-V</td>
<td>FPGA initialization done.</td>
</tr>
<tr>
<td>JTAG_TCK</td>
<td>P3</td>
<td>AV34</td>
<td>2.5-V</td>
<td>JTAG chain clock</td>
</tr>
<tr>
<td>JTAG_TMS</td>
<td>N4</td>
<td>AU34</td>
<td>2.5-V</td>
<td>JTAG chain mode</td>
</tr>
<tr>
<td>MAX_2_MAX_INITDONE</td>
<td>H2</td>
<td>—</td>
<td>2.5-V</td>
<td>Control signal between the MAX II System Controller and the MAX II embedded USB-Blaster to indicate that initialization is done.</td>
</tr>
<tr>
<td>MAX_FPP_TDI</td>
<td>L6</td>
<td>—</td>
<td>2.5-V</td>
<td>Fast Passive Parallel (FPP) programming data in</td>
</tr>
<tr>
<td>MAX_FPP_TDO</td>
<td>M5</td>
<td>—</td>
<td>2.5-V</td>
<td>FPP programming data out</td>
</tr>
<tr>
<td>Schematic Signal Name</td>
<td>MAX II CPLD Pin Number</td>
<td>Stratix V GT Pin Number</td>
<td>I/O Standard</td>
<td>Description</td>
</tr>
<tr>
<td>-----------------------</td>
<td>------------------------</td>
<td>-------------------------</td>
<td>--------------</td>
<td>-------------</td>
</tr>
<tr>
<td>MAXLL_BEN0</td>
<td>F5</td>
<td>AN15</td>
<td>2.5-V</td>
<td>Flash bus MAX II byte enable 0</td>
</tr>
<tr>
<td>MAXLL_BEN1</td>
<td>F2</td>
<td>AN14</td>
<td>2.5-V</td>
<td>Flash bus MAX II byte enable 1</td>
</tr>
<tr>
<td>MAXLL_BEN2</td>
<td>F6</td>
<td>AM14</td>
<td>2.5-V</td>
<td>Flash bus MAX II byte enable 2</td>
</tr>
<tr>
<td>MAXLL_BEN3</td>
<td>F1</td>
<td>AR14</td>
<td>2.5-V</td>
<td>Flash bus MAX II byte enable 3</td>
</tr>
<tr>
<td>MAXLL_CLK</td>
<td>G3</td>
<td>AR13</td>
<td>2.5-V</td>
<td>Flash bus MAX II clock</td>
</tr>
<tr>
<td>MAXLL_CSn</td>
<td>G2</td>
<td>AR15</td>
<td>2.5-V</td>
<td>Flash bus MAX II chip select</td>
</tr>
<tr>
<td>MAXLL_OEn</td>
<td>G4</td>
<td>AP15</td>
<td>2.5-V</td>
<td>Flash bus MAX II output enable</td>
</tr>
<tr>
<td>MAXLL_WEn</td>
<td>G1</td>
<td>AT15</td>
<td>2.5-V</td>
<td>Flash bus MAX II write enable</td>
</tr>
<tr>
<td>MSEL0</td>
<td>D13</td>
<td>W12</td>
<td>2.5-V</td>
<td>DIP - FPGA mode select 0</td>
</tr>
<tr>
<td>MSEL1</td>
<td>K12</td>
<td>Y11</td>
<td>2.5-V</td>
<td>DIP - FPGA mode select 1</td>
</tr>
<tr>
<td>MSEL2</td>
<td>K13</td>
<td>AA12</td>
<td>2.5-V</td>
<td>DIP - FPGA mode select 2</td>
</tr>
<tr>
<td>MSEL3</td>
<td>L11</td>
<td>AA11</td>
<td>2.5-V</td>
<td>DIP - FPGA mode select 3</td>
</tr>
<tr>
<td>MSEL4</td>
<td>L12</td>
<td>W11</td>
<td>2.5-V</td>
<td>DIP - FPGA mode select 4</td>
</tr>
<tr>
<td>NCONFIG</td>
<td>R14</td>
<td>U26</td>
<td>2.5-V</td>
<td>FPGA configuration active LED</td>
</tr>
<tr>
<td>NSTATUS</td>
<td>R12</td>
<td>AL10</td>
<td>2.5-V</td>
<td>FPGA configuration ready status LED</td>
</tr>
<tr>
<td>OVERTEMPn</td>
<td>E4</td>
<td>E7</td>
<td>2.5-V</td>
<td>Over-temperature indicator LED</td>
</tr>
<tr>
<td>PFL_STATUS</td>
<td>P4</td>
<td>—</td>
<td>2.5-V</td>
<td>Parallel Flash Loader (PFL) programming status</td>
</tr>
<tr>
<td>PGM0</td>
<td>T6</td>
<td>AW10</td>
<td>2.5-V</td>
<td>Flash memory PGM select indicator 0</td>
</tr>
<tr>
<td>PGM1</td>
<td>T5</td>
<td>AV10</td>
<td>2.5-V</td>
<td>Flash memory PGM select indicator 1</td>
</tr>
<tr>
<td>PGM2</td>
<td>T4</td>
<td>AR12</td>
<td>2.5-V</td>
<td>Flash memory PGM select indicator 2</td>
</tr>
<tr>
<td>PGMSEL</td>
<td>T7</td>
<td>—</td>
<td>2.5-V</td>
<td>Toggles the PGM_LED[0:2] sequence</td>
</tr>
<tr>
<td>PM1_FAULTB00</td>
<td>C4</td>
<td>U14</td>
<td>2.5-V</td>
<td>Power monitor bus</td>
</tr>
<tr>
<td>PM1_FAULTB01</td>
<td>C6</td>
<td>U13</td>
<td>2.5-V</td>
<td>Power monitor bus</td>
</tr>
<tr>
<td>PM1_FAULTB10</td>
<td>B3</td>
<td>R12</td>
<td>2.5-V</td>
<td>Power monitor bus</td>
</tr>
<tr>
<td>PM1_FAULTB11</td>
<td>C5</td>
<td>P11</td>
<td>2.5-V</td>
<td>Power monitor bus</td>
</tr>
<tr>
<td>PM2_FAULTB00</td>
<td>A2</td>
<td>N13</td>
<td>2.5-V</td>
<td>Power monitor bus</td>
</tr>
<tr>
<td>PM2_FAULTB01</td>
<td>D5</td>
<td>N12</td>
<td>2.5-V</td>
<td>Power monitor bus</td>
</tr>
<tr>
<td>PM2_FAULTB10</td>
<td>B1</td>
<td>R13</td>
<td>2.5-V</td>
<td>Power monitor bus</td>
</tr>
<tr>
<td>PM2_FAULTB11</td>
<td>D4</td>
<td>P13</td>
<td>2.5-V</td>
<td>Power monitor bus</td>
</tr>
<tr>
<td>PM_ALERTB</td>
<td>B4</td>
<td>L12</td>
<td>2.5-V</td>
<td>Power monitor alert</td>
</tr>
<tr>
<td>PM_CNTL0</td>
<td>C7</td>
<td>K12</td>
<td>2.5-V</td>
<td>Power monitor control bus</td>
</tr>
<tr>
<td>PM_CNTL1</td>
<td>A4</td>
<td>K13</td>
<td>2.5-V</td>
<td>Power monitor control bus</td>
</tr>
<tr>
<td>PM_PWRGD</td>
<td>D6</td>
<td>V12</td>
<td>2.5-V</td>
<td>Power monitor power</td>
</tr>
<tr>
<td>PM_RSTN</td>
<td>E6</td>
<td>J13</td>
<td>2.5-V</td>
<td>Power monitor reset</td>
</tr>
<tr>
<td>PM_SHARE_CLK</td>
<td>B5</td>
<td>M12</td>
<td>2.5-V</td>
<td>Power monitor clock</td>
</tr>
<tr>
<td>PR_DONE</td>
<td>B6</td>
<td>AB29</td>
<td>2.5-V</td>
<td>FPGA partial reconfiguration done</td>
</tr>
<tr>
<td>PR_ERROR</td>
<td>D7</td>
<td>AC27</td>
<td>2.5-V</td>
<td>FPGA partial reconfiguration error</td>
</tr>
<tr>
<td>PR_READY</td>
<td>A5</td>
<td>AD29</td>
<td>2.5-V</td>
<td>FPGA partial reconfiguration ready</td>
</tr>
<tr>
<td>PR_REQUEST</td>
<td>E7</td>
<td>AE29</td>
<td>2.5-V</td>
<td>FPGA partial reconfiguration request</td>
</tr>
</tbody>
</table>
Table 2–5. MAX II CPLD System Controller Device Pin-Out (Part 5 of 5)

<table>
<thead>
<tr>
<th>Schematic Signal Name</th>
<th>MAX II CPLD Pin Number</th>
<th>Stratix V GT Pin Number</th>
<th>I/O Standard</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>PWR_GOOD</td>
<td>J1</td>
<td>—</td>
<td>—</td>
<td>Power good signal to indicate that all voltage rails have come up to their proper levels.</td>
</tr>
<tr>
<td>RESETN</td>
<td>T2</td>
<td>—</td>
<td>2.5-V</td>
<td>FPGA reset LED</td>
</tr>
<tr>
<td>S5_RSTN</td>
<td>T15</td>
<td>AV19</td>
<td>2.5-V</td>
<td>FPGA reset</td>
</tr>
<tr>
<td>S5_SMBCLOCK_TEMP</td>
<td>D3</td>
<td>B8</td>
<td>2.5-V</td>
<td>Temperature monitor SMB clock</td>
</tr>
<tr>
<td>S5_SMBDATA_TEMP</td>
<td>C2</td>
<td>A8</td>
<td>2.5-V</td>
<td>Temperature monitor SMB data</td>
</tr>
<tr>
<td>SCL_OSC</td>
<td>D8</td>
<td>—</td>
<td>2.5-V</td>
<td>Configuration clock oscillator</td>
</tr>
<tr>
<td>SCL_PM</td>
<td>C8</td>
<td>L11</td>
<td>2.5-V</td>
<td>Configuration clock power monitor</td>
</tr>
<tr>
<td>SDA_OSC</td>
<td>B7</td>
<td>—</td>
<td>2.5-V</td>
<td>Configuration data oscillator</td>
</tr>
<tr>
<td>SDA_PM</td>
<td>A6</td>
<td>M11</td>
<td>2.5-V</td>
<td>Configuration data power monitor</td>
</tr>
<tr>
<td>SPARE0</td>
<td>A10</td>
<td>AH19</td>
<td>2.5-V</td>
<td>Spare signals to the MAX II CPLD</td>
</tr>
<tr>
<td>SPARE1</td>
<td>A9</td>
<td>AG19</td>
<td>2.5-V</td>
<td>Spare signals to the MAX II CPLD</td>
</tr>
<tr>
<td>SPARE2</td>
<td>A8</td>
<td>AJ18</td>
<td>2.5-V</td>
<td>Spare signals to the MAX II CPLD</td>
</tr>
<tr>
<td>SPARE3</td>
<td>A7</td>
<td>AH18</td>
<td>2.5-V</td>
<td>Spare signals to the MAX II CPLD</td>
</tr>
<tr>
<td>SPARE4</td>
<td>B11</td>
<td>AN19</td>
<td>2.5-V</td>
<td>Spare signals to the MAX II CPLD</td>
</tr>
<tr>
<td>SPARE5</td>
<td>B10</td>
<td>AM19</td>
<td>2.5-V</td>
<td>Spare signals to the MAX II CPLD</td>
</tr>
<tr>
<td>SPARE6</td>
<td>B9</td>
<td>AR19</td>
<td>2.5-V</td>
<td>Spare signals to the MAX II CPLD</td>
</tr>
<tr>
<td>SPARE7</td>
<td>B8</td>
<td>AP19</td>
<td>2.5-V</td>
<td>Spare signals to the MAX II CPLD</td>
</tr>
<tr>
<td>USB_MAX_D0</td>
<td>M3</td>
<td>—</td>
<td>2.5-V</td>
<td>USB configuration data bus</td>
</tr>
<tr>
<td>USB_MAX_D1</td>
<td>L4</td>
<td>—</td>
<td>2.5-V</td>
<td>USB configuration data bus</td>
</tr>
<tr>
<td>USB_MAX_D2</td>
<td>N1</td>
<td>—</td>
<td>2.5-V</td>
<td>USB configuration data bus</td>
</tr>
<tr>
<td>USB_MAX_D3</td>
<td>L3</td>
<td>—</td>
<td>2.5-V</td>
<td>USB configuration data bus</td>
</tr>
<tr>
<td>USB_MAX_D4</td>
<td>N2</td>
<td>—</td>
<td>2.5-V</td>
<td>USB configuration data bus</td>
</tr>
<tr>
<td>USB_MAX_D5</td>
<td>M4</td>
<td>—</td>
<td>2.5-V</td>
<td>USB configuration data bus</td>
</tr>
<tr>
<td>USB_MAX_D6</td>
<td>N3</td>
<td>—</td>
<td>2.5-V</td>
<td>USB configuration data bus</td>
</tr>
<tr>
<td>USB_MAX_D7</td>
<td>P2</td>
<td>—</td>
<td>2.5-V</td>
<td>USB configuration data bus</td>
</tr>
<tr>
<td>USB_MAX_PWR_ENn</td>
<td>E1</td>
<td>—</td>
<td>2.5-V</td>
<td>USB configuration power enable</td>
</tr>
<tr>
<td>USB_MAX_RDn</td>
<td>D1</td>
<td>—</td>
<td>2.5-V</td>
<td>USB configuration read from FIFO</td>
</tr>
<tr>
<td>USB_MAX_RXFn</td>
<td>F4</td>
<td>—</td>
<td>2.5-V</td>
<td>USB configuration receive enable</td>
</tr>
<tr>
<td>USB_MAX_TXEn</td>
<td>E2</td>
<td>—</td>
<td>2.5-V</td>
<td>USB configuration transmit enable</td>
</tr>
<tr>
<td>USB_MAX_WR</td>
<td>F3</td>
<td>—</td>
<td>2.5-V</td>
<td>USB configuration write to FIFO</td>
</tr>
<tr>
<td>USER_IMAGE</td>
<td>R7</td>
<td>—</td>
<td>2.5-V</td>
<td>User image for configuration</td>
</tr>
</tbody>
</table>
Table 2–6 lists the MAX II CPLD System Controller component reference and manufacturing information.

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturing Part Number</th>
<th>Manufacturer Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>U19</td>
<td>MAX II CPLD 256FBGA -3 LF 3.3 V VCCINT</td>
<td>Altera Corporation</td>
<td>EPM2210F256C3N</td>
<td><a href="http://www.altera.com">www.altera.com</a></td>
</tr>
</tbody>
</table>

### Configuration, Status, and Setup Elements

This section describes the board’s configuration, status, and setup elements.

#### Configuration

This section describes the FPGA, flash memory, and MAX II CPLD System Controller device programming methods supported by the Stratix V GT transceiver signal integrity development board.

The Stratix V GT transceiver signal integrity development board supports three configuration methods:

- Embedded USB-Blaster is the default method for configuring the FPGA at any time using the Quartus II Programmer in JTAG mode with the supplied USB cable.
- MAX II and flash FPP download for configuring the FPGA using stored images from the flash on either power-up or pressing the reset push-button (S5).
- JTAG header (J93) for initial debugging and to bring up the on-board USB-Blaster circuitry.

#### FPGA Programming over Embedded USB-Blaster

Programming the FPGA over embedded USB-Blaster is implemented using a type-B USB connector (CN1), a USB 2.0 PHY device, and an Altera MAX II CPLD EPM2210F256C3N (U19). This allows configuration of the FPGA using a USB cable that connects directly between the USB port on the board (CN1) and a USB port of a PC running the Quartus II software. The embedded USB-Blaster in the MAX II CPLD System Controller acts as a master to the JTAG chain.

A green USB-Blaster LED (D8) indicates the USB-Blaster activity. The embedded USB-Blaster is automatically disabled when you connect an external USB-Blaster to the JTAG chain at the JTAG header (J93).
Figure 2–3 shows the block diagram for the embedded USB-Blaster connection.

**MAX II CPLD System Controller**

The EPM570M100 MAX II CPLD (U16) is dedicated to the on-board USB-Blaster functionality. The CPLD connects to the FT245BL USB FIFO device on one side and drives the JTAG signals out the other side on the general purpose I/O (GPIO) pins. A 64x16 EEPROM connects to the CPLD device and stores the factory image for USB-JTAG functionality.

**FPGA Programming from Flash Memory**

On power-up, the MAX II CPLD System Controller’s parallel flash loader (PFL) configures the FPGA from the flash memory. The system controller uses the Altera Parallel Flash Loader (PFL) megafunction to read 16-bit data from the flash memory and converts it to FPP format. This 8-bit data is then written to the FPGA’s dedicated configuration pins during configuration.

The FPP configuration is implemented with an Altera MAX II CPLD together with the Micron PC2800AP30BF 1-Gb CFI NOR-type flash device (U21). The CPLD shares the flash interface with the FPGA. The configuration program select (`PGMSEL`) jumper (J28), selects between two Programmer Object Files (.pof) files (factory or user) stored in the flash. The configuration mode select signals, `MSEL[4:0]`, are pulled to `[00100]` FPP x16 on the board for FPP mode configuration.

There are three configuration status LEDs, `CONFIG_ERR`, `FACTORY_IMAGE`, and `USER_IMAGE` (D9, D10, D11) that indicate the status of the FPP configuration. For information on the configuration status LEDs, refer to “Status Elements” on page 2–18.

Table 2–7 lists the PGMSEL jumper settings.

**Table 2–7. PGMSEL Jumper Settings**

<table>
<thead>
<tr>
<th>Jumper</th>
<th>PGMSEL Setting</th>
<th>File Selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>Not installed (default)</td>
<td>0</td>
<td>Factory image</td>
</tr>
<tr>
<td>Installed</td>
<td>1</td>
<td>User image</td>
</tr>
</tbody>
</table>
Figure 2–4 shows the MAX II and flash FPP configuration.

**Flash Programming**

Flash programming is possible through a variety of methods using the Stratix V GT device.

The first method is to use the factory design called the Board Update Portal. This design is an embedded webserver, which serves the Board Update Portal web page. The web page allows you to select new FPGA designs including hardware, software, or both in an industry-standard S-Record File (.flash) and write the design to the user hardware page (page 1) of the flash over the network.

The secondary method is to use the pre-built PFL design included in the development kit. The development board implements the Altera PFL megafunction for flash programming. The PFL megafunction is a block of logic that is programmed into an Altera programmable logic device (FPGA or CPLD). The PFL functions as a utility for writing to a compatible flash device. This pre-built design contains the PFL megafunction that allows you to write either page 0, page 1, or other areas of flash over the USB interface using the Quartus II software. This method is used to restore the development board to its factory default settings.

Other methods to program the flash can be used as well, including the Nios® II processor.

For more information on the flash memory map storage, refer to the *Transceiver Signal Integrity Development Kit, Stratix V GT Edition User Guide.*
For more information on the Nios II processor, refer to the Nios II Processor page of the Altera website.

**FPGA Programming over External USB-Blaster**

The JTAG header provides another method for configuring the FPGA (U29) using an external USB-Blaster device with the Quartus II Programmer running on a PC. The external USB-Blaster connects to the board through the JTAG header (J93). The JTAG DIP switch (S7) allows the MAX II CPLD device to be removed from the JTAG chain so that the FPGA is the only device on the JTAG chain.

**JTAG Header**

The JTAG header provides another method for configuring the FPGA using an Altera USB-Blaster dongle with the Quartus II Programmer running on a PC. Figure 2–5 shows the schematic connections for the dedicated JTAG programming header (J93). The program MSEL switch (S7) allows the MAX II CPLD device to be removed from the JTAG chain so that the FPGA is the only device on the JTAG chain.

**Figure 2–5. JTAG Header**

The MAX II CPLD System Controller must be in the chain to use some of the GUI interfaces. To connect the MAX II CPLD in chain, set pins 6-7 of the program MSEL switch (S7) to 1.

For more information on the following topics, refer to the respective documents:

- PFL megafunction, refer to AN 386: Using the Parallel Flash Loader with the Quartus II Software.
Status Elements

The development board includes board-specific status LEDs and switches for enabling and configuring various features on the board, as well as a 16 character × 2 line LCD for displaying board power and temperature measurements. This section describes these status elements.

Status LEDs

Surface mount LEDs indicate the various status of the board. A logic 0 is driven on the I/O port to turn the LED on while a logic 1 is driven to turn the LED off.

Table 2–8 lists the LED board references, names, and functional descriptions.

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>LED Name</th>
<th>Schematic Signal Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>D3</td>
<td>POWER</td>
<td>—</td>
<td>Blue LED. Illuminates when 5-V power is active.</td>
</tr>
<tr>
<td>D7</td>
<td>FAN</td>
<td>FAN_LED</td>
<td>Amber LED. Illuminates when an over-temperature condition occurs. This occurrence should automatically turn on the fan.</td>
</tr>
<tr>
<td>D8</td>
<td>USB</td>
<td>USB_LED</td>
<td>Green LED. Illuminates when the MAX II CPLD System Controller is actively configuring the FPGA using the embedded USB-Blaster.</td>
</tr>
<tr>
<td>D9</td>
<td>ERROR</td>
<td>CONFIG_ERR</td>
<td>Red LED. Illuminates when the MAX II CPLD System Controller fails to configure the FPGA. Driven by the MAX II CPLD System Controller.</td>
</tr>
<tr>
<td>D10</td>
<td>FACTORY</td>
<td>FACTORY_IMAGE</td>
<td>Green LED. Illuminates when the factory image is successfully loaded into the FPGA. Driven by the MAX II CPLD System Controller.</td>
</tr>
<tr>
<td>D11</td>
<td>USER</td>
<td>USER_IMAGE</td>
<td>Green LED. Illuminates when the user image is successfully loaded into the FPGA. Driven by the MAX II CPLD System Controller.</td>
</tr>
<tr>
<td>D12</td>
<td>TX</td>
<td>ENET_LED_TX</td>
<td>Green LED. Blinks to indicate Ethernet PHY transmit activity. Driven by the Marvell 88E1111 PHY.</td>
</tr>
<tr>
<td>D13</td>
<td>RX</td>
<td>ENET_LED_RX</td>
<td>Green LED. Blinks to indicate Ethernet PHY receive activity. Driven by the Marvell 88E1111 PHY.</td>
</tr>
<tr>
<td>D14</td>
<td>DUPLEX</td>
<td>ENET_LED_DUPLEX</td>
<td>Green LED. Illuminates to indicate Ethernet full duplex status.</td>
</tr>
<tr>
<td>D15</td>
<td>1000</td>
<td>ENET_LED_LINK1000</td>
<td>Green LED. Illuminates to indicate Ethernet linked at 1000 Mbps connection speed. Driven by the Marvell 88E1111 PHY.</td>
</tr>
<tr>
<td>D16</td>
<td>100</td>
<td>ENET_LED_LINK100</td>
<td>Green LED. Illuminates to indicate Ethernet linked at 100 Mbps connection speed. Driven by the Marvell 88E1111 PHY.</td>
</tr>
<tr>
<td>D17</td>
<td>10</td>
<td>ENET_LED_LINK10</td>
<td>Green LED. Illuminates to indicate Ethernet linked at 10 Mbps connection speed. Driven by the Marvell 88E1111 PHY.</td>
</tr>
</tbody>
</table>
Table 2–9 lists the board-specific LEDs component references and manufacturing information.

### Setup Elements

The development board includes several different kinds of setup elements. This section describes the following setup elements:

- FPP configuration or MAX II bypass DIP switch
- Program select jumper
- MAX II reset push button
- CPU reset push button

#### FPP Configuration/MAX II Bypass DIP Switch

The FPP configuration or MAX II bypass DIP switch (S7) controls the FPP configuration mode and also selects the MAX II CPLD to be in the JTAG chain. Table 2–10 lists the switch settings and descriptions.

<table>
<thead>
<tr>
<th>Board Reference ($S7$)</th>
<th>Schematic Signal Name</th>
<th>Description</th>
<th>Default</th>
</tr>
</thead>
</table>
| 1–12                   | MSEL0                  | ON : Logic 0 is selected for MSEL0
                          |                        | OFF : Logic 1 is selected for MSEL0 | ON     |
| 2–11                   | MSEL1                  | ON : Logic 0 is selected for MSEL1
                          |                        | OFF : Logic 1 is selected for MSEL1 | ON     |
| 3–10                   | MSEL2                  | ON : Logic 0 is selected for MSEL2
                          |                        | OFF : Logic 1 is selected for MSEL2 | OFF    |
| 4–9                    | MSEL3                  | ON : Logic 0 is selected for MSEL3
                          |                        | OFF : Logic 1 is selected for MSEL3 | ON     |
| 5–8                    | MSEL4                  | ON : Logic 0 is selected for MSEL4
                          |                        | OFF : Logic 1 is selected for MSEL4 | ON     |
| 6–7                    | MAX_BYPASS             | ON : MAX II CPLD EPM2210 System Controller in-chain
                          |                        | OFF : Bypass MAX II CPLD EPM2210 System Controller | ON     |
Table 2–11 lists the DIP switch component reference and manufacturing information.

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
<th>Manufacturer Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>S7</td>
<td>Six-Position slide DIP switch</td>
<td>Grayhill</td>
<td>97C06RT</td>
<td><a href="http://www.grayhill.com">www.grayhill.com</a></td>
</tr>
</tbody>
</table>

**Program Select Jumper**

The program select jumper, PGMSEL (J28) is an input to the MAX II CPLD System Controller. After a power-on or reset configuration, the MAX II CPLD System Controller configures the FPGA to either factory or user image. For information on the jumper settings, refer to “FPGA Programming from Flash Memory” on page 2–15.

**Reset Push Button**

The reset push button, \( \text{RESETn} \), is an input to the MAX II CPLD System Controller. This push button is the default logic reset for the CPLD logic.

Table 2–12 lists the MAX II reset push button component reference and manufacturing information.

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
<th>Manufacturer Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>S5</td>
<td>Push Button</td>
<td>Panasonic Corporation</td>
<td>EVQPAC07K</td>
<td><a href="http://www.panasonic.com">www.panasonic.com</a></td>
</tr>
</tbody>
</table>

**CPU Reset Push Button**

The CPU reset push button, \( \text{CPURSTn} \), (S6) connects to a regular I/O pin of the FPGA and serves as a reset for the NIOS II when you load the application.

Table 2–13 lists the CPU reset configuration push button component reference and manufacturing information.

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
<th>Manufacturer Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>S6</td>
<td>Push Button</td>
<td>Panasonic Corporation</td>
<td>EVQPAC07K</td>
<td><a href="http://www.panasonic.com">www.panasonic.com</a></td>
</tr>
</tbody>
</table>
Clock Circuitry

This section describes the board’s dedicated and general purpose clocks.

Dedicated Transceiver Clocks

Four differential clock sources are provided from the I2C programmable VCO oscillators to the dedicated REFCLK input pins of transceiver blocks on both sides of the FPGA. The default frequencies for these four oscillators at startup are 625 MHz, 644.53125 MHz, 706.25 MHz, and 875 MHz. The default frequencies can be overridden and you can program a different frequency into the oscillators to support other protocols. Each oscillator supports a programmable frequency range of 10 MHz–1.4 GHz and provides a trigger output to an SMA connector for scope or other lab equipment triggering purposes.

Figure 2–6 shows the default frequencies of all external clocks going to the Stratix V GT transceiver signal integrity development board.

Table 2–14 lists the frequency of these oscillators and the application it supports.

<table>
<thead>
<tr>
<th>Frequency</th>
<th>I/O Standard</th>
<th>Clock Buffer</th>
</tr>
</thead>
<tbody>
<tr>
<td>644.53125 MHz</td>
<td>LVDS</td>
<td>IDT5T9306</td>
</tr>
<tr>
<td>625 MHz</td>
<td>LVDS</td>
<td>IDT5T9306</td>
</tr>
<tr>
<td>706.25 MHz</td>
<td>LVDS</td>
<td>IDT5T9306</td>
</tr>
<tr>
<td>875 MHz</td>
<td>LVDS</td>
<td>IDT5T9306</td>
</tr>
</tbody>
</table>
In addition to the four oscillators, each side has a dedicated differential REFCLK input from a pair of SMA connectors to allow an external clock source.

**General-Purpose Clocks**

Three general-purpose clocks are provided to the FPGA global clock inputs for general FPGA design. The clocks consist of the following components:

- A 50-MHz oscillator through an ICS8304 buffer for NIOS II applications at clock input CLK2p. This clock also routes to the MAX II device for FPP configuration and to the clock inputs CLK12p and CLK16p of banks 7 and 8.

- A 25-MHz crystal oscillator through an ICS557-03 spread spectrum differential clock buffer. The available frequencies and down spread percentages available from the spread spectrum buffer is shown in Table 2–15.

- An external differential clock source from SMA at CLK10p/n (J70/J71).

Figure 2–7 shows the general purpose clocks going in to the Stratix V GT transceiver signal integrity development board.

**Figure 2–7. Transceiver Signal Integrity Development Kit General Purpose Clocks**

| Table 2–15 | lists the spread spectrum clock settings and frequencies. |

**Table 2–15. Spread Spectrum Clock Settings and Frequencies**

<table>
<thead>
<tr>
<th>Spread Spectrum Buffer (inputs)</th>
<th>Output Clock Select</th>
<th>Spread (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SS1/S1 0</td>
<td>SS0/S0 0</td>
<td>25 MHz (default)</td>
</tr>
<tr>
<td>0 1</td>
<td>100 MHz</td>
<td>Down −0.5</td>
</tr>
<tr>
<td>1 0</td>
<td>125 MHz</td>
<td>Down −0.75</td>
</tr>
<tr>
<td>1 1</td>
<td>200 MHz</td>
<td>No spread</td>
</tr>
</tbody>
</table>
Embedded USB-Blaster Clocks

A separate 6-MHz crystal and 24-MHz oscillator are dedicated for the embedded USB-Blaster circuitry. The 6-MHz oscillator is to clock the FTDI FT245 USB PHY device while the 24-MHz oscillator is to clock the MAX II CPLD device. Refer to “FPGA Programming over Embedded USB-Blaster” on page 2–14 for the embedded USB-Blaster implementation.

Table 2–16 lists the crystal oscillators component references and manufacturing information.

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
<th>Manufacturer Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>X1</td>
<td>Crystal oscillator, 6.0 MHz, SMD</td>
<td>ESC Inc.</td>
<td>ECSX-60-32-5P-TR</td>
<td><a href="http://www.ecsxtal.com">www.ecsxtal.com</a></td>
</tr>
<tr>
<td>Y1</td>
<td>Crystal oscillator, CMOS, 2.5 V, 24.000 MHz, SMT, ±50ppm</td>
<td>Epson</td>
<td>SG-310SDF 24.0000M-B3</td>
<td><a href="http://www.epsontoyocom.co.jp/english/index.html">www.epsontoyocom.co.jp/english/index.html</a></td>
</tr>
</tbody>
</table>

Transceiver Channels

The transceiver signal integrity development board dedicates 31 (out of 32) 12.5-Gbps transceiver channels from both the left and right sides of the device to various backplane connectors—SFP+ and XFP cages, and SMA connectors. One 12.5-Gbps channel on the 28 Gbps side of the device is a dedicated CMU clock input from the SMA connectors. For the Stratix V GT device, the four 25.78-Gbps ATT channels connects to the MMPX connectors.
Figure 2–8 shows the complete transceiver usage diagram.

Table 2–17 lists the connection requirements for the transceiver channels.

<table>
<thead>
<tr>
<th>Signal Group</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>5-12.5-Gbps TX to Tyco backplane connector (left side of transceiver block)</td>
<td>Length match between this TX group</td>
</tr>
<tr>
<td>5-12.5-Gbps RX to Tyco backplane connector (left side of transceiver block)</td>
<td>Length match between this RX group</td>
</tr>
<tr>
<td>2-12.5-Gbps TX to Tyco backplane connector (right side of transceiver block)</td>
<td>Length match between this TX pair</td>
</tr>
<tr>
<td>2-12.5-Gbps RX to Tyco backplane connector (right side of transceiver block)</td>
<td>Length match between this RX pair</td>
</tr>
<tr>
<td>5-12.5-Gbps TX to Amphenol/FCI backplane connector (left side of transceiver block)</td>
<td>Length match between this TX group</td>
</tr>
<tr>
<td>5-12.5-Gbps RX to Amphenol/FCI backplane connector (left side of transceiver block)</td>
<td>Length match between this RX group</td>
</tr>
<tr>
<td>2-12.5-Gbps TX to Amphenol/FCI backplane connector (right side of transceiver block)</td>
<td>Length match between this TX pair</td>
</tr>
<tr>
<td>2-12.5-Gbps RX to Amphenol/FCI backplane connector (right side of transceiver block)</td>
<td>Length match between this RX pair</td>
</tr>
<tr>
<td>5-12.5-Gbps TX to Molex connector (left side of transceiver block)</td>
<td>Length match between this TX group</td>
</tr>
<tr>
<td>5-12.5-Gbps RX to Molex connector (left side of transceiver block)</td>
<td>Length match between this RX group</td>
</tr>
<tr>
<td>2-12.5-Gbps TX to Molex connector (right side of transceiver block)</td>
<td>Length match between this TX pair</td>
</tr>
<tr>
<td>2-12.5-Gbps RX to Molex connector (right side of transceiver block)</td>
<td>Length match between this RX pair</td>
</tr>
</tbody>
</table>
Backplane Connectors

The development board supports three different types of 10Gbase-KR reference backplanes by directly mating with the backplanes made from Tyco, Amphenol, and Molex manufacturers.

Table 2–18 lists the Amphenol backplane connector pin assignments.

Table 2–18. Amphenol Backplane Connector Pin Assignments, Signal Names and Functions  
(Part 1 of 2)

<table>
<thead>
<tr>
<th>Board Reference (J32)</th>
<th>Schematic Signal Name</th>
<th>I/O Standard</th>
<th>Stratix V GT Device Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>G5</td>
<td>GXB_TXLN_19</td>
<td>1.4-V PCML</td>
<td>K35</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>H5</td>
<td>GXB_TXLP_19</td>
<td>1.4-V PCML</td>
<td>K34</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>E5</td>
<td>GXB_TXLN_20</td>
<td>1.4-V PCML</td>
<td>J37</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>F5</td>
<td>GXB_TXLP_20</td>
<td>1.4-V PCML</td>
<td>J36</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>E4</td>
<td>GXB_TXLN_21</td>
<td>1.4-V PCML</td>
<td>G37</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>F4</td>
<td>GXB_TXLP_21</td>
<td>1.4-V PCML</td>
<td>G36</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>C5</td>
<td>GXB_TXLN_22</td>
<td>1.4-V PCML</td>
<td>E37</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>D5</td>
<td>GXB_TXLP_22</td>
<td>1.4-V PCML</td>
<td>E36</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>C4</td>
<td>GXB_TXLN_23</td>
<td>1.4-V PCML</td>
<td>C37</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>D4</td>
<td>GXB_TXLP_23</td>
<td>1.4-V PCML</td>
<td>C36</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>E6</td>
<td>GXB_TXRN_18</td>
<td>1.4-V PCML</td>
<td>M5</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>F6</td>
<td>GXB_TXRP_18</td>
<td>1.4-V PCML</td>
<td>M6</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>C6</td>
<td>GXB_TXRN_23</td>
<td>1.4-V PCML</td>
<td>C3</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>D6</td>
<td>GXB_TXRP_23</td>
<td>1.4-V PCML</td>
<td>C4</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>C1</td>
<td>GXBRXLN_19</td>
<td>1.4-V PCML</td>
<td>K39</td>
<td>GXB receive</td>
</tr>
<tr>
<td>D1</td>
<td>GXBRXLP_19</td>
<td>1.4-V PCML</td>
<td>K38</td>
<td>GXB receive</td>
</tr>
<tr>
<td>C2</td>
<td>GXBRXLN_20</td>
<td>1.4-V PCML</td>
<td>H39</td>
<td>GXB receive</td>
</tr>
<tr>
<td>D2</td>
<td>GXBRXLP_20</td>
<td>1.4-V PCML</td>
<td>H38</td>
<td>GXB receive</td>
</tr>
<tr>
<td>E1</td>
<td>GXBRXLN_21</td>
<td>1.4-V PCML</td>
<td>F39</td>
<td>GXB receive</td>
</tr>
<tr>
<td>F1</td>
<td>GXBRXLP_21</td>
<td>1.4-V PCML</td>
<td>F38</td>
<td>GXB receive</td>
</tr>
<tr>
<td>E2</td>
<td>GXBRXLN_22</td>
<td>1.4-V PCML</td>
<td>D39</td>
<td>GXB receive</td>
</tr>
</tbody>
</table>
Table 2–18. Amphenol Backplane Connector Pin Assignments, Signal Names and Functions (Part 2 of 2)

<table>
<thead>
<tr>
<th>Board Reference (J32)</th>
<th>Schematic Signal Name</th>
<th>I/O Standard</th>
<th>Stratix V GT Device Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F2</td>
<td>GXBRXLP_22</td>
<td>1.4-V PCML</td>
<td>D38</td>
<td>GXB receive</td>
</tr>
<tr>
<td>G2</td>
<td>GXBRXLN_23</td>
<td>1.4-V PCML</td>
<td>B39</td>
<td>GXB receive</td>
</tr>
<tr>
<td>H2</td>
<td>GXBRXLP_23</td>
<td>1.4-V PCML</td>
<td>B38</td>
<td>GXB receive</td>
</tr>
<tr>
<td>E3</td>
<td>GXBRXRN_18</td>
<td>1.4-V PCML</td>
<td>L3</td>
<td>GXB receive</td>
</tr>
<tr>
<td>F3</td>
<td>GXBRXRP_18</td>
<td>1.4-V PCML</td>
<td>L4</td>
<td>GXB receive</td>
</tr>
<tr>
<td>C3</td>
<td>GXBRXRN_23</td>
<td>1.4-V PCML</td>
<td>B1</td>
<td>GXB receive</td>
</tr>
<tr>
<td>D3</td>
<td>GXBRXRP_23</td>
<td>1.4-V PCML</td>
<td>B2</td>
<td>GXB receive</td>
</tr>
</tbody>
</table>

Table 2–19 lists the Tyco backplane connector pin assignments.

Table 2–19. Tyco Backplane Connector Pin Assignments, Signal Names and Functions (Part 1 of 2)

<table>
<thead>
<tr>
<th>Board Reference (J33)</th>
<th>Schematic Signal Name</th>
<th>I/O Standard</th>
<th>Stratix V GT Device Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F11</td>
<td>GXB_TXLN_0</td>
<td>1.4-V PCML</td>
<td>AU37</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>G11</td>
<td>GXB_TXLN_1</td>
<td>1.4-V PCML</td>
<td>AR37</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>H11</td>
<td>GXB_TXLN_2</td>
<td>1.4-V PCML</td>
<td>AN37</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>F14</td>
<td>GXB_TXLN_3</td>
<td>1.4-V PCML</td>
<td>AL37</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>G14</td>
<td>GXB_TXLN_4</td>
<td>1.4-V PCML</td>
<td>AK35</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>F12</td>
<td>GXB_TXLP_0</td>
<td>1.4-V PCML</td>
<td>AU36</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>G12</td>
<td>GXB_TXLP_1</td>
<td>1.4-V PCML</td>
<td>AR36</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>H12</td>
<td>GXB_TXLP_2</td>
<td>1.4-V PCML</td>
<td>AN36</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>F15</td>
<td>GXB_TXLP_3</td>
<td>1.4-V PCML</td>
<td>AL36</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>G15</td>
<td>GXB_TXLP_4</td>
<td>1.4-V PCML</td>
<td>AK34</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>F18</td>
<td>GXB_TXRN_0</td>
<td>1.4-V PCML</td>
<td>AU3</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>G18</td>
<td>GXB_TXRN_5</td>
<td>1.4-V PCML</td>
<td>AH5</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>F17</td>
<td>GXB_TXRP_0</td>
<td>1.4-V PCML</td>
<td>AU4</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>G17</td>
<td>GXB_TXRP_5</td>
<td>1.4-V PCML</td>
<td>AH6</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>B2</td>
<td>GXBRXLN_0</td>
<td>1.4-V PCML</td>
<td>AV39</td>
<td>GXB receive</td>
</tr>
<tr>
<td>C2</td>
<td>GXBRXLN_1</td>
<td>1.4-V PCML</td>
<td>AT39</td>
<td>GXB receive</td>
</tr>
<tr>
<td>B5</td>
<td>GXBRXLN_2</td>
<td>1.4-V PCML</td>
<td>AP39</td>
<td>GXB receive</td>
</tr>
<tr>
<td>A5</td>
<td>GXBRXLN_3</td>
<td>1.4-V PCML</td>
<td>AM39</td>
<td>GXB receive</td>
</tr>
<tr>
<td>A2</td>
<td>GXBRXLN_4</td>
<td>1.4-V PCML</td>
<td>AJ37</td>
<td>GXB receive</td>
</tr>
<tr>
<td>B3</td>
<td>GXBRXLP_0</td>
<td>1.4-V PCML</td>
<td>AV38</td>
<td>GXB receive</td>
</tr>
<tr>
<td>C3</td>
<td>GXBRXLP_1</td>
<td>1.4-V PCML</td>
<td>AT38</td>
<td>GXB receive</td>
</tr>
<tr>
<td>B6</td>
<td>GXBRXLP_2</td>
<td>1.4-V PCML</td>
<td>AP38</td>
<td>GXB receive</td>
</tr>
<tr>
<td>A6</td>
<td>GXBRXLP_3</td>
<td>1.4-V PCML</td>
<td>AM38</td>
<td>GXB receive</td>
</tr>
<tr>
<td>A3</td>
<td>GXBRXLP_4</td>
<td>1.4-V PCML</td>
<td>AJ36</td>
<td>GXB receive</td>
</tr>
<tr>
<td>A9</td>
<td>GXBRXRN_0</td>
<td>1.4-V PCML</td>
<td>AV1</td>
<td>GXB receive</td>
</tr>
<tr>
<td>B9</td>
<td>GXBRXRN_5</td>
<td>1.4-V PCML</td>
<td>AJ3</td>
<td>GXB receive</td>
</tr>
</tbody>
</table>
### Table 2–19. Tyco Backplane Connector Pin Assignments, Signal Names and Functions (Part 2 of 2)

<table>
<thead>
<tr>
<th>Board Reference (J33)</th>
<th>Schematic Signal Name</th>
<th>I/O Standard</th>
<th>Stratix V GT Device Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A8</td>
<td>GXBRXRP_0</td>
<td>1.4-V PCML</td>
<td>AV2</td>
<td>GXB receive</td>
</tr>
<tr>
<td>B8</td>
<td>GXBRXRP_5</td>
<td>1.4-V PCML</td>
<td>AJ4</td>
<td>GXB receive</td>
</tr>
</tbody>
</table>

Table 2–20 lists the Molex backplane connector pin assignments.

### Table 2–20. Molex Backplane Connector Pin Assignments, Signal Names and Functions

<table>
<thead>
<tr>
<th>Board Reference (J34)</th>
<th>Schematic Signal Name</th>
<th>I/O Standard</th>
<th>Stratix V GT Device Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>E9</td>
<td>GXB_TXLN_6</td>
<td>1.4-V PCML</td>
<td>AG37</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>H9</td>
<td>GXB_TXLN_7</td>
<td>1.4-V PCML</td>
<td>AF35</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>B9</td>
<td>GXB_TXLN_8</td>
<td>1.4-V PCML</td>
<td>AD35</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>D10</td>
<td>GXB_TXLN_9</td>
<td>1.4-V PCML</td>
<td>AC37</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>G10</td>
<td>GXB_TXLN_10</td>
<td>1.4-V PCML</td>
<td>AB35</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>F9</td>
<td>GXB_TXLP_6</td>
<td>1.4-V PCML</td>
<td>AG36</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>J9</td>
<td>GXB_TXLP_7</td>
<td>1.4-V PCML</td>
<td>AF34</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>C9</td>
<td>GXB_TXLP_8</td>
<td>1.4-V PCML</td>
<td>AD34</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>E10</td>
<td>GXB_TXLP_9</td>
<td>1.4-V PCML</td>
<td>AC36</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>H10</td>
<td>GXB_TXLP_10</td>
<td>1.4-V PCML</td>
<td>AB34</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>D8</td>
<td>GXB_TXRN_6</td>
<td>1.4-V PCML</td>
<td>AG3</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>G8</td>
<td>GXB_TXRN_11</td>
<td>1.4-V PCML</td>
<td>Y5</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>E8</td>
<td>GXB_TXRP_6</td>
<td>1.4-V PCML</td>
<td>AG4</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>H8</td>
<td>GXB_TXRP_11</td>
<td>1.4-V PCML</td>
<td>Y6</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>H3</td>
<td>GXBRLXLN_6</td>
<td>1.4-V PCML</td>
<td>AH39</td>
<td>GXB receive</td>
</tr>
<tr>
<td>K2</td>
<td>GXBRLXLN_7</td>
<td>1.4-V PCML</td>
<td>AE37</td>
<td>GXB receive</td>
</tr>
<tr>
<td>G4</td>
<td>GXBRLXLN_8</td>
<td>1.4-V PCML</td>
<td>AF39</td>
<td>GXB receive</td>
</tr>
<tr>
<td>L3</td>
<td>GXBRLXLN_9</td>
<td>1.4-V PCML</td>
<td>AD39</td>
<td>GXB receive</td>
</tr>
<tr>
<td>K4</td>
<td>GXBRLXLN_10</td>
<td>1.4-V PCML</td>
<td>AB39</td>
<td>GXB receive</td>
</tr>
<tr>
<td>J3</td>
<td>GXBRLXLP_6</td>
<td>1.4-V PCML</td>
<td>AH38</td>
<td>GXB receive</td>
</tr>
<tr>
<td>L2</td>
<td>GXBRLXLP_7</td>
<td>1.4-V PCML</td>
<td>AE36</td>
<td>GXB receive</td>
</tr>
<tr>
<td>H4</td>
<td>GXBRLXLP_8</td>
<td>1.4-V PCML</td>
<td>AF38</td>
<td>GXB receive</td>
</tr>
<tr>
<td>M3</td>
<td>GXBRLXLP_9</td>
<td>1.4-V PCML</td>
<td>AD38</td>
<td>GXB receive</td>
</tr>
<tr>
<td>L4</td>
<td>GXBRLXLP_10</td>
<td>1.4-V PCML</td>
<td>AB38</td>
<td>GXB receive</td>
</tr>
<tr>
<td>E3</td>
<td>GXBRLRXN_6</td>
<td>1.4-V PCML</td>
<td>AH1</td>
<td>GXB receive</td>
</tr>
<tr>
<td>G2</td>
<td>GXBRLRXN_11</td>
<td>1.4-V PCML</td>
<td>AA3</td>
<td>GXB receive</td>
</tr>
<tr>
<td>F3</td>
<td>GXBRLXRP_6</td>
<td>1.4-V PCML</td>
<td>AH2</td>
<td>GXB receive</td>
</tr>
<tr>
<td>H2</td>
<td>GXBRLXRP_11</td>
<td>1.4-V PCML</td>
<td>AA4</td>
<td>GXB receive</td>
</tr>
</tbody>
</table>
Table 2–21 lists the backplane connector component reference and the manufacturing information.

### Table 2–21. User-Defined Push Button Component Reference and Manufacturing Information

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
<th>Manufacturer Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>J32</td>
<td>Connector, 4-pair, 6 position, Amphenol Xcede</td>
<td>Amphenol</td>
<td>AX400-00682</td>
<td><a href="http://www.amphenol.com">www.amphenol.com</a></td>
</tr>
<tr>
<td>J33</td>
<td>Connector, 8-pair, 6-columns, receptacle, Tyco Strada</td>
<td>Tyco Electronics</td>
<td>2149323-1</td>
<td><a href="http://www.te.com">www.te.com</a></td>
</tr>
<tr>
<td>J34</td>
<td>Connector, 4-pair, receptacle, Molex Impact</td>
<td>Molex</td>
<td>76160-5020</td>
<td><a href="http://www.molex.com">www.molex.com</a></td>
</tr>
</tbody>
</table>

### General User Input/Output

This section describes the user I/O interface to the FPGA. This section describes the following I/O elements:

- User-defined push buttons
- User-defined DIP switch
- User-defined LEDs
- Character LCD

### User-Defined Push Buttons

The development board includes four user-defined push buttons that allow you to interact with the Stratix V GT device. When you press and hold down the push button, the device pin is set to logic 0; when you release the push button, the device pin is set to logic 1. There is no board-specific function for these general user push buttons.

Table 2–22 lists the user-defined push button schematic signal names and their corresponding Stratix V GT device pin numbers.

### Table 2–22. User-Defined Push Button Schematic Signal Names and Functions

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Schematic Signal Name</th>
<th>I/O Standard</th>
<th>Stratix V GT Device Pin Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1</td>
<td>USER_PB0</td>
<td>2.5-V</td>
<td>H29</td>
</tr>
<tr>
<td>S2</td>
<td>USER_PB1</td>
<td>2.5-V</td>
<td>G28</td>
</tr>
<tr>
<td>S3</td>
<td>USER_PB2</td>
<td>2.5-V</td>
<td>K27</td>
</tr>
<tr>
<td>S4</td>
<td>USER_PB3</td>
<td>2.5-V</td>
<td>J27</td>
</tr>
</tbody>
</table>

Table 2–23 lists the user-defined push button component reference and the manufacturing information.

### Table 2–23. User-Defined Push Button Component Reference and Manufacturing Information

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
<th>Manufacturer Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>S1–S4</td>
<td>Push button</td>
<td>Panasonic Corporation</td>
<td>EVQPAC07K</td>
<td><a href="http://www.panasonic.com">www.panasonic.com</a></td>
</tr>
</tbody>
</table>
User-Defined DIP Switch

Board reference SW4 is a 8-pin DIP switch. The switches are user-defined, and are provided additional FPGA input control. When the switch is in the OPEN or ON position, a logic 1 is selected. When the switch is in the CLOSED or OFF position, a logic 0 is selected. There is no board-specific function for these switches.

Table 2–24 lists the user-defined DIP switch schematic signal names and their corresponding Stratix V GT pin numbers.

<table>
<thead>
<tr>
<th>Board Reference (SW4)</th>
<th>Schematic Signal Name</th>
<th>I/O Standard</th>
<th>Stratix V GT Device Pin Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>S5_UNLOCK</td>
<td>2.5-V</td>
<td>—</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>(Connects to USB MAX II pin B6)</td>
</tr>
<tr>
<td>2</td>
<td>USER_DIP6</td>
<td>2.5-V</td>
<td>H34</td>
</tr>
<tr>
<td>3</td>
<td>USER_DIP5</td>
<td>2.5-V</td>
<td>F33</td>
</tr>
<tr>
<td>4</td>
<td>USER_DIP4</td>
<td>2.5-V</td>
<td>G33</td>
</tr>
<tr>
<td>5</td>
<td>USER_DIP3</td>
<td>2.5-V</td>
<td>H32</td>
</tr>
<tr>
<td>6</td>
<td>USER_DIP2</td>
<td>2.5-V</td>
<td>D34</td>
</tr>
<tr>
<td>7</td>
<td>USER_DIP1</td>
<td>2.5-V</td>
<td>E34</td>
</tr>
<tr>
<td>8</td>
<td>USER_DIP0</td>
<td>2.5-V</td>
<td>D33</td>
</tr>
</tbody>
</table>

Table 2–25 lists the user-defined DIP switch component reference and the manufacturing information.

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
<th>Manufacturer Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>SW4</td>
<td>Eight-Position DIP switch</td>
<td>Grayhill</td>
<td>76SB08ST</td>
<td><a href="http://www.grayhill.com">www.grayhill.com</a></td>
</tr>
</tbody>
</table>

User-Defined LEDs

The development board includes eight user-defined LEDs. Board references D18 through D25 are user LEDs that allow status and debugging signals to be driven to the LEDs from the designs loaded into the Stratix V GT device. The LEDs illuminate when a logic 0 is driven, and turns off when a logic 1 is driven. There is no board-specific function for these LEDs.

Table 2–26 lists the user-defined LED schematic signal names and their corresponding Stratix V GT pin numbers.

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Schematic Signal Name</th>
<th>I/O Standard</th>
<th>Stratix V GT Device Pin Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>D18</td>
<td>USER_LED_0</td>
<td>2.5-V</td>
<td>B32</td>
</tr>
<tr>
<td>D19</td>
<td>USER_LED_1</td>
<td>2.5-V</td>
<td>A32</td>
</tr>
<tr>
<td>D20</td>
<td>USER_LED_2</td>
<td>2.5-V</td>
<td>B34</td>
</tr>
<tr>
<td>D21</td>
<td>USER_LED_3</td>
<td>2.5-V</td>
<td>A34</td>
</tr>
</tbody>
</table>
Table 2–26. User-Defined LED Schematic Signal Names and Functions (Part 2 of 2)

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Schematic Signal Name</th>
<th>I/O Standard</th>
<th>Stratix V GT Device Pin Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>D22</td>
<td>USER_LED_4</td>
<td>2.5-V</td>
<td>C34</td>
</tr>
<tr>
<td>D23</td>
<td>USER_LED_5</td>
<td>2.5-V</td>
<td>C33</td>
</tr>
<tr>
<td>D24</td>
<td>USER_LED_6</td>
<td>2.5-V</td>
<td>F32</td>
</tr>
<tr>
<td>D25</td>
<td>USER_LED_7</td>
<td>2.5-V</td>
<td>E32</td>
</tr>
</tbody>
</table>

Table 2–27 lists the user-defined LED component reference and the manufacturing information.

Table 2–27. User-Defined LED Component Reference and Manufacturing Information

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Device Description</th>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
<th>Manufacturer Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>D18–D25</td>
<td>Green LEDs, 1206, SMT, Clear Lens, 2.1 V</td>
<td>Lumex Inc.</td>
<td>SML-LX1206GC-TR</td>
<td><a href="http://www.lumex.com">www.lumex.com</a></td>
</tr>
</tbody>
</table>

Character LCD

The development board includes a single 14-pin 0.1” pitch dual-row header that interfaces to a 16 character x 2 line Lumex LCD display. The LCD has a 14-pin receptacle that mounts directly to the board’s 14-pin header, so it can be easily removed for access to components under the display. You can also use the header for debugging or other purposes.

Table 2–28 summarizes the LCD pin assignments. The signal names and directions are relative to the Stratix V GT device.

Table 2–28. LCD Pin Assignments, Schematic Signal Names, and Functions

<table>
<thead>
<tr>
<th>Board Reference (J30)</th>
<th>Schematic Signal Name</th>
<th>I/O Standard</th>
<th>Stratix V GT Device Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>4</td>
<td>LCD_D_Cn</td>
<td>2.5-V</td>
<td>B14</td>
<td>LCD data or command select</td>
</tr>
<tr>
<td>5</td>
<td>LCD_Wen</td>
<td>2.5-V</td>
<td>B13</td>
<td>LCD write enable</td>
</tr>
<tr>
<td>6</td>
<td>LCD_EN</td>
<td>2.5-V</td>
<td>A14</td>
<td>LCD chip select</td>
</tr>
<tr>
<td>7</td>
<td>LCD_DATA0</td>
<td>2.5-V</td>
<td>A13</td>
<td>LCD data bus</td>
</tr>
<tr>
<td>8</td>
<td>LCD_DATA1</td>
<td>2.5-V</td>
<td>B16</td>
<td>LCD data bus</td>
</tr>
<tr>
<td>9</td>
<td>LCD_DATA2</td>
<td>2.5-V</td>
<td>A16</td>
<td>LCD data bus</td>
</tr>
<tr>
<td>10</td>
<td>LCD_DATA3</td>
<td>2.5-V</td>
<td>C15</td>
<td>LCD data bus</td>
</tr>
<tr>
<td>11</td>
<td>LCD_DATA4</td>
<td>2.5-V</td>
<td>C14</td>
<td>LCD data bus</td>
</tr>
<tr>
<td>12</td>
<td>LCD_DATA5</td>
<td>2.5-V</td>
<td>D15</td>
<td>LCD data bus</td>
</tr>
<tr>
<td>13</td>
<td>LCD_DATA6</td>
<td>2.5-V</td>
<td>D16</td>
<td>LCD data bus</td>
</tr>
<tr>
<td>14</td>
<td>LCD_DATA7</td>
<td>2.5-V</td>
<td>F14</td>
<td>LCD data bus</td>
</tr>
</tbody>
</table>
Table 2–29 shows the LCD pin definitions, and is an excerpt from the Lumex data sheet.

Table 2–29. LCD Pin Definitions and Functions

<table>
<thead>
<tr>
<th>Pin Number</th>
<th>Symbol</th>
<th>Level</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$V_{DD}$</td>
<td>—</td>
<td>Power supply 5 V</td>
</tr>
<tr>
<td>2</td>
<td>$V_{SS}$</td>
<td>—</td>
<td>GND (0 V)</td>
</tr>
<tr>
<td>3</td>
<td>$V_0$</td>
<td>—</td>
<td>For LCD drive</td>
</tr>
<tr>
<td>4</td>
<td>RS</td>
<td>H/L</td>
<td>Register select signal</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>H: Data input</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>L: Instruction input</td>
</tr>
<tr>
<td>5</td>
<td>R/W</td>
<td>H/L</td>
<td>H: Data read (module to MPU)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>L: Data write (MPU to module)</td>
</tr>
<tr>
<td>6</td>
<td>E</td>
<td>H, H to L</td>
<td>Enable</td>
</tr>
<tr>
<td>7–14</td>
<td>DB0–DB7</td>
<td>H/L</td>
<td>Data bus, software selectable 4-bit or 8-bit mode</td>
</tr>
</tbody>
</table>

For more information such as timing, character maps, interface guidelines, and other related documentation, visit www.lumex.com.

Table 2–30 lists the LCD component references and the manufacturing information.

Table 2–30. LCD Component References and Manufacturing Information

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturer Part Number</th>
<th>Manufacturer Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>J30</td>
<td>2×7 pin, 100 mil, vertical header</td>
<td>Samtec</td>
<td>TSM-107-01-G-DV</td>
<td><a href="http://www.samtec.com">www.samtec.com</a></td>
</tr>
<tr>
<td></td>
<td>2×16 character display, 5×8 dot</td>
<td>Lumex Inc.</td>
<td>LCM-S01602DSR/C</td>
<td><a href="http://www.lumex.com">www.lumex.com</a></td>
</tr>
<tr>
<td></td>
<td>matrix</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Components and Interfaces

This section describes the development board’s communication ports and interface cards relative to the Stratix V GT device. The development board supports the following components and interfaces:

- 10/100/1000 Ethernet
- Transceiver interfaces
  - XFP interface
  - Small Form-Factor Pluggable (SFP+) interface

10/100/1000 Ethernet

The development board supports a 10/100/1000 BASE-T Ethernet connection using a Marvell 88E1111 PHY device and the Altera Triple-Speed Ethernet MegaCore MAC function. The device is an auto-negotiating Ethernet PHY with an SGMII interface to the FPGA. The Stratix V GT device can communicate with the LVDS interfaces at up to 1.25 Gbps. The MAC function must be provided in the FPGA for typical networking applications. The Marvell 88E1111 PHY uses 2.5-V and 1.2-V power rails and requires a 25-MHz reference clock driven from a dedicated oscillator. It interfaces to an RJ-45 with internal magnetics that can be used for driving copper lines with Ethernet traffic.

Figure 2–9 shows the SGMII interface between the FPGA (MAC) and Marvell 88E1111 PHY.

Figure 2–9. SGMII Interface between FPGA (MAC) and Marvell 88E1111 PHY

Table 2–31 lists the Ethernet PHY interface pin assignments.

<table>
<thead>
<tr>
<th>Board Reference (U22)</th>
<th>Schematic Signal Name</th>
<th>I/O Standard</th>
<th>Stratix V GT Device Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>23</td>
<td>ENET_INTN</td>
<td>2.5-V</td>
<td>AL14</td>
<td>Management bus Interrupt</td>
</tr>
<tr>
<td>70</td>
<td>ENET_LED_DUPLEX</td>
<td>2.5-V</td>
<td>—</td>
<td>Duplex LED</td>
</tr>
<tr>
<td>76</td>
<td>ENET_LED_LINK10</td>
<td>2.5-V</td>
<td>—</td>
<td>10-Mb link LED</td>
</tr>
<tr>
<td>74</td>
<td>ENET_LED_LINK1000</td>
<td>2.5-V</td>
<td>—</td>
<td>1000-Mb link LED</td>
</tr>
<tr>
<td>73</td>
<td>ENET_LED_LINK1000</td>
<td>2.5-V</td>
<td>—</td>
<td>1000-Mb link LED</td>
</tr>
</tbody>
</table>
Table 2–31. Ethernet PHY Pin Assignments, Signal Names and Functions (Part 2 of 2)

<table>
<thead>
<tr>
<th>Board Reference (U22)</th>
<th>Schematic Signal Name</th>
<th>I/O Standard</th>
<th>Stratix V GT Device Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>69</td>
<td>ENET_LED_RX</td>
<td>2.5-V</td>
<td>—</td>
<td>RX data active LED</td>
</tr>
<tr>
<td>68</td>
<td>ENET_LED_TX</td>
<td>2.5-V</td>
<td>—</td>
<td>TX data active LED</td>
</tr>
<tr>
<td>28</td>
<td>ENET_RSTN</td>
<td>2.5-V</td>
<td>AT6</td>
<td>Device reset</td>
</tr>
<tr>
<td>75</td>
<td>ENET_SGMII_RX_N</td>
<td>2.5-V</td>
<td>AJ15</td>
<td>SGMII receive</td>
</tr>
<tr>
<td>77</td>
<td>ENET_SGMII_RX_P</td>
<td>2.5-V</td>
<td>AH15</td>
<td>SGMII receive</td>
</tr>
<tr>
<td>81</td>
<td>ENET_SGMII_TX_N</td>
<td>2.5-V</td>
<td>AL15</td>
<td>SGMII transmit</td>
</tr>
<tr>
<td>82</td>
<td>ENET_SGMII_TX_P</td>
<td>2.5-V</td>
<td>AK15</td>
<td>SGMII transmit</td>
</tr>
<tr>
<td>55</td>
<td>ENET_XTAL_25MHZ</td>
<td>2.5-V</td>
<td>—</td>
<td>25-MHz clock</td>
</tr>
<tr>
<td>8</td>
<td>GTXCLK</td>
<td>2.5-V</td>
<td>AE15</td>
<td>Ethernet transmit clock</td>
</tr>
<tr>
<td>25</td>
<td>MDI</td>
<td>2.5-V</td>
<td>AB16</td>
<td>Management bus data clock</td>
</tr>
<tr>
<td>31</td>
<td>MDI_N0</td>
<td>2.5-V</td>
<td>—</td>
<td>Management bus data</td>
</tr>
<tr>
<td>34</td>
<td>MDI_N1</td>
<td>2.5-V</td>
<td>—</td>
<td>Management bus data</td>
</tr>
<tr>
<td>41</td>
<td>MDI_N2</td>
<td>2.5-V</td>
<td>—</td>
<td>Management bus data</td>
</tr>
<tr>
<td>43</td>
<td>MDI_N3</td>
<td>2.5-V</td>
<td>—</td>
<td>Management bus data</td>
</tr>
<tr>
<td>29</td>
<td>MDI_P0</td>
<td>2.5-V</td>
<td>—</td>
<td>Management bus data</td>
</tr>
<tr>
<td>33</td>
<td>MDI_P1</td>
<td>2.5-V</td>
<td>—</td>
<td>Management bus data</td>
</tr>
<tr>
<td>39</td>
<td>MDI_P2</td>
<td>2.5-V</td>
<td>—</td>
<td>Management bus data</td>
</tr>
<tr>
<td>42</td>
<td>MDI_P3</td>
<td>2.5-V</td>
<td>—</td>
<td>Management bus data</td>
</tr>
<tr>
<td>24</td>
<td>MDIO</td>
<td>2.5-V</td>
<td>AC16</td>
<td>Management bus data input/output</td>
</tr>
<tr>
<td>2</td>
<td>RXCLK</td>
<td>2.5-V</td>
<td>AH16</td>
<td>SGMII receive clock</td>
</tr>
<tr>
<td>95</td>
<td>RXD0</td>
<td>2.5-V</td>
<td>AG17</td>
<td>SGMII receive data</td>
</tr>
<tr>
<td>92</td>
<td>RXD1</td>
<td>2.5-V</td>
<td>AD15</td>
<td>SGMII receive data</td>
</tr>
<tr>
<td>93</td>
<td>RXD2</td>
<td>2.5-V</td>
<td>AE16</td>
<td>SGMII receive data</td>
</tr>
<tr>
<td>91</td>
<td>RXD3</td>
<td>2.5-V</td>
<td>AB15</td>
<td>SGMII receive data</td>
</tr>
<tr>
<td>94</td>
<td>RXDV</td>
<td>2.5-V</td>
<td>AF17</td>
<td>SGMII receive data valid</td>
</tr>
<tr>
<td>11</td>
<td>TXD0</td>
<td>2.5-V</td>
<td>AK17</td>
<td>SGMII transmit data</td>
</tr>
<tr>
<td>12</td>
<td>TXD1</td>
<td>2.5-V</td>
<td>AL17</td>
<td>SGMII transmit data</td>
</tr>
<tr>
<td>14</td>
<td>TXD2</td>
<td>2.5-V</td>
<td>AJ16</td>
<td>SGMII transmit data</td>
</tr>
<tr>
<td>16</td>
<td>TXD3</td>
<td>2.5-V</td>
<td>AJ17</td>
<td>SGMII transmit data</td>
</tr>
<tr>
<td>9</td>
<td>TXEN</td>
<td>2.5-V</td>
<td>AF16</td>
<td>SGMII transmit enable</td>
</tr>
</tbody>
</table>

Table 2–32 lists the Ethernet PHY interface component reference and manufacturing information.

Table 2–32. Ethernet PHY Component Reference and Manufacturing Information

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturing Part Number</th>
<th>Manufacturer Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>U22</td>
<td>Ethernet PHY BASE-T device</td>
<td>Marvel Semiconductor</td>
<td>88E1111-B2-CAAIC000</td>
<td><a href="http://www.marvell.com">www.marvell.com</a></td>
</tr>
</tbody>
</table>
Transceiver Interfaces

The transceiver signal integrity development board incorporates an XFP and SFP+ transceiver module. Each module has a single duplex channel.

XFP Interface

Table 2–33 lists the XFP connector cage interface pin assignments.

Table 2–33. XFP Interface Pin Assignments, Signal Names and Functions

<table>
<thead>
<tr>
<th>Board Reference (U25)</th>
<th>Schematic Signal Name</th>
<th>I/O Standard</th>
<th>Stratix V GT Device Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>28</td>
<td>GXB_TXLN_5</td>
<td>1.4-V PCML</td>
<td>AH35</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>29</td>
<td>GXB_TXLP_5</td>
<td>1.4-V PCML</td>
<td>AH34</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>18</td>
<td>GXB_RXLN_5</td>
<td>1.4-V PCML</td>
<td>AK39</td>
<td>GXB receive</td>
</tr>
<tr>
<td>16</td>
<td>GXB_RXLP_5</td>
<td>1.4-V PCML</td>
<td>AK38</td>
<td>GXB receive</td>
</tr>
<tr>
<td>24</td>
<td>REFCLK_XFPN</td>
<td>1.8-V</td>
<td></td>
<td>XFP reference clock</td>
</tr>
<tr>
<td>25</td>
<td>REFCLK_XFPP</td>
<td>1.8-V</td>
<td></td>
<td>XFP reference clock</td>
</tr>
<tr>
<td>3</td>
<td>XFP_MOD_DESEL</td>
<td>1.8-V</td>
<td>AV23</td>
<td>Module deselect</td>
</tr>
<tr>
<td>21</td>
<td>XFP_PDOWN_RST</td>
<td>1.8-V</td>
<td>AW23</td>
<td>Power down reset</td>
</tr>
<tr>
<td>4</td>
<td>XFP_T_INTERRUPT</td>
<td>1.8-V</td>
<td>AV22</td>
<td>Interrupt</td>
</tr>
<tr>
<td>12</td>
<td>XFP_T_MOD_ABS</td>
<td>1.8-V</td>
<td>AW26</td>
<td>Module absent</td>
</tr>
<tr>
<td>10</td>
<td>XFP_T_SCL</td>
<td>1.8-V</td>
<td>AW25</td>
<td>Two-wire serial interface clock line</td>
</tr>
<tr>
<td>11</td>
<td>XFP_T_SDA</td>
<td>1.8-V</td>
<td>AV25</td>
<td>Two-wire serial interface data line</td>
</tr>
<tr>
<td>5</td>
<td>XFP_TX_DIS</td>
<td>1.8-V</td>
<td>AW22</td>
<td>Disables transmitter output</td>
</tr>
</tbody>
</table>

Table 2–34 lists the XFP interface component reference and manufacturing information.

Table 2–34. XFP Interface Component Reference and Manufacturing Information

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturing Part Number</th>
<th>Manufacturer Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>U25</td>
<td>XFP 30-pin connector, 30UM gold plating, high speed</td>
<td>Amphenol Tyco</td>
<td>1367500-1</td>
<td><a href="http://www.amphenol.com">www.amphenol.com</a></td>
</tr>
<tr>
<td></td>
<td>XFP cage without light pipe, press fit</td>
<td>Amphenol Tyco</td>
<td>1489951-1</td>
<td><a href="http://www.te.com">www.te.com</a></td>
</tr>
</tbody>
</table>
SFP+ Interface

Table 2–31 lists the pin assignments for the SFP+ interface (SFPA) and their corresponding schematic signal names and Stratix V GT pin numbers.

Table 2–35. SFP+ Interface Pin Assignments, Signal Names and Functions

<table>
<thead>
<tr>
<th>Board Reference (J51)</th>
<th>Schematic Signal Name</th>
<th>I/O Standard</th>
<th>Stratix V GT Device Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>19</td>
<td>GXB_TXLN_18</td>
<td>1.8-V</td>
<td>M35</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>18</td>
<td>GXB_TXLP_18</td>
<td>1.8-V</td>
<td>M34</td>
<td>GXB transmit</td>
</tr>
<tr>
<td>12</td>
<td>GXB_RXLN_18</td>
<td>1.8-V</td>
<td>L37</td>
<td>GXB receive</td>
</tr>
<tr>
<td>13</td>
<td>GXB_RXLP_18</td>
<td>1.8-V</td>
<td>L36</td>
<td>GXB receive</td>
</tr>
<tr>
<td>8</td>
<td>SFPA_LOS</td>
<td>1.8-V</td>
<td>B28</td>
<td>Signal loss indicator</td>
</tr>
<tr>
<td>6</td>
<td>SFPA_MOD0_PRSNTN</td>
<td>1.8-V</td>
<td>B26</td>
<td>Module present indicator</td>
</tr>
<tr>
<td>5</td>
<td>SFPA_MOD1_SCL</td>
<td>1.8-V</td>
<td>A26</td>
<td>Two-wire serial interface clock line</td>
</tr>
<tr>
<td>4</td>
<td>SFPA_MOD2_SDA</td>
<td>1.8-V</td>
<td>B25</td>
<td>Two-wire serial interface data line</td>
</tr>
<tr>
<td>7</td>
<td>SFPA_RATESEL0</td>
<td>1.8-V</td>
<td>C27</td>
<td>Rate select 0. Controls the SFP+ interface receiver.</td>
</tr>
<tr>
<td>9</td>
<td>SFPA_RATESEL1</td>
<td>1.8-V</td>
<td>C26</td>
<td>Rate select 1. Controls the SFP+ interface receiver.</td>
</tr>
<tr>
<td>3</td>
<td>SFPA_TXDISABLE</td>
<td>1.8-V</td>
<td>A28</td>
<td>Turns off and disables the transmitter output</td>
</tr>
<tr>
<td>2</td>
<td>SFPA_TXFAULT</td>
<td>1.8-V</td>
<td>A25</td>
<td>Transmitter fault</td>
</tr>
</tbody>
</table>

Table 2–34 lists the SFP+ interface component reference and manufacturing information.

Table 2–36. SFP+ Interface Component Reference and Manufacturing Information

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturing Part Number</th>
<th>Manufacturer Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>J51</td>
<td>SFP+ connector - Mect family standard SFP right-angle 20-pin SMT</td>
<td>Samtec</td>
<td>MECT-110-01-M-D-RA1</td>
<td><a href="http://www.samtec.com">www.samtec.com</a></td>
</tr>
<tr>
<td></td>
<td>SFP+ cage</td>
<td>Molex</td>
<td>74754-0101</td>
<td><a href="http://www.molex.com">www.molex.com</a></td>
</tr>
</tbody>
</table>
The development board has a 1-Gb CFI-compatible synchronous flash device for non-volatile storage of the FPGA configuration data, board information, test application data, and user code space. The FPGA and MAX II System Controller shares this device.

This 16-bit data memory interface can sustain burst read operations at up to 52 MHz for a throughput of 832 Mbps per device. The write performance is 270 µs for a single word and 310 µs for a 32-word buffer. The erase time is 800 ms for a 128 K parameter block.

Table 2–37 lists the flash pin assignments, signal names, and functions. The signal names and types are relative to the Stratix V GT device in terms of I/O setting and direction.

<table>
<thead>
<tr>
<th>Board Reference (U21)</th>
<th>Schematic Signal Name</th>
<th>I/O Standard</th>
<th>Stratix V GT Device Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>F_AD1</td>
<td>1.8-V</td>
<td>AE14</td>
<td>Address bus</td>
</tr>
<tr>
<td>B1</td>
<td>F_AD2</td>
<td>1.8-V</td>
<td>AD14</td>
<td>Address bus</td>
</tr>
<tr>
<td>C1</td>
<td>F_AD3</td>
<td>1.8-V</td>
<td>AC13</td>
<td>Address bus</td>
</tr>
<tr>
<td>D1</td>
<td>F_AD4</td>
<td>1.8-V</td>
<td>AC12</td>
<td>Address bus</td>
</tr>
<tr>
<td>D2</td>
<td>F_AD5</td>
<td>1.8-V</td>
<td>AG14</td>
<td>Address bus</td>
</tr>
<tr>
<td>A2</td>
<td>F_AD6</td>
<td>1.8-V</td>
<td>AF14</td>
<td>Address bus</td>
</tr>
<tr>
<td>C2</td>
<td>F_AD7</td>
<td>1.8-V</td>
<td>AD11</td>
<td>Address bus</td>
</tr>
<tr>
<td>A3</td>
<td>F_AD8</td>
<td>1.8-V</td>
<td>AC11</td>
<td>Address bus</td>
</tr>
<tr>
<td>B3</td>
<td>F_AD9</td>
<td>1.8-V</td>
<td>AF11</td>
<td>Address bus</td>
</tr>
<tr>
<td>C3</td>
<td>F_AD10</td>
<td>1.8-V</td>
<td>AE11</td>
<td>Address bus</td>
</tr>
<tr>
<td>D3</td>
<td>F_AD11</td>
<td>1.8-V</td>
<td>AE13</td>
<td>Address bus</td>
</tr>
<tr>
<td>C4</td>
<td>F_AD12</td>
<td>1.8-V</td>
<td>AE12</td>
<td>Address bus</td>
</tr>
<tr>
<td>A5</td>
<td>F_AD13</td>
<td>1.8-V</td>
<td>AJ14</td>
<td>Address bus</td>
</tr>
<tr>
<td>B5</td>
<td>F_AD14</td>
<td>1.8-V</td>
<td>AH13</td>
<td>Address bus</td>
</tr>
<tr>
<td>C5</td>
<td>F_AD15</td>
<td>1.8-V</td>
<td>AG13</td>
<td>Address bus</td>
</tr>
<tr>
<td>D7</td>
<td>F_AD16</td>
<td>1.8-V</td>
<td>AF13</td>
<td>Address bus</td>
</tr>
<tr>
<td>D8</td>
<td>F_AD17</td>
<td>1.8-V</td>
<td>AJ13</td>
<td>Address bus</td>
</tr>
<tr>
<td>A7</td>
<td>F_AD18</td>
<td>1.8-V</td>
<td>AJ12</td>
<td>Address bus</td>
</tr>
<tr>
<td>B7</td>
<td>F_AD19</td>
<td>1.8-V</td>
<td>AH12</td>
<td>Address bus</td>
</tr>
<tr>
<td>C7</td>
<td>F_AD20</td>
<td>1.8-V</td>
<td>AG11</td>
<td>Address bus</td>
</tr>
<tr>
<td>C8</td>
<td>F_AD21</td>
<td>1.8-V</td>
<td>AK12</td>
<td>Address bus</td>
</tr>
<tr>
<td>A8</td>
<td>F_AD22</td>
<td>1.8-V</td>
<td>AK11</td>
<td>Address bus</td>
</tr>
<tr>
<td>G1</td>
<td>F_AD23</td>
<td>1.8-V</td>
<td>AL12</td>
<td>Address bus</td>
</tr>
<tr>
<td>H8</td>
<td>F_AD24</td>
<td>1.8-V</td>
<td>AL11</td>
<td>Address bus</td>
</tr>
<tr>
<td>B6</td>
<td>F_AD25</td>
<td>1.8-V</td>
<td>AM13</td>
<td>Address bus</td>
</tr>
<tr>
<td>B8</td>
<td>F_AD26</td>
<td>1.8-V</td>
<td>AL13</td>
<td>Address bus</td>
</tr>
<tr>
<td>F6</td>
<td>F_ADVN</td>
<td>1.8-V</td>
<td>AP7</td>
<td>Address valid</td>
</tr>
</tbody>
</table>
Table 2–37. Flash Pin Assignments, Schematic Signal Names, and Functions (Part 2 of 2)

<table>
<thead>
<tr>
<th>Board Reference (U21)</th>
<th>Schematic Signal Name</th>
<th>I/O Standard</th>
<th>Stratix V GT Device Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>F7</td>
<td>F_BSYN</td>
<td>1.8-V</td>
<td>AR7</td>
<td>Ready</td>
</tr>
<tr>
<td>B4</td>
<td>F_CEN</td>
<td>1.8-V</td>
<td>AP9</td>
<td>Chip enable</td>
</tr>
<tr>
<td>E6</td>
<td>F_CLK</td>
<td>1.8-V</td>
<td>AN6</td>
<td>Clock</td>
</tr>
<tr>
<td>F2</td>
<td>F_D0</td>
<td>1.8-V</td>
<td>AN11</td>
<td>Data bus</td>
</tr>
<tr>
<td>E2</td>
<td>F_D1</td>
<td>1.8-V</td>
<td>AM11</td>
<td>Data bus</td>
</tr>
<tr>
<td>G3</td>
<td>F_D2</td>
<td>1.8-V</td>
<td>AP12</td>
<td>Data bus</td>
</tr>
<tr>
<td>E4</td>
<td>F_D3</td>
<td>1.8-V</td>
<td>AN12</td>
<td>Data bus</td>
</tr>
<tr>
<td>E5</td>
<td>F_D4</td>
<td>1.8-V</td>
<td>AN10</td>
<td>Data bus</td>
</tr>
<tr>
<td>G5</td>
<td>F_D5</td>
<td>1.8-V</td>
<td>AM10</td>
<td>Data bus</td>
</tr>
<tr>
<td>G6</td>
<td>F_D6</td>
<td>1.8-V</td>
<td>AR11</td>
<td>Data bus</td>
</tr>
<tr>
<td>H7</td>
<td>F_D7</td>
<td>1.8-V</td>
<td>AR10</td>
<td>Data bus</td>
</tr>
<tr>
<td>E1</td>
<td>F_D8</td>
<td>1.8-V</td>
<td>AT12</td>
<td>Data bus</td>
</tr>
<tr>
<td>E3</td>
<td>F_D9</td>
<td>1.8-V</td>
<td>AU13</td>
<td>Data bus</td>
</tr>
<tr>
<td>F3</td>
<td>F_D10</td>
<td>1.8-V</td>
<td>AU12</td>
<td>Data bus</td>
</tr>
<tr>
<td>F4</td>
<td>F_D11</td>
<td>1.8-V</td>
<td>AU11</td>
<td>Data bus</td>
</tr>
<tr>
<td>F5</td>
<td>F_D12</td>
<td>1.8-V</td>
<td>AT11</td>
<td>Data bus</td>
</tr>
<tr>
<td>H5</td>
<td>F_D13</td>
<td>1.8-V</td>
<td>AW13</td>
<td>Data bus</td>
</tr>
<tr>
<td>G7</td>
<td>F_D14</td>
<td>1.8-V</td>
<td>AV13</td>
<td>Data bus</td>
</tr>
<tr>
<td>E7</td>
<td>F_D15</td>
<td>1.8-V</td>
<td>AW11</td>
<td>Data bus</td>
</tr>
<tr>
<td>F8</td>
<td>F_OEN</td>
<td>1.8-V</td>
<td>AN9</td>
<td>Output enable</td>
</tr>
<tr>
<td>D4</td>
<td>F_RSTN</td>
<td>1.8-V</td>
<td>AL8</td>
<td>Reset</td>
</tr>
<tr>
<td>G8</td>
<td>F_WEN</td>
<td>1.8-V</td>
<td>AM8</td>
<td>Write enable</td>
</tr>
<tr>
<td>C6</td>
<td>F_WPN</td>
<td>1.8-V</td>
<td>AP6</td>
<td>Write protect</td>
</tr>
</tbody>
</table>

Table 2–38 lists the flash memory component reference and manufacturing information.

Table 2–38. Flash Memory Component Reference and Manufacturing Information

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturing Part Number</th>
<th>Manufacturer Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>U21</td>
<td>1-Gb synchronous flash</td>
<td>Micron</td>
<td>PC28F00AP30BF</td>
<td><a href="http://www.micron.com">www.micron.com</a></td>
</tr>
</tbody>
</table>

Power Supply

The development board’s power is provided through a laptop style DC power input. The input voltage must be in the range of 14 V to 20 V. The DC voltage is then stepped down to the various power rails used by the components on the board.

An on-board multi-channel power monitor device (LTC2978) measures both the voltage and current for several specific board rails. This device has the capability to trim voltage outputs ±10%.
Table 2–39 lists the power requirements for each major component on the board.

<table>
<thead>
<tr>
<th>Device</th>
<th>Voltage Name</th>
<th>Voltage (V)</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>FPGA</strong></td>
<td><strong>S5GX_VCC</strong></td>
<td>0.85</td>
<td>VCC, VCCHIP, VCCHSSI</td>
</tr>
<tr>
<td></td>
<td>2p5V</td>
<td>2.5</td>
<td>VCCIO, VCCPD, VCCREF, VCCPGM, VCCBAT, VCC_CLKIN</td>
</tr>
<tr>
<td></td>
<td>2p5V_FLTR</td>
<td>2.5</td>
<td>Ferrite filtered from 2p5V, VCCA_PLL, and VCCAUX</td>
</tr>
<tr>
<td></td>
<td>1p5V</td>
<td>1.5</td>
<td>VCCPT, VCC_H_GXB, VCCD_PLL</td>
</tr>
<tr>
<td></td>
<td>VCCBAT</td>
<td>1.5</td>
<td>BT1 socket</td>
</tr>
<tr>
<td></td>
<td>VCCH_GTB (28G channels)</td>
<td>0.85 or 1.0</td>
<td>LDO</td>
</tr>
<tr>
<td></td>
<td>VCCT_GTB (28G channels)</td>
<td>0.85 or 1.0</td>
<td>LDO</td>
</tr>
<tr>
<td></td>
<td>VCCL_GTB (28G channels)</td>
<td>0.85 or 1.0</td>
<td>LDO</td>
</tr>
<tr>
<td></td>
<td>VCCRT_GXB</td>
<td>0.85 or 1.0</td>
<td>Low noise switcher</td>
</tr>
<tr>
<td></td>
<td>VCCA_GXB</td>
<td>2.5 or 3</td>
<td>Low noise switcher</td>
</tr>
<tr>
<td></td>
<td>VCCH_GXB</td>
<td>1.5</td>
<td>Tied to 1p5V (low noise switcher)</td>
</tr>
<tr>
<td><strong>MAX II (for FPP configuration)</strong></td>
<td>2p5V</td>
<td>2.5</td>
<td>—</td>
</tr>
<tr>
<td><strong>Flash</strong></td>
<td>2p5V</td>
<td>2.5</td>
<td>Core</td>
</tr>
<tr>
<td></td>
<td>XFP_1p8V</td>
<td>1.8</td>
<td>I/O</td>
</tr>
<tr>
<td><strong>MAX II (for USB-Blaster)</strong></td>
<td>2p5V</td>
<td>3.3</td>
<td>Core or I/O</td>
</tr>
<tr>
<td><strong>EEPROM</strong></td>
<td>USBVCC</td>
<td>5.0</td>
<td>—</td>
</tr>
<tr>
<td><strong>USB PHY</strong></td>
<td>USBVCC</td>
<td>5.0</td>
<td>Core</td>
</tr>
<tr>
<td></td>
<td>2p5V_USB</td>
<td>2.5</td>
<td>I/O</td>
</tr>
<tr>
<td><strong>Power monitor</strong></td>
<td>5V</td>
<td>5.0</td>
<td>—</td>
</tr>
<tr>
<td><strong>Temperature sense ADC</strong></td>
<td>3p3V</td>
<td>3.3</td>
<td>—</td>
</tr>
<tr>
<td><strong>ICS557-03 spread spectrum clock buffer (x1)</strong></td>
<td>3p3V</td>
<td>3.3</td>
<td>25-MHz clock output to the FPGA</td>
</tr>
<tr>
<td><strong>ICS8304 clock buffer</strong></td>
<td>3p3V/2p5V</td>
<td>3.3/2.5</td>
<td>50-MHz clock outputs</td>
</tr>
<tr>
<td><strong>IDT5T9306 transceiver REFCLK clock buffers (x4)</strong></td>
<td>2p5V</td>
<td>2.5</td>
<td>Programmable clock outputs</td>
</tr>
<tr>
<td><strong>T85A23157 dual analog switch</strong></td>
<td>5V</td>
<td>5.0</td>
<td>—</td>
</tr>
<tr>
<td><strong>Character LCD</strong></td>
<td>5V</td>
<td>5.0</td>
<td>—</td>
</tr>
<tr>
<td><strong>LEDs (x13)</strong></td>
<td>2p5V</td>
<td>2.5</td>
<td>—</td>
</tr>
<tr>
<td><strong>Board power LED</strong></td>
<td>5V</td>
<td>5.0</td>
<td>—</td>
</tr>
</tbody>
</table>
Power Measurement

There are six voltage rails tied to two LTC2978 power monitor devices. These devices are capable of measuring the voltage and current for each voltage rail and also provide power sequencing. A sense resistor at each voltage rail is in place for these measurements. These devices are capable of trimming the output voltage ±10%. An I²C bus connects to the MAX II CPLD and FPGA devices for control.

Table 2–40 lists the voltage rails. Each voltage is identified by its schematic signal name.

Table 2–40. Voltage Rails

<table>
<thead>
<tr>
<th>Schematic Signal Name</th>
<th>Voltage (V)</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Production Silicon</td>
<td>Engineering Silicon</td>
</tr>
<tr>
<td>S5GX_VCC</td>
<td>0.85</td>
<td>0.9</td>
</tr>
<tr>
<td>VCCR_GTB</td>
<td>0.85 or 1.0</td>
<td>1.1</td>
</tr>
<tr>
<td>VCCT_GTB</td>
<td>0.85 or 1.0</td>
<td>1.1</td>
</tr>
<tr>
<td>VCCL_GTB</td>
<td>0.85 or 1.0</td>
<td>1.1</td>
</tr>
<tr>
<td>VCCRT_GXB</td>
<td>0.85 or 1.0</td>
<td>1.2</td>
</tr>
<tr>
<td>VCCA_GXB</td>
<td>2.5 or 3.0</td>
<td>3.3</td>
</tr>
<tr>
<td>VCCH_GXB</td>
<td>—</td>
<td>1.6</td>
</tr>
<tr>
<td>VCCD_FPLL</td>
<td>—</td>
<td>1.6</td>
</tr>
<tr>
<td>VCCPT</td>
<td>—</td>
<td>1.6</td>
</tr>
</tbody>
</table>

The LTC2978 power monitor devices on this board are programmed with a project file that sets up each voltage rail according to a sequence. Each voltage rail adjusts its voltage level to within a certain tolerance. These two voltage rails can be adjusted using switch SW2.

Table 2–41 lists the VCCRT_GXB and VCCA_GXB voltage rails and their voltage level depending on the switch position.

Table 2–41. Voltage Level Setting

<table>
<thead>
<tr>
<th>Switch SW2 (Position 1 and 2)</th>
<th>Schematic Net Name</th>
<th>Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Close (Default)</td>
<td>VCCRT_GXB</td>
<td>1.0</td>
</tr>
<tr>
<td></td>
<td>VCCA_GXB</td>
<td>3.0</td>
</tr>
<tr>
<td>Open</td>
<td>VCCRT_GXB</td>
<td>0.9</td>
</tr>
<tr>
<td></td>
<td>VCCA_GXB</td>
<td>2.5</td>
</tr>
</tbody>
</table>

If you power off and power on the board again with SW2 in the open position, the voltages for VCCRT_GXB and VCCA_GXB voltage rails read 0.90 V and 2.5 V respectively and will not come up to the proper levels. This is due to the LTC2978 device trying to adjust these rails to their programmed values, which it cannot due to the switch position of SW2. The work around to this issue is to set switch SW2 in the close position at power up.
Table 2–42 lists the power monitor devices component reference and manufacturing information.

Table 2–42. Power Measurement ADC Component References and Manufacturing Information

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturing Part Number</th>
<th>Manufacturer Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>U10, U11</td>
<td>IC, power supply monitor w/EPROM, octal PMBUS</td>
<td>Linear Technology</td>
<td>LTC2978CUP#PBF</td>
<td><a href="http://www.linear.com">www.linear.com</a></td>
</tr>
</tbody>
</table>

**Power Distribution System**

Figure 2–10 shows the power distribution system on the development board. The VCCR\_GTB, VCCT\_GTB, and VCCL\_GTB power rails are separated on the 28G transceivers but are combined on the 12.5G transceivers.

Figure 2–10. Power Distribution System
Temperature Sense

The Stratix V GT die uses a MAX1619 temperature sense device for temperature monitoring. The device connects to the MAX II CPLD EPM2210 System Controller and the Stratix V GT device by a 2-wire SMB interface. The MAX1619 device is located at slave address 0011000b (18h).

The OVERTEMPn and TSENSE_ALERTn signals are driven by the MAX1619 temperature sense device based on a programmable threshold temperature. The OVERTEMPn signal is driven to the MAX II System Controller. An over-temperature warning LED (D7) indicates the temperature fault condition.

Table 2–43 lists the temperature sense interface pin assignments, signal names, and functions.

Table 2–43. Temperature Sense Pin Assignments, Schematic Signal Names, and Functions

<table>
<thead>
<tr>
<th>Board Reference (U12)</th>
<th>Schematic Signal Name</th>
<th>I/O Standard</th>
<th>MAX II CPLD System Controller Pin Number</th>
<th>Stratix V GT Device Pin Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>14 SMBCLK_TEMP</td>
<td>3.3-V</td>
<td>D3</td>
<td>B8</td>
<td>SMB clock</td>
<td></td>
</tr>
<tr>
<td>12 SMBDATA_TEMP</td>
<td>3.3-V</td>
<td>C2</td>
<td>A8</td>
<td>SMB data</td>
<td></td>
</tr>
<tr>
<td>11 ALERTn</td>
<td>3.3-V</td>
<td>D2</td>
<td>E8</td>
<td>Programmable alert</td>
<td></td>
</tr>
<tr>
<td>9 OVERTEMPn</td>
<td>3.3-V</td>
<td>E4</td>
<td>E7</td>
<td>Fan enable</td>
<td></td>
</tr>
<tr>
<td>3 TEMPDIODE_P</td>
<td>3.3-V</td>
<td>—</td>
<td>V11</td>
<td>Current source and remote diode input</td>
<td></td>
</tr>
<tr>
<td>4 TEMPDIODE_N</td>
<td>3.3-V</td>
<td>—</td>
<td>U11</td>
<td>Remote diode input</td>
<td></td>
</tr>
</tbody>
</table>

Table 2–44 lists the temperature sense component reference and manufacturing information.

Table 2–44. Temperature Sense Component Reference and Manufacturing Information

<table>
<thead>
<tr>
<th>Board Reference</th>
<th>Description</th>
<th>Manufacturer</th>
<th>Manufacturing Part Number</th>
<th>Manufacturer Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>U12</td>
<td>Temperature sense, remote and local, programmable alert.</td>
<td>Maxim</td>
<td>MAX1619MEE+T</td>
<td><a href="http://www.maxim-ic.com">www.maxim-ic.com</a></td>
</tr>
</tbody>
</table>
Statement of China-RoHS Compliance

Table 2–45 lists hazardous substances included with the kit.

Table 2–45. Table of Hazardous Substances’ Name and Concentration

<table>
<thead>
<tr>
<th>Part Name</th>
<th>Lead (Pb)</th>
<th>Cadmium (Cd)</th>
<th>Hexavalent Chromium (Cr6+)</th>
<th>Mercury (Hg)</th>
<th>Polybrominated Biphenyls (PBB)</th>
<th>Polybrominated Diphenyl Ethers (PBDE)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Stratix V GT transceiver signal integrity development board</td>
<td>X* 0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>14 V power supply</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Type A-B USB cable</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>User guide</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Notes to Table 2–45:

1. 0 indicates that the concentration of the hazardous substance in all homogeneous materials in the parts is below the relevant threshold of the SJ/T11363-2006 standard.

2. X* indicates that the concentration of the hazardous substance of at least one of all homogeneous materials in the parts is above the relevant threshold of the SJ/T11363-2006 standard, but it is exempted by EU RoHS.
This chapter provides additional information about the document and Altera.

**Board Revision History**

The following table lists the versions of all releases of the Stratix V GT transceiver signal integrity development board.

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>December 2015</td>
<td>Production</td>
<td>New device part number—5SGTMC7K3F40C2.</td>
</tr>
<tr>
<td></td>
<td>silicon</td>
<td></td>
</tr>
<tr>
<td>January 2013</td>
<td>Production</td>
<td>New device part number—5SGTMC7K2F40C2.</td>
</tr>
<tr>
<td></td>
<td>silicon</td>
<td></td>
</tr>
<tr>
<td>February 2012</td>
<td>Engineering</td>
<td>Initial release.</td>
</tr>
<tr>
<td></td>
<td>silicon</td>
<td></td>
</tr>
</tbody>
</table>

**Document Revision History**

The following table shows the revision history for this document.

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<thead>
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<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>January 2016</td>
<td>1.3</td>
<td>Revised the FPGA device part number</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>May 2014</td>
<td>1.2</td>
<td>Corrected ALM amount in the “Board Component Blocks” section and in Table 2–2.</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>January 2013</td>
<td>1.1</td>
<td>■ Revised the FPGA device part number for production silicon release.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Added Table 2–41 on page 2–39 to define the voltage levels for VCCRT_GXB and VCCA_GXB voltage rails.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>■ Removed appendix A and appended the board revision history table in “Additional Information” chapter.</td>
</tr>
<tr>
<td>February 2012</td>
<td>1.0</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>

**How to Contact Altera**

To locate the most up-to-date information about Altera products, refer to the following table.

<table>
<thead>
<tr>
<th>Contact (1)</th>
<th>Contact Method</th>
<th>Address</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technical support</td>
<td>Website</td>
<td><a href="http://www.altera.com/support">www.altera.com/support</a></td>
</tr>
<tr>
<td>Technical training</td>
<td>Website</td>
<td><a href="http://www.altera.com/training">www.altera.com/training</a></td>
</tr>
<tr>
<td></td>
<td>Email</td>
<td><a href="mailto:custrain@altera.com">custrain@altera.com</a></td>
</tr>
<tr>
<td>Product literature</td>
<td>Website</td>
<td><a href="http://www.altera.com/literature">www.altera.com/literature</a></td>
</tr>
<tr>
<td>Nontechnical</td>
<td></td>
<td></td>
</tr>
<tr>
<td>support (general)</td>
<td>Email</td>
<td><a href="mailto:nacomp@altera.com">nacomp@altera.com</a></td>
</tr>
<tr>
<td>(software licensing)</td>
<td>Email</td>
<td><a href="mailto:authorization@altera.com">authorization@altera.com</a></td>
</tr>
</tbody>
</table>

**Note to Table:**

(1) You can also contact your local Altera sales office or sales representative.
## Typographic Conventions

The following table shows the typographic conventions this document uses.

<table>
<thead>
<tr>
<th>Visual Cue</th>
<th>Meaning</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Bold Type with Initial Capital Letters</strong></td>
<td>Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, <strong>Save As</strong> dialog box. For GUI elements, capitalization matches the GUI.</td>
</tr>
<tr>
<td><strong>bold type</strong></td>
<td>Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, <code>\qdesigns</code> directory, <strong>D:</strong> drive, and <strong>chiptrip.gdf</strong> file.</td>
</tr>
<tr>
<td><strong>Italic Type with Initial Capital Letters</strong></td>
<td>Indicate document titles. For example, <em>Stratix IV Design Guidelines</em>.</td>
</tr>
<tr>
<td><strong>italic type</strong></td>
<td>Indicates variables. For example, $n + 1$. Variable names are enclosed in angle brackets (<code>&lt;&gt;</code>). For example, <code>&lt;file name&gt;</code> and <code>&lt;project name&gt;.pof</code> file.</td>
</tr>
<tr>
<td><strong>Initial Capital Letters</strong></td>
<td>Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.</td>
</tr>
<tr>
<td><strong>“Subheading Title”</strong></td>
<td>Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, “Typographic Conventions.”</td>
</tr>
<tr>
<td><strong>Courier type</strong></td>
<td>Indicates signal, port, register, bit, block, and primitive names. For example, <code>data1</code>, <code>tdi</code>, and <code>input</code>. The suffix <code>n</code> denotes an active-low signal. For example, <code>resetn</code>. Indicates command line commands and anything that must be typed exactly as it appears. For example, <code>c:\qdesigns\tutorial\chiptrip.gdf</code>. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword <code>SUBDESIGN</code>), and logic function names (for example, <code>TRI</code>).</td>
</tr>
<tr>
<td>An angled arrow</td>
<td>An angled arrow instructs you to press the Enter key.</td>
</tr>
<tr>
<td>1., 2., 3., and a., b., c., and so on</td>
<td>Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.</td>
</tr>
<tr>
<td>■ ■ ■</td>
<td>Bullets indicate a list of items when the sequence of the items is not important.</td>
</tr>
<tr>
<td>The hand points to information that requires special attention.</td>
<td>The hand points to information that requires special attention.</td>
</tr>
<tr>
<td>The question mark directs you to a software help system with related information.</td>
<td>The question mark directs you to a software help system with related information.</td>
</tr>
<tr>
<td>The feet direct you to another document or website with related information.</td>
<td>The feet direct you to another document or website with related information.</td>
</tr>
<tr>
<td>The multimedia icon directs you to a related multimedia presentation.</td>
<td>The multimedia icon directs you to a related multimedia presentation.</td>
</tr>
<tr>
<td>A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.</td>
<td>A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.</td>
</tr>
<tr>
<td>A warning calls attention to a condition or possible situation that can cause you injury.</td>
<td>A warning calls attention to a condition or possible situation that can cause you injury.</td>
</tr>
<tr>
<td>The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.</td>
<td>The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.</td>
</tr>
<tr>
<td>The feedback icon allows you to submit feedback to Altera about the document. Methods for collecting feedback vary as appropriate for each document.</td>
<td>The feedback icon allows you to submit feedback to Altera about the document. Methods for collecting feedback vary as appropriate for each document.</td>
</tr>
</tbody>
</table>