

# Altera® Quartus® Prime Standard Edition Settings File Reference Manual

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MNL-Q21005



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## Advanced I/O Timing Assignments

### BOARD\_MODEL\_EBD\_FAR\_END

Specifies the far-end node to be used in the Electronic Board Description (EBD) path description.

#### Type

String

#### Device Support

This setting can be used in projects targeting any Altera device family.

#### Notes

The value of this assignment is case sensitive.

#### Syntax

```
set_instance_assignment -name BOARD_MODEL_EBD_FAR_END -to <to> -entity  
<entity name> <value>
```

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## BOARD\_MODEL\_EBD\_FILE\_NAME

Specifies the Electronic Board Description (EBD) file that contains the path description for an I/O pin.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports wildcards.

The value of this assignment is case sensitive.

### Syntax

```
set_instance_assignment -name BOARD_MODEL_EBD_FILE_NAME -to <to> -entity  
<entity name> <value>
```

## BOARD\_MODEL\_EBD\_SIGNAL\_NAME

Specifies the Electronic Board Description (EBD) path description to be used with an I/O pin. You must specify the EBD file name.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_instance_assignment -name BOARD_MODEL_EBD_SIGNAL_NAME -to <to> -entity  
<entity name> <value>
```

## BOARD\_MODEL\_FAR\_C

Specifies, in farads, the board trace model far capacitance.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name BOARD_MODEL_FAR_C -to <to> -entity <entity  
name> <value>  
set_global_assignment -name BOARD_MODEL_FAR_C -section_id <section  
identifier> <value>
```

## BOARD\_MODEL\_FAR\_DIFFERENTIAL\_R

Specifies, in ohms, the board trace model far differential resistance.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name BOARD_MODEL_FAR_DIFFERENTIAL_R -to <to> -  
entity <entity name> <value>  
set_global_assignment -name BOARD_MODEL_FAR_DIFFERENTIAL_R -section_id  
<section identifier> <value>
```

## BOARD\_MODEL\_FAR\_PULLDOWN\_R

Specifies, in ohms, the board trace model far pull-down resistance.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name BOARD_MODEL_FAR_PULLDOWN_R -to <to> -entity  
<entity name> <value>  
set_global_assignment -name BOARD_MODEL_FAR_PULLDOWN_R -section_id <section  
identifier> <value>
```

## BOARD\_MODEL\_FAR\_PULLUP\_R

Specifies, in ohms, the board trace model far pull-up resistance.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name BOARD_MODEL_FAR_PULLUP_R -to <to> -entity  
<entity name> <value>  
set_global_assignment -name BOARD_MODEL_FAR_PULLUP_R -section_id <section  
identifier> <value>
```

## BOARD\_MODEL\_FAR\_SERIES\_R

Specifies, in ohms, the board trace model far series resistance.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name BOARD_MODEL_FAR_SERIES_R -to <to> -entity  
<entity name> <value>  
set_global_assignment -name BOARD_MODEL_FAR_SERIES_R -section_id <section  
identifier> <value>
```



## BOARD\_MODEL\_NEAR\_C

Specifies, in farads, the board trace model near capacitance.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name BOARD_MODEL_NEAR_C -to <to> -entity <entity  
name> <value>  
set_global_assignment -name BOARD_MODEL_NEAR_C -section_id <section  
identifier> <value>
```

## BOARD\_MODEL\_NEAR\_DIFFERENTIAL\_R

Specifies, in ohms, the board trace model near differential resistance.

### Type

String

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name BOARD_MODEL_NEAR_DIFFERENTIAL_R -to <to> -  
entity <entity name> <value>  
set_global_assignment -name BOARD_MODEL_NEAR_DIFFERENTIAL_R -section_id  
<section identifier> <value>
```



## BOARD\_MODEL\_NEAR\_PULLDOWN\_R

Specifies, in ohms, the board trace model near pull-down resistance.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name BOARD_MODEL_NEAR_PULLDOWN_R -to <to> -entity  
<entity name> <value>  
set_global_assignment -name BOARD_MODEL_NEAR_PULLDOWN_R -section_id  
<section identifier> <value>
```

## BOARD\_MODEL\_NEAR\_PULLUP\_R

Specifies, in ohms, the board trace model near pull-up resistance.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name BOARD_MODEL_NEAR_PULLUP_R -to <to> -entity  
<entity name> <value>  
set_global_assignment -name BOARD_MODEL_NEAR_PULLUP_R -section_id <section  
identifier> <value>
```

## BOARD\_MODEL\_NEAR\_SERIES\_R

Specifies, in ohms, the board trace model near series resistance.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name BOARD_MODEL_NEAR_SERIES_R -to <to> -entity  
<entity name> <value>  
set_global_assignment -name BOARD_MODEL_NEAR_SERIES_R -section_id <section  
identifier> <value>
```

## BOARD\_MODEL\_NEAR\_TLINE\_C\_PER\_LENGTH

Specifies, in farads/inch, the board trace model near transmission line distributed capacitance.

### Type

String

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name BOARD_MODEL_NEAR_TLINE_C_PER_LENGTH -to <to> -  
entity <entity name> <value>  
set_global_assignment -name BOARD_MODEL_NEAR_TLINE_C_PER_LENGTH -section_id  
<section identifier> <value>
```

## BOARD\_MODEL\_NEAR\_TLINE\_LENGTH

Specifies, in inches, the board trace model near transmission line length.

### Type

String

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name BOARD_MODEL_NEAR_TLINE_LENGTH -to <to> -  
entity <entity name> <value>  
set_global_assignment -name BOARD_MODEL_NEAR_TLINE_LENGTH -section_id  
<section identifier> <value>
```

## BOARD\_MODEL\_NEAR\_TLINE\_L\_PER\_LENGTH

Specifies, in henrys/inch, the board trace model near transmission line distributed inductance.

### Type

String

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name BOARD_MODEL_NEAR_TLINE_L_PER_LENGTH -to <to> -  
entity <entity name> <value>  
set_global_assignment -name BOARD_MODEL_NEAR_TLINE_L_PER_LENGTH -section_id  
<section identifier> <value>
```



## BOARD\_MODEL\_TERMINATION\_V

Specifies, in volts, the board trace model termination voltage.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name BOARD_MODEL_TERMINATION_V -to <to> -entity  
<entity name> <value>  
set_global_assignment -name BOARD_MODEL_TERMINATION_V -section_id <section  
identifier> <value>
```

## BOARD\_MODEL\_TLINE\_C\_PER\_LENGTH

Specifies, in farads/inch, the board trace model far transmission line distributed capacitance.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name BOARD_MODEL_TLINE_C_PER_LENGTH -to <to> -  
entity <entity name> <value>  
set_global_assignment -name BOARD_MODEL_TLINE_C_PER_LENGTH -section_id  
<section identifier> <value>
```



## BOARD\_MODEL\_TLINE\_LENGTH

Specifies, in inches, the board trace model far transmission line length.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name BOARD_MODEL_TLINE_LENGTH -to <to> -entity  
<entity name> <value>  
set_global_assignment -name BOARD_MODEL_TLINE_LENGTH -section_id <section  
identifier> <value>
```

## BOARD\_MODEL\_TLINE\_L\_PER\_LENGTH

Specifies, in henrys/inch, the board trace model far transmission line distributed inductance.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name BOARD_MODEL_TLINE_L_PER_LENGTH -to <to> -  
entity <entity name> <value>  
set_global_assignment -name BOARD_MODEL_TLINE_L_PER_LENGTH -section_id  
<section identifier> <value>
```

## ENABLE\_ADVANCED\_IO\_TIMING

Allows the TimeQuest Timing Analyzer to use Advanced I/O Timing to generate I/O timing results. Timing results are based on the board trace model specified for each pin, and may differ from the results currently reported.

### Type

Boolean

### Device Support

- Arria GX
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_ADVANCED_IO_TIMING <value>
```

## OUTPUT\_IO\_TIMING\_ENDPOINT

Specifies the node at which output I/O Timing ends.

### Type

Enumeration

### Values

- Far End
- Near End

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name OUTPUT_IO_TIMING_ENDPOINT -to <to> -entity  
<entity name> <value>  
set_global_assignment -name OUTPUT_IO_TIMING_ENDPOINT -entity <entity name>  
<value>  
set_global_assignment -name OUTPUT_IO_TIMING_ENDPOINT <value>
```

### Default Value

Near End

## OUTPUT\_IO\_TIMING\_FAR\_END\_VMEAS

Specifies, in volts, the measurement voltage at the far-end.

### Type

String

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name OUTPUT_IO_TIMING_FAR_END_VMEAS -to <to> -  
entity <entity name> <value>  
set_global_assignment -name OUTPUT_IO_TIMING_FAR_END_VMEAS -section_id  
<section identifier> <value>  
set_global_assignment -name OUTPUT_IO_TIMING_FAR_END_VMEAS <value>
```

## OUTPUT\_IO\_TIMING\_NEAR\_END\_VMEAS

Specifies, in volts, the measurement voltage at the near-end.

### Type

String

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name OUTPUT_IO_TIMING_NEAR_END_VMEAS -to <to> -  
entity <entity name> <value>  
set_global_assignment -name OUTPUT_IO_TIMING_NEAR_END_VMEAS -section_id  
<section identifier> <value>  
set_global_assignment -name OUTPUT_IO_TIMING_NEAR_END_VMEAS <value>
```



## PCB\_LAYER

Specifies which PCB layer the signal breaks out on

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports wildcards.

### Syntax

```
<value> set_instance_assignment -name PCB_LAYER -to <to> -entity <entity name>  
<value> set_global_assignment -name PCB_LAYER -section_id <section identifier>
```

## PCB\_LAYERS

Specifies the properties of all PCB layers

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name PCB_LAYERS -to <to> <value>
```



## PCB\_LAYER\_THICKNESS

Thickness of the specific PCB layer

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name PCB_LAYER_THICKNESS -to <to> -entity <entity  
name> <value>  
set_global_assignment -name PCB_LAYER_THICKNESS -section_id <section  
identifier> <value>
```

## SYNCHRONOUS\_GROUP

A logic option that assigns a synchronous group number for the specified node. This option directs the SSN Analyzer to view the specified nodes as a synchronous group during SSN voltage noise analysis. This option can be set in the Assignment Editor.

### Type

Integer

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- MAX 10
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name SYNCHRONOUS_GROUP -to <to> -entity <entity  
name> <value>
```

# Analysis & Synthesis Assignments

## ADV\_NETLIST\_OPT\_ALLOWED

Specifies whether the Compiler should perform advanced netlist optimizations, such as gate-level retiming or physical synthesis, on the specified node or entity. If this option is set to 'Default', the Compiler duplicates, moves, or changes the synthesis of the node or entity, or allows register retiming during netlist optimization, only if doing so does not negatively affect the timing or performance of the design. If this option is set to 'Always Allow', the Compiler can alter the node or entity, even if doing so affects the timing or performance of the design. Altera does not recommend using this setting. If this option is set to 'Never Allow' the Compiler cannot alter the node or entity.

### Type

Enumeration

### Values

- Always Allow
- Default
- Never Allow

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

- Stratix III
- Stratix IV
- Stratix V

## Notes

This assignment supports synthesis wildcards.

## Syntax

```
set_global_assignment -name ADV_NETLIST_OPT_ALLOWED -entity <entity name>  
<value>  
set_instance_assignment -name ADV_NETLIST_OPT_ALLOWED -to <to> -entity  
<entity name> <value>
```

## Example

```
set_instance_assignment -name adv_netlist_opt_allowed "always allow" -to reg
```

## ALLOW\_ANY\_RAM\_SIZE\_FOR\_RECOGNITION

Allows the Compiler to infer RAMs of any size, even if they don't meet the current minimum requirements.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name ALLOW_ANY_RAM_SIZE_FOR_RECOGNITION <value>  
set_global_assignment -name ALLOW_ANY_RAM_SIZE_FOR_RECOGNITION -entity  
<entity name> <value>
```

```
set_instance_assignment -name ALLOW_ANY_RAM_SIZE_FOR_RECOGNITION -to <to> -  
entity <entity name> <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name allow_any_ram_size_for_recognition off  
set_instance_assignment -name allow_any_ram_size_for_recognition off -to foo
```



## ALLOW\_ANY\_ROM\_SIZE\_FOR\_RECOGNITION

Allows the Compiler to infer ROMs of any size even if the ROMs do not meet the design's current minimum size requirements.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name ALLOW_ANY_ROM_SIZE_FOR_RECOGNITION <value>  
set_global_assignment -name ALLOW_ANY_ROM_SIZE_FOR_RECOGNITION -entity  
<entity name> <value>
```

```
set_instance_assignment -name ALLOW_ANY_ROM_SIZE_FOR_RECOGNITION -to <to> -  
entity <entity name> <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name allow_any_rom_size_for_recognition off  
set_instance_assignment -name allow_any_rom_size_for_recognition off -to foo
```



## ALLOW\_ANY\_SHIFT\_REGISTER\_SIZE\_FOR\_RECOGNITION

Allows the Compiler to infer shift registers of any size even if they do not meet the design's current minimum size requirements.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name ALLOW_ANY_SHIFT_REGISTER_SIZE_FOR_RECOGNITION  
<value>  
set_global_assignment -name ALLOW_ANY_SHIFT_REGISTER_SIZE_FOR_RECOGNITION -  
entity <entity name> <value>  
set_instance_assignment -name ALLOW_ANY_SHIFT_REGISTER_SIZE_FOR_RECOGNITION  
-to <to> -entity <entity name> <value>
```

**Default Value**

Off

**Example**

```
set_global_assignment -name allow_any_shift_register_size_for_recognition  
off  
set_instance_assignment -name allow_any_shift_register_size_for_recognition  
off -to foo
```

## ALLOW\_CHILD\_PARTITIONS

Specifies whether or not an instance or a section of design hierarchy can contain user partitions.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name ALLOW_CHILD_PARTITIONS -entity <entity name>  
<value>  
set_instance_assignment -name ALLOW_CHILD_PARTITIONS -to <to> -entity  
<entity name> <value>
```

### Example

```
set_global_assignment -name allow_child_partitions off  
set_instance_assignment -name allow_child_partitions off -to "sub:inst"
```

## ALLOW\_POWER\_UP\_DONT\_CARE

Causes registers that do not have a Power-Up Level logic option setting to power up with a don't care logic level (X). A don't care setting allows the Compiler to change the power-up level of a register to minimize the area of the design.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name ALLOW_POWER_UP_DONT_CARE <value>
```

### Default Value

On

### Example

```
set_global_assignment -name allow_power_up_dont_care off
```

### See Also

Power-Up Level

## ALLOW\_SHIFT\_REGISTER\_MERGING\_ACROSS\_HIERARCHIES

Allows the Compiler to take shift registers from different hierarchies of the design and put them in the same RAM.

### Type

Enumeration

### Values

- Always
- Auto
- Off

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

## Syntax

```
<value>      set_global_assignment -name ALLOW_SHIFT_REGISTER_MERGING_ACROSS_HIERARCHIES
set_global_assignment -name ALLOW_SHIFT_REGISTER_MERGING_ACROSS_HIERARCHIES
-entity <entity name> <value>
set_instance_assignment -name
ALLOW_SHIFT_REGISTER_MERGING_ACROSS_HIERARCHIES -to <to> -entity <entity name>
<value>
```

## Default Value

Auto

## Example

```
off          set_global_assignment -name allow_shift_register_merging_across_hierarchies
set_instance_assignment -name
allow_shift_register_merging_across_hierarchies off -to foo
```

## See Also

Auto Shift Register Replacement





## ALLOW\_SYNCH\_CTRL\_USAGE

Allows the Compiler to utilize synchronous clear and/or synchronous load signals in normal mode logic cells. Turning on this option helps to reduce the total number of logic cells used in the design, but might negatively impact the fitting since synchronous control signals are shared by all the logic cells in a LAB.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name ALLOW_SYNCH_CTRL_USAGE <value>
set_global_assignment -name ALLOW_SYNCH_CTRL_USAGE -entity <entity name>
<value>
```

```
set_instance_assignment -name ALLOW_SYNCH_CTRL_USAGE -to <to> -entity  
<entity name> <value>
```

### Default Value

On

### Example

```
set_global_assignment -name allow_synch_ctrl_usage off  
set_instance_assignment -name allow_synch_ctrl_usage off -to foo
```

### See Also

Force Use of Synchronous Clear Signals



## ALLOW\_XOR\_GATE\_USAGE

Allows the Compiler to use the XOR gate that exists in a macrocell (that is, in an embedded cell within an Embedded System Block [ESB] that is set to use Product Term mode). This option is ignored if you select 'LUT' or 'ROM' as the setting for the Technology Mapper option.

### Type

Boolean

### Device Support

- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name ALLOW_XOR_GATE_USAGE <value>
set_global_assignment -name ALLOW_XOR_GATE_USAGE -entity <entity name>
<value>
set_instance_assignment -name ALLOW_XOR_GATE_USAGE -to <to> -entity <entity
name> <value>
```

### Default Value

On

### Example

```
set_instance_assignment -name allow_xor_gate_usage off -to clock
```

## ALTERA\_A10\_IOPLL\_BOOTSTRAP

Turns on the A10 IOPLL bootstrap fix

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name ALTERA_A10_IOPLL_BOOTSTRAP <value>
```



## AUTO\_CARRY\_CHAINS

Allows the Compiler to create carry chains automatically by inserting CARRY\_SUM buffers into the design. This option is also required to recognize carry chains in any design containing MAX+PLUS II-style CARRY buffers. The length of the chains is controlled with the Carry Chain Length option. If this option is turned off, CARRY buffers are ignored, but CARRY\_SUM buffers are unaffected. The Auto Carry Chains option is ignored if you select 'Product Term' or 'ROM' as the setting for the Technology Mapper option.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

## Syntax

```
set_global_assignment -name AUTO_CARRY_CHAINS <value>  
set_global_assignment -name AUTO_CARRY_CHAINS -entity <entity name> <value>  
set_instance_assignment -name AUTO_CARRY_CHAINS -to <to> -entity <entity  
name> <value>
```

## Default Value

On

## AUTO\_CASCADE\_CHAINS

Allows the Compiler to create cascade chains automatically by inserting CASCADE buffers into the design. The length of the chains is controlled with the Cascade Chain Length option. The Auto Cascade Chains option is ignored if you select 'Product Term' or 'ROM' as the setting for the Technology Mapper option.

### Type

Boolean

### Device Support

- A
- E

### Notes

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name AUTO_CASCADE_CHAINS <value>
set_global_assignment -name AUTO_CASCADE_CHAINS -entity <entity name>
<value>
set_instance_assignment -name AUTO_CASCADE_CHAINS -to <to> -entity <entity
name> <value>
```

### Default Value

On

## AUTO\_CLOCK\_ENABLE\_RECOGNITION

Allows the Compiler to find logic that feeds a register and move the logic to the register's clock enable input port.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.



## Syntax

```
set_global_assignment -name AUTO_CLOCK_ENABLE_RECOGNITION <value>
set_global_assignment -name AUTO_CLOCK_ENABLE_RECOGNITION -entity <entity
name> <value>
set_instance_assignment -name AUTO_CLOCK_ENABLE_RECOGNITION -to <to> -
entity <entity name> <value>
```

## Default Value

On

## Example

```
set_global_assignment -name auto_clock_enable_replacement off
set_instance_assignment -name auto_clock_enable_replacement off -to reg
```

## AUTO\_DSP\_RECOGNITION

Allows the Compiler to find a multiply-accumulate function or a multiply-add function that can be replaced with the `altmult_accum` or the `altmult_add` megafunction.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name AUTO_DSP_RECOGNITION <value>
set_global_assignment -name AUTO_DSP_RECOGNITION -entity <entity name>
<value>
set_instance_assignment -name AUTO_DSP_RECOGNITION -to <to> -entity <entity
name> <value>
```

## Default Value

On

## Example

```
set_global_assignment -name auto_dsp_recognition off  
set_instance_assignment -name auto_dsp_recognition off -to foo
```

## AUTO\_ENABLE\_SMART\_COMPILE

Specifies whether the SignalTap II Logic Analyzer should perform a smart compilation if conditions exist in which SignalTap II with incremental routing is used.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name AUTO_ENABLE_SMART_COMPILE <value>
```



## AUTO\_GLOBAL\_CLOCK\_MAX

Allows the Compiler to choose the signal that feeds the most clock inputs to flipflops as a global clock signal that is made available throughout the device on the global routing paths. If you want to prevent the Compiler from automatically selecting a particular signal as global clock, set the Global Signal option to 'Off' on that signal.

### Old Name

Auto Global Clock -- MAX 7000B/7000AE/3000A/7000S/7000A

### Type

Boolean

### Device Support

- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S

### Notes

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name AUTO_GLOBAL_CLOCK_MAX <value>
set_global_assignment -name AUTO_GLOBAL_CLOCK_MAX -entity <entity name>
<value>
set_instance_assignment -name AUTO_GLOBAL_CLOCK_MAX -to <to> -entity
<entity name> <value>
```

### Default Value

On

### Example

```
set_global_assignment -name auto_global_clock_max off
set_instance_assignment -name auto_global_clock_max off -to foo
```

## AUTO\_GLOBAL\_OE\_MAX

Allows the Compiler to choose the signal that feeds the most TRI buffers as a global output enable signal that is made available throughout the device on the global routing paths. If you want to prevent the Compiler from automatically selecting a particular signal as global output enable, set the Global Signal option to 'Off' on that signal.

### Old Name

Auto Global Output Enable -- MAX 7000B/7000AE/3000A/7000S/7000A

### Type

Boolean

### Device Support

- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S

### Notes

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name AUTO_GLOBAL_OE_MAX <value>
set_global_assignment -name AUTO_GLOBAL_OE_MAX -entity <entity name> <value>
set_instance_assignment -name AUTO_GLOBAL_OE_MAX -to <to> -entity <entity
name> <value>
```

### Default Value

On

### Example

```
set_global_assignment -name auto_global_oe_max off
set_instance_assignment -name auto_global_oe_max off -to foo
```

## AUTO\_IMPLEMENT\_IN\_ROM

Allows the Compiler to automatically implement combinatorial logic in ROM (that is, in an embedded cell within an Embedded System Block [ESB] or Embedded Array Block [EAB] that is set to use ROM mode), to improve speed or area usage. Using ROM in this way can free up logic cells that would otherwise be needed to implement the combinatorial logic. This option is ignored if you select 'Product Term' as the setting for the Technology Mapper option.

### Type

Boolean

### Device Support

- A
- E
- Mercury

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name AUTO_IMPLEMENT_IN_ROM <value>
set_global_assignment -name AUTO_IMPLEMENT_IN_ROM -entity <entity name>
<value>
set_instance_assignment -name AUTO_IMPLEMENT_IN_ROM -to <to> -entity
<entity name> <value>
```

### Default Value

Off

## AUTO\_LCELL\_INSERTION

Allows the Compiler to insert macrocells into the design. This option is ignored if it is assigned to anything other than a design entity. If you want to prevent the Compiler from automatically inserting macrocells into the design, set the Auto Logic Cell Insertion option to 'Off' on that signal.

### Type

Boolean

### Device Support

- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name AUTO_LCELL_INSERTION <value>
set_global_assignment -name AUTO_LCELL_INSERTION -entity <entity name>
<value>
set_instance_assignment -name AUTO_LCELL_INSERTION -to <to> -entity <entity
name> <value>
```

### Default Value

On

### Example

```
set_global_assignment -name auto_lcell_insertion off
set_instance_assignment -name auto_lcell_insertion off -to foo
```



## AUTO\_OPEN\_DRAIN\_PINS

Allows the Compiler to automatically convert a tri-state buffer with a strong low data input into the equivalent open-drain buffer.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

## Syntax

```
set_global_assignment -name AUTO_OPEN_DRAIN_PINS <value>
set_global_assignment -name AUTO_OPEN_DRAIN_PINS -entity <entity name>
<value>
set_instance_assignment -name AUTO_OPEN_DRAIN_PINS -to <to> -entity <entity
name> <value>
```

## Default Value

On

## Example

```
set_global_assignment -name auto_open_drain_pins off
set_instance_assignment -name auto_open_drain_pins off -to foo
```



## AUTO\_PARALLEL\_EXPANDERS

Allows the Compiler to automatically create chains of parallel expander product terms. Parallel expanders are available in macrocells, that is, embedded cells within an Embedded System Block [ESB] that is set to use Product Term mode. The length of the chains is controlled with the Parallel Expander Chain Length option. The Auto Parallel Expanders option is ignored if you select 'LUT' or 'ROM' as the setting for the Technology Mapper option.

### Type

Boolean

### Device Support

- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name AUTO_PARALLEL_EXPANDERS <value>
set_global_assignment -name AUTO_PARALLEL_EXPANDERS -entity <entity name>
<value>
set_instance_assignment -name AUTO_PARALLEL_EXPANDERS -to <to> -entity
<entity name> <value>
```

### Default Value

On

### Example

```
set_instance_assignment -name auto_parallel_expanders on -to clock
```

## AUTO\_PARALLEL\_SYNTHESIS

Option to enable/disable automatic parallel synthesis. This option can be used to speed up synthesis compile time by using multiple processors when available.

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name AUTO_PARALLEL_SYNTHESIS <value>
```

### Default Value

On

### Example

```
set_global_assignment -name auto_parallel_synthesis on
```

## AUTO\_RAM\_BLOCK\_BALANCING

Enables the Compiler to automatically use different memory types when using auto RAM blocks and allows the Compiler to use different RAM partitions with the same memory types.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name AUTO_RAM_BLOCK_BALANCING <value>
```

### Default Value

On

### Example

```
set_global_assignment -name auto_ram_block_balancing off
```

## AUTO\_RAM\_RECOGNITION

Allows the Compiler to find a set of registers and logic that can be replaced with the altsyncram or the lpm\_ram\_dp megafunction. Turning on this option may change the functionality of the design.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name AUTO_RAM_RECOGNITION <value>  
set_global_assignment -name AUTO_RAM_RECOGNITION -entity <entity name>  
<value>
```

```
set_instance_assignment -name AUTO_RAM_RECOGNITION -to <to> -entity <entity  
name> <value>
```

## Default Value

On

## Example

```
set_global_assignment -name auto_ram_recognition off  
set_instance_assignment -name auto_ram_recognition off -to foo
```

## AUTO\_RAM\_TO\_LCELL\_CONVERSION

Allows the Compiler to convert small RAM blocks into logic cells.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name AUTO_RAM_TO_LCELL_CONVERSION <value>
set_global_assignment -name AUTO_RAM_TO_LCELL_CONVERSION -entity <entity
name> <value>
set_instance_assignment -name AUTO_RAM_TO_LCELL_CONVERSION -to <to> -entity
<entity name> <value>
```

### Default Value

Off



## AUTO\_RESOURCE\_SHARING

Allows the Compiler to share hardware resources among many similar, but mutually exclusive, operations in your HDL source code. If you enable this option, the Compiler will merge compatible addition, subtraction, and multiplication operations. By merging operations, this may reduce the area required by your design. Because resource sharing introduces extra muxing and control logic on each shared resource, it may negatively impact the final fmax of your design.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name AUTO_RESOURCE_SHARING <value>
set_global_assignment -name AUTO_RESOURCE_SHARING -entity <entity name>
<value>
set_instance_assignment -name AUTO_RESOURCE_SHARING -to <to> -entity
<entity name> <value>
```

### Default Value

Off

## AUTO\_ROM\_RECOGNITION

Allows the Compiler to find logic that can be replaced with the altsyncram or the lpm\_rom megafunction. Turning on this option may change the power-up state of the design.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name AUTO_ROM_RECOGNITION <value>  
set_global_assignment -name AUTO_ROM_RECOGNITION -entity <entity name>  
<value>
```

```
set_instance_assignment -name AUTO_ROM_RECOGNITION -to <to> -entity <entity  
name> <value>
```

## Default Value

On

## Example

```
set_global_assignment -name auto_rom_recognition off  
set_instance_assignment -name auto_rom_recognition off -to foo
```

## AUTO\_SHIFT\_REGISTER\_RECOGNITION

Allows the Compiler to find a group of shift registers of the same length that can be replaced with the `altshift_taps` megafunction. The shift registers must all use the same clock and clock enable signals, must not have any other secondary signals, and must have equally spaced taps that are at least three registers apart.

### Type

Enumeration

### Values

- Always
- Auto
- Off

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

## Syntax

```
set_global_assignment -name AUTO_SHIFT_REGISTER_RECOGNITION <value>
set_global_assignment -name AUTO_SHIFT_REGISTER_RECOGNITION -entity <entity
name> <value>
set_instance_assignment -name AUTO_SHIFT_REGISTER_RECOGNITION -to <to> -
entity <entity name> <value>
```

## Default Value

Auto

## Example

```
set_global_assignment -name auto_shift_register_recognition off
set_instance_assignment -name auto_shift_register_recognition off -to foo
```

## BLOCK\_DESIGN\_NAMING

Specify the naming scheme used for the block design. This option is ignored if it is assigned to anything other than a design entity.

### Type

Enumeration

### Values

- Auto
- MaxPlusII
- QuartusII

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name BLOCK_DESIGN_NAMING -entity <entity name>
<value>
set_instance_assignment -name BLOCK_DESIGN_NAMING -to <to> -entity <entity
name> <value>
set_global_assignment -name BLOCK_DESIGN_NAMING <value>
```

### Default Value

Auto

### Example

```
set_global_assignment -name block_design_naming MaxPlusII
set_instance_assignment -name block_design_naming MaxPlusII -to top
```

## BOARD

Specifies the board or development kit to use.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name BOARD <value>
```

## CARRY\_CHAIN\_LENGTH

Specifies the maximum allowable length of a chain of both user-entered and Compiler-synthesized CARRY\_SUM buffers. Carry chains that exceed this length are broken into separate chains. (This option also applies to MAX+PLUS II-style CARRY buffers.)

### Type

Integer

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name CARRY_CHAIN_LENGTH <value>
set_global_assignment -name CARRY_CHAIN_LENGTH -entity <entity name> <value>
set_instance_assignment -name CARRY_CHAIN_LENGTH -to <to> -entity <entity
name> <value>
```

### Default Value

48



## CASCADE\_CHAIN\_LENGTH

Specifies the maximum allowable length of a chain of both user-entered and Compiler-synthesized CASCADE buffers. Cascade chains that exceed this length are broken into separate chains.

### Type

Integer

### Device Support

- A
- E

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name CASCADE_CHAIN_LENGTH <value>
set_global_assignment -name CASCADE_CHAIN_LENGTH -entity <entity name>
<value>
set_instance_assignment -name CASCADE_CHAIN_LENGTH -to <to> -entity <entity
name> <value>
```

### Default Value

2



## CLKLOCKX1\_INPUT\_FREQ

Creates an internal ClockLock phase-locked loop (PLL) and specifies its frequency. Turning this option on is equivalent to instantiating an altclklock megafunction with either of its ClockBoost parameters set to a value of 1. The CLKLOCKx1 Input Frequency option is provided primarily for backward compatibility with MAX+PLUS II designs. Altera recommends using the MegaWizard Plug-In Manager to instantiate PLLs in new designs. This option is ignored if it is assigned to anything other than an input pin or to a device that does not have the PLL feature.

### Type

Frequency

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

None

### Syntax

```
set_instance_assignment -name CLKLOCKX1_INPUT_FREQ -to <to> -entity <entity name> <value>
```

## CYCLONEII\_OPTIMIZATION\_TECHNIQUE

Specifies the overall optimization goal for Analysis & Synthesis: attempt to maximize performance, minimize logic usage, or balance high performance with minimal logic usage.

### Old Name

Optimization Technique -- Cyclone II/Cyclone III

### Type

Enumeration

### Values

- Area
- Balanced
- Speed

### Device Support

- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- MAX 10

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name CYCLONEII_OPTIMIZATION_TECHNIQUE <value>
set_global_assignment -name CYCLONEII_OPTIMIZATION_TECHNIQUE -entity
<entity name> <value>
set_instance_assignment -name CYCLONEII_OPTIMIZATION_TECHNIQUE -to <to> -
entity <entity name> <value>
```

### Default Value

Balanced

### Example

```
set_global_assignment -name cycloneii_optimization_technique speed
```

## CYCLONE\_OPTIMIZATION\_TECHNIQUE

Specifies the overall optimization goal for Analysis & Synthesis: attempt to maximize performance, minimize logic usage, or balance high performance with minimal logic usage.

### Old Name

Optimization Technique -- Cyclone

### Type

Enumeration

### Values

- Area
- Balanced
- Speed

### Device Support

Cyclone

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name CYCLONE_OPTIMIZATION_TECHNIQUE <value>
set_global_assignment -name CYCLONE_OPTIMIZATION_TECHNIQUE -entity <entity
name> <value>
set_instance_assignment -name CYCLONE_OPTIMIZATION_TECHNIQUE -to <to> -
entity <entity name> <value>
```

### Default Value

Balanced

### Example

```
set_global_assignment -name cyclone_optimization_technique speed
```

## DEVICE\_FILTER\_PACKAGE

Package filter for available devices.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name DEVICE_FILTER_PACKAGE <value>
```

### Default Value

Any

## DEVICE\_FILTER\_PIN\_COUNT

Pin count filter for available devices.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name DEVICE_FILTER_PIN_COUNT <value>
```

### Default Value

Any



## DEVICE\_FILTER\_SPEED\_GRADE

Speed grade filter for available devices.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name DEVICE_FILTER_SPEED_GRADE <value>
```

### Default Value

Any

## DEVICE\_FILTER\_VOLTAGE

Voltage filter for available devices.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name DEVICE_FILTER_VOLTAGE <value>
```



## DISABLE\_DSP\_NEGATE\_INFERENCING

Allow you to specify whether to use the negate port on an inferred DSP block.

### Type

Boolean

### Device Support

- Arria 10

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name DISABLE_DSP_NEGATE_INFERENCING -entity <entity
name> <value>
set_instance_assignment -name DISABLE_DSP_NEGATE_INFERENCING -to <to> -
entity <entity name> <value>
set_global_assignment -name DISABLE_DSP_NEGATE_INFERENCING <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name DISABLE_DSP_NEGATE_INFERENCING ON
set_instance_assignment -name DISABLE_DSP_NEGATE_INFERENCING OFF -to dps1
```

## DISABLE\_REGISTER\_MERGING\_ACROSS\_HIERARCHIES

Specifies whether registers that are in different hierarchies are allowed to be merged if their inputs are the same.

### Type

Enumeration

### Values

- Auto
- Off
- On

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
<value> set_global_assignment -name DISABLE_REGISTER_MERGING_ACROSS_HIERARCHIES
```

### Default Value

Auto

## DONT\_MERGE\_REGISTER

When set to On, this option prevents the specified register from merging with other registers, and prevents other registers from merging with the specified register.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports Fitter wildcards.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name DONT_MERGE_REGISTER -entity <entity name>  
<value>  
set_instance_assignment -name DONT_MERGE_REGISTER -to <to> -entity <entity  
name> <value>
```

### Example

```
set_instance_assignment -name dont_merge_register on -to foo
```

## DQS\_DELAY

Increases the propagation delay from a DQS I/O pin to the interior of the device. This option is used to center-align the DQS signal to the DQ data signals and should be selected to ensure the desired setup and hold margins across process, voltage, and temperature ranges.

### Type

Time

### Device Support

- Cyclone
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX

### Notes

None

### Syntax

```
<value> set_instance_assignment -name DQS_DELAY -to <to> -entity <entity name>
```



## DQS\_FREQUENCY

Specifies the DQS system clock frequency by which data is transferred between a device and an external RAM that uses double data rate (DDR). You can specify the desired frequency setting.

### Type

Frequency

### Device Support

- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- MAX 10
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
<value> set_instance_assignment -name DQS_FREQUENCY -to <to> -entity <entity name>
```

## DQS\_SHIFT

Specifies the interval of arrival between the DQ data signals and DQS signal during data transfer between a device and an external RAM that uses double data rate (DDR). This option is ignored if it is applied to anything other than pins intended for use with the dedicated DDR SDRAM interface.

### Type

Enumeration

### Values

- Phase of 0 degrees
- Phase of 72 degrees
- Phase of 90 degrees

### Device Support

- Stratix
- Stratix GX

### Notes

None

### Syntax

```
<value> set_instance_assignment -name DQS_SHIFT -to <to> -entity <entity name>
```

## DQS\_SYSTEM\_CLOCK

Specifies the clock input used as a frequency reference for a DQS I/O pin. The clock is the pin that drives the DDIO circuitry for the dedicated DDR SDRAM interface.

### Type

String

### Device Support

- Stratix
- Stratix GX

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_instance_assignment -name DQS_SYSTEM_CLOCK -to <to> -entity <entity  
name> <value>
```

## DSE\_SYNTH\_EXTRA\_EFFORT\_MODE

Specifies the Design Space Explorer synthesis extra effort mode.

### Type

Enumeration

### Values

- MODE\_1
- MODE\_2
- MODE\_3
- MODE\_4
- MODE\_5
- MODE\_DEFAULT

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name DSE_SYNTH_EXTRA_EFFORT_MODE <value>
```





## DSP\_BLOCK\_BALANCING

Allows you to control the conversion of certain DSP block slices during DSP block balancing.

### Type

Enumeration

### Values

- Auto
- DSP blocks
- Logic Elements
- Off
- Simple 18-bit Multipliers
- Simple Multipliers
- Width 18-bit Multipliers

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

## Syntax

```
set_global_assignment -name DSP_BLOCK_BALANCING -entity <entity name>  
<value>  
set_instance_assignment -name DSP_BLOCK_BALANCING -to <to> -entity <entity  
name> <value>  
set_global_assignment -name DSP_BLOCK_BALANCING <value>
```

## Default Value

Auto

## Example

```
set_global_assignment -name dsp_block_balancing "dsp blocks"  
set_instance_assignment -name dsp_block_balancing "logic elements" -to mult0
```

## EDA\_DESIGN\_ENTRY\_SYNTHESIS\_TOOL

Specifies the third-party EDA tool used for design entry/synthesis

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_DESIGN_ENTRY_SYNTHESIS_TOOL <value>  
set_global_assignment -name EDA_DESIGN_ENTRY_SYNTHESIS_TOOL -entity <entity  
name> <value>
```

### Default Value

<None>

## EDA\_INPUT\_DATA\_FORMAT

Specifies the format of the input data read from other EDA design entry/synthesis tools.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EDA_INPUT_DATA_FORMAT -section_id <section  
identifier> <value>  
set_global_assignment -name EDA_INPUT_DATA_FORMAT -entity <entity name> -  
section_id <section identifier> <value>
```

### Default Value

NONE, requires section identifier

## EDA\_INPUT\_GND\_NAME

Specifies the global high signal used in the files generated by the EDA synthesis tool, which is GND.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EDA_INPUT_GND_NAME -section_id <section  
identifier> <value>  
set_global_assignment -name EDA_INPUT_GND_NAME -entity <entity name> -  
section_id <section identifier> <value>
```

### Default Value

GND, requires section identifier

## EDA\_INPUT\_VCC\_NAME

Specifies the global power-down signal.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EDA_INPUT_VCC_NAME -section_id <section  
identifier> <value>  
set_global_assignment -name EDA_INPUT_VCC_NAME -entity <entity name> -  
section_id <section identifier> <value>
```

### Default Value

VCC, requires section identifier

## EDA\_LMF\_FILE

Specifies the default Library Mapping File (.lmf) for the current compilation.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_LMF_FILE -section_id <section identifier>  
<value>  
set_global_assignment -name EDA_LMF_FILE -entity <entity name> -section_id  
<section identifier> <value>
```

## EDA\_RUN\_TOOL\_AUTOMATICALLY

Runs the third-party EDA tool automatically from Quartus Prime when a design is compiled.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EDA_RUN_TOOL_AUTOMATICALLY -section_id <section  
identifier> <value>  
set_global_assignment -name EDA_RUN_TOOL_AUTOMATICALLY -entity <entity  
name> -section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier



## EDA\_SHOW\_LMF\_MAPPING\_MESSAGES

Determines whether to display messages describing the mappings used in the Library Mapping File.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EDA_SHOW_LMF_MAPPING_MESSAGES -section_id  
<section identifier> <value>  
set_global_assignment -name EDA_SHOW_LMF_MAPPING_MESSAGES -entity <entity  
name> -section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier

## EDA\_VHDL\_LIBRARY

Specifies the logical name of a user-defined VHDL design library : physical name.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_instance_assignment -name EDA_VHDL_LIBRARY -to <to> -section_id  
<section identifier> <value>  
set_instance_assignment -name EDA_VHDL_LIBRARY -to <to> -entity <entity  
name> -section_id <section identifier> <value>
```

## ENABLE\_IP\_DEBUG

Make certain nodes (for example, important registers, pins, and state machines) visible for all the MegaCore functions in a design. You can use a MegaCore function's nodes to effectively debug the megafunction, particularly when using the megafunction with the SignalTap II Logic Analyzer. The Node Finder, using SignalTap II Logic Analyzer filters, displays all the nodes that Analysis & Synthesis makes visible. When making the debugging nodes visible, Analysis & Synthesis can change the fmax and number of logic cells in MegaCore functions.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name ENABLE_IP_DEBUG <value>
```

### Default Value

Off

## ENABLE\_M512

Enables the compiler to use M512 memory blocks in a design. Because HardCopy II designs do not support M512 memory blocks, this option is useful when you migrate a compiled Stratix II design to a HardCopy II design.

### Type

Boolean

### Device Support

- Arria GX
- Cyclone
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name ENABLE_M512 <value>
```

### Example

```
set_global_assignment -name enable_m512 off
```

## ENABLE\_STATE\_MACHINE\_INFERENCE

Allows the Compiler to infer state machines from Verilog/Vhdl Design Files. The Compiler optimizes state machines using special techniques to reduce area and/or improve performance. If set to Off, the Compiler extracts and optimizes state machines in Verilog/VHDL Design Files as regular logic.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name ENABLE_STATE_MACHINE_INFERENCE <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name enable_state_machine_inference on
```

## EXTRACT\_VERILOG\_STATE\_MACHINES

Allows the Compiler to extract state machines from Verilog Design Files. The Compiler optimizes state machines using special techniques to reduce area and/or improve performance. If set to Off, the Compiler extracts and optimizes state machines in Verilog Design Files as regular logic.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name EXTRACT_VERILOG_STATE_MACHINES <value>
```

### Default Value

On

### Example

```
set_global_assignment -name extract_verilog_state_machines off
```

### See Also

State Machine Processing Extract VHDL State Machines

## EXTRACT\_VHDL\_STATE\_MACHINES

Allows the Compiler to extract state machines from VHDL Design Files. The Compiler optimizes state machines using special techniques to reduce area and/or improve performance. If set to Off, the Compiler extracts and optimizes state machines in VHDL Design Files as regular logic.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name EXTRACT_VHDL_STATE_MACHINES <value>
```

### Default Value

On

### Example

```
set_global_assignment -name extract_vhdl_state_machines off
```

### See Also

State Machine Processing Extract Verilog State Machines

## FAMILY

Specifies the device family to use for compilation.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name FAMILY <value>
```

### Default Value

Cyclone V



## FORCE\_SYNCH\_CLEAR

Forces the Compiler to utilize synchronous clear signals in normal mode logic cells. Turning on this option helps to reduce the total number of logic cells used in the design, but might negatively impact the fitting since synchronous control signals are shared by all the logic cells in a LAB.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name FORCE_SYNCH_CLEAR <value>
set_global_assignment -name FORCE_SYNCH_CLEAR -entity <entity name> <value>
set_instance_assignment -name FORCE_SYNCH_CLEAR -to <to> -entity <entity
```

name> <value>

### Default Value

Off

### Example

```
set_global_assignment -name force_synch_clear on  
set_instance_assignment -name force_synch_clear on -to foo
```

### See Also

Allow Synchronous Control Signals

## HDL\_INITIAL\_FANOUT\_LIMIT

Directs Integrated Synthesis to check the initial fan-out of each net in the netlist immediately after elaboration but prior to any netlist optimizations. If the fan-out for a net exceeds the specified limit, then Integrated Synthesis will issue a warning.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name HDL_INITIAL_FANOUT_LIMIT -entity <entity name>  
<value>  
set_instance_assignment -name HDL_INITIAL_FANOUT_LIMIT -to <to> -entity  
<entity name> <value>
```

### Example

```
set_instance_assignment -name hdl_initial_fanout_limit 100 -to foo
```

## HDL\_MESSAGE\_LEVEL

Specifies the type of HDL messages you want to view, including messages that display processing errors in the HDL source code. 'Level1' allows you to view only the most important HDL messages. 'Level2' allows you to view most HDL messages, including warning and information based messages. 'Level3' allows you to view all HDL messages, including warning and information based messages and alerts about potential design problems or lint errors.

### Type

Enumeration

### Values

- Level1
- Level2
- Level3

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name HDL_MESSAGE_LEVEL <value>
```

### Default Value

Level2

## HDL\_MESSAGE\_OFF

Specifies the list of HDL message ids you want to turn off for this project.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### INTEGER\_RANGE

10000, 11000

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name HDL_MESSAGE_OFF <value>
```

## HDL\_MESSAGE\_ON

Specifies the list of HDL message ids you want to turn on for this project.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### INTEGER\_RANGE

10000, 11000

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name HDL_MESSAGE_ON <value>
```



## HPS\_PARTITION

Specifies whether an entity or instance is a special-purpose partition that models the internals of the Hard Processor System (HPS).

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name HPS_PARTITION -entity <entity name> <value>  
set_instance_assignment -name HPS_PARTITION -to <to> -entity <entity name>  
<value>
```

### Example

```
set_instance_assignment -name hps_partition on -entity hps
```

## IGNORE\_CARRY\_BUFFERS

Ignores CARRY\_SUM buffers that are instantiated in the design. The Ignore CARRY Buffers option is ignored if it is applied to anything other than an individual CARRY\_SUM buffer or to a design entity containing CARRY\_SUM buffers. (This option also applies to MAX+PLUS II-style CARRY buffers.)

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name IGNORE_CARRY_BUFFERS <value>
set_global_assignment -name IGNORE_CARRY_BUFFERS -entity <entity name>
<value>
set_instance_assignment -name IGNORE_CARRY_BUFFERS -to <to> -entity <entity
name> <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name ignore_carry_buffers on
set_instance_assignment -name ignore_carry_buffers on -to foo
```





## IGNORE\_CASCADE\_BUFFERS

Ignores CASCADE buffers that are instantiated in the design. This option is ignored if it is applied to anything other than an individual CASCADE buffer or a design entity containing CASCADE buffers.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name IGNORE_CASCADE_BUFFERS <value>
set_global_assignment -name IGNORE_CASCADE_BUFFERS -entity <entity name>
<value>
set_instance_assignment -name IGNORE_CASCADE_BUFFERS -to <to> -entity
<entity name> <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name ignore_cascade_buffers on
set_instance_assignment -name ignore_cascade_buffers on -to foo
```

## IGNORE\_GLOBAL\_BUFFERS

Ignores GLOBAL buffers that are instantiated in the design. This option is ignored if it is applied to anything other than an individual GLOBAL buffer or a design entity containing GLOBAL buffers.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name IGNORE_GLOBAL_BUFFERS <value>  
set_global_assignment -name IGNORE_GLOBAL_BUFFERS -entity <entity name>  
<value>  
set_instance_assignment -name IGNORE_GLOBAL_BUFFERS -to <to> -entity  
<entity name> <value>
```

### Default Value

Off

## IGNORE\_LCELL\_BUFFERS

Ignores LCELL buffers that are instantiated in the design. This option is ignored if it is applied to anything other than an individual LCELL buffer or a design entity containing LCELL buffers.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

## Syntax

```
set_global_assignment -name IGNORE_LCELL_BUFFERS <value>
set_global_assignment -name IGNORE_LCELL_BUFFERS -entity <entity name>
<value>
set_instance_assignment -name IGNORE_LCELL_BUFFERS -to <to> -entity <entity
name> <value>
```

## Default Value

Off

## Example

```
set_global_assignment -name ignore_lcell_buffers on
set_instance_assignment -name ignore_lcell_buffers on -to foo
```

## IGNORE\_MAX\_FANOUT\_ASSIGNMENTS

Directs the Compiler to ignore the Maximum Fan-Out Assignments on a node, an entity, or the whole design. For HCII migration, the Maximum Fan-Out assignments can cause mismatches in Revision Compare. One can remove the Maximum Fan-Out assignments from the project but it is inconvenient/impossible as some assignments are embedded in the HDL sources. One should turn on this assignment to direct Quartus Prime to ignore the Maximum Fan-Out assignments.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

## Syntax

```
set_global_assignment -name IGNORE_MAX_FANOUT_ASSIGNMENTS <value>  
set_global_assignment -name IGNORE_MAX_FANOUT_ASSIGNMENTS -entity <entity  
name> <value>  
set_instance_assignment -name IGNORE_MAX_FANOUT_ASSIGNMENTS -to <to> -  
entity <entity name> <value>
```

## Default Value

Off

## IGNORE\_ROW\_GLOBAL\_BUFFERS

Ignores ROW GLOBAL buffers that are instantiated in the design. This option is ignored if it is applied to anything other than an individual GLOBAL buffer or a design entity containing GLOBAL buffers.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name IGNORE_ROW_GLOBAL_BUFFERS <value>  
set_global_assignment -name IGNORE_ROW_GLOBAL_BUFFERS -entity <entity name>  
<value>  
set_instance_assignment -name IGNORE_ROW_GLOBAL_BUFFERS -to <to> -entity  
<entity name> <value>
```

### Default Value

Off

## IGNORE\_SOFT\_BUFFERS

Ignores SOFT buffers that are instantiated in the design. This option is ignored if it is applied to anything other than an individual SOFT buffer or a design entity containing SOFT buffers.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.



## Syntax

```
set_global_assignment -name IGNORE_SOFT_BUFFERS <value>
set_global_assignment -name IGNORE_SOFT_BUFFERS -entity <entity name>
<value>
set_instance_assignment -name IGNORE_SOFT_BUFFERS -to <to> -entity <entity
name> <value>
```

## Default Value

On

## Example

```
set_global_assignment -name ignore_soft_buffers off
set_instance_assignment -name ignore_soft_buffers off -to foo
```

## IGNORE\_TRANSLATE\_OFF\_AND\_SYNTHESIS\_OFF

Instructs Analysis & Synthesis to ignore all `translate_off/synthesis_off` synthesis directives in your Verilog and VHDL design files. You can use this option to disable these synthesis directives and include previously ignored code during elaboration.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name IGNORE_TRANSLATE_OFF_AND_SYNTHESIS_OFF <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name ignore_translate_off_and_synthesis_off on
```

## IGNORE\_VERILOG\_INITIAL\_CONSTRUCTS

Instructs Analysis & Synthesis to ignore initial constructs and variable declaration assignments in your Verilog HDL design files. By default, Analysis & Synthesis derives power-up conditions for your design by elaborating these constructs. This option is provided for backwards compatibility with previous versions of the Quartus Prime software that ignored these constructs by default. You can use this option to restore the previous behavior of your design in the current version of the software.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name IGNORE_VERILOG_INITIAL_CONSTRUCTS <value>  
set_global_assignment -name IGNORE_VERILOG_INITIAL_CONSTRUCTS -entity  
<entity name> <value>  
set_instance_assignment -name IGNORE_VERILOG_INITIAL_CONSTRUCTS -to <to> -  
entity <entity name> <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name ignore_verilog_initial_constructs off
```

## IMPLEMENT\_AS\_CLOCK\_ENABLE

Specifies that this node should function as a clock enable signal for one or more registers.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_instance_assignment -name IMPLEMENT_AS_CLOCK_ENABLE -to <to> -entity  
<entity name> <value>
```

## IMPLEMENT\_AS\_OUTPUT\_OF\_LOGIC\_CELL

Implements the output of a primitive in a logic cell. You can apply this option to a logic function that would not ordinarily be implemented in a logic cell, typically a combinatorial function such as an AND2 gate. Implementing the output of a primitive a logic cell makes it possible to observe its output in simulation and timing analysis. However, because an additional logic cell is used, overall device utilization will increase. This option does not insert an additional logic cell on a function that is already implemented in a logic cell, such as a flipflop. This option is ignored if it is applied to anything other than a primitive.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_instance_assignment -name IMPLEMENT_AS_OUTPUT_OF_LOGIC_CELL -to <to> -  
entity <entity name> <value>
```

### Example

```
set_instance_assignment -name implement_as_output_of_logic_cell on -to foo
```

## INFER\_RAMs\_FROM\_RAW\_LOGIC

Instructs the Compiler to infer RAM from registers and multiplexers. Some HDL patterns that differ from Altera RAM templates are initially converted into logic. However, these structures function as RAM and, because of that, the Compiler may create an altsyncram megafunction instance for them at a later stage when this assignment is on. With this assignment is turned on, the Compiler may use more device RAM resources and less LABs.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name INFER_RAMs_FROM_RAW_LOGIC <value>
set_global_assignment -name INFER_RAMs_FROM_RAW_LOGIC -entity <entity name>
<value>
set_instance_assignment -name INFER_RAMs_FROM_RAW_LOGIC -to <to> -entity
<entity name> <value>
```

### Default Value

On

### Example

```
set_global_assignment -name infer_rams_from_raw_logic off
set_instance_assignment -name infer_rams_from_raw_logic off -to foo
```

## IP\_SEARCH\_PATHS

Specifies the IP search paths specific to the project.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IP_SEARCH_PATHS <value>
```

## LCELL\_INSERTION

Allows you to insert one or more logic cells between two nodes without changing the design files. The value you assign this option is the number of logic cells you want to insert. The inserted logic cell(s) act as a simple buffer and do not alter the functionality of the design. For more detailed information, go to Quartus Prime online help.

### Type

Integer

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- A
- E
- HardCopy II
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_instance_assignment -name LCELL_INSERTION -to <to> -entity <entity  
name> <value>  
set_instance_assignment -name LCELL_INSERTION -from <from> -to <to> -entity  
<entity name> <value>
```



## LIMIT\_AHDL\_INTEGERS\_TO\_32\_BITS

Specifies whether an AHDL-based design should have a limit on integer size of 32 bits. This option is provided for backward compatibility with pre-2000.09 releases of the Quartus software, which do not support integers larger than 32 bits in AHDL.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name LIMIT_AHDL_INTEGERS_TO_32_BITS <value>
```

### Default Value

Off

## MAX7000\_FANIN\_PER\_CELL

Specifies the maximum fan-in per macrocell. Legal integer values, in percentage terms, range from 20 through 100.

### Old Name

Maximum Fan-in Per Macrocell -- MAX 7000B/7000AE/3000A/7000S/7000A

### Type

Integer

### Device Support

- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name MAX7000_FANIN_PER_CELL <value>
set_global_assignment -name MAX7000_FANIN_PER_CELL -entity <entity name>
<value>
set_instance_assignment -name MAX7000_FANIN_PER_CELL -to <to> -entity
<entity name> <value>
```

### Default Value

100

### Example

```
set_global_assignment -name max7000_fanin_per_cell 20
set_instance_assignment -name max7000_fanin_per_cell 20 -to foo
```

## MAX7000\_IGNORE\_LCELL\_BUFFERS

Ignores LCELL buffers that are instantiated in the design. This option is ignored if it is applied to anything other than an individual LCELL buffer or a design entity containing LCELL buffers.

### Old Name

Ignore LCELL Buffers -- MAX 7000B/7000AE/3000A/7000S/7000A

### Type

Enumeration

### Values

- Auto
- Off
- On

### Device Support

- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name MAX7000_IGNORE_LCELL_BUFFERS <value>
set_global_assignment -name MAX7000_IGNORE_LCELL_BUFFERS -entity <entity
name> <value>
set_instance_assignment -name MAX7000_IGNORE_LCELL_BUFFERS -to <to> -entity
<entity name> <value>
```

### Default Value

AUTO

### Example

```
set_global_assignment -name max7000_ignore_lcell_buffers on
set_instance_assignment -name max7000_ignore_lcell_buffers on -to foo
```

## MAX7000\_IGNORE\_SOFT\_BUFFERS

Ignores SOFT buffers that are instantiated in the design. This option is ignored if it is applied to anything other than an individual SOFT buffer or a design entity containing SOFT buffers.

### Old Name

Ignore SOFT Buffers -- MAX 7000B/7000AE/3000A/7000S/7000A

### Type

Boolean

### Device Support

- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name MAX7000_IGNORE_SOFT_BUFFERS <value>
set_global_assignment -name MAX7000_IGNORE_SOFT_BUFFERS -entity <entity
name> <value>
set_instance_assignment -name MAX7000_IGNORE_SOFT_BUFFERS -to <to> -entity
<entity name> <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name max7000_ignore_soft_buffers on
set_instance_assignment -name max7000_ignore_soft_buffers on -to foo
```

## MAX7000\_OPTIMIZATION\_TECHNIQUE

Specifies the overall optimization goal for Analysis & Synthesis: attempt to maximize performance or minimize logic usage.

### Old Name

Optimization Technique -- MAX 7000B/7000AE/3000A/7000S/7000A

### Type

Enumeration

### Values

- Area
- Balanced
- Speed

### Device Support

- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name MAX7000_OPTIMIZATION_TECHNIQUE <value>
set_global_assignment -name MAX7000_OPTIMIZATION_TECHNIQUE -entity <entity
name> <value>
set_instance_assignment -name MAX7000_OPTIMIZATION_TECHNIQUE -to <to> -
entity <entity name> <value>
```

### Default Value

Speed

### Example

```
set_global_assignment -name max7000_optimization_technique balanced
```

## MAX7000\_PARALLEL\_EXPANDER\_CHAIN\_LENGTH

Specifies the maximum allowable length of a chain of Compiler-synthesized parallel expander product terms.

### Old Name

Parallel Expander Chain Length -- MAX 7000B/7000AE/3000A/7000S/7000A

### Type

Integer

### Device Support

- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name MAX7000_PARALLEL_EXPANDER_CHAIN_LENGTH <value>
set_global_assignment -name MAX7000_PARALLEL_EXPANDER_CHAIN_LENGTH -entity
<entity name> <value>
set_instance_assignment -name MAX7000_PARALLEL_EXPANDER_CHAIN_LENGTH -to
<to> -entity <entity name> <value>
```

### Default Value

4

### Example

```
set_global_assignment -name max7000_parallel_expander_chain_length 3
```



## MAXII\_OPTIMIZATION\_TECHNIQUE

Specifies the overall optimization goal for Analysis & Synthesis: attempt to maximize performance, minimize logic usage, or balance high performance with minimal logic usage.

### Old Name

Optimization Technique -- MAX II, TSUNAMI\_OPTIMIZATION\_TECHNIQUE

### Type

Enumeration

### Values

- Area
- Balanced
- Speed

### Device Support

- MAX II
- MAX V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name MAXII_OPTIMIZATION_TECHNIQUE <value>
set_global_assignment -name MAXII_OPTIMIZATION_TECHNIQUE -entity <entity
name> <value>
set_instance_assignment -name MAXII_OPTIMIZATION_TECHNIQUE -to <to> -entity
<entity name> <value>
```

### Default Value

Balanced

### Example

```
set_global_assignment -name maxii_optimization_technique speed
```

## MAX\_AUTO\_GLOBAL\_REGISTER\_CONTROLS

Allows the Compiler to choose the signals that feed the most control signal inputs to flipflops (excluding clock signals) as global signals that are made available throughout the device on the global routing paths. Depending on the target device family, these control signals can include asynchronous clear and load, synchronous clear and load, clock enable, and preset signals. If you want to prevent the Compiler from automatically selecting a particular signal as global register control signal, set the Global Signal option to 'Off' on that signal.

### Old Name

Auto Global Register Control Signals -- MAX 7000B/7000AE/3000A/7000S/7000A

### Type

Boolean

### Device Support

- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S

### Notes

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name MAX_AUTO_GLOBAL_REGISTER_CONTROLS <value>
set_global_assignment -name MAX_AUTO_GLOBAL_REGISTER_CONTROLS -entity
<entity name> <value>
set_instance_assignment -name MAX_AUTO_GLOBAL_REGISTER_CONTROLS -to <to> -
entity <entity name> <value>
```

### Default Value

On

### Example

```
set_global_assignment -name max_auto_global_register_controls off
set_instance_assignment -name max_auto_global_register_controls off -to foo
```



## MAX\_BALANCING\_DSP\_BLOCKS

Allows you to specify the maximum number of DSP blocks that the DSP block balancer will assume exist in the current device for each partition. This option overrides the usual method of using the maximum number of DSP blocks the current device supports. For HardCopy II devices, the number of DSP blocks represents the number of DSP blocks used in the equivalent Stratix II device. This option is useful for HardCopy II device migration, where the number of DSP blocks that can be implemented in a HardCopy II device is more than the number of DSP blocks that can be implemented in its equivalent Stratix II device. This option is also useful in incremental compilation to set different DSP block usage limits for different partitions.

### Type

Integer

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

## Syntax

```
set_global_assignment -name MAX_BALANCING_DSP_BLOCKS <value>  
set_instance_assignment -name MAX_BALANCING_DSP_BLOCKS -to <to> -entity  
<entity name> <value>
```

## Default Value

-1 (Unlimited)

## Example

```
set_global_assignment -name max_balancing_dsp_blocks 4  
set_instance_assignment -name max_balancing_dsp -to  
"my_partition_root_entity:my_partition_root_entity_inst"
```

## MAX\_FANOUT

Directs the Compiler to control the number of destinations the specified node feeds so the fan-out count does not exceed the value specified as the maximum number of fan-out allowed from the node.

### Type

Integer

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name MAX_FANOUT -entity <entity name> <value>  
set_instance_assignment -name MAX_FANOUT -to <to> -entity <entity name>  
<value>
```

### Example

```
set_instance_assignment -name max_fanout 10 -to foo
```



## MAX\_LABS

Allows you to specify the maximum number of LABs that Analysis & Synthesis should try to utilize for a device. This option overrides the usual method of using the maximum number of LABs the current device supports, when the value is non-negative and is less than the maximum number of LABs available on the current device.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name MAX_LABS <value>  
set_instance_assignment -name MAX_LABS -to <to> -entity <entity name>  
<value>
```

### Default Value

-1 (Unlimited)

### Example

```
set_global_assignment -name max_labs 100
```

## MAX\_NUMBER\_OF\_REGISTERS\_FROM\_UNINFERRED\_RAMs

Allows you to specify the maximum number of registers that Analysis & Synthesis can use for conversion of uninferred RAMs. You can use this option as a project-wide option or on a specific partition by setting the assignment on the instance name of the partition root. The assignment on a partition overrides the global assignment (if any) for that particular partition. This option prevents synthesis from causing long compilations and running out of memory when many registers are used for uninferred RAMs. Instead of continuing the compilation, the Quartus Prime software issues an error and exits.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name MAX_NUMBER_OF_REGISTERS_FROM_UNINFERRED_RAMs  
<value>  
set_instance_assignment -name MAX_NUMBER_OF_REGISTERS_FROM_UNINFERRED_RAMs -  
to <to> -entity <entity name> <value>
```

### Default Value

-1 (Unlimited)

### Example

```
2048 set_global_assignment -name max_number_of_registers_from_uninferred_rams
```

## MAX\_RAM\_BLOCKS\_M4K

Allows you to specify the maximum number of M4K,M9K,M20K,or M10K memory blocks that the Compiler may use for a device. This option overrides the usual method of using the maximum number of M4K,M9K,M20K, or M10K memory blocks the current device supports, when the value is non-negative and is less than the maximum number of M4K,M9K,M20K, or M10K memory blocks available on the current device.

### Type

Integer

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

## Syntax

```
set_global_assignment -name MAX_RAM_BLOCKS_M4K <value>  
set_instance_assignment -name MAX_RAM_BLOCKS_M4K -to <to> -entity <entity  
name> <value>
```

## Default Value

-1 (Unlimited)

## Example

```
set_global_assignment -name max_ram_blocks_m4k 4
```

## See Also

Maximum Number of M512 Memory Blocks Maximum Number of M-RAM Memory Blocks



## MAX\_RAM\_BLOCKS\_M512

Allows you to specify the maximum number of M512 memory blocks that the Compiler may utilize for a device. This option overrides the usual method of using the maximum number of M512 memory blocks the current device supports, when the value is non-negative and is less than the maximum number of M512 memory blocks available on the current device.

### Type

Integer

### Device Support

- Arria GX
- Cyclone
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name MAX_RAM_BLOCKS_M512 <value>  
set_instance_assignment -name MAX_RAM_BLOCKS_M512 -to <to> -entity <entity  
name> <value>
```

### Default Value

-1 (Unlimited)

### Example

```
set_global_assignment -name max_ram_blocks_m512 4
```

### See Also

Maximum Number of M4K Memory Blocks Maximum Number of M-RAM Memory Blocks

## MAX\_RAM\_BLOCKS\_MRAM

Allows you to specify the maximum number of M-RAM/M144K memory blocks that the Compiler may utilize for a device. This option overrides the usual method of using the maximum number of M-RAM/M144K memory blocks the selected device supports, when the value is non-negative and is less than the maximum number of M-RAM/M144K memory blocks available on the current device.

### Type

Integer

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name MAX_RAM_BLOCKS_MRAM <value>  
set_instance_assignment -name MAX_RAM_BLOCKS_MRAM -to <to> -entity <entity  
name> <value>
```

### Default Value

-1 (Unlimited)

### Example

```
set_global_assignment -name max_ram_blocks_mram 4
```

## See Also

Maximum Number of M512 Memory Blocks Maximum Number of M4K Memory Blocks

## MERCURY\_CARRY\_CHAIN\_LENGTH

Specifies the maximum allowable length of a chain of both user-entered and Compiler-synthesized CARRY\_SUM buffers. Carry chains that exceed this length are broken into separate chains. (This option also applies to MAX+PLUS II-style CARRY buffers.)

### Old Name

Carry Chain Length -- Mercury

### Type

Integer

### Device Support

Mercury

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name MERCURY_CARRY_CHAIN_LENGTH <value>
set_global_assignment -name MERCURY_CARRY_CHAIN_LENGTH -entity <entity
name> <value>
set_instance_assignment -name MERCURY_CARRY_CHAIN_LENGTH -to <to> -entity
<entity name> <value>
```

### Default Value

48

## MERCURY\_OPTIMIZATION\_TECHNIQUE

Specifies the overall optimization goal for Analysis & Synthesis: attempt to maximize performance or minimize logic usage.

### Old Name

Optimization Technique -- Mercury

### Type

Enumeration

### Values

- Area
- Speed

### Device Support

Mercury

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name MERCURY_OPTIMIZATION_TECHNIQUE <value>
set_global_assignment -name MERCURY_OPTIMIZATION_TECHNIQUE -entity <entity
name> <value>
set_instance_assignment -name MERCURY_OPTIMIZATION_TECHNIQUE -to <to> -
entity <entity name> <value>
```

### Default Value

Area

### Example

```
set_global_assignment -name mercury_optimization_technique speed
```

## MLAB\_ADD\_TIMING\_CONSTRAINTS\_FOR\_MIXED\_PORT\_FEED\_THROUGH\_MODE\_SETTING\_DONT\_CARE

Allows you to specify whether you want the TimeQuest Timing Analyzer to evaluate timing constraints between the write and the read operation of the MLAB memory block. Performing a write and read operation simultaneously at the same address might result in metastability because no timing constraints between those operations exist by default. Turning on this option introduces timing constraints between the write and read operation on the MLAB memory block and thereby avoids metastability issues; however, turning on this option degrades the performance of the MLAB memory blocks. If your design does not perform write and read operations simultaneously at the same address you do not need to set this option.

### Type

Boolean

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone V
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name
MLAB_ADD_TIMING_CONSTRAINTS_FOR_MIXED_PORT_FEED_THROUGH_MODE_SETTING_DONT_CARE -
entity <entity name> <value>
set_instance_assignment -name
MLAB_ADD_TIMING_CONSTRAINTS_FOR_MIXED_PORT_FEED_THROUGH_MODE_SETTING_DONT_CARE -to
<to> -entity <entity name> <value>
set_global_assignment -name
MLAB_ADD_TIMING_CONSTRAINTS_FOR_MIXED_PORT_FEED_THROUGH_MODE_SETTING_DONT_CARE
<value>
```

### Default Value

Off

## MUX\_RESTRUCTURE

Allows the Compiler to reduce the number of logic elements required to implement multiplexers in a design. This option is useful if your design contains buses of fragmented multiplexers. This option repacks multiplexers more efficiently for area, allowing the design to implement multiplexers with a reduced number of logic elements. You can select the 'On' setting to minimize your design area; it will decrease logic element usage but may negatively affect design clock speed (fMAX). You can select the 'Off' to disable multiplexer restructuring; it does not decrease logic element usage and does not affect design clock speed (fMAX). You may select 'Auto' setting to allow the Quartus Prime software to determine whether multiplexer restructuring should be enabled. The Quartus Prime software uses other synthesis settings, for example, the Optimization Technique option, to determine if multiplexer restructuring should be applied to the design; the 'Auto' setting will decrease logic element usage but may negatively affect design clock speed (fMAX).

### Type

Enumeration

### Values

- Auto
- Off
- On

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

- Stratix III
- Stratix IV
- Stratix V

## Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

## Syntax

```
set_global_assignment -name MUX_RESTRUCTURE <value>
set_global_assignment -name MUX_RESTRUCTURE -entity <entity name> <value>
set_instance_assignment -name MUX_RESTRUCTURE -to <to> -entity <entity
name> <value>
```

## Default Value

Auto

## Example

```
set_global_assignment -name mux_restructure off
set_instance_assignment -name mux_restructure on -to accel
```



## NOT\_GATE\_PUSH\_BACK

Allows the Compiler to push an inversion (that is, a NOT gate) back through a register and implement it on that register's data input if it is necessary to implement the design. If this option is turned on, a register may power up to an active-high state, so it may need to be explicitly cleared during initial operation of the device. This option is ignored if it is applied to anything other than an individual register or a design entity containing registers. If it is applied to an output pin that is directly fed by a register, it is automatically transferred to that register.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name NOT_GATE_PUSH_BACK -entity <entity name> <value>
set_instance_assignment -name NOT_GATE_PUSH_BACK -to <to> -entity <entity
name> <value>
set_global_assignment -name NOT_GATE_PUSH_BACK <value>
```

### Default Value

On

### Example

```
set_global_assignment -name not_gate_push_back off
set_instance_assignment -name not_gate_push_back off -to reg
```

## NUMBER\_OF\_INVERTED\_REGISTERS\_REPORTED

Allows you to specify the maximum number of inverted registers that the Synthesis Report should display.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name NUMBER_OF_INVERTED_REGISTERS_REPORTED <value>
```

### Default Value

100

### Example

```
set_global_assignment -name NUMBER_OF_INVERTED_REGISTERS_REPORTED 200
```

## NUMBER\_OF\_PROTECTED\_REGISTERS\_REPORTED

Allows you to specify the maximum number of protected registers that the Synthesis Report should display.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name NUMBER_OF_PROTECTED_REGISTERS_REPORTED <value>
```

### Default Value

100

### Example

```
set_global_assignment -name NUMBER_OF_PROTECTED_REGISTERS_REPORTED 200
```

## NUMBER\_OF\_REMOVED\_REGISTERS\_REPORTED

Allows you to specify the maximum number of removed registers that the Synthesis Report should display.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name NUMBER_OF_REMOVED_REGISTERS_REPORTED <value>
```

### Default Value

5000

### Example

```
set_global_assignment -name NUMBER_OF_REMOVED_REGISTERS_REPORTED 200
```



## NUMBER\_OF\_SWEPT\_NODES\_REPORTED

Allows you to specify the maximum number of swept nodes that the Synthesis Report displays. A swept node is any node which was eliminated from your design because the Quartus Prime software found the node to be unnecessary.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name NUMBER_OF_SWEPT_NODES_REPORTED <value>
```

### Default Value

5000

### Example

```
set_global_assignment -name NUMBER_OF_SWEPT_NODES_REPORTED 200
```

## NUMBER\_OF\_SYNTHESIS\_MIGRATION\_ROWS

Allows you to specify the maximum number of rows that a report in Synthesis Migration Checks should display.

### Type

Integer

### Device Support

Arria 10

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name NUMBER_OF_SYNTHESIS_MIGRATION_ROWS <value>
```

### Default Value

5000

### Example

```
set_global_assignment -name NUMBER_OF_SYNTHESIS_MIGRATION_ROWS 200
```

## OCP\_HW\_EVAL

Enables or disables OpenCore Plus hardware evaluation feature.

### Type

Enumeration

### Values

- Disable
- Enable

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name OCP_HW_EVAL <value>
```

### Default Value

Enable

## OPTIMIZATION\_TECHNIQUE

Specifies the overall optimization goal for Analysis & Synthesis: attempt to maximize performance, minimize logic usage, or balance high performance with minimal logic usage.

### Old Name

Optimization Technique -- Stratix IV

### Type

Enumeration

### Values

- Area
- Balanced
- Speed

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone V
- HardCopy IV
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name OPTIMIZATION_TECHNIQUE <value>
set_global_assignment -name OPTIMIZATION_TECHNIQUE -entity <entity name>
<value>
set_instance_assignment -name OPTIMIZATION_TECHNIQUE -to <to> -entity
<entity name> <value>
```

### Default Value

Balanced



## Example

```
set_global_assignment -name optimization_technique speed
```

## OPTIMIZE\_POWER\_DURING\_SYNTHESIS

Controls the power-driven compilation setting of Analysis & Synthesis. This option determines how aggressively Analysis & Synthesis optimizes the design for power. If this option is set to 'Off', Analysis & Synthesis does not perform any power optimizations. If this option is set to 'Normal compilation', Analysis & Synthesis performs power optimizations as long as they are not expected to reduce design performance. When this option is set to 'Extra effort', Analysis & Synthesis will perform additional power optimizations which may reduce design performance.

### Type

Enumeration

### Values

- Extra effort
- Normal compilation
- Off

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

## Notes

This assignment is included in the Fitter report.

This assignment supports synthesis wildcards.

## Syntax

```
set_global_assignment -name OPTIMIZE_POWER_DURING_SYNTHESIS <value>
set_global_assignment -name OPTIMIZE_POWER_DURING_SYNTHESIS -entity <entity
name> <value>
set_instance_assignment -name OPTIMIZE_POWER_DURING_SYNTHESIS -to <to> -
entity <entity name> <value>
```

## Default Value

Normal compilation

## Example

```
set_global_assignment -name optimize_power_during_synthesis off
```

## PARALLEL\_EXPANDER\_CHAIN\_LENGTH

Specifies the maximum allowable length of a chain of Compiler-synthesized parallel expander product terms.

### Old Name

Parallel Expander Chain Length -- APEX 20K/APEX 20KE/APEX 20KC/APEX II/ARM-based Excalibur

### Type

Integer

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name PARALLEL_EXPANDER_CHAIN_LENGTH <value>
set_global_assignment -name PARALLEL_EXPANDER_CHAIN_LENGTH -entity <entity
name> <value>
set_instance_assignment -name PARALLEL_EXPANDER_CHAIN_LENGTH -to <to> -
entity <entity name> <value>
```

### Default Value

16

## PARALLEL\_SYNTHESIS

Option to enable/disable parallel synthesis

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name PARALLEL_SYNTHESIS <value>
```

### Default Value

On

### Example

```
set_global_assignment -name parallel_synthesis on
```

## PARAMETER

Assigns an attribute that determines the logic created or used to implement the function, for example, the width of a bus. Parameters are characteristics that determine the size, behavior, or silicon implementation of a function. Parameter values are inherited from project defaults or higher hierarchical levels unless you make explicit assignments to individual nodes. Parameters are also overridden by explicit logic synthesis and fitting options.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_parameter <value>  
set_parameter -entity <entity name> <value>
```

## POWER\_UP\_LEVEL

Causes a register to power up with the specified logic level, either High (1) or Low (0). If this option is specified for an input pin, it is automatically transferred to the register that is driven by the pin if the following conditions are present: (1) there is no intervening logic, other than inversion, between the pin and the register; (2) the input pin drives the data input of the register; and (3) the input pin does not fan-out to any other logic. If this option is specified for an output or bidirectional pin, it is automatically transferred to the register that feeds the pin if: (1) there is no intervening logic, other than inversion, between the register and the pin; and (2) the register does not fan-out to any other logic. You can assign this option to any register, or to a pin with any logic configuration other than those described above. You can also assign this option to a design entity containing registers if you want to set the power level for all registers in the design entity. In order for the register to power up with the specified logic level, the Compiler may perform NOT Gate Push-Back on the register.

### Type

Enumeration

### Values

- High
- Low

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name POWER_UP_LEVEL -entity <entity name> <value>
set_instance_assignment -name POWER_UP_LEVEL -to <to> -entity <entity name>
<value>
```

### Example

```
set_instance_assignment -name power_up_level low -to foo
```

### See Also

Power-Up Don't Care

## PRESERVE\_FANOUT\_FREE\_NODE

Prevents a register that has no fan-out from being removed during synthesis.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

None

### Syntax

```
set_instance_assignment -name PRESERVE_FANOUT_FREE_NODE -to <to> -entity  
<entity name> <value>
```

### Example

```
set_instance_assignment -name preserve_fanout_free_node on -to reg
```



## PRESERVE\_REGISTER

Prevents a register from minimizing away during synthesis and prevents sequential netlist optimizations. Sequential netlist optimizations can eliminate redundant registers and registers with constant drivers.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports Fitter wildcards.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name PRESERVE_REGISTER -entity <entity name> <value>  
set_instance_assignment -name PRESERVE_REGISTER -to <to> -entity <entity  
name> <value>
```

### Example

```
set_instance_assignment -name preserve_register on -to foo
```

## PRE\_MAPPING\_RESYNTHESIS

Specifies that the Quartus Prime software should perform a resynthesis optimization step immediately before technology mapping. The 'On' setting increases design performance; it will increase design clock speed (fMAX) but may also slightly increase logic element usage and compilation time. The 'Off' selection disables this optimization.

### Type

Boolean

### Device Support

- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- MAX 10
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name PRE_MAPPING_RESYNTHESIS <value>
```

### Default Value

Off



## PRPOF\_ID

Specifies whether a register is a unique partial reconfiguration bitstream identifier. The same identifier value will be used to generate the partial reconfiguration bitstream.

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment is included in the Fitter report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name PRPOF_ID -entity <entity name> <value>
set_instance_assignment -name PRPOF_ID -to <to> -entity <entity name>
<value>
set_global_assignment -name PRPOF_ID <value>
```

### Default Value

Off

### Example

```
set_instance_assignment -name prpof_id on -to reg
```

## RBCGEN\_CRITICAL\_WARNING\_TO\_ERROR

To convert Quartus Prime critical warning to error.

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name RBCGEN_CRITICAL_WARNING_TO_ERROR <value>
```

### Default Value

On



## REMOVE\_DUPLICATE\_REGISTERS

Removes a register if it is identical to another register. If two registers generate the same logic, the second one will be deleted and the first one will be made to fan out to the second one's destinations. Also, if the deleted register has different logic option assignments, they will be ignored. This option is useful if you wish to prevent the Compiler from removing duplicate registers that you have used deliberately. You can do this by setting the option to Off. This option is ignored if it is applied to anything other than an individual register or a design entity containing registers.

### Old Name

DUPLICATE\_REGISTER\_EXTRACTION

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name REMOVE_DUPLICATE_REGISTERS <value>
set_global_assignment -name REMOVE_DUPLICATE_REGISTERS -entity <entity
name> <value>
set_instance_assignment -name REMOVE_DUPLICATE_REGISTERS -to <to> -entity
<entity name> <value>
```

### Default Value

On

### Example

```
set_global_assignment -name remove_duplicate_registers off
set_instance_assignment -name remove_duplicate_registers off -to foo
```

## REMOVE\_REDUNDANT\_LOGIC\_CELLS

Removes redundant LCELL primitives or WYSIWYG primitives. Turning this option on optimizes a circuit for area and speed. This option is ignored if it is applied to anything other than a design entity.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

## Syntax

```
set_global_assignment -name REMOVE_REDUNDANT_LOGIC_CELLS -entity <entity  
name> <value>  
set_instance_assignment -name REMOVE_REDUNDANT_LOGIC_CELLS -to <to> -entity  
<entity name> <value>  
set_global_assignment -name REMOVE_REDUNDANT_LOGIC_CELLS <value>
```

## Default Value

Off

## Example

```
set_global_assignment -name remove_redundant_logic_cells on  
set_instance_assignment -name remove_redundant_logic_cells on -to node
```

## REPORT\_CONNECTIVITY\_CHECKS

Specifies whether the synthesis report should include the panels in the Connectivity Checks folder

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name REPORT_CONNECTIVITY_CHECKS <value>
```

### Default Value

On





## REPORT\_PARAMETER\_SETTINGS

Specifies whether the synthesis report should include the panels in the Parameter Settings by Entity Instance folder

### Old Name

SHOW\_PARAMETER\_SETTINGS\_TABLES\_IN\_SYNTHESIS\_REPORT

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name REPORT_PARAMETER_SETTINGS <value>
```

### Default Value

On

## REPORT\_PARAMETER\_SETTINGS\_PRO

Specifies whether the synthesis report should include the panels in the Parameter Settings by Entity Instance folder

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name REPORT_PARAMETER_SETTINGS_PRO <value>
```

### Default Value

On



## REPORT\_SOURCE\_ASSIGNMENTS

Specifies whether the synthesis report should include the panels in the Source Assignments folder

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name REPORT_SOURCE_ASSIGNMENTS <value>
```

### Default Value

On

## REPORT\_SOURCE\_ASSIGNMENTS\_PRO

Specifies whether the synthesis report should include the panels in the Source Assignments folder

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name REPORT_SOURCE_ASSIGNMENTS_PRO <value>
```

### Default Value

On

## RESYNTHESIS\_OPTIMIZATION\_EFFORT

Specifies whether the resynthesis tool should focus on fmax or area during resynthesis.

### Type

Enumeration

### Values

- Low
- Normal

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name RESYNTHESIS_OPTIMIZATION_EFFORT -section_id  
<section identifier> <value>  
set_global_assignment -name RESYNTHESIS_OPTIMIZATION_EFFORT -entity <entity  
name> -section_id <section identifier> <value>
```

### Default Value

Normal, requires section identifier

## RESYNTHESIS\_PHYSICAL\_SYNTHESIS

Specifies the physical synthesis level for resynthesis.

### Type

Enumeration

### Values

- ADVANCED
- Normal

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name RESYNTHESIS_PHYSICAL_SYNTHESIS -section_id  
<section identifier> <value>  
set_global_assignment -name RESYNTHESIS_PHYSICAL_SYNTHESIS -entity <entity  
name> -section_id <section identifier> <value>
```

### Default Value

Normal, requires section identifier

## RESYNTHESIS\_RETIMING

Specifies the paths on which retiming will be performed: all paths, register-to-register paths only, or none.

### Type

Enumeration

### Values

- CORE
- Full
- Off

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name RESYNTHESIS_RETIMING -section_id <section  
identifier> <value>  
set_global_assignment -name RESYNTHESIS_RETIMING -entity <entity name> -  
section_id <section identifier> <value>
```

### Default Value

FULL, requires section identifier

## SAFE\_STATE\_MACHINE

Tells the compiler to implement state machines that can recover gracefully from an illegal state.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name SAFE_STATE_MACHINE -entity <entity name> <value>
set_instance_assignment -name SAFE_STATE_MACHINE -to <to> -entity <entity
name> <value>
set_global_assignment -name SAFE_STATE_MACHINE <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name safe_state_machine on
set_instance_assignment -name safe_state_machine on -to foo
```

### See Also

State Machine Processing Extract Verilog State Machines Extract VHDL State Machines



## SAVE\_DISK\_SPACE

Saves disk space by reducing the number of node names available for entering assignments, simulation, timing analysis, reporting, etc.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name SAVE_DISK_SPACE <value>
```

### Default Value

On

## SEARCH\_PATH

Specifies the path name of a user-defined library.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SEARCH_PATH <value>
```



## SHIFT\_REGISTER\_RECOGNITION\_ACLR\_SIGNAL

Allows the Compiler to find a group of shift registers of the same length that can be replaced with the `altshift_taps` megafunction. The shift registers must all use the same `aclr` signals, must not have any other secondary signals, and must have equally spaced taps that are at least three registers apart. To use this option, you must turn on the Auto Shift Register Replacement logic option.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name SHIFT_REGISTER_RECOGNITION_ACLR_SIGNAL <value>
set_global_assignment -name SHIFT_REGISTER_RECOGNITION_ACLR_SIGNAL -entity
<entity name> <value>
set_instance_assignment -name SHIFT_REGISTER_RECOGNITION_ACLR_SIGNAL -to
<to> -entity <entity name> <value>
```

### Default Value

On

### Example

```
set_global_assignment -name shift_register_recognition_aclr_signal off
set_instance_assignment -name shift_register_recognition_aclr_signal off -
to foo
```



## SMART\_COMPILE\_IGNORES\_TDC\_FOR\_STRATIX\_PLL\_CHANGES

Allows the Compiler to skip the fitting stage during smart recompilation when design changes may affect timing requirements. This option is available only for changes to Cyclone, Stratix, and Stratix GX PLL parameters, and Stratix GX gigabit transceiver block (GXB) parameters.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name  
SMART_COMPILE_IGNORES_TDC_FOR_STRATIX_PLL_CHANGES <value>
```

### Default Value

Off

## STATE\_MACHINE\_PROCESSING

Specifies the processing style used to compile a state machine. You can use your own 'User-Encoded' style, or select 'One-Hot', 'Minimal Bits', 'Gray', 'Johnson', 'Sequential' or 'Auto' (Compiler-selected) encoding.

### Type

Enumeration

### Values

- Auto
- Gray
- Johnson
- Minimal Bits
- One-Hot
- Sequential
- User-Encoded

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
<value> set_global_assignment -name STATE_MACHINE_PROCESSING -entity <entity name>  
<entity name> <value> set_instance_assignment -name STATE_MACHINE_PROCESSING -to <to> -entity  
set_global_assignment -name STATE_MACHINE_PROCESSING <value>
```

### Default Value

Auto

### Example

```
set_global_assignment -name state_machine_processing "one-hot"  
set_instance_assignment -name state_machine_processing "one-hot" -to foo
```

### See Also

Extract Verilog State Machines Extract VHDL State Machines

## STRATIXGX\_BYPASS\_REMAPPING\_OF\_FORCE\_SIGNAL\_DETECT\_SIGNAL\_THRESHOLD\_SELECT

Directs the compiler to not modify the Force Signal Detect and Signal Threshold Select parameters on GXB Receiver channels

### Type

Boolean

### Device Support

- Arria GX
- Stratix GX
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name  
STRATIXGX_BYPASS_REMAPPING_OF_FORCE_SIGNAL_DETECT_SIGNAL_THRESHOLD_SELECT <value>
```

### Default Value

Off

## STRATIXII\_CARRY\_CHAIN\_LENGTH

Specifies the maximum allowable length of a chain of both user-entered and Compiler-synthesized CARRY\_SUM buffers. Carry chains that exceed this length are broken into separate chains. (This option also applies to MAX+PLUS II-style CARRY buffers.)

### Old Name

ARMSTRONG\_CARRY\_CHAIN\_LENGTH, Carry Chain Length -- Stratix II/Stratix III

### Type

Integer

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name STRATIXII_CARRY_CHAIN_LENGTH <value>
set_global_assignment -name STRATIXII_CARRY_CHAIN_LENGTH -entity <entity
name> <value>
set_instance_assignment -name STRATIXII_CARRY_CHAIN_LENGTH -to <to> -entity
<entity name> <value>
```

### Default Value

70

## STRATIXII\_OPTIMIZATION\_TECHNIQUE

Specifies the overall optimization goal for Analysis & Synthesis: attempt to maximize performance, minimize logic usage, or balance high performance with minimal logic usage.

### Old Name

ARMSTRONG\_OPTIMIZATION\_TECHNIQUE, Optimization Technique -- Stratix II/III/HardCopy II/  
Stratix II GX/Arria GX

### Type

Enumeration

### Values

- Area
- Balanced
- Speed

### Device Support

- Arria GX
- HardCopy II
- HardCopy III
- Stratix II
- Stratix II GX
- Stratix III

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name STRATIXII_OPTIMIZATION_TECHNIQUE <value>
set_global_assignment -name STRATIXII_OPTIMIZATION_TECHNIQUE -entity
<entity name> <value>
set_instance_assignment -name STRATIXII_OPTIMIZATION_TECHNIQUE -to <to> -
entity <entity name> <value>
```

### Default Value

Balanced

### Example

```
set_global_assignment -name stratixii_optimization_technique speed
```



## STRATIX\_CARRY\_CHAIN\_LENGTH

Specifies the maximum allowable length of a chain of both user-entered and Compiler-synthesized CARRY\_SUM buffers. Carry chains that exceed this length are broken into separate chains. (This option also applies to MAX+PLUS II-style CARRY buffers.)

### Old Name

Carry Chain Length -- Stratix/Stratix GX/Cyclone/MAX II/Cyclone II/Cyclone III

### Type

Integer

### Device Support

- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name STRATIX_CARRY_CHAIN_LENGTH <value>
set_global_assignment -name STRATIX_CARRY_CHAIN_LENGTH -entity <entity
name> <value>
set_instance_assignment -name STRATIX_CARRY_CHAIN_LENGTH -to <to> -entity
<entity name> <value>
```

### Default Value

70



## STRATIX\_OPTIMIZATION\_TECHNIQUE

Specifies the overall optimization goal for Analysis & Synthesis: attempt to maximize performance, minimize logic usage, or balance high performance with minimal logic usage.

### Old Name

Optimization Technique -- Stratix/Stratix GX, YEAGER\_OPTIMIZATION\_TECHNIQUE

### Type

Enumeration

### Values

- Area
- Balanced
- Speed

### Device Support

- Stratix
- Stratix GX

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name STRATIX_OPTIMIZATION_TECHNIQUE <value>  
set_global_assignment -name STRATIX_OPTIMIZATION_TECHNIQUE -entity <entity  
name> <value>  
set_instance_assignment -name STRATIX_OPTIMIZATION_TECHNIQUE -to <to> -  
entity <entity name> <value>
```

### Default Value

Balanced

### Example

```
set_global_assignment -name stratix_optimization_technique speed
```

## STRICT\_RAM\_RECOGNITION

When this option is ON, the Compiler is only allowed to replace RAM if the hardware matches the design exactly.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name STRICT_RAM_RECOGNITION <value>  
set_global_assignment -name STRICT_RAM_RECOGNITION -entity <entity name>  
<value>
```

```
set_instance_assignment -name STRICT_RAM_RECOGNITION -to <to> -entity  
<entity name> <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name strict_ram_recognition on  
set_global_assignment -name strict_ram_recognition on -to foo
```

## SYNCHRONIZATION\_REGISTER\_CHAIN\_LENGTH

This setting specifies the maximum number of registers in a row to be considered as a synchronization chain. Synchronization chains are sequences of registers with the same clock, no fanout in between, such that the first register is fed by a pin, or by logic in another clock domain. These registers will be considered for metastability analysis (available for some families), and are also protected from optimizations such as retiming. When gate-level retiming is turned on, these registers will not be moved. The default length is device-specific.

### Old Name

ADV\_NETLIST\_OPT\_METASTABLE\_REGS

### Type

Integer

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name SYNCHRONIZATION_REGISTER_CHAIN_LENGTH <value>
set_global_assignment -name SYNCHRONIZATION_REGISTER_CHAIN_LENGTH -entity
<entity name> <value>
set_instance_assignment -name SYNCHRONIZATION_REGISTER_CHAIN_LENGTH -to
<to> -entity <entity name> <value>
```

## SYNTHESIS\_EFFORT

Controls the synthesis trade-off between compilation speed and performance and area. The default is 'Auto'. You can select 'Fast' for faster compilation speed at the cost of performance and area.

### Type

Enumeration

### Values

- Auto
- Fast

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name SYNTHESIS_EFFORT <value>
```

### Default Value

Auto

### Example

```
set_global_assignment -name synthesis_effort fast
```

## SYNTHESIS\_KEEP\_SYNCH\_CLEAR\_PRESET\_BEHAVIOR\_IN\_UNMAPPER

When this option is set to On, synthesis will keep the synchronous clear/preset behavior when remap I/O wysiwyg primitives (from other device families) using DDIO INPUT feature to the targeted device family.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name  
SYNTHESIS_KEEP_SYNCH_CLEAR_PRESET_BEHAVIOR_IN_UNMAPPER -entity <entity name> <value>  
set_instance_assignment -name  
SYNTHESIS_KEEP_SYNCH_CLEAR_PRESET_BEHAVIOR_IN_UNMAPPER -to <to> -entity <entity  
name> <value>  
set_global_assignment -name  
SYNTHESIS_KEEP_SYNCH_CLEAR_PRESET_BEHAVIOR_IN_UNMAPPER <value>
```

### Example

```
set_global_assignment -name  
synthesis_keep_synch_clear_preset_behavior_in_unmapper on  
set_instance_assignment -name  
synthesis_keep_synch_clear_preset_behavior_in_unmapper on -to foo
```



## SYNTH\_CLOCK\_MUX\_PROTECTION

Causes the multiplexers in the clock network to be decomposed to 2to1 multiplexer trees, and protected from being merged with, or transferred to, other logic. This option helps the TimeQuest timing analyzer to understand clock behavior.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name SYNTH_CLOCK_MUX_PROTECTION <value>
```

**Default Value**

On

**Example**

```
set_global_assignment -name synth_clock_mux_protection off
```



## SYNTH\_GATED\_CLOCK\_CONVERSION

Automatically converts gated clocks in the design to use clock enable pins if clock enable pins are not used in the original design. Clock gating logic can contain AND, OR, MUX, and NOT gates. Turning on this option may increase memory use and overall run time. You must use the TimeQuest Timing Analyzer for timing analysis, and you must define all base clocks in Synopsys Design Constraints (SDC) format.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name SYNTH_GATED_CLOCK_CONVERSION -entity <entity  
name> <value>  
set_instance_assignment -name SYNTH_GATED_CLOCK_CONVERSION -to <to> -entity  
<entity name> <value>  
set_global_assignment -name SYNTH_GATED_CLOCK_CONVERSION <value>
```

**Default Value**

Off

**Example**

```
set_global_assignment -name synth_gated_clock_conversion on  
set_instance_assignment -name synth_gated_clock_conversion on -to foo
```

## SYNTH\_MESSAGE\_LEVEL

Specifies the type of Analysis & Synthesis messages you want to view. Setting this option to 'Low' allows you to view only the most important Analysis & Synthesis messages. Setting this option to 'Medium' allows you to view most Analysis & Synthesis messages, but hides the detailed messages in Analysis & Synthesis report. Setting this option to 'High' allows you to view all Analysis & Synthesis messages.

### Type

Enumeration

### Values

- High
- Low
- Medium

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name SYNTH_MESSAGE_LEVEL <value>
```

### Default Value

Medium

## SYNTH\_PROTECT\_SDC\_CONSTRAINT

Causes SDC constraint checking in register merging. It helps to maintain the validity of SDC constraints through compilation.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name SYNTH_PROTECT_SDC_CONSTRAINT <value>
```

### Default Value

Off



## Example

```
set_global_assignment -name synth_protect_sdc_constraint on
```

## SYNTH\_RESOURCE\_AWARE\_INFERENCE\_FOR\_BLOCK\_RAM

Specifies whether RAM, ROM, and shift-register inference should take the design and device resources into account.

### Type

Boolean

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix
- Stratix II
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name SYNTH_RESOURCE_AWARE_INFERENCE_FOR_BLOCK_RAM  
<value>
```

### Example

```
set_global_assignment -name synth_resource_aware_inference_for_block_ram on
```



## SYNTH\_TIMING\_DRIVEN\_SYNTHESIS

Allows synthesis to use timing information during synthesis to better optimize the design.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name SYNTH_TIMING_DRIVEN_SYNTHESIS <value>
set_global_assignment -name SYNTH_TIMING_DRIVEN_SYNTHESIS -entity <entity
name> <value>
set_instance_assignment -name SYNTH_TIMING_DRIVEN_SYNTHESIS -to <to> -
entity <entity name> <value>
```

### Example

```
set_global_assignment -name synth_timing_driven_synthesis on
```



## TOP\_LEVEL\_ENTITY

Specifies the full hierarchical path of the entity that is the focus of the current compilation or simulation.

### Old Name

FOCUS\_ENTITY\_NAME

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name TOP_LEVEL_ENTITY <value>
```

## TRUE\_WYSIWYG\_FLOW

Specifies that the Quartus Prime software should not try to optimize this WYSIWYG design.

### Type

Boolean

### Device Support

- Cyclone
- A
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name TRUE_WYSIWYG_FLOW <value>
```

### Default Value

Off



## USER\_LIBRARIES

Specifies the pathnames of user-defined libraries.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name USER_LIBRARIES <value>
```

## USE\_GENERATED\_PHYSICAL\_CONSTRAINTS

Specifies the physical constraints file generated by the resynthesis tool to be used by the Quartus Prime software

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name USE_GENERATED_PHYSICAL_CONSTRAINTS -section_id  
<section identifier> <value>  
set_global_assignment -name USE_GENERATED_PHYSICAL_CONSTRAINTS -entity  
<entity name> -section_id <section identifier> <value>
```

### Default Value

On, requires section identifier

## USE\_HIGH\_SPEED\_ADDER

Tells the Compiler whether to use high speed adder circuitry to implement arithmetic functions or not. This option is useful for improving the performance of the design when set to On and minimizing the total number of HCells used in the design when set to Off. This option applies to HardCopy series devices only. It can only be used as a project-wide option. This option defaults to Auto, which has the same behavior as On when the Optimization Technique is set to Speed or Balanced, and as Off when the Optimization Technique is set to Area.

### Type

Enumeration

### Values

- Auto
- Off
- On

### Device Support

- HardCopy II
- HardCopy III
- HardCopy IV

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name USE_HIGH_SPEED_ADDER <value>
set_global_assignment -name USE_HIGH_SPEED_ADDER -entity <entity name>
<value>
set_instance_assignment -name USE_HIGH_SPEED_ADDER -to <to> -entity <entity
name> <value>
```

### Default Value

Auto

### Example

```
set_global_assignment -name use_high_speed_adder off
```

## USE\_LOGICLOCK\_CONSTRAINTS\_IN\_BALANCING

Directs the compiler to use LogicLock constraints during DSP and RAM balancing.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name USE_LOGICLOCK_CONSTRAINTS_IN_BALANCING <value>
```

### Default Value

On

### Example

```
set_global_assignment -name use_logiclock_constraints_in_balancing on
```



## VERILOG\_CONSTANT\_LOOP\_LIMIT

Defines the iteration limit for Verilog loops with loop conditions that evaluate to compile-time constants on each loop iteration. This limit exists primarily to identify potential infinite loops before they exhaust memory or trap the software in an actual infinite loop.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name VERILOG_CONSTANT_LOOP_LIMIT <value>  
set_global_assignment -name VERILOG_CONSTANT_LOOP_LIMIT -entity <entity  
name> <value>  
set_instance_assignment -name VERILOG_CONSTANT_LOOP_LIMIT -to <to> -entity  
<entity name> <value>
```

### Default Value

5000

### Example

```
set_global_assignment -name verilog_constant_loop_limit 3000
```

## VERILOG\_INPUT\_VERSION

Specifies the language dialect to use when processing Verilog Design Files: Verilog-1995 (IEEE Std. 1364-1995), Verilog-2001 (IEEE Std. 1364-2001), or SystemVerilog-2005 (IEEE Std. 1800-2005). Verilog 2001 is the default dialect.

### Type

Enumeration

### Values

- SystemVerilog\_2005
- Verilog\_1995
- Verilog\_2001

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name VERILOG_INPUT_VERSION <value>
```

### Default Value

Verilog\_2001

## VERILOG\_LMF\_FILE

Specifies the default Library Mapping File (.lmf) for the current compilation.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name VERILOG_LMF_FILE <value>
```

## VERILOG\_MACRO

Defines Verilog HDL macro - same as `define directive

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name VERILOG_MACRO <value>
```



## VERILOG\_NON\_CONSTANT\_LOOP\_LIMIT

Defines the iteration limit for Verilog loops with loop conditions that do not evaluate to compile-time constants on each loop iteration. This limit exists primarily to identify potential infinite loops before they exhaust memory or trap the software in an actual infinite loop.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name VERILOG_NON_CONSTANT_LOOP_LIMIT <value>
set_global_assignment -name VERILOG_NON_CONSTANT_LOOP_LIMIT -entity <entity
name> <value>
set_instance_assignment -name VERILOG_NON_CONSTANT_LOOP_LIMIT -to <to> -
entity <entity name> <value>
```

### Default Value

250

### Example

```
set_global_assignment -name verilog_non_constant_loop_limit 3000
```

## VERILOG\_SHOW\_LMF\_MAPPING\_MESSAGES

Determines whether to display messages describing the mappings used in the Library Mapping File.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name VERILOG_SHOW_LMF_MAPPING_MESSAGES <value>
```



## VHDL\_INPUT\_LIBRARY

Specifies the logical name of a user-defined VHDL design library : physical name.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_instance_assignment -name VHDL_INPUT_LIBRARY -to <to> <value>
```

## VHDL\_INPUT\_VERSION

Specifies the language dialect to use when processing VHDL Design Files: VHDL-1987 (IEEE Std 1076-1987), VHDL-1993 (IEEE Std 1076-1993) or VHDL-2008 (IEEE Std 1076-2008). VHDL-1993 is the default dialect.

### Type

Enumeration

### Values

- VHDL\_1987
- VHDL\_1993
- VHDL\_2008

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name VHDL_INPUT_VERSION <value>
```

### Default Value

VHDL\_1993





## VHDL\_LMF\_FILE

Specifies the default Library Mapping File (.lmf) for the current compilation.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name VHDL_LMF_FILE <value>
```

## VHDL\_SHOW\_LMF\_MAPPING\_MESSAGES

Determines whether to display messages describing the mappings used in the Library Mapping File.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name VHDL_SHOW_LMF_MAPPING_MESSAGES <value>
```



## Assembler Assignments

## ARRIAIIGX\_RX\_CDR\_LOCKUP\_FIX\_OVERRIDE

Allows signaldetect to propagate from PCS to the core, which will be blocked if you fix the CDR lockup issue. This is because a PMA direct route is unavailable in Arria II GX devices.

### Type

Boolean

### Device Support

Arria II GX

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name ARRIAIIGX_RX_CDR_LOCKUP_FIX_OVERRIDE <value>  
set_instance_assignment -name ARRIAIIGX_RX_CDR_LOCKUP_FIX_OVERRIDE -to <to>  
<value>
```

### Default Value

Off

## AUTO\_INCREMENT\_CONFIG\_DEVICE\_JTAG\_USER\_CODE

Automatically increments the JTAG user code in the second and subsequent configuration devices if the target device requires multiple configuration devices.

### Old Name

AUTO\_INCREMENT\_USER\_JTAG\_CODE

### Type

Boolean

### Device Support

- Cyclone
- E
- Mercury
- Stratix
- Stratix GX

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name AUTO_INCREMENT_CONFIG_DEVICE_JTAG_USER_CODE  
<value>
```

### Default Value

On

## AUTO\_RESTART\_CONFIGURATION

Directs the device to restart the configuration process automatically if a data error is encountered. If this option is turned off, you must externally direct the device to restart the configuration process if an error occurs.

### Old Name

Auto restart on configuration error

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.



## Syntax

```
set_global_assignment -name AUTO_RESTART_CONFIGURATION <value>
```

## Default Value

On

## CLOCK\_SOURCE

Specifies whether the configuration device generates an internal clock or applies an external clock.

### Type

Enumeration

### Values

- External
- Internal

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name CLOCK_SOURCE <value>
```

### Default Value

Internal



## COMPRESSION\_MODE

Allows you to compress SRAM Object Files (.sof) stored in a Programmer Object File (.pof) for a configuration device.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name COMPRESSION_MODE <value>
```

### Default Value

Off

## CONFIGURATION\_CLOCK\_DIVISOR

Specifies the clock frequency divisor, which is used to determine the period of the system clock.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name CONFIGURATION_CLOCK_DIVISOR <value>
```

### Default Value

1

## CONFIGURATION\_CLOCK\_FREQUENCY

Specifies the clock frequency of the configuration device.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name CONFIGURATION_CLOCK_FREQUENCY <value>
```

### Default Value

10 MHz

## CYCLONEIII\_CONFIGURATION\_DEVICE

Specifies the configuration device that you want to use as the means of configuring the target device.

### Type

String

### Device Support

- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- MAX 10

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name CYCLONEIII_CONFIGURATION_DEVICE <value>
```

### Default Value

Auto

## CYCLONEII\_M4K\_COMPATIBILITY

Direct Quartus Prime software to produce programming files that are compatible with both rev A and rev B silicon. This option applies only to Cyclone II device family. Please see the Cyclone II FPGA Family Errata Sheet for more details.

### Type

Boolean

### Device Support

Cyclone II

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name CYCLONEII_M4K_COMPATIBILITY <value>
```

### Default Value

On

## CYCLONE\_CONFIGURATION\_DEVICE

Specifies the configuration device that you want to use as the means of configuring the target Cyclone device.

### Type

String

### Device Support

Cyclone

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name CYCLONE_CONFIGURATION_DEVICE <value>
```

### Default Value

Auto



## DISABLE\_NCS\_AND\_OE\_PULLUPS\_ON\_CONFIG\_DEVICE

Disables the nCS and OE internal pull-ups on the configuration device(s).

### Old Name

DISABLE\_CONF\_DONE\_AND\_NSTATUS\_PULLUPS\_ON\_CONFIG\_DEVICE

### Type

Boolean

### Device Support

- E
- Mercury
- Stratix
- Stratix GX

### Notes

This assignment is included in the Fitter report.

### Syntax

```
<value> set_global_assignment -name DISABLE_NCS_AND_OE_PULLUPS_ON_CONFIG_DEVICE
```

### Default Value

Off

## ENABLE\_ADV\_SEU\_DETECTION

Allows you to enable the Advanced SEU Detection compiler to generate design SEU sensitivity map file. If this option is turned on, the SMH file will be generated.

### Type

Boolean

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone V
- Stratix III
- Stratix IV
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_ADV_SEU_DETECTION <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name ENABLE_ADV_SEU_DETECTION ON
```

### See Also

PARTITION\_ASD\_REGION\_ID





## ENABLE\_AUTONOMOUS\_PCIE\_HIP

Directs the device to release the PCIe HIP after the periphery is configured and before core configuration is completed. This option doesn't take effect in CvP Init mode since the periphery automatically comes up first, all other modes bring the PCIe HIP up first when this option is selected.

### Old Name

Auto restart on configuration error

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name ENABLE_AUTONOMOUS_PCIE_HIP <value>
```

### Default Value

Off

## ENABLE\_LOW\_VOLTAGE\_MODE\_ON\_CONFIG\_DEVICE

Allows an EPC1 configuration device to operate in a 3.3 V environment.

### Type

Boolean

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name ENABLE_LOW_VOLTAGE_MODE_ON_CONFIG_DEVICE <value>
```

### Default Value

On



## ENABLE\_OCT\_DONE

This option controls whether the INIT\_DONE signal will be gated by OCT\_DONE signal which indicates the Power-Up OCT calibration is completed. If this option is turned off, the INIT\_DONE signal is not gated by the OCT\_DONE signal.

### Type

Boolean

### Device Support

- Arria 10
- Arria II GX
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- MAX 10
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name ENABLE_OCT_DONE <value>
```

## ENABLE\_SPI\_MODE\_CHECK

Configure device in Active Serial mode after power-up.

### Type

Boolean

### Device Support

MAX 10

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_SPI_MODE_CHECK <value>
```

### Default Value

Off

## EN\_SPI\_IO\_WEAK\_PULLUP

Set SPI IO pins to weak pull-up prior to usermode, otherwise SPI IO pins will be input tri-stated

### Type

Boolean

### Device Support

MAX 10

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EN_SPI_IO_WEAK_PULLUP <value>
```

### Default Value

On

## EN\_USER\_IO\_WEAK\_PULLUP

Set IO to weak pull-up prior to usermode, otherwise IO will be input tri-stated

### Type

Boolean

### Device Support

MAX 10

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EN_USER_IO_WEAK_PULLUP <value>
```

### Default Value

On



## EPROM\_USE\_CHECKSUM\_AS\_USERCODE

Uses the checksum value from the Programmer Object File (.pof) as the JTAG user code.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EPROM_USE_CHECKSUM_AS_USERCODE <value>
```

### Default Value

Off

## EXTERNAL\_FLASH\_FALLBACK\_ADDRESS

Specifies the fallback image location address in EPCQ configuration device when external fallback is enabled.

### Type

String

### Device Support

MAX 10

### Notes

None

### Syntax

```
set_global_assignment -name EXTERNAL_FLASH_FALLBACK_ADDRESS <value>
```

### Default Value

0

### See Also

FALLBACK\_TO\_EXTERNAL\_FLASH





## FALLBACK\_TO\_EXTERNAL\_FLASH

During power up, if the default internal configuration image is corrupted, the device will look for primary fallback image in internal flash, if it is also corrupted and if secondary fallback is been enabled, image store in external Flash will be use. This option is only valid when Internal Configuration scheme is selected and to be use with multi images.

### Type

Boolean

### Device Support

MAX 10

### Notes

None

### Syntax

```
set_global_assignment -name FALLBACK_TO_EXTERNAL_FLASH <value>
```

### Default Value

Off

## FORCE\_SSMCLK\_TO\_ISMCLK

Force SSM clock to use internal oscillator clock.

### Type

Boolean

### Device Support

MAX 10

### Notes

None

### Syntax

```
set_global_assignment -name FORCE_SSMCLK_TO_ISMCLK <value>
```

### Default Value

On



## GENERATE\_HEX\_FILE

Generates a Hexadecimal (Intel-format) Output File (.hexout) containing configuration data that can be programmed into a parallel data source, such as an EPROM or a mass storage device, which then in turn configures the target device.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name GENERATE_HEX_FILE <value>
```

### Default Value

Off

## GENERATE\_PMSF\_FILES

Generate Partial-Masked SOF file (.pmsf) containing both configuration data and region definitions that can be used to re-configure a device region. If this option is turned on, the Partial-Masked SOF files (.pmsf) will be generated instead of Mask Settings files (.msf).

### Type

Boolean

### Device Support

- Arria 10

### Syntax

```
set_global_assignment -name GENERATE_PMSF_FILES <value>
```

### Default Value

On

### Example

```
set_global_assignment -name GENERATE_PMSF_FILES ON
```

### See Also

GENERATE\_PMSF\_FILES

## GENERATE\_RBF\_FILE

Generates a Raw Binary File (.rbf) containing configuration data that an intelligent external controller can use to configure the target device.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name GENERATE_RBF_FILE <value>
```

### Default Value

Off

## GENERATE\_TTF\_FILE

Generates a Tabular Text File (.tff) containing configuration data that an intelligent external controller can use to configure the target device.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name GENERATE_TTF_FILE <value>
```

### Default Value

Off

## HARDCOPYII\_POWER\_ON\_EXTRA\_DELAY

Directs HardCopy chip to wait before INIT\_DONE pin goes high and before the chip is in user mode.

### Type

Enumeration

### Values

- Off
- Wait 1 ms
- Wait 2 ms
- Wait 4 ms
- Wait 50 ms
- Wait 8 ms

### Device Support

- HardCopy II
- HardCopy III
- HardCopy IV

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name HARDCOPYII_POWER_ON_EXTRA_DELAY <value>
```

### Default Value

Off

## HEXOUT\_FILE\_COUNT\_DIRECTION

Specifies the count direction for the data in a Hexadecimal (Intel-Format) Output File (.hexout) as up or down.

### Old Name

HEX\_FILE\_COUNT\_UP\_DOWN

### Type

Enumeration

### Values

- Down
- Up

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name HEXOUT_FILE_COUNT_DIRECTION <value>
```

### Default Value

Up



## HEXOUT\_FILE\_START\_ADDRESS

Specifies the starting memory address for a Hexadecimal (Intel-Format) Output File (.hexout).

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name HEXOUT_FILE_START_ADDRESS <value>
```

### Default Value

0

## MAX7000S\_JTAG\_USER\_CODE

Specifies user-defined information about the target device. The JTAG user code is an extension of the option register. This data can be read with the JTAG USERCODE instruction.

### Type

String

### Device Support

- MAX7000A
- MAX7000S

### Notes

None

### Syntax

```
set_global_assignment -name MAX7000S_JTAG_USER_CODE <value>
```

### Default Value

FFFF

## MAX7000\_JTAG\_USER\_CODE

Specifies user-defined information about the target device. The JTAG user code is an extension of the option register. This data can be read with the JTAG USERCODE instruction.

### Type

String

### Device Support

- MAX3000A
- MAX7000AE
- MAX7000B

### Notes

None

### Syntax

```
set_global_assignment -name MAX7000_JTAG_USER_CODE <value>
```

### Default Value

FFFFFFFF

## MAX7000\_USE\_CHECKSUM\_AS\_USERCODE

Sets the JTAG user code to match the checksum value of the device programming file. The programming file is a Programmer Object File (.pof) for non-volatile devices, such as MAX II devices, or an SRAM Object File (.sof) for SRAM-based devices. If you turn this option on, the JTAG user code option is not available.

### Type

Boolean

### Device Support

- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name MAX7000_USE_CHECKSUM_AS_USERCODE <value>
```

### Default Value

Off

## MERCURY\_CONFIGURATION\_DEVICE

Specifies the configuration device that you want to use as the means of configuring the target Mercury device.

### Old Name

CONFIGURATION\_DEVICE\_DALI

### Type

String

### Device Support

Mercury

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name MERCURY_CONFIGURATION_DEVICE <value>
```

### Default Value

Auto

## MERCURY\_CONFIG\_DEVICE\_JTAG\_USER\_CODE

Specifies user-defined information about the configuration device. The JTAG user code is an extension of the option register. This data can be read with the JTAG USERCODE instruction.

### Old Name

CONFIG\_DEVICE\_JTAG\_USER\_CODE\_DALI

### Type

String

### Device Support

Mercury

### Notes

None

### Syntax

```
set_global_assignment -name MERCURY_CONFIG_DEVICE_JTAG_USER_CODE <value>
```

### Default Value

FFFFFFFF

## MERCURY\_JTAG\_USER\_CODE

Specifies user-defined information about the target device. The JTAG user code is an extension of the option register. This data can be read with the JTAG USERCODE instruction.

### Old Name

JTAG\_USER\_CODE\_DALI

### Type

String

### Device Support

Mercury

### Notes

None

### Syntax

```
set_global_assignment -name MERCURY_JTAG_USER_CODE <value>
```

### Default Value

FFFFFFFF

## ON\_CHIP\_BITSTREAM\_DECOMPRESSION

Allows the device to accept and decompress bitstreams during configuration. Produces compressed bitstreams and enables bitstream decompression.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name ON_CHIP_BITSTREAM_DECOMPRESSION <value>
```

### Default Value

On



## POF\_VERIFY\_PROTECT

Protect configuration data in internal flash from being read through JTAG

### Type

Boolean

### Device Support

MAX 10

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POF_VERIFY_PROTECT <value>
```

### Default Value

Off

## POR\_SCHEME

Specifies device Power On Reset (POR) scheme.

### Type

Enumeration

### Values

- Fast POR delay
- Instant ON
- Slow POR delay

### Device Support

MAX 10

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POR_SCHEME <value>
```

### Default Value

Instant ON



## PR\_BASE\_MSF

Specify block name and path of base revision MSF file for mask comparison in a PR project.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name PR_BASE_MSF <value>
```

## PR\_BASE\_SOF

Specify path of base revision SOF file for bit settings comparison in a PR project.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name PR_BASE_SOF <value>
```



## PR\_SKIP\_BASE\_CHECK

Disable mask comparison and logic verification for a reconfigurable partition in a PR project.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name PR_SKIP_BASE_CHECK <value>
```

## PWRMGT\_VOLTAGE\_OUTPUT\_FORMAT

Specifies the output format when operation mode is PMBus master.

### Type

Enumeration

### Values

- Auto discovery
- Direct format
- Linear format

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT <value>
```

### Default Value

Auto discovery

## RELEASE\_CLEARS\_BEFORE\_TRI\_STATES

Directs the device to release the clear signal on registered logic cells and I/O cells before releasing the output enable override on tri-state buffers. If this option is turned off, the output enable signals are released before the clear overrides are released.

### Old Name

Release clears before tri-states

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name RELEASE_CLEARS_BEFORE_TRI_STATES <value>
```

## Default Value

Off



## RESERVE\_ALL\_UNUSED\_PINS\_NO\_OUTPUT\_GND

Reserves all unused pins on the target device in one of three states: as inputs that are tri-stated, or as outputs that drive an unspecified signal.

### Old Name

RESERVED\_ALL\_UNUSED\_PINS\_NO\_OUTPUT\_GND

### Type

Enumeration

### Values

- As input tri-stated
- As output driving an unspecified signal

### Device Support

- MAX3000A
- MAX7000A
- MAX7000S

### Notes

None

### Syntax

```
set_global_assignment -name RESERVE_ALL_UNUSED_PINS_NO_OUTPUT_GND <value>
```

### Default Value

As output driving an unspecified signal

## SECURITY\_BIT

Enables the security bit support, which prevents a device from being examined and reprogrammed.

### Type

Boolean

### Device Support

- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name SECURITY_BIT <value>
```

### Default Value

Off

## STRATIXII\_CONFIGURATION\_DEVICE

Specifies the configuration device that you want to use as the means of configuring the target device.

### Old Name

STRATIX\_II\_CONFIGURATION\_DEVICE

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone V
- HardCopy III
- HardCopy IV
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name STRATIXII_CONFIGURATION_DEVICE <value>
```

### Default Value

Auto

## STRATIXII\_MRAM\_COMPATIBILITY

Direct Quartus Prime software to produce programming files that are compatible with both rev A and rev B silicon. This option applies only to EP2S30, EP2S90, EP2S130, EP2S180. Please see the Stratix II Errata Sheet for more details.

### Old Name

STRATIXII\_SILICON\_VERSION

### Type

Boolean

### Device Support

Stratix II

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name STRATIXII_MRAM_COMPATIBILITY <value>
```

### Default Value

Off



## STRATIX\_CONFIGURATION\_DEVICE

Specifies the configuration device that you want to use as the means of configuring the target device.

### Old Name

YEAGER\_CONFIGURATION\_DEVICE

### Type

String

### Device Support

- Cyclone II
- MAX II
- MAX V
- Stratix
- Stratix GX

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name STRATIX_CONFIGURATION_DEVICE <value>
```

### Default Value

Auto

## STRATIX\_CONFIG\_DEVICE\_JTAG\_USER\_CODE

Specifies user-defined information about the configuration device. The JTAG user code is an extension of the option register. This data can be read with the JTAG USERCODE instruction.

### Type

String

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name STRATIX_CONFIG_DEVICE_JTAG_USER_CODE <value>
```

### Default Value

FFFFFFFF

## STRATIX\_JTAG\_USER\_CODE

Specifies user-defined information about the target device. The JTAG user code is an extension of the option register. This data can be read with the JTAG USERCODE instruction.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name STRATIX_JTAG_USER_CODE <value>
```

**Default Value**

FFFFFFFF





## USE\_CHECKERED\_PATTERN\_AS\_UNINITIALIZED\_RAM\_CONTENT

Loads a checkered pattern as initial RAM content into all RAM blocks without specified RAM content that supports content initialization. Turning on this option does not affect simulation, which may cause on-chip behavior to differ from simulation results.

### Type

Enumeration

### Values

- 0000
- 0101
- 1010
- 1111
- OFF
- ON
- RANDOM

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone V
- Stratix
- Stratix II
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name USE_CHECKERED_PATTERN_AS_UNINITIALIZED_RAM_CONTENT <value>
```

### Default Value

OFF

## USE\_CHECKSUM\_AS\_USERCODE

Sets the JTAG user code to match the checksum value of the device programming file. The programming file is a Programmer Object File (.pof) for non-volatile devices, such as MAX II devices, or an SRAM Object File (.sof) for SRAM-based devices. If you turn this option on, the JTAG user code option is not available.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- E
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name USE_CHECKSUM_AS_USERCODE <value>
```

Default Value

On

## USE\_CONFIGURATION\_DEVICE

Specifies that you intend to use a configuration device(s) such as the EPC2 as the means of configuring the target device. This option directs the Compiler to create a Programmer Output File (.pof) for programming the configuration device. If multiple configuration devices are needed, one POF is created for each device, with names of the following format: name.pof, name\_1.pof, name\_2.pof, etc.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- EPC1
- EPC2
- Enhanced Configuration Devices
- A
- B
- E
- FLEX8000
- Flash Memory
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- MAX9000
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

- Stratix III
- Stratix IV
- Virtual JTAG TAP

## Notes

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name USE_CONFIGURATION_DEVICE <value>
```

## Assignment Group Assignments

### ASSIGNMENT\_GROUP\_EXCEPTION

Defines a node(s) to be excluded as an exception to a previously added member. It can be an instance name or a wildcard representing multiple instance names

#### Type

String

#### Device Support

This setting can be used in projects targeting any Altera device family.

#### Notes

The value of this assignment is case sensitive.

#### Syntax

```
set_global_assignment -name ASSIGNMENT_GROUP_EXCEPTION -section_id <section  
identifier> <value>
```



## ASSIGNMENT\_GROUP\_MEMBER

Defines an element of a group. It can be an instance name or a wildcard representing multiple instance names

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name ASSIGNMENT_GROUP_MEMBER -section_id <section  
identifier> <value>
```

## Classic Timing Assignments

### ANALYZE\_LATCHES\_AS\_SYNCHRONOUS\_ELEMENTS

Directs the Timing Analyzer to analyze latches as synchronous elements, rather than as combinational elements. Although latches continue to be implemented as a LUT feeding back onto itself, turning on this option directs the Timing Analyzer to analyze all latches as synchronous elements. Specifically, the clock enable is analyzed as an inverted clock. The Timing Analyzer reports the results of setup and hold analysis on these latches

#### Type

Boolean

#### Device Support

This setting can be used in projects targeting any Altera device family.

#### Notes

None

#### Syntax

```
set_global_assignment -name ANALYZE_LATCHES_AS_SYNCHRONOUS_ELEMENTS <value>
```

#### Default Value

On





## CUT\_OFF\_IO\_PIN\_FEEDBACK

Cuts off feedback from I/O pins during timing analysis. Cutting off I/O pin feedback is especially useful when a bidirectional pin is connected directly or indirectly to both the input and the output of a latch. This type of feedback path is continuous because it is not interrupted by any clocked logic primitives.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name CUT_OFF_IO_PIN_FEEDBACK <value>
```

### Default Value

On

## CUT\_OFF\_PATHS\_BETWEEN\_CLOCK\_DOMAINS

Cuts the paths between registers clocked by unrelated clocks. This option makes the timing analysis reporting similar to MAX+PLUS II timing analysis reporting.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name CUT_OFF_PATHS_BETWEEN_CLOCK_DOMAINS <value>
```

### Default Value

On

## CUT\_OFF\_READ\_DURING\_WRITE\_PATHS

Cuts the path from the write enable register through the ESB to a destination register.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name CUT_OFF_READ_DURING_WRITE_PATHS <value>
```

### Default Value

On

## DEFAULT\_HOLD\_MULTICYCLE

Determines the default hold multicycle. The 'Same as Multicycle' setting ensures that the signal is latched on the final edge only. The 'One' setting assumes that the design can latch on any edge, up to and including the final edge. The 'Same as Multicycle' setting will give fewer hold time violation warnings. The 'One' setting is more restrictive, but it is the default setting for the TimeQuest Timing Analyzer and other third-party timing analyzers. This setting can be overridden on specific nodes with the Hold Multicycle option.

### Type

Enumeration

### Values

- One
- Same as Multicycle

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name DEFAULT_HOLD_MULTICYCLE <value>
```

### Default Value

Same as Multicycle

### Example

```
set_global_assignment -name default_hold_multicycle "Same as Multicycle"  
set_global_assignment -name default_hold_multicycle "One"
```

### See Also

MULTICYCLE, SRC\_MULTICYCLE, HOLD\_MULTICYCLE, SRC\_HOLD\_MULTICYCLE, SETUP\_RELATIONSHIP, HOLD\_RELATIONSHIP

## DO\_COMBINED\_ANALYSIS

Analyze both the fast corner (min delays) and the slow corner (max delays) and to report the results from each analysis.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name DO_COMBINED_ANALYSIS <value>
```

### Default Value

Off

## EMIF\_SOC\_PHYCLK\_ADVANCE\_MODELING

Instructs routing annotation to adjust the AV-SoC Phyclk delays.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EMIF_SOC_PHYCLK_ADVANCE_MODELING <value>
```

### Default Value

Off

## ENABLE\_HPS\_INTERNAL\_TIMING

Enable HPS Internal Timing Characteristics

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name ENABLE_HPS_INTERNAL_TIMING <value>
```

### Default Value

Off

## INPUT\_TRANSITION\_TIME

Specifies the input transition time. This assignment is used in Quartus to adjust the timing of the I/O buffers for all families that support AIOT. It is also used when generating the PrimeTime script that it is used by the HardCopy back end. This assignment gets converted as a set\_input\_transition SDC command. If the assignment does not exist, Quartus will generate a set\_input\_transition using 80% of  $VCCN * 1V/ns$  where VCCN depends on the I/O Standard used

### Type

Time

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix
- Stratix II
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports wildcards.

This assignment is copied to any duplicated nodes.

### Syntax

```
set_instance_assignment -name INPUT_TRANSITION_TIME -to <to> -entity  
<entity name> <value>
```



## LVDS\_FIXED\_CLOCK\_DATA\_PHASE

Specifies exact skew compensation. When the fixed clock-to-data skew is known, clock data synchronization (CDS) can be pre-programmed into the device during configuration. If CDS is pre-programmed into the device, training patterns do not need to be transmitted to the receiver channels. The resolution of each pre-programmed setting is 25% of the data period, to compensate for skew up to 50% of the data period. This option is applied only to input pins that drive the rx\_in[] port of the altlvds\_rx megafunction. This option is available for APEX II devices only.

### Type

Enumeration

### Values

- Default
- Negative 180
- Negative 90
- Positive 180
- Positive 90
- Zero

### Notes

None

### Syntax

```
set_instance_assignment -name LVDS_FIXED_CLOCK_DATA_PHASE -to <to> -entity  
<entity name> <value>
```

## MAX\_CORE\_JUNCTION\_TEMP

This is the maximum core junction temperature that will be encountered during operation. Specified in degrees Celsius

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name MAX_CORE_JUNCTION_TEMP <value>
```

## MIN\_CORE\_JUNCTION\_TEMP

This is the minimum core junction temperature that will be encountered during operation. Specified in degrees Celsius

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name MIN_CORE_JUNCTION_TEMP <value>
```

## NOMINAL\_CORE\_SUPPLY\_VOLTAGE

Specifies the voltage for the core power supply. For Stratix III devices, the core supply voltage applies only to the VCCL power rail. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix III
- Stratix IV
- Stratix V

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name NOMINAL_CORE_SUPPLY_VOLTAGE <value>
```



## PACKAGE\_SKEW\_COMPENSATION

Indicates that that the package skew for the signal has been compensated by the board trace delays.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name PACKAGE_SKEW_COMPENSATION -to <to> -entity  
<entity name> <value>
```

## PLL\_EXTERNAL\_FEEDBACK\_BOARD\_DELAY

Specifies an external board delay between a feedback output pin and a feedback input pin (fbin) for a PLL in external feedback mode. This option is ignored if it is assigned to anything other than the fbin pin of a PLL.

### Type

Time

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

None

### Syntax

```
set_instance_assignment -name PLL_EXTERNAL_FEEDBACK_BOARD_DELAY -to <to> -  
entity <entity name> <value>  
set_global_assignment -name PLL_EXTERNAL_FEEDBACK_BOARD_DELAY <value>
```

## TDC\_AGGRESSIVE\_HOLD\_CLOSURE\_EFFORT

Instructs the Fitter to aggressively optimize for hold timing closure.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name TDC_AGGRESSIVE_HOLD_CLOSURE_EFFORT <value>
```

### Default Value

Off

## TIMEQUEST\_DO\_CCPP\_REMOVAL

Directs the TimeQuest Timing Analyzer to remove common clock path pessimism (CCPP) during slack computation.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- EPC1
- EPC2
- Enhanced Configuration Devices
- A
- B
- E
- FLEX8000
- Flash Memory
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- MAX9000
- Mercury
- Stratix
- Stratix GX
- Stratix II



- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V
- Virtual JTAG TAP

## Notes

None

## Syntax

```
set_global_assignment -name TIMEQUEST_DO_CCPP_REMOVAL <value>
```

## TIMEQUEST\_DO\_REPORT\_TIMING

Directs the TimeQuest Timing Analyzer to report the worst-case path per clock domain and analysis.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name TIMEQUEST_DO_REPORT_TIMING <value>
```

### Default Value

Off

## TIMEQUEST\_MULTICORNER\_ANALYSIS

Directs the TimeQuest Timing Analyzer to perform multicorner timing analysis, which analyzes the design against best-case and worst-case operating conditions. Turning on this option does not enable multicorner analysis in the Fitter. To optimize fast-corner timing, see the Fitter Settings page of the Settings dialog box.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- EPC1
- EPC2
- Enhanced Configuration Devices
- A
- B
- E
- FLEX8000
- Flash Memory
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- MAX9000
- Mercury
- Stratix

- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V
- Virtual JTAG TAP

## Notes

None

## Syntax

```
set_global_assignment -name TIMEQUEST_MULTICORNER_ANALYSIS <value>
```



## TIMEQUEST\_REPORT\_NUM\_WORST\_CASE\_TIMING\_PATHS

Specifies the maximum number of worst-case timing paths for the TimeQuest Timing Analyzer to report per clock domain and analysis.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### INTEGER\_RANGE

1, 100000

### Notes

None

### Syntax

```
set_global_assignment -name TIMEQUEST_REPORT_NUM_WORST_CASE_TIMING_PATHS  
<value>
```

### Default Value

100

## TIMEQUEST\_REPORT\_SCRIPT

Specifies the name of the tcl script that will be used to overwrite the default TimeQuest report panels created during a normal compile.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name TIMEQUEST_REPORT_SCRIPT <value>
```



## TIMEQUEST\_REPORT\_SCRIPT\_INCLUDE\_DEFAULT\_ANALYSIS

Directs the TimeQuest Timing Analyzer to perform default timing analysis prior to running the user-specified report script specified by TIMEQUEST\_REPORT\_SCRIPT.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name  
TIMEQUEST_REPORT_SCRIPT_INCLUDE_DEFAULT_ANALYSIS <value>
```

### Default Value

On

## TIMEQUEST\_REPORT\_WORST\_CASE\_TIMING\_PATHS

Directs the TimeQuest Timing Analyzer to report worst-case timing paths per clock domain and analysis.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- EPC1
- EPC2
- Enhanced Configuration Devices
- A
- B
- E
- FLEX8000
- Flash Memory
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- MAX9000
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX





- Stratix III
- Stratix IV
- Stratix V
- Virtual JTAG TAP

## Notes

None

## Syntax

```
set_global_assignment -name TIMEQUEST_REPORT_WORST_CASE_TIMING_PATHS <value>
```

## USE\_DLL\_FREQUENCY\_FOR\_DQS\_DELAY\_CHAIN

Instructs STA to take DLL frequency into account while calculating phase shift of DQS delay chain

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name USE_DLL_FREQUENCY_FOR_DQS_DELAY_CHAIN <value>
```

### Default Value

Off

# Compiler Assignments

## ALLOW\_REGISTER\_DUPLICATION

Controls whether the Compiler is allowed to duplicate registers to improve design performance. When register duplication is allowed, the Compiler may perform optimizations that create a second copy of a register and move a portion of its fan-out to this new node, in order to improve routability and/or reduce the total routing wire required to route a net with many fan-outs. If register duplication is disabled, optimizations that retime registers will also be disabled. This setting affects Analysis & Synthesis and the Fitter.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name ALLOW_REGISTER_DUPLICATION <value>
```

### Default Value

On

### Example

```
set_global_assignment -name allow_register_duplication on
```

## ALLOW\_REGISTER\_MERGING

Controls whether the Compiler is allowed to remove registers that are identical to other registers in the design. When register merging is allowed, in cases where two registers generate the same logic, one may be deleted and the remaining one will be made to also fan-out to the deleted register's destinations. This option is useful if you wish to prevent the Compiler from removing duplicate registers that you have used deliberately.

If register merging is disabled, optimizations that retime registers will also be disabled.

This setting affects Analysis & Synthesis and the Fitter.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V



**Notes**

This assignment is included in the Fitter report.

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name ALLOW_REGISTER_MERGING <value>
```

**Default Value**

On

**Example**

```
set_global_assignment -name allow_register_merging off
```

## OPTIMIZATION\_MODE

Controls the Compiler's high-level optimization strategy. By default, the Quartus Prime Compiler optimizes in a balanced mode, targeting the design's timing constraints. The alternate modes cause the Compiler to prioritize a particular optimization metric. High effort modes primarily enable additional optimizations that increase compilation time. Aggressive modes may increase compilation time and also make trade-offs that may harm the other optimization metrics (performance, area, etc.).

'High Performance Effort' mode will cause the compiler to target increased positive timing margin (via Standard Fit compilation), increase the timing optimization effort applied during placement and routing, and enable timing-related Physical Synthesis optimizations (as allowed by the register optimization settings below). Each of these additional optimizations can increase compilation time. 'Aggressive Performance' mode enables the same optimizations as 'High Performance Effort' mode, and additionally enables options during Analysis & Synthesis to maximize design performance at a potential increase to logic area. If design utilization is already very high, this option may lead to difficulty in fitting which could also negatively affect overall optimization quality.

'High Power Effort' mode guides the Compiler to spend additional compilation time reducing routing utilization, which saves dynamic power. In 'Aggressive Power' mode, the Compiler will further target reducing the routing usage of signals with the highest specified (via Signal Activity File) or estimated toggle rates, saving additional dynamic power but potentially affecting performance.

'Aggressive Area' mode instructs the Compiler to target an area minimal solution, even if this reduces overall timing performance.

This setting affects Analysis & Synthesis and the Fitter.

### Type

Enumeration

### Values

- Aggressive Area
- Aggressive Performance
- Aggressive Power
- Balanced
- High Performance Effort
- High Power Effort

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name OPTIMIZATION_MODE <value>
```

**Default Value**

Balanced





## TIMEQUEST\_SPECTRA\_Q

Controls when the Compiler will use TimeQuest Spectra-Q as its timing analysis engine. This setting is not configurable in Quartus Prime Pro Edition, where TimeQuest Spectra-Q is always used.

### Old Name

TIMEQUEST2

### Type

Enumeration

### Values

- FITTER\_ONLY
- OFF
- ON
- SIGNOFF\_ONLY

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

- Stratix III
- Stratix IV
- Stratix V

## Notes

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name TIMEQUEST_SPECTRA_Q <value>
```

## Example

```
set_global_assignment -name TIMEQUEST_SPECTRA_Q ON
```

# Design Assistant Assignments

## ACLK\_CAT

Direct Design Assistant to detect asynchronous clock domains on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name ACLK_CAT <value>
```

## ACLK\_RULE\_IMSZER\_ADOMAIN

Direct Design Assistant to detect improper synchronizer which moves data across asynchronous domain boundaries on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name ACLK_RULE_IMSZER_ADOMAIN <value>
```

## ACLK\_RULE\_NO\_SZER\_ACLK\_DOMAIN

Direct Design Assistant to detect synchronizer between asynchronous clock domains on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name ACLK_RULE_NO_SZER_ACLK_DOMAIN <value>
```

## ACLK\_RULE\_SZER\_BTW\_ACLK\_DOMAIN

Direct Design Assistant to detect synchronizer for every signal between asynchronous clock domains on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name ACLK_RULE_SZER_BTW_ACLK_DOMAIN <value>
```

## CLK\_CAT

Direct Design Assistant to check all clock-related violations on the design. Expand the items to turn off the rule checking if irrelevant.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name CLK_CAT <value>
```

## CLK\_RULE\_CLKNET\_CLKSPINES

Direct Design Assistant to check clock net not mapped to clock spines used on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name CLK_RULE_CLKNET_CLKSPINES <value>
```



## CLK\_RULE\_CLKNET\_CLKSPINES\_THRESHOLD

Specifies the threshold value for clock net not mapped to clock spines rule.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name CLK_RULE_CLKNET_CLKSPINES_THRESHOLD <value>
```

### Default Value

25

## CLK\_RULE\_COMB\_CLOCK

Direct Design Assistant to check combinatorial logic output used as on-chip clock on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name CLK_RULE_COMB_CLOCK <value>
```



## CLK\_RULE\_GATED\_CLK\_FANOUT

Direct Design Assistant to check gated clock have feed to certain number of clock port to effectively save power.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name CLK_RULE_GATED_CLK_FANOUT <value>
```

## CLK\_RULE\_INPINS\_CLKNET

Direct Design Assistant to check illegal input pins connected to clock net used on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name CLK_RULE_INPINS_CLKNET <value>
```



## CLK\_RULE\_INV\_CLOCK

Direct Design Assistant to check inverted clock used on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name CLK_RULE_INV_CLOCK <value>
```

## CLK\_RULE\_MIX\_EDGES

Direct Design Assistant to check mixed-clock edges used on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name CLK_RULE_MIX_EDGES <value>
```

## DA\_CUSTOM\_RULE\_FILE

Used to set the path for DA custom rule file

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name DA_CUSTOM_RULE_FILE <value>
```

## DISABLE\_DA\_GX\_RULE

Prevents Design Assistant from running when the Fitter is running.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

### Syntax

```
set_global_assignment -name DISABLE_DA_GX_RULE <value>  
set_instance_assignment -name DISABLE_DA_GX_RULE -to <to> -entity <entity  
name> <value>
```



## DISABLE\_DA\_RULE

Suppress design assistant rule locally or turn off design assistant rule globally for general user

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports wildcards.

This assignment is copied to any duplicated nodes.

### Syntax

```
set_global_assignment -name DISABLE_DA_RULE <value>  
set_instance_assignment -name DISABLE_DA_RULE -to <to> -entity <entity  
name> <value>
```

## DRC\_DEADLOCK\_STATE\_LIMIT

Specifies the maximum number of states that you want the Design Assistant to detect as a deadlock condition. A larger number will results in longer processing time.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name DRC_DEADLOCK_STATE_LIMIT <value>
```

### Default Value

2

## DRC\_DETAIL\_MESSAGE\_LIMIT

Specifies the maximum number of detail messages that you want the Design Assistant to report.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name DRC_DETAIL_MESSAGE_LIMIT <value>
```

### Default Value

10

## DRC\_FANOUT\_EXCEEDING

Specifies the minimum amount of fan-out that a node must have to be reported by the Design Assistant.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name DRC_FANOUT_EXCEEDING <value>
```

### Default Value

30



## DRC\_GATED\_CLOCK\_FEED

Specifies the minimum amount of clock port a gated clock must feed so that it's an acceptable gated clock.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name DRC_GATED_CLOCK_FEED <value>
```

### Default Value

30

## DRC\_REPORT\_FANOUT\_EXCEEDING

Directs the Design Assistant to report all nodes with more than the specified amount of fan-out.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name DRC_REPORT_FANOUT_EXCEEDING <value>
```



## DRC\_REPORT\_TOP\_FANOUT

Directs the Design Assistant to report the specified number of nodes with the highest fan-out.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name DRC_REPORT_TOP_FANOUT <value>
```

## DRC\_TOP\_FANOUT

Specifies the number of nodes with the highest fan-out that you want the Design Assistant to report.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name DRC_TOP_FANOUT <value>
```

### Default Value

50



## DRC\_VIOLATION\_MESSAGE\_LIMIT

Specifies the maximum number of violation messages that you want the Design Assistant to report.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name DRC_VIOLATION_MESSAGE_LIMIT <value>
```

### Default Value

30

## ENABLE\_DA\_RULE

Desuppress design assistant rule locally or turn on design assistant rule globally for general user

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports wildcards.

This assignment is copied to any duplicated nodes.

### Syntax

```
set_global_assignment -name ENABLE_DA_RULE <value>  
set_instance_assignment -name ENABLE_DA_RULE -to <to> -entity <entity name>  
<value>
```

## ENABLE\_DRC\_SETTINGS

Directs the Design Assistant to run during a compilation based on user settings.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_DRC_SETTINGS <value>
```

### Default Value

Off

## FSM\_CAT

Direct Design Assistant to detect finite state machine rules on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name FSM_CAT <value>
```



## FSM\_RULE\_DEADLOCK\_STATE

Direct Design Assistant to detect deadlock state in state machine on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name FSM_RULE_DEADLOCK_STATE <value>
```

## FSM\_RULE\_NO\_RESET\_STATE

Direct Design Assistant to detect if reset state is specified for state machine on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name FSM_RULE_NO_RESET_STATE <value>
```

## FSM\_RULE\_NO\_SZER\_ACLK\_DOMAIN

Direct Design Assistant to detect synchronizer between asynchronous clock domains feeding to state machine on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name FSM_RULE_NO_SZER_ACLK_DOMAIN <value>
```

## FSM\_RULE\_UNREACHABLE\_STATE

Direct Design Assistant to detect unreachable state in state machine on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name FSM_RULE_UNREACHABLE_STATE <value>
```



## FSM\_RULE\_UNUSED\_TRANSITION

Direct Design Assistant to detect unused transition in state machine on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name FSM_RULE_UNUSED_TRANSITION <value>
```

## HARDCOPY\_FLOW\_AUTOMATION

Specifies which HardCopy flow will be run in HardCopy timing wizard

### Type

Enumeration

### Values

- COMPILE\_NEW\_PROJECT
- FULL\_COMPILATION
- MIGRATION\_ONLY

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name HARDCOPY_FLOW_AUTOMATION <value>
```

### Default Value

MIGRATION\_ONLY

## HARDCOPY\_NEW\_PROJECT\_PATH

Specifies the directory path for the new/migrated HardCopy project.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name HARDCOPY_NEW_PROJECT_PATH <value>
```

## HCPY\_CAT

Direct Design Assistant to detect HardCopy rules on the design. All HardCopy rules apply to HardCopy devices only.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name HCPY_CAT <value>
```

## HCPY\_PLL\_MULTIPLE\_CLK\_NETWORK\_TYPES

Direct Design Assistant to detect PLL that feeds multiple clock network types.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name HCPY_PLL_MULTIPLE_CLK_NETWORK_TYPES <value>
```

## HCPY\_VREF\_PINS

Direct Design Assistant to detect VREF pins on the design. This rule applies to HardCopy devices only.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name HCPY_VREF_PINS <value>
```



## NONSYNCHSTRUCT\_CAT

Direct Design Assistant to check for non-synchronous design structures on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name NONSYNCHSTRUCT_CAT <value>
```

## NONSYNCHSTRUCT\_RULE\_ASYN\_RAM

Directs the Design Assistant to detect asynchronous memories targeted by the design. This rule applies to HardCopy devices only.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name NONSYNCHSTRUCT_RULE_ASYN_RAM <value>
```



## NONSYNCHSTRUCT\_RULE\_COMBLOOP

Direct Design Assistant to check for combinatorial loop with unidentified function on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name NONSYNCHSTRUCT_RULE_COMBLOOP <value>
```

## NONSYNCHSTRUCT\_RULE\_COMB\_DRIVES\_RAM\_WE

Direct Design Assistant to detect combinatorial logic driving asynchronous RAM Write Enable signals on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name NONSYNCHSTRUCT_RULE_COMB_DRIVES_RAM_WE <value>
```

## NONSYNCHSTRUCT\_RULE\_DELAY\_CHAIN

Direct Design Assistant to check for delay chain with unidentified function on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name NONSYNCHSTRUCT_RULE_DELAY_CHAIN <value>
```

## NONSYNCHSTRUCT\_RULE\_ILLEGAL\_PULSE\_GEN

Direct Design Assistant to check illegal pulse generator on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name NONSYNCHSTRUCT_RULE_ILLEGAL_PULSE_GEN <value>
```

## NONSYNCHSTRUCT\_RULE\_LATCH\_UNIDENTIFIED

Direct Design Assistant to detect latch of unidentified type on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name NONSYNCHSTRUCT_RULE_LATCH_UNIDENTIFIED <value>
```

## NONSYNCHSTRUCT\_RULE\_MULTI\_VIBRATOR

Direct Design Assistant to check multi-vibrator on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name NONSYNCHSTRUCT_RULE_MULTI_VIBRATOR <value>
```



## NONSYNCHSTRUCT\_RULE\_REG\_LOOP

Direct Design Assistant to check for combinatorial loop with output of register feeding its own control signal on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name NONSYNCHSTRUCT_RULE_REG_LOOP <value>
```

## NONSYNCHSTRUCT\_RULE\_RIPPLE\_CLK

Direct Design Assistant to check ripple clock structure on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name NONSYNCHSTRUCT_RULE_RIPPLE_CLK <value>
```





## NONSYNCHSTRUCT\_RULE\_SRLATCH

Direct Design Assistant to detect SR-latch on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name NONSYNCHSTRUCT_RULE_SRLATCH <value>
```

## RESET\_CAT

Direct Design Assistant to check reset-related violations on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name RESET_CAT <value>
```



## RESET\_RULE\_COMB\_ASYNC\_RESET

Direct Design Assistant to check combinatorial logic output used as on-chip asynchronous reset on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name RESET_RULE_COMB_ASYNC_RESET <value>
```

## RESET\_RULE\_IMSYNCH\_ASYNCH\_DOMAIN

Direct Design Assistant to check for reset which is improperly synchronized in receiving asynchronous domain on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name RESET_RULE_IMSYNCH_ASYNCH_DOMAIN <value>
```

## RESET\_RULE\_IMSYNCH\_EXRESET

Direct Design Assistant to check improper synchronization of external reset on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name RESET_RULE_IMSYNCH_EXRESET <value>
```

## RESET\_RULE\_UNSYNCH\_ASYNCH\_DOMAIN

Direct Design Assistant to check for reset which is not synchronized in receiving asynchronous domain on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name RESET_RULE_UNSYNCH_ASYNCH_DOMAIN <value>
```

## RESET\_RULE\_UNSYNCH\_EXRESET

Suppress unsynchronized external reset rule.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name RESET_RULE_UNSYNCH_EXRESET <value>
```

## SIGNALRACE\_CAT

Direct Design Assistant to check signal race on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name SIGNALRACE_CAT <value>
```





## SIGNALRACE\_RULE\_CLK\_PORT\_RACE

Direct Design Assistant to check race condition between clock port and any other port of the same register.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name SIGNALRACE_RULE_CLK_PORT_RACE <value>
```

## SIGNALRACE\_RULE\_RESET\_RACE

Direct Design Assistant to detect synchronous port and asynchronous port of same register driven by same signal source

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name SIGNALRACE_RULE_RESET_RACE <value>
```

## SIGNALRACE\_RULE\_SECOND\_SIGNAL\_RACE

Direct Design Assistant to detect more than one secondary signal of same register driven by same signal source

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name SIGNALRACE_RULE_SECOND_SIGNAL_RACE <value>
```

## SIGNALRACE\_RULE\_TRISTATE

Direct Design Assistant to detect Tri-state signal race condition

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name SIGNALRACE_RULE_TRISTATE <value>
```

## TIMING\_CAT

Direct Design Assistant to check timing closure related violations on the design.

### Type

Boolean

### Device Support

- Cyclone
- E
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name TIMING_CAT <value>
```

## EDA Netlist Writer Assignments

### EDA\_BOARD\_BOUNDARY\_SCAN\_OPERATION

Specify the BSDL file operation either for pre-configuration or post-configuration

#### Type

Enumeration

#### Values

- POST\_CONFIG
- PRE\_CONFIG

#### Device Support

This setting can be used in projects targeting any Altera device family.

#### Syntax

```
set_global_assignment -name EDA_BOARD_BOUNDARY_SCAN_OPERATION -section_id  
<section identifier> <value>
```

#### Default Value

PRE\_CONFIG, requires section identifier

## EDA\_BOARD\_DESIGN\_BOUNDARY\_SCAN\_TOOL

Specifies the boundary scan format used for board level boundary scan testing.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_BOARD_DESIGN_BOUNDARY_SCAN_TOOL <value>  
set_global_assignment -name EDA_BOARD_DESIGN_BOUNDARY_SCAN_TOOL -entity  
<entity name> <value>
```

### Default Value

<None>

## EDA\_BOARD\_DESIGN\_SIGNAL\_INTEGRITY\_TOOL

Specifies the EDA third-party tool used for board level signal integrity analysis.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_BOARD_DESIGN_SIGNAL_INTEGRITY_TOOL <value>  
set_global_assignment -name EDA_BOARD_DESIGN_SIGNAL_INTEGRITY_TOOL -entity  
<entity name> <value>
```

### Default Value

<None>





## EDA\_BOARD\_DESIGN\_SYMBOL\_TOOL

Specifies the EDA third-party tool used for board level schematic design.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_BOARD_DESIGN_SYMBOL_TOOL <value>  
set_global_assignment -name EDA_BOARD_DESIGN_SYMBOL_TOOL -entity <entity  
name> <value>
```

### Default Value

<None>

## EDA\_BOARD\_DESIGN\_TIMING\_TOOL

Specifies the EDA third-party tool used for board level timing analysis.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_BOARD_DESIGN_TIMING_TOOL <value>  
set_global_assignment -name EDA_BOARD_DESIGN_TIMING_TOOL -entity <entity  
name> <value>
```

### Default Value

<None>

## EDA\_BOARD\_DESIGN\_TOOL

Specifies the EDA third-party tool used for board level design and analysis.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_BOARD_DESIGN_TOOL <value>  
set_global_assignment -name EDA_BOARD_DESIGN_TOOL -entity <entity name>  
<value>
```

### Default Value

<None>

## EDA\_DESIGN\_EXTRA\_ALTERA\_SIM\_LIB

Specify additional ALTERA simulation model libraries required is used by the design files

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_DESIGN_EXTRA_ALTERA_SIM_LIB -section_id  
<section identifier> <value>
```

## EDA\_DESIGN\_INSTANCE\_NAME

Specify the instance name of the design in the test bench

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_DESIGN_INSTANCE_NAME -section_id <section  
identifier> <value>
```

## EDA\_ENABLE\_GLITCH\_FILTERING

Write logic to filter glitches in the simulation netlist.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_ENABLE_GLITCH_FILTERING -section_id  
<section identifier> <value>  
set_global_assignment -name EDA_ENABLE_GLITCH_FILTERING -entity <entity  
name> -section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier

## EDA\_ENABLE\_IPUTF\_MODE

Allows you to simulate designs containing hw.tcl based IP cores. This may require adding .sip files to your Quartus Prime project. This variable may be removed in future releases.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_ENABLE_IPUTF_MODE -section_id <section  
identifier> <value>  
set_global_assignment -name EDA_ENABLE_IPUTF_MODE -entity <entity name> -  
section_id <section identifier> <value>
```

### Default Value

On, requires section identifier

## EDA\_EXTRA\_ELAB\_OPTION

Additional custom simulation elaboration options for one or more simulators.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_EXTRA_ELAB_OPTION -section_id <section  
identifier> <value>  
set_global_assignment -name EDA_EXTRA_ELAB_OPTION -entity <entity name> -  
section_id <section identifier> <value>
```

### Default Value

"" , requires section identifier



## EDA\_FLATTEN\_BUSES

Flattens all buses when creating the VHDL Output File (.vho). You should turn on this option if your third-party EDA environment does not support buses.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_FLATTEN_BUSES -section_id <section  
identifier> <value>  
set_global_assignment -name EDA_FLATTEN_BUSES -entity <entity name> -  
section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier

## EDA\_FORMAL\_VERIFICATION\_ALLOW\_RETIMING

Allow register retiming to be turned on for formal verification

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EDA_FORMAL_VERIFICATION_ALLOW_RETIMING -  
section_id <section identifier> <value>  
set_global_assignment -name EDA_FORMAL_VERIFICATION_ALLOW_RETIMING -entity  
<entity name> -section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier

## EDA\_FORMAL\_VERIFICATION\_TOOL

Specifies the EDA third-party tool used for formal verification.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_FORMAL_VERIFICATION_TOOL <value>  
set_global_assignment -name EDA_FORMAL_VERIFICATION_TOOL -entity <entity  
name> <value>
```

### Default Value

<None>

## EDA\_FV\_HIERARCHY

Determines how the hierarchy of design entities is to be processed during compilation. 'BLACKBOX' setting causes the entity to be handled as a black-box in the EDA flow. 'NONE' setting is the default and means no special handling to be done. The option applies only to the design entity to which it is assigned; lower-level entities do not inherit their parent entity's setting for this option.

### Type

Enumeration

### Values

- BLACKBOX
- Off

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EDA_FV_HIERARCHY -entity <entity name> <value>  
set_instance_assignment -name EDA_FV_HIERARCHY -to <to> -entity <entity  
name> <value>
```

## EDA\_GENERATE\_FUNCTIONAL\_NETLIST

Generate Verilog/VHDL netlist for functional or timing simulation with EDA simulation tools. When this option is 'On', the EDA Netlist Writer does not generate a Standard Delay Format Output File (.sdo). If the device does not support timing simulation, then only the functional-simulation netlist is available.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_GENERATE_FUNCTIONAL_NETLIST -section_id  
<section identifier> <value>  
set_global_assignment -name EDA_GENERATE_FUNCTIONAL_NETLIST -entity <entity  
name> -section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier

## EDA\_GENERATE\_GATE\_LEVEL\_SIMULATION\_COMMAND\_SCRIPT

Directs the EDA Netlist Writer to generate a command script to run gate-level simulation with a third-party EDA tool.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

### Syntax

```
set_global_assignment -name  
EDA_GENERATE_GATE_LEVEL_SIMULATION_COMMAND_SCRIPT -section_id <section identifier>  
<value>  
set_global_assignment -name  
EDA_GENERATE_GATE_LEVEL_SIMULATION_COMMAND_SCRIPT -entity <entity name> -section_id  
<section identifier> <value>
```

### Default Value

Off, requires section identifier

## EDA\_GENERATE\_POWER\_INPUT\_FILE

Generates a Power Input File (.pwf) to perform power analysis in the Quartus Prime software when using third-party simulation tools.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_GENERATE_POWER_INPUT_FILE -section_id  
<section identifier> <value>  
set_global_assignment -name EDA_GENERATE_POWER_INPUT_FILE -entity <entity  
name> -section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier

## EDA\_GENERATE\_RTL\_SIMULATION\_COMMAND\_SCRIPT

Directs the EDA Netlist Writer to generate a command script to run RTL functional simulation with a third-party EDA tool.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

### Syntax

```
set_global_assignment -name EDA_GENERATE_RTL_SIMULATION_COMMAND_SCRIPT -  
section_id <section identifier> <value>  
set_global_assignment -name EDA_GENERATE_RTL_SIMULATION_COMMAND_SCRIPT -  
entity <entity name> -section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier





## EDA\_GENERATE\_TIMING\_CLOSURE\_DATA

Generates back-annotation data for performing in-place optimization with the LeonardoSpectrum software.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_GENERATE_TIMING_CLOSURE_DATA -section_id  
<section identifier> <value>  
set_global_assignment -name EDA_GENERATE_TIMING_CLOSURE_DATA -entity  
<entity name> -section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier

## EDA\_IBIS\_EXTENDED\_MODEL\_SELECTOR

Enable or disable information about related IO Standards in the model selector section of IBIS files. Will turn on EDA\_IBIS\_MODEL\_SELECTOR when set to true.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EDA_IBIS_EXTENDED_MODEL_SELECTOR -section_id  
<section identifier> <value>  
set_global_assignment -name EDA_IBIS_EXTENDED_MODEL_SELECTOR -entity  
<entity name> -section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier

## EDA\_IBIS\_MODEL\_SELECTOR

Enable or disable model selector feature for IBIS Writer

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EDA_IBIS_MODEL_SELECTOR -section_id <section  
identifier> <value>  
set_global_assignment -name EDA_IBIS_MODEL_SELECTOR -entity <entity name> -  
section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier

## EDA\_IBIS\_MUTUAL\_COUPLING

Allows you to print the per pin RLC package model with mutual coupling when generating IBIS Output Files (.ibs) with the EDA Netlist Writer. The lumped RLC package model information appears in the IBIS Output File.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EDA_IBIS_MUTUAL_COUPLING -section_id <section  
identifier> <value>  
set_global_assignment -name EDA_IBIS_MUTUAL_COUPLING -entity <entity name> -  
section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier

## EDA\_IBIS\_SPECIFICATION\_VERSION

Specifies the IBIS Specification version.

### Type

Enumeration

### Values

- 4p2
- 5p0

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Syntax

```
set_global_assignment -name EDA_IBIS_SPECIFICATION_VERSION -section_id  
<section identifier> <value>
```

### Default Value

4p2, requires section identifier

## EDA\_IPFS\_FILE

Specifies the library to which IPFS file should be compiled

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
<value> set_global_assignment -name EDA_IPFS_FILE -section_id <section identifier>
```



## EDA\_LAUNCH\_CMD\_LINE\_TOOL

Allows you to launch third-party EDA tools in the command-line mode rather than opening the graphical user interface.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_LAUNCH_CMD_LINE_TOOL -section_id <section
identifier> <value>
set_global_assignment -name EDA_LAUNCH_CMD_LINE_TOOL -entity <entity name> -
section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier

## EDA\_MAINTAIN\_DESIGN\_HIERARCHY

Maintain the original user design hierarchy when generating Verilog or VHDL simulation netlist for the project.

### Type

Enumeration

### Values

- OFF
- ON
- PARTITION\_ONLY

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_MAINTAIN_DESIGN_HIERARCHY -section_id  
<section identifier> <value>  
set_global_assignment -name EDA_MAINTAIN_DESIGN_HIERARCHY -entity <entity  
name> -section_id <section identifier> <value>
```

### Default Value

OFF, requires section identifier



## EDA\_MAP\_ILLEGAL\_CHARACTERS

Maps the vertical bar (|), tilde (~), and colon (:) characters in Quartus Prime hierarchical node names to the legal Verilog HDL characters z, x, and underscore (\_), respectively, in Verilog Output Files. Turning on this option also maps other illegal non-alphanumeric characters, including brackets [], parentheses (), angle brackets <>, and braces {} to underscores (\_).

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_MAP_ILLEGAL_CHARACTERS -section_id <section  
identifier> <value>  
set_global_assignment -name EDA_MAP_ILLEGAL_CHARACTERS -entity <entity  
name> -section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier

## EDA\_NATIVELINK\_GENERATE\_SCRIPT\_ONLY

Allows you to generate the script for a third-party EDA tool without running the EDA tool.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name EDA_NATIVELINK_GENERATE_SCRIPT_ONLY -section_id  
<section identifier> <value>
```

### Default Value

Off, requires section identifier



## EDA\_NATIVELINK\_PORTABLE\_FILE\_PATHS

Specifies that the file paths in the generated third-party EDA tool command scripts should be written out using relative paths for design and testbench files, and by using a variable to refer to Quartus Prime simulation library path.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_NATIVELINK_PORTABLE_FILE_PATHS -section_id  
<section identifier> <value>  
set_global_assignment -name EDA_NATIVELINK_PORTABLE_FILE_PATHS -entity  
<entity name> -section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier

## EDA\_NATIVELINK\_SIMULATION\_SETUP\_SCRIPT

Specify the script for EDA Tool. After compiling models, design files and test bench files, Native Link uses this script to set up the simulation

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_NATIVELINK_SIMULATION_SETUP_SCRIPT -  
section_id <section identifier> <value>
```

## EDA\_NATIVELINK\_SIMULATION\_TEST\_BENCH

Specify the active logical name of the test bench, that will be used to perform NativeLink Simulation

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_NATIVELINK_SIMULATION_TEST_BENCH -  
section_id <section identifier> <value>
```

## EDA\_NETLIST\_WRITER\_OUTPUT\_DIR

Specify the output directory for EDA Netlist Writer

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_NETLIST_WRITER_OUTPUT_DIR -section_id  
<section identifier> <value>
```



## EDA\_RESYNTHESIS\_TOOL

Specifies the EDA tool used for resynthesis.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_RESYNTHESIS_TOOL <value>  
set_global_assignment -name EDA_RESYNTHESIS_TOOL -entity <entity name>  
<value>
```

### Default Value

<None>

## EDA\_RTL\_SIMULATION\_RUN\_SCRIPT

Specifies the script file for performing RTL simulation using third-party simulation software.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_RTL_SIMULATION_RUN_SCRIPT -section_id  
<section identifier> <value>  
set_global_assignment -name EDA_RTL_SIMULATION_RUN_SCRIPT -entity <entity  
name> -section_id <section identifier> <value>
```



## EDA\_RTL\_SIM\_MODE

Enables the Advanced Options - VHDL or Verilog Simulation options for Test Bench mode or Command/macro mode.

### Type

Enumeration

### Values

- COMMAND\_MACRO\_MODE
- NOT\_USED
- TEST\_BENCH\_MODE

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EDA_RTL_SIM_MODE -section_id <section  
identifier> <value>  
set_global_assignment -name EDA_RTL_SIM_MODE -entity <entity name> -  
section_id <section identifier> <value>
```

### Default Value

NOT\_USED, requires section identifier

## EDA\_RTL\_TEST\_BENCH\_FILE\_NAME

Specifies the RTL simulation test bench file name for Test Bench Mode. File type can be a VHDL Test Bench File (.vht), VHDL File (.vhd), Verilog HDL Test Bench File (.vt), or Verilog HDL file (.v).

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_RTL_TEST_BENCH_FILE_NAME -section_id  
<section identifier> <value>  
set_global_assignment -name EDA_RTL_TEST_BENCH_FILE_NAME -entity <entity  
name> -section_id <section identifier> <value>
```



## EDA\_RTL\_TEST\_BENCH\_NAME

Specifies the name of top-level test bench in RTL simulation test bench file.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_RTL_TEST_BENCH_NAME -section_id <section  
identifier> <value>  
set_global_assignment -name EDA_RTL_TEST_BENCH_NAME -entity <entity name> -  
section_id <section identifier> <value>
```

## EDA\_RTL\_TEST\_BENCH\_RUN\_FOR

Specifies the time duration for RTL simulation using third-party simulation.

### Type

Time

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EDA_RTL_TEST_BENCH_RUN_FOR -section_id <section  
identifier> <value>  
set_global_assignment -name EDA_RTL_TEST_BENCH_RUN_FOR -entity <entity  
name> -section_id <section identifier> <value>
```

## EDA\_SDC\_FILE\_NAME

Name of Design Constraints file to be sourced in scripts generated for third party tools

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_SDC_FILE_NAME -section_id <section  
identifier> <value>  
set_global_assignment -name EDA_SDC_FILE_NAME -entity <entity name> -  
section_id <section identifier> <value>
```

## EDA\_SETUP\_HOLD\_DETECTION\_INPUT\_REGISTERS\_BIDIR\_PINS\_DISABLED

Disables setup and hold time violations detection in input registers of bi-directional pins. This setting has no effect when 'Generate functional simulation netlist' is 'On'.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name  
EDA_SETUP_HOLD_DETECTION_INPUT_REGISTERS_BIDIR_PINS_DISABLED -section_id <section  
identifier> <value>
```

### Default Value

Off, requires section identifier



## EDA\_SIMULATION\_RUN\_SCRIPT

Specifies the script file for running a third-party simulation in Command/macro mode.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_SIMULATION_RUN_SCRIPT -section_id <section  
identifier> <value>  
set_global_assignment -name EDA_SIMULATION_RUN_SCRIPT -entity <entity name>  
-section_id <section identifier> <value>
```

## EDA\_SIMULATION\_TOOL

Specifies the third-party EDA tool used for simulation.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_SIMULATION_TOOL <value>  
set_global_assignment -name EDA_SIMULATION_TOOL -entity <entity name>  
<value>
```

### Default Value

<None>



## EDA\_SIMULATION\_VCD\_OUTPUT\_SIGNALS\_TO\_TCL\_FILE

Specifies which type of output signals should be written out to the TCL file which can be used in a third-party EDA simulation tool to generate a VCD file. Writing out all output signals to the TCL file may result in a very large VCD file being generated by the third-party simulation tool.

### Type

Enumeration

### Values

- All
- All Except Combinational Logic Element Outputs

### Device Support

- Arria GX
- Cyclone
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name EDA_SIMULATION_VCD_OUTPUT_SIGNALS_TO_TCL_FILE -  
section_id <section identifier> <value>
```

### Default Value

All Except Combinational Logic Element Outputs, requires section identifier

## EDA\_SIMULATION\_VCD\_OUTPUT\_TCL\_FILE

Specifies whether or not a TCL file should be written out which can be used in a third-party EDA simulation tool to generate a VCD file.

### Type

Boolean

### Device Support

- Arria GX
- Cyclone
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name EDA_SIMULATION_VCD_OUTPUT_TCL_FILE -section_id  
<section identifier> <value>
```

### Default Value

Off, requires section identifier

## EDA\_SIMULATION\_VCD\_OUTPUT\_TCL\_FILE\_NAME

Specifies the name the TCL file should be written to which can be used in a third-party EDA simulation tool to generate a VCD file.

### Type

File name

### Device Support

- Arria GX
- Cyclone
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_SIMULATION_VCD_OUTPUT_TCL_FILE_NAME -  
section_id <section identifier> <value>
```

## EDA\_TEST\_BENCH\_DESIGN\_INSTANCE\_NAME

Specifies the instance name of the design entity in the test bench file.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_TEST_BENCH_DESIGN_INSTANCE_NAME -section_id  
<section identifier> <value>  
set_global_assignment -name EDA_TEST_BENCH_DESIGN_INSTANCE_NAME -entity  
<entity name> -section_id <section identifier> <value>
```



## EDA\_TEST\_BENCH\_ENABLE\_STATUS

Enables the Advanced Options - VHDL or Verilog Simulation options for Test Bench mode or Command/macro mode.

### Type

Enumeration

### Values

- COMMAND\_MACRO\_MODE
- NOT\_USED
- TEST\_BENCH\_MODE

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EDA_TEST_BENCH_ENABLE_STATUS -section_id  
<section identifier> <value>  
set_global_assignment -name EDA_TEST_BENCH_ENABLE_STATUS -entity <entity  
name> -section_id <section identifier> <value>
```

### Default Value

NOT\_USED, requires section identifier

## EDA\_TEST\_BENCH\_ENTITY\_MODULE\_NAME

Specifies the top-level design entity in the test bench file.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_TEST_BENCH_ENTITY_MODULE_NAME -section_id  
<section identifier> <value>  
set_global_assignment -name EDA_TEST_BENCH_ENTITY_MODULE_NAME -entity  
<entity name> -section_id <section identifier> <value>
```

## EDA\_TEST\_BENCH\_EXTRA\_ALTERA\_SIM\_LIB

Tells NativeLink to add extra simulation libraries to the specified module. This is required by the memory controllers (both new and legacy).

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_TEST_BENCH_EXTRA_ALTERA_SIM_LIB -section_id  
<section identifier> <value>
```

## EDA\_TEST\_BENCH\_FILE

Associates a test bench file with the logical test bench name

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_TEST_BENCH_FILE -section_id <section  
identifier> <value>
```





## EDA\_TEST\_BENCH\_FILE\_NAME

Specifies the test bench file name for Test Bench Mode. File type can be a VHDL Test Bench File (.vht), Verilog HDL Test Bench File (.vt), or another design file type.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_TEST_BENCH_FILE_NAME -section_id <section  
identifier> <value>  
set_global_assignment -name EDA_TEST_BENCH_FILE_NAME -entity <entity name> -  
section_id <section identifier> <value>
```

## EDA\_TEST\_BENCH\_GATE\_LEVEL\_NETLIST\_LIBRARY

Specify the simulation library to which Gate Level Netlist will be compiled

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_TEST_BENCH_GATE_LEVEL_NETLIST_LIBRARY -  
section_id <section identifier> <value>
```



## EDA\_TEST\_BENCH\_MODULE\_NAME

Associates a test bench file with the logical test bench name

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_TEST_BENCH_MODULE_NAME -section_id <section  
identifier> <value>
```

## EDA\_TEST\_BENCH\_NAME

Define a logical name for test bench. Each test bench logical name has associated section, containing test bench information, and section\_id being the logical test bench name.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_TEST_BENCH_NAME -section_id <section  
identifier> <value>
```

## EDA\_TEST\_BENCH\_RUN\_FOR

Specifies the simulation run time for a third-party simulation in Test Bench Mode.

### Type

Time

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EDA_TEST_BENCH_RUN_FOR -section_id <section  
identifier> <value>  
set_global_assignment -name EDA_TEST_BENCH_RUN_FOR -entity <entity name> -  
section_id <section identifier> <value>
```

## EDA\_TEST\_BENCH\_RUN\_SIM\_FOR

Specify the time interval for running EDA Simulation

### Type

Time

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EDA_TEST_BENCH_RUN_SIM_FOR -section_id <section  
identifier> <value>
```



## EDA\_TIME\_SCALE

Specifies the time unit used to represent timing delays in each Verilog Output File. The value for the Time Scale option may be between 0.001 ns and 10ns, and should be a multiple of 10.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_TIME_SCALE -section_id <section identifier>  
<value>  
set_global_assignment -name EDA_TIME_SCALE -entity <entity name> -  
section_id <section identifier> <value>
```

## EDA\_TIMING\_ANALYSIS\_TOOL

Specifies the EDA third-party tool used for timing analysis.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_TIMING_ANALYSIS_TOOL <value>  
set_global_assignment -name EDA_TIMING_ANALYSIS_TOOL -entity <entity name>  
<value>
```

### Default Value

<None>



## EDA\_TRUNCATE\_LONG\_HIERARCHY\_PATHS

Truncate hierarchical node names to 80 characters.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_TRUNCATE_LONG_HIERARCHY_PATHS -section_id  
<section identifier> <value>  
set_global_assignment -name EDA_TRUNCATE_LONG_HIERARCHY_PATHS -entity  
<entity name> -section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier

## EDA\_USER\_COMPILED\_SIMULATION\_LIBRARY\_DIRECTORY

Specify the directory where you store the library generated with the EDA Simulation Library Compiler tool. Note: Do not use this option to specify the directory for ModelSim-Altera precompiled libraries or Active-HDL precompiled libraries.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_USER_COMPILED_SIMULATION_LIBRARY_DIRECTORY -  
section_id <section identifier> <value>
```

### Default Value

<None>, requires section identifier



## EDA\_VHDL\_ARCH\_NAME

Specify the name of Architecture in the generated VHDL simulation netlist.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_VHDL_ARCH_NAME -section_id <section  
identifier> <value>
```

### Default Value

structure, requires section identifier

## EDA\_WAIT\_FOR\_GUI\_TOOL\_COMPLETION

Specifies that NativeLink should wait for the EDA tool GUI launched by it to finish.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EDA_WAIT_FOR_GUI_TOOL_COMPLETION -section_id  
<section identifier> <value>
```

### Default Value

Off, requires section identifier

## EDA\_WRITER\_DONT\_WRITE\_TOP\_ENTITY

Do not write top-level entity in VHDL Output File (.vho).

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_WRITER_DONT_WRITE_TOP_ENTITY -section_id  
<section identifier> <value>
```

### Default Value

Off, requires section identifier

## EDA\_WRITE\_DEVICE\_CONTROL\_PORTS

Add the devpor, devclrn, and devoe signals in the design as input ports in the top-level design hierarchy in the Verilog or VHDL simulation netlist for the project.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_WRITE_DEVICE_CONTROL_PORTS -section_id  
<section identifier> <value>  
set_global_assignment -name EDA_WRITE_DEVICE_CONTROL_PORTS -entity <entity  
name> -section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier

## EDA\_WRITE\_NODES\_FOR\_POWER\_ESTIMATION

Write script for Simulation tool to generate VCD file for outputs for power estimation.

### Type

Enumeration

### Values

- ALL\_NODES
- NO\_COMBINATIONAL\_OUTPUT
- Off

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name EDA_WRITE_NODES_FOR_POWER_ESTIMATION -  
section_id <section identifier> <value>  
set_global_assignment -name EDA_WRITE_NODES_FOR_POWER_ESTIMATION -entity  
<entity name> -section_id <section identifier> <value>
```

### Default Value

OFF, requires section identifier

## Equivalence Checker Assignments

### EQC\_AUTO\_BREAK\_CONE

Enable EQC for auto cone break when compare is abort.

#### Type

Boolean

#### Device Support

This setting can be used in projects targeting any Altera device family.

#### Syntax

```
set_global_assignment -name EQC_AUTO_BREAK_CONE <value>
```

#### Default Value

On



## EQC\_AUTO\_COMP\_LOOP\_CUT

Enable EQC for auto cut comp loop.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_AUTO_COMP_LOOP_CUT <value>
```

### Default Value

On

## EQC\_AUTO\_INVERSION

Enable EQC for auto check inversion level.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_AUTO_INVERSION <value>
```

### Default Value

On



## EQC\_AUTO\_PORTSWAP

Enable EQC auto swap the port.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_AUTO_PORTSWAP <value>
```

### Default Value

On

## EQC\_AUTO\_TERMINATE

Enable auto terminates when conclusion(not equivalent or undecided) is met.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_AUTO_TERMINATE <value>
```

### Default Value

On

## EQC\_BBOX\_MERGE

Enable EQC automatic merge black box.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_BBOX_MERGE <value>
```

### Default Value

On

## EQC\_CONSTANT\_DFF\_DETECTION

Enable EQC automatic constant DFF detection

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_CONSTANT_DFF_DETECTION <value>
```

### Default Value

On

## EQC\_DETECT\_DONT\_CARES

Enable EQC detect don't cares.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_DETECT_DONT_CARES <value>
```

### Default Value

On

## EQC\_DFF\_SS\_EMULATION

Enable EQC DFF secondary signal emulation.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_DFF_SS_EMULATION <value>
```

### Default Value

On



## EQC\_DUPLICATE\_DFF\_DETECTION

Enable EQC automatic duplicate DFF detection

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_DUPLICATE_DFF_DETECTION <value>
```

### Default Value

On

## EQC\_LVDS\_MERGE

Enable EQC automatic merge LVDS.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_LVDS_MERGE <value>
```

### Default Value

On



## EQC\_MAC\_REGISTER\_UNPACK

Enable EQC for auto unpack MAC register.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_MAC_REGISTER_UNPACK <value>
```

### Default Value

On

## EQC\_PARAMETER\_CHECK

Enable EQC check parameter.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_PARAMETER_CHECK <value>
```

### Default Value

On



## EQC\_POWER\_UP\_COMPARE

Enable EQC for comparing on the power-up level .

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_POWER_UP_COMPARE <value>
```

### Default Value

Off

## EQC\_RAM\_REGISTER\_UNPACK

Enable EQC for auto unpack RAM register.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_RAM_REGISTER_UNPACK <value>
```

### Default Value

On

## EQC\_RAM\_UNMERGING

Enable EQC automatic unmerge RAM.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_RAM_UNMERGING <value>
```

### Default Value

On

## EQC\_RENAMING\_RULES

Enable EQC use renaming rules.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_RENAMING_RULES <value>
```

### Default Value

On



## EQC\_RENAMING\_RULES\_LIST

Store eqc renaming rules

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EQC_RENAMING_RULES_LIST <value>
```

## EQC\_SET\_PARTITION\_BB\_TO\_VCC\_GND

Enable EQC for set partition Black-box unconnected input to VCC or GND.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_SET_PARTITION_BB_TO_VCC_GND <value>
```

### Default Value

On



## EQC\_SHOW\_ALL\_MAPPED\_POINTS

Enable EQC show all mapped points.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_SHOW_ALL_MAPPED_POINTS <value>
```

### Default Value

Off

## EQC\_STRUCTURE\_MATCHING

Enable EQC for map using structure matching.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_STRUCTURE_MATCHING <value>
```

### Default Value

On



## EQC\_SUB\_CONE\_REPORT

Enable EQC show sub cone report.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name EQC_SUB_CONE_REPORT <value>
```

### Default Value

Off

## Fitter Assignments

### ACTIVE\_SERIAL\_CLOCK

Specifies the clock source for Fast Active Serial programming. In 14nm family, maximum frequency is within +/-15% range of specified if internal oscillator is used.

#### Type

Enumeration

#### Values

- AS\_FREQ\_100MHZ
- AS\_FREQ\_25MHZ
- AS\_FREQ\_50MHZ
- CLKUSR
- FREQ\_100MHz
- FREQ\_12\_5MHz
- FREQ\_20MHz
- FREQ\_25MHz
- FREQ\_40MHz
- FREQ\_50MHz

#### Device Support

- Altera® Arria® 10
- Arria II GX
- Arria V
- Arria V GZ
- Cyclone IV GX
- Cyclone V
- Stratix V

#### Notes

This assignment is included in the Fitter report.

#### Syntax

```
set_global_assignment -name ACTIVE_SERIAL_CLOCK <value>
```

#### Example

```
set_global_assignment -name active_serial_clock "CLKUSR"
```

## See Also

USER\_START\_UP\_CLOCK



## ADCE\_ENABLED

To disable ADCE on a PMA direct channel for RX PMA. Setting this option to Off will disable ADCE. Setting this option to Auto will leave the ADCE setting unchanged. The default value is Auto.

### Type

Enumeration

### Values

- Auto
- Off

### Device Support

- Arria II GZ
- HardCopy IV
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name ADCE_ENABLED <value>  
set_instance_assignment -name ADCE_ENABLED -to <to> <value>
```

### Default Value

Auto



## ADVANCED\_PHYSICAL\_OPTIMIZATION

Enable Advanced Physical Optimization to improve the quality of results with more consistent timing closure.

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name ADVANCED_PHYSICAL_OPTIMIZATION <value>
```

## ALLOW\_LVTTL\_LVCMOS\_INPUT\_LEVELS\_TO\_OVERDRIVE\_INPUT\_BUFFER

Specifies whether the Fitter allows input pins with LVTTL or LVCMOS I/O standards to be placed inside an I/O bank with a lower VCCIO voltage than the voltage specified by the pins. Overdriving the I/O bank results in higher leakage current, which can cause the design to not function as intended.

### Type

Boolean

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name  
ALLOW_LVTTL_LVCMOS_INPUT_LEVELS_TO_OVERDRIVE_INPUT_BUFFER <value>
```

### Default Value

Off



## ALM\_REGISTER\_PACKING\_EFFORT

This guides how aggressively the Fitter will pack ALMs when trying to place registers into desired LAB locations. Specifically, this option can be used to increase the usage of secondary register locations during placement. Increasing ALM packing density may lower the number of ALMs needed to fit the design but it may also reduce routing flexibility and timing performance. It should also be noted that this setting is used as a hint for the Fitter only. Low - The Fitter will avoid ALM packing configurations that combine LUTs and registers which have no direct connectivity. Avoiding these configurations may improve timing performance but will increase the number of ALMs used to implement the design. Medium - The Fitter allows some configurations that combine unconnected LUTs and registers to be implemented in ALM locations. The Fitter will make more usage of secondary register locations within the ALM.> High - The Fitter enables all legal and desired ALM packing configurations. In dense designs, the Fitter will automatically increase the ALM register packing effort as required to enable the design to fit.

### Type

Enumeration

### Values

- High
- Low
- Medium

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name ALM_REGISTER_PACKING_EFFORT <value>
```

### Default Value

Medium



## ALWAYS\_ENABLE\_INPUT\_BUFFERS

Enables input buffers on all I/O pins including output pins. This option is required for the SAMPLE/PRELOAD JTAG instruction to function correctly on output pins. Turning on this option consumes more power.

### Type

Boolean

### Device Support

- Arria GX
- Cyclone II
- HardCopy II
- MAX II
- MAX V
- Stratix II
- Stratix II GX

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name ALWAYS_ENABLE_INPUT_BUFFERS <value>
```

### Default Value

Off



## ASYNC\_PIPELINE\_DISABLE\_DESTINATION\_CHECK

Allows the Automatic Asynchronous Signal Pipelining algorithm to run on the specified asynchronous signal even if it feeds synchronous inputs. However, turning this option ON can change circuit functionality. This option is intended for advanced users

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

### Syntax

```
set_global_assignment -name ASYNC_PIPELINE_DISABLE_DESTINATION_CHECK -  
entity <entity name> <value>  
set_instance_assignment -name ASYNC_PIPELINE_DISABLE_DESTINATION_CHECK -to  
<to> -entity <entity name> <value>
```

## ASYNC\_PIPELINE\_REG\_REACH

Specify the maximum number of LABs that the asynchronous signal sourcing at the To register can go across before a new pipeline register is inserted. This requirement might not be met for all pipeline stages, when, due to congestion or over-filled LABs, the register cannot be placed at the desired location

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

### Syntax

```
set_global_assignment -name ASYNC_PIPELINE_REG_REACH -entity <entity name>  
<value>  
set_instance_assignment -name ASYNC_PIPELINE_REG_REACH -to <to> -entity  
<entity name> <value>
```

## AUTO\_C3\_M9K\_BIT\_SKIP

Directs the fitter to skip certain bitlines in Cyclone III (including LS) M9K blocks that may be susceptible to read bit error when used in affected modes. 'Standard' setting will reserve the necessary M9K bitlines to ensure correct operation for all devices within the selected temperature range. 'Auto' setting applies the necessary bitline reservation to additional modes (x16/x18) to provide extra margin. 'Maximum' setting applies the most conservative bitline reservation required for Industrial temperature ranges regardless of the targeted device settings. Enabling any of these options can increase the number of M9K blocks required to implement the design. This global setting can be overridden for each memory instance in the Assignment Editor to customize the solution. Certain RAM modes may not be supported for Commercial temperature range devices when the 'Standard' or 'Auto' setting is applied. The fitter will issue an error for these cases. Those RAM cells can be implemented by making an instance assignment with the 'Maximum' setting, in which case additional M9K blocks may be used. Refer to the Cyclone III M9K Errata documentation for more details.

### Type

Enumeration

### Values

- Auto
- MAXIMUM
- Off
- Standard

### Device Support

- Cyclone III
- Cyclone III LS

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name AUTO_C3_M9K_BIT_SKIP <value>
```

### Default Value

Off

## AUTO\_DELAY\_CHAINS

Allows the Fitter to choose the optimal delay chain to meet tsu and tco timing requirements for all I/O elements. Turning on this option may reduce the number of tsu violations while introducing a minimal number of th violations. Turning on this option does not override delay chain settings on individual nodes.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name AUTO_DELAY_CHAINS <value>
```



## AUTO\_DELAY\_CHAINS\_FOR\_HIGH\_FANOUT\_INPUT\_PINS

Allows the Fitter to choose how to optimize the delay chains for high fanout input pins. You must enable the Auto Delay Chains option for this option to work. Enabling this option may reduce the number of tsu violation, but the compile time increases significantly, as the Fitter tries to optimize the settings for all fanouts.

### Type

Enumeration

### Values

- Off
- On

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

## Syntax

```
<value> set_global_assignment -name AUTO_DELAY_CHAINS_FOR_HIGH_FANOUT_INPUT_PINS
```

## Default Value

OFF

## AUTO\_GLOBAL\_CLOCK

Allows the Compiler to choose the signal that feeds the most clock inputs to flipflops as a global clock signal that is made available throughout the device on the global routing paths. If you want to prevent the Compiler from automatically selecting a particular signal as global clock, set the Global Signal option to 'Off' on that signal.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- EPC1
- EPC2
- Enhanced Configuration Devices
- A
- B
- E
- FLEX8000
- Flash Memory
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX9000
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III

- Stratix IV
- Stratix V
- Virtual JTAG TAP

## Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name AUTO_GLOBAL_CLOCK <value>
set_global_assignment -name AUTO_GLOBAL_CLOCK -entity <entity name> <value>
set_instance_assignment -name AUTO_GLOBAL_CLOCK -to <to> -entity <entity
name> <value>
```

## Default Value

On

## AUTO\_GLOBAL\_MEMORY\_CONTROLS

Allows the Compiler to choose the signals that feed the most write enable and read enable inputs to memories as global write enable and read enable signals that are made available throughout the device on the global routing paths. If you want to prevent the Compiler from automatically selecting a particular signal as global memory control signal, set the Global Signal option to 'Off' on that signal.

### Type

Boolean

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- Cyclone III LS
- A
- E
- HardCopy II
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name AUTO_GLOBAL_MEMORY_CONTROLS <value>
set_global_assignment -name AUTO_GLOBAL_MEMORY_CONTROLS -entity <entity
name> <value>
set_instance_assignment -name AUTO_GLOBAL_MEMORY_CONTROLS -to <to> -entity
<entity name> <value>
```

### Default Value

Off

## AUTO\_GLOBAL\_OE

Allows the Compiler to choose the signal that feeds the most TRI buffers as a global output enable signal that is made available throughout the device on the global routing paths. If you want to prevent the Compiler from automatically selecting a particular signal as global output enable, set the Global Signal option to 'Off' on that signal.

### Type

Boolean

### Device Support

- A
- E

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name AUTO_GLOBAL_OE <value>
set_global_assignment -name AUTO_GLOBAL_OE -entity <entity name> <value>
set_instance_assignment -name AUTO_GLOBAL_OE -to <to> -entity <entity name>
<value>
```

### Default Value

On

## AUTO\_GLOBAL\_REGISTER\_CONTROLS

Allows the Compiler to choose the signals that feed the most control signal inputs to flipflops (excluding clock signals) as global signals that are made available throughout the device on the global routing paths. Depending on the target device family, these control signals can include asynchronous clear and load, synchronous clear and load, clock enable, and preset signals. If you want to prevent the Compiler from automatically selecting a particular signal as global register control signal, set the Global Signal option to 'Off' on that signal.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- EPC1
- EPC2
- Enhanced Configuration Devices
- A
- B
- E
- FLEX8000
- Flash Memory
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX9000
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

- Stratix III
- Stratix IV
- Stratix V
- Virtual JTAG TAP

## Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name AUTO_GLOBAL_REGISTER_CONTROLS <value>
set_global_assignment -name AUTO_GLOBAL_REGISTER_CONTROLS -entity <entity
name> <value>
set_instance_assignment -name AUTO_GLOBAL_REGISTER_CONTROLS -to <to> -
entity <entity name> <value>
```

## Default Value

On



## AUTO\_MERGE\_PLLS

Allows the Compiler to automatically find and merge together two compatible phase-locked loops (PLL) driven by the same clock source, reducing the total number of PLLs used in a design.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name AUTO_MERGE_PLLS <value>
set_global_assignment -name AUTO_MERGE_PLLS -entity <entity name> <value>
set_instance_assignment -name AUTO_MERGE_PLLS -to <to> -entity <entity
name> <value>
```

### Default Value

On

## AUTO\_PACKED\_REGISTERS\_MAX

Allows the Compiler to automatically implement a register and a combinational function in the same logic cell. This option controls how aggressively the Fitter combines registers with other function blocks in order to reduce logic element count. If this option is set to 'Off', the Fitter does not attempt to place a pair of logic functions in a single logic cell; however, logic cells specified during synthesis to perform both a combinational and a sequential function are maintained. If this option is set to 'Normal', the Fitter places both a combinational and a sequential operation in a logic cell when it is expected that the placement does not affect design performance. When this option is set to 'Minimize Area', the Fitter aggressively combines unrelated sequential and combinational functions into a single logic cell in order to reduce the logic cell count, even at the expense of design performance. When this option is set to 'Minimize Area with Chains', the Fitter even more aggressively combines sequential and combinational functions that are part of arithmetic or register cascade chains or that can be converted to register cascade chains. When this setting is Auto, the fitter attempts to achieve the best performance while maintaining a fit for the design in the specified device. The fitter will combine all combinational and sequential functions that are deemed to benefit circuit speed. In addition, more aggressive combinations of unrelated combinational and sequential functions are performed to the extent required to reduce the area of the design in order to achieve a fit in the specified device.

### Old Name

AUTO\_PACKED\_REGISTERS\_MAXII, AUTO\_PACKED\_REGISTERS\_TSUNAMI, Auto Packed Registers -- MAX II

### Type

Enumeration

### Values

- Auto
- Minimize Area
- Minimize Area with Chains
- Normal
- Off

### Device Support

- MAX II
- MAX V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_global_assignment -name AUTO_PACKED_REGISTERS_MAX <value>
set_global_assignment -name AUTO_PACKED_REGISTERS_MAX -entity <entity name>
<value>
set_instance_assignment -name AUTO_PACKED_REGISTERS_MAX -to <to> -entity
```

<entity name> <value>

Default Value

Auto

## AUTO\_RESERVE\_CLKUSR\_FOR\_CALIBRATION

Automatically reserve CLKUSR pin for calibration purposes

### Type

Boolean

### Device Support

Arria 10

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name AUTO_RESERVE_CLKUSR_FOR_CALIBRATION <value>
```

### Default Value

On

### Example

```
set_global_assignment -name AUTO_RESERVE_CLKUSR_FOR_CALIBRATION OFF
```



## AUTO\_TURBO\_BIT

Controls the speed vs. power usage trade-off for a macrocell. If the Turbo Bit is on, the macrocell's speed increases; if it is off, its power consumption decreases; if you choose the 'Auto' setting, the Compiler chooses the most appropriate setting for the design.

### Type

Enumeration

### Values

- Auto
- Off
- On

### Device Support

- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S

### Notes

This assignment is included in the Analysis & Synthesis report.

### Syntax

```
set_global_assignment -name AUTO_TURBO_BIT <value>
set_global_assignment -name AUTO_TURBO_BIT -entity <entity name> <value>
set_instance_assignment -name AUTO_TURBO_BIT -to <to> -entity <entity name>
<value>
```

### Default Value

ON

## BASE\_PIN\_OUT\_FILE\_ON\_SAMEFRAME\_DEVICE

Directs the Compiler to base the Pin-Out File (.pin) and floorplan package views on the largest selected SameFrame device.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name BASE_PIN_OUT_FILE_ON_SAMEFRAME_DEVICE <value>
```

### Default Value

Off



## BLOCK\_RAM\_AND\_MLAB\_EQUIVALENT\_PAUSED\_READ\_CAPABILITIES

Controls whether RAMs implemented in MLAB cells must have equivalent pause read capabilities as RAMs implemented in block RAM. Pausing a read is the ability to keep around the last read value when reading is disabled. Allowing differences in paused read capabilities will provide the fitter more flexibility in implementing RAMs using MLAB cells. If this option is set to 'Don't Care', the Fitter may convert RAMs to MLAB cells even if they won't have equivalent paused read capabilities to a block RAM implementation. The Fitter will also output an information message notifying the user of RAMs with different paused read capabilities. If this option is set to 'Care', the Fitter will not convert RAMs to MLAB cells unless they have the equivalent paused read capabilities to a block RAM implementation. To allow the fitter the most flexibility in deciding which RAMs are implemented using MLAB cells, set this option to 'Don't Care'.

### Type

Enumeration

### Values

- Care
- Dont Care

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone V
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name  
BLOCK_RAM_AND_MLAB_EQUIVALENT_PAUSED_READ_CAPABILITIES <value>  
set_global_assignment -name  
BLOCK_RAM_AND_MLAB_EQUIVALENT_PAUSED_READ_CAPABILITIES -entity <entity name> <value>  
set_instance_assignment -name  
BLOCK_RAM_AND_MLAB_EQUIVALENT_PAUSED_READ_CAPABILITIES -to <to> -entity <entity  
name> <value>
```

**Default Value**

Care





## BLOCK\_RAM\_AND\_MLAB\_EQUIVALENT\_POWER\_UP\_CONDITIONS

Controls whether RAMs implemented in MLAB cells must have equivalent power up conditions as RAMs implemented in block RAM. Power up conditions occur when the device is powered up or globally reset. Allowing non-equivalent power up conditions will provide the fitter more flexibility in implementing RAMs using MLAB cells. If this option is set to 'Auto', the Fitter may convert RAMs to MLAB cells even if they won't have equivalent power up conditions to a block RAM implementation. The Fitter will also output a warning message notifying the user of RAMs with non-equivalent power up conditions. If this option is set to 'Don't Care', the same behavior as 'Auto' applies, but the warning message will instead be an information message. If this option is set to 'Care', the Fitter will not convert RAMs to MLAB cells unless they have equivalent power up conditions to a block RAM implementation. To allow the fitter the most flexibility in deciding which RAMs are implemented using MLAB cells, set this option to 'Auto' or 'Don't Care'.

### Type

Enumeration

### Values

- Auto
- Care
- Dont Care

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone V
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name  
BLOCK_RAM_AND_MLAB_EQUIVALENT_POWER_UP_CONDITIONS <value>  
set_global_assignment -name  
BLOCK_RAM_AND_MLAB_EQUIVALENT_POWER_UP_CONDITIONS -entity <entity name> <value>  
set_instance_assignment -name  
BLOCK_RAM_AND_MLAB_EQUIVALENT_POWER_UP_CONDITIONS -to <to> -entity <entity name>  
<value>
```

**Default Value**

Auto



## BLOCK\_RAM\_TO\_MLAB\_CELL\_CONVERSION

Controls whether the fitter is able to convert RAMs to use LAB locations when those RAMs use 'Auto' as the selected block type. If this option is changed to 'Off' then only MLAB cells in the design or RAM cells with a block type setting of 'MLAB' will use LAB locations to implement memory.

### Type

Boolean

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone V
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name BLOCK_RAM_TO_MLAB_CELL_CONVERSION <value>
set_global_assignment -name BLOCK_RAM_TO_MLAB_CELL_CONVERSION -entity
<entity name> <value>
set_instance_assignment -name BLOCK_RAM_TO_MLAB_CELL_CONVERSION -to <to> -
entity <entity name> <value>
```

### Default Value

On

## C3\_M9K\_BIT\_SKIP

Directs the fitter to skip certain bitlines in Cyclone III M9K blocks when implementing the specified RAM or ROM cell. The default remapping behavior is determined by the overall RAM Bit Reservation fitter setting, accessible from the More Fitter Settings page of the Settings dialog. This setting can be used to override that behavior for a specified RAM. Refer to the description of the global setting for more details of the setting values.

### Type

Enumeration

### Values

- Auto
- MAXIMUM
- Off

### Device Support

- Cyclone III
- Cyclone III LS

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name C3_M9K_BIT_SKIP -to <to> -entity <entity  
name> <value>
```



## CARRY\_OUT\_PINS\_LCELL\_INSERT

Directs the Fitter to enable or disable logic cell insertion when the I/Os are fed by carry or cascade chains. When this option is turned on, the Fitter inserts logic cells where they are needed to improve fitting. When this option is turned off, the Fitter inserts logic cells only to solve deterministic no fits.

### Type

Boolean

### Device Support

- A
- E

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name CARRY_OUT_PINS_LCELL_INSERT <value>
set_global_assignment -name CARRY_OUT_PINS_LCELL_INSERT -entity <entity
name> <value>
set_instance_assignment -name CARRY_OUT_PINS_LCELL_INSERT -to <to> -entity
<entity name> <value>
```

### Default Value

On

## CDR\_BANDWIDTH\_PRESET

Specifies the CDR (clock data recovery) bandwidth preset setting.

### Type

Enumeration

### Values

- Auto
- High
- Low
- Medium

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_instance_assignment -name CDR_BANDWIDTH_PRESET -to <to> -entity <entity  
name> <value>
```



## CKN\_CK\_PAIR

Specifies the pairing of a CKn pin to a CK pin. The I/O pin of a CK CKn pair must be placed on a differential pin pair. This option is ignored if is assigned to anything other than an I/O pad, input buffer, or output buffer.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name CKN_CK_PAIR -from <from> -to <to> -entity  
<entity name> <value>
```

## CLAMPING\_DIODE

Turns on the Clamping Diode of a pin. The clamping diode can be turned on to limit overshoot voltage for a pin in input operation. The clamping diode is turned on by default for 3.0-V PCI/PCI-X I/O standards. The clamping diode is turned off by default for 3.3-V LVTTL/LVCMOS I/O standards. This option is ignored if it is applied to anything other than a pin or a top-level design entity.

### Type

Boolean

### Device Support

- Arria II GX
- Arria II GZ
- Arria V
- Cyclone V
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name CLAMPING_DIODE -entity <entity name> <value>
set_instance_assignment -name CLAMPING_DIODE -to <to> -entity <entity name>
<value>
set_global_assignment -name CLAMPING_DIODE <value>
```

### Default Value

Off

### Example

```
set_instance_assignment -name CLAMPING_DIODE ON -to pin
```



## CLOCK\_ENABLE\_ROUTING

Specifies whether a clock enable signal in an I/O cell should be driven by the peripheral bus or the single-pin path. The Single-Pin setting drives the clock enable signal with the local interconnect shared by the I/O cell and the adjacent LAB. The Peripheral setting drives the clock enable signal with a peripheral control bus. This option is ignored if it is assigned to anything other than a logic function assigned to an I/O cell or the signal that drives the clock enable of the I/O cell.

### Type

Enumeration

### Values

- Peripheral
- Single-Pin

### Device Support

- A
- E

### Notes

None

### Syntax

```
set_instance_assignment -name CLOCK_ENABLE_ROUTING -to <to> -entity <entity  
name> <value>
```

## CLOCK\_REGION

Specifies that a signal routed using global routing paths should use the specified clock region. Valid values are clock region descriptions of the form "Regional Clock Region 1" or "Periphery Clock Region 1". The clock region names should match those displayed in the Chip Planner, and can include Global, Regional, Periphery or Spine Clock regions. For Arria 10 designs, one can also specify a comma separated list of assignments (e.g., "Periphery Clock Region 0, Periphery Clock Region 1"). If multiple regions are specified, the logic fed by the signal will be constrained to the smallest rectangular clock region that fully contains all of the regions specified. This assignment can also be used in conjunction with the "Global Signal" assignment to constrain the logic fed by a clock signal to an area of the chip that is smaller than the clock region specified by the Global Signal assignment. For example, a Global Signal assignment of "Global Clock" and a Clock Region assignment of "Regional Clock Region 1" constrains the logic to the area fed by Regional Clock Region 1.

### Type

String

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports wildcards.

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name CLOCK_REGION -to <to> -entity <entity name>
<value>
set_instance_assignment -name CLOCK_REGION -from <from> -to <to> -entity
<entity name> <value>
```

## CLOCK\_TO\_OUTPUT\_DELAY

Specifies the propagation delay to the output or bidirectional pin from the output register implemented in an I/O cell. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is off by default. This option is ignored if it is applied to anything other than an output or bidirectional pin.

### Type

Integer

### Device Support

- Arria GX
- Arria II GX
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- MAX 10
- Stratix II
- Stratix II GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name CLOCK_TO_OUTPUT_DELAY -to <to> -entity  
<entity name> <value>
```

## CONFIGURATION\_VCCIO\_LEVEL

Specifies the VCCIO voltage of the configuration pins for the current configuration scheme on the target device.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name CONFIGURATION_VCCIO_LEVEL <value>
```

### Default Value

Auto

### Example

```
set_global_assignment -name CONFIGURATION_VCCIO_LEVEL 1.8V
```

## See Also

FORCE\_CONFIGURATION\_VCCIO



## CONVERT\_PR\_WARNINGS\_TO\_ERRORS

Turns PR warnings into errors when enabled.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

### Syntax

```
set_global_assignment -name CONVERT_PR_WARNINGS_TO_ERRORS <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name CONVERT_PR_WARNINGS_TO_ERRORS ON
```



## CRC\_ERROR\_CHECKING

Specifies error detection CRC usage for the selected device. If error detection CRC is turned on, the device checks the validity of the programming data in the device. Any changes in the data while the device is in operation generates an error.

### Old Name

STRATIX\_CRC\_ERROR\_CHECKING, YEAGER\_CRC\_ERROR\_CHECKING

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- HardCopy III
- HardCopy IV
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name CRC_ERROR_CHECKING <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name CRC_ERROR_CHECKING ON
```

### See Also

ERROR\_CHECK\_FREQUENCY\_DIVISOR CRC\_ERROR\_OPEN\_DRAIN





## CRC\_ERROR\_OPEN\_DRAIN

Specify open drain on the CRC Error pin should be enabled or not

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone V
- HardCopy III
- MAX 10
- Stratix III
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name CRC_ERROR_OPEN_DRAIN <value>
```

### Example

```
set_global_assignment -name crc_error_open_drain on  
set_global_assignment -name crc_error_open_drain off
```

### See Also

CRC\_ERROR\_CHECKING ERROR\_CHECK\_FREQUENCY\_DIVISOR

## CURRENT\_STRENGTH\_NEW

Sets the drive strength of a pin. Specify a number (in mA), MIN, or MAX for output or bidirectional pins that support programmable drive strength. Please refer to the family data sheet for which drive strengths are allowed for each I/O standard. This option is ignored if it is applied to anything other than an output or bidirectional pin.

### Old Name

CURRENT\_STRENGTH

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.



## Syntax

```
set_instance_assignment -name CURRENT_STRENGTH_NEW -to <to> -entity <entity  
name> <value>
```

## Example

```
set_instance_assignment -name CURRENT_STRENGTH_NEW 12MA -to output_pin
```

## See Also

IO\_STANDARD OUTPUT\_TERMINATION

## CVP\_CONFDONE\_OPEN\_DRAIN

Specify open drain on the Cvp\_CONFDONE pin should be enabled or not

### Old Name

CVPCIE\_CONFDONE\_OPEN\_DRAIN

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name CVP_CONFDONE_OPEN_DRAIN <value>
```

### Default Value

On

### Example

```
set_global_assignment -name CVP_CONFDONE_OPEN_DRAIN on  
set_global_assignment -name CVP_CONFDONE_OPEN_DRAIN off
```

### See Also

ENABLE\_CVP\_CONFDONE

## CVP\_MODE

Specifies the configuration mode for Configuration via Protocol (CvP). In Core initialization mode, the peripheral image is stored in an external configuration device and is loaded into the FPGA through the conventional configuration scheme. The core image is stored in a host memory and is loaded into the FPGA through the PCIe link. In core update mode, the FPGA device is initialized after initial system power up by loading the full configuration image from the external local configuration device to the FPGA. User can use the PCIe link to perform one or more FPGA core image update through this mode. In the Off mode, CvP is turned off.

### Old Name

CVPCIE\_MODE

### Type

Enumeration

### Values

- Core initialization
- Core initialization and update
- Core update
- Off

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name CVP_MODE <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name CVP_MODE "Power up and subsequent core configuration"
```

## CYCLONEIII\_CONFIGURATION\_SCHEME

The method used to load data into the device. Up to four configuration schemes are available, depending on the selected device: Passive Serial (PS); Fast Passive Parallel (FPP), Active Parallel (AP) and Active Serial (AS).

### Type

Enumeration

### Device Support

- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX

### Notes

None

### Syntax

```
set_global_assignment -name CYCLONEIII_CONFIGURATION_SCHEME <value>
```

### Default Value

Active Serial

### Example

```
set_global_assignment -name CYCLONEIII_CONFIGURATION_SCHEME "Active Serial"
```

## CYCLONEII\_CONFIGURATION\_SCHEME

The method used to load data into the device. Two configuration schemes are available: Passive Serial (PS); and Active Serial (AS).

### Type

Enumeration

### Values

- Active Serial
- Passive Serial

### Device Support

Cyclone II

### Notes

None

### Syntax

```
set_global_assignment -name CYCLONEII_CONFIGURATION_SCHEME <value>
```

### Default Value

Active Serial

## CYCLONEII\_RESERVE\_NCEO\_AFTER\_CONFIGURATION

Specifies how the nCEO pin should be used when the device is operating in user mode after configuration is complete. The nCEO pin can be reserved as dedicated nCEO programming pin or a regular I/O pin.

### Type

Enumeration

### Values

- Use as programming pin
- Use as regular IO

### Device Support

- Arria II GX
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX

### Notes

None

### Syntax

```
<value> set_global_assignment -name CYCLONEII_RESERVE_NCEO_AFTER_CONFIGURATION
```

### Default Value

Use as programming pin

### Example

```
set_global_assignment -name CYCLONEII_RESERVE_NCEO_AFTER_CONFIGURATION "Use  
as programming pin"
```



## CYCLONEII\_TERMINATION

Allows the Compiler to configure the on-chip termination (OCT) and impedance matching for an I/O pin. OCT helps to prevent signal reflections and maintain signal integrity. This option is ignored if it is applied to anything other than an I/O pin.

### Old Name

Termination -- CYCLONE II

### Type

Enumeration

### Values

- Off
- Series 25 Ohms
- Series 50 Ohms

### Device Support

Cyclone II

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name CYCLONEII_TERMINATION -to <to> -entity  
<entity name> <value>
```



## CYCLONE\_CONFIGURATION\_SCHEME

The method used to load data into the device. Two configuration schemes are available: Passive Serial (PS); and Active Serial (AS).

### Type

Enumeration

### Values

- Active Serial
- Passive Serial

### Device Support

Cyclone

### Notes

None

### Syntax

```
set_global_assignment -name CYCLONE_CONFIGURATION_SCHEME <value>
```

### Default Value

Active Serial

## D1\_DELAY

Specifies the propagation delay for D1 Delay Cell. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Old Name

T1\_DELAY

### Type

Integer

### Device Support

- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone V
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name D1_DELAY -to <to> -entity <entity name>
```

## D1\_FINE\_DELAY

Enable the fine delay resolution on D1 Delay

### Old Name

T1\_FINE\_DELAY

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

## Syntax

```
<value> set_instance_assignment -name D1_FINE_DELAY -to <to> -entity <entity name>
```

## D2\_DELAY

Specifies the propagation delay for D2 Delay Cell. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Old Name

T2\_DELAY

### Type

Integer

### Device Support

- Arria II GZ
- Arria V GZ
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name D2_DELAY -to <to> -entity <entity name>
```

## D3\_DELAY

Specifies the propagation delay for D3 Delay Cell. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Old Name

T3\_DELAY

### Type

Integer

### Device Support

- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone V
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name D3_DELAY -to <to> -entity <entity name>
<value>
set_instance_assignment -name D3_DELAY -from <from> -to <to> -entity
<entity name> <value>
```

## D4\_DELAY

Specifies the propagation delay for D4 Delay Cell. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Old Name

T7\_DELAY

### Type

Integer

### Device Support

- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone V
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name D4_DELAY -to <to> -entity <entity name>
```



## D4\_FINE\_DELAY

Enable the fine delay resolution on D4 Delay

### Old Name

T7\_FINE\_DELAY

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

## Syntax

```
<value> set_instance_assignment -name D4_FINE_DELAY -to <to> -entity <entity name>
```

## D5\_DELAY

Specifies the propagation delay for D5 Delay Cell. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an output or bidirectional pin.

### Old Name

T9\_DELAY

### Type

Integer

### Device Support

- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone V
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name D5_DELAY -to <to> -entity <entity name>
```

## D5\_FINE\_DELAY

Enable the fine delay resolution on D5 Delay

### Old Name

T9\_FINE\_DELAY

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

## Syntax

```
<value> set_instance_assignment -name D5_FINE_DELAY -to <to> -entity <entity name>
```

## D5\_OCT\_DELAY

Specifies the propagation delay for D5 OCT Delay Cell. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Old Name

T9\_OCT\_DELAY

### Type

Integer

### Device Support

- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone V
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name D5_OCT_DELAY -to <to> -entity <entity name>
```

## D5\_OE\_DELAY

Specifies the propagation delay for D5 Output-Enable Delay Cell. Use this advanced option only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For more information about this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an output or bidirectional pin.

### Old Name

T9\_OE\_DELAY

### Type

Integer

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

## Notes

This assignment supports Fitter wildcards.

## Syntax

```
<value> set_instance_assignment -name D5_OE_DELAY -to <to> -entity <entity name>
```



## D6\_DELAY

Specifies the propagation delay for D6 Delay Cell. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an output or bidirectional pin.

### Old Name

T10\_DELAY

### Type

Integer

### Device Support

- Arria II GZ
- Arria V GZ
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name D6_DELAY -to <to> -entity <entity name>
```

## D6\_FINE\_DELAY

Enable the fine delay resolution on D6 Delay

### Old Name

T10\_FINE\_DELAY

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

## Syntax

```
<value> set_instance_assignment -name D6_FINE_DELAY -to <to> -entity <entity name>
```

## D6\_OCT\_DELAY

Specifies the propagation delay for D6 OCT Delay Cell. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Old Name

T10\_OCT\_DELAY

### Type

Integer

### Device Support

- Arria II GZ
- Arria V GZ
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name D6_OCT_DELAY -to <to> -entity <entity name>
```

## D6\_OE\_DELAY

Specifies the propagation delay for D6 Output-Enable Delay Cell. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an output or bidirectional pin.

### Old Name

T10\_OE\_DELAY

### Type

Integer

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

## Notes

This assignment supports Fitter wildcards.

## Syntax

```
<value> set_instance_assignment -name D6_OE_DELAY -to <to> -entity <entity name>
```

## D6\_OE\_FINE\_DELAY

Enable the fine delay resolution on D6 Output-Enable Delay

### Old Name

T10\_OE\_FINE\_DELAY

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

## Syntax

```
set_instance_assignment -name D6_OE_FINE_DELAY -to <to> -entity <entity  
name> <value>
```



## DATA0\_PIN

Specifies the Data[0] configuration pin.

### Type

Boolean

### Device Support

- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- MAX 10

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_instance_assignment -name DATA0_PIN -to <to> <value>
```

## DCLK\_PIN

Specifies the DCLK configuration pin.

### Type

Boolean

### Device Support

- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- MAX 10

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_instance_assignment -name DCLK_PIN -to <to> <value>
```



## DC\_CURRENT\_FOR\_ELECTROMIGRATION\_CHECK

Specifies the maximum amount of DC current, in mA, allowed when the Fitter checks for electromigration violations.

### Type

Integer

### Device Support

- Arria GX
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_instance_assignment -name DC_CURRENT_FOR_ELECTROMIGRATION_CHECK -to  
<to> <value>
```

## DDIO\_INPUT\_REGISTER

Directs the Compiler to perform special placement and routing of the specified register to prevent register packing of the input registers into the IO registers. This is used for registers involved in DDR memory interfaces. A setting of High designates the input register that gets set on the rising edge of the clock; a setting of Low designates the input register that gets set on the falling edge of the clock.

### Type

Enumeration

### Values

- High
- Low
- Off

### Device Support

- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- MAX 10

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name DDIO_INPUT_REGISTER -to <to> -entity <entity  
name> <value>
```

## DDIO\_OUTPUT\_REGISTER

Directs the Compiler to perform special placement and routing of the specified register to provide a glitch-free output. This is used for registers involved in DDR memory interfaces. A setting of High designates the output register used when the output mux select is 1; a setting of Low designates the output register used when the output mux select is 0.

### Type

Enumeration

### Values

- High
- Low
- Off

### Device Support

- Cyclone
- Cyclone II

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name DDIO_OUTPUT_REGISTER -to <to> -entity <entity  
name> <value>
```

## DDIO\_OUTPUT\_REGISTER\_DISTANCE

Directs the Fitter to place the DDIO output registers (and output mux) that feed this I/O pin in a location whose LAB distance is specified by this option. This option is ignored if applied to an input pin or if applied to an output or bidir pin that is not fed by a DDIO Output configuration.

### Type

Integer

### Device Support

Cyclone II

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name DDIO_OUTPUT_REGISTER_DISTANCE -to <to> -  
entity <entity name> <value>
```

## DECREASE\_INPUT\_DELAY\_TO\_INPUT\_REGISTER

Decreases the propagation delay from an input pin to the data input of the input register implemented in the I/O cell associated with the pin. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Type

Enumeration

### Values

- Off
- On

### Device Support

- Cyclone
- MAX7000B
- Mercury
- Stratix
- Stratix GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name DECREASE_INPUT_DELAY_TO_INPUT_REGISTER -to  
<to> -entity <entity name> <value>
```

## DECREASE\_INPUT\_DELAY\_TO\_OUTPUT\_REGISTER

Decreases the propagation delay from the interior of the device to the data input of the output register implemented in an I/O cell. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other an output or bidirectional pin that is associated with an output register implemented in an I/O cell.

### Old Name

DELAY\_SETTING\_TO\_CORE\_TO\_OUTPUT\_REGISTER

### Type

Enumeration

### Values

- Off
- On

### Device Support

- Stratix
- Stratix GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name DECREASE_INPUT_DELAY_TO_OUTPUT_REGISTER -to  
<to> -entity <entity name> <value>
```





## DELAY\_SETTING\_FROM\_VIO\_TO\_CORE

Increases the propagation delay from a vertical pin to the interior of the device when the vertical pin is using the FastRow Interconnect option to route the fan-outs of an input or bidirectional pin. Both the pin and its fan-out(s) must be assigned to the same Fast Region. The FastRow Interconnect and FastRow Interconnect Delay options are ignored if they are applied to anything other than a column (vertical) pin that is implemented as an input or bidirectional pin.

### Type

Time

### Notes

None

### Syntax

```
set_instance_assignment -name DELAY_SETTING_FROM_VIO_TO_CORE -to <to> -  
entity <entity name> <value>
```

## DEVICE

Specifies the device to use.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name DEVICE <value>
```

### Default Value

AUTO



## DEVICE\_INITIALIZATION\_CLOCK

Specifies the clock source for device initialization (the duration between CONF\_DONE signal went high and before INIT\_DONE signal goes high). In 20nm or prior device families, three options are available when AS x1 or AS x4 configuration mode is not selected, which are Internal Oscillator (default value), DCLK pin, and CLKUSR pin; For AS x1 or AS x4 configuration mode, you can select either the Internal Oscillator or CLKUSR pin only. The DCLK pin is an illegal option for AS mode. In 14 nm family, only Internal Oscillator or OSC\_CLK\_1 pins are available.

### Type

Enumeration

### Values

- INIT\_CLKUSR
- INIT\_DCLK
- INIT\_INTOSC
- OSC\_CLK\_1\_100MHZ
- OSC\_CLK\_1\_125MHZ
- OSC\_CLK\_1\_25MHZ

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name DEVICE_INITIALIZATION_CLOCK <value>
```

### Default Value

INIT\_INTOSC

### Example

```
set_global_assignment -name DEVICE_INITIALIZATION_CLOCK "CLKUSR"
```

### See Also

USER\_START\_UP\_CLOCK

## DEVICE\_MIGRATION\_LIST

Shows the selected migration devices for the current device.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name DEVICE_MIGRATION_LIST <value>
```



## DEVICE\_TECHNOLOGY\_MIGRATION\_LIST

Shows the selected technology migration devices for the current device.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name DEVICE_TECHNOLOGY_MIGRATION_LIST <value>
```

## DM\_PIN

Specifies the DM pin. The DM pin of a DQS group must be placed in the DM pin location of the DQS group. This option is ignored if is assigned to anything other than an I/O pad, input buffer, or output buffer.

### Type

Boolean

### Device Support

MAX 10

### Notes

None

### Syntax

```
set_instance_assignment -name DM_PIN -to <to> -entity <entity name> <value>
```

### Example

```
set_instance_assignment -name DM_PIN ON -to mem_dm
```

### See Also

DQ\_GROUP

## DPRIO\_CHANNEL\_NUM

RX/TX channel number for DPRIO logic

### Type

Integer

### Device Support

Stratix II GX

### Notes

None

### Syntax

```
set_instance_assignment -name DPRIO_CHANNEL_NUM -to <to> -entity <entity  
name> <value>
```

## DPRIO\_CRUCLK\_NUM

Logical RX CRU clock number

### Type

Integer

### Device Support

Stratix II GX

### Notes

None

### Syntax

```
set_instance_assignment -name DPRIO_CRUCLK_NUM -to <to> -entity <entity  
name> <value>
```





## DPRIO\_INTERFACE\_REG

Interface input/output register of DPRIO logic

### Type

Boolean

### Device Support

Stratix II GX

### Notes

None

### Syntax

```
set_instance_assignment -name DPRIO_INTERFACE_REG -to <to> -entity <entity  
name> <value>
```

## DPRIO\_QUAD\_NUM

RX/TX quad number for DPRIO logic

### Type

Integer

### Device Support

Stratix II GX

### Notes

None

### Syntax

```
<value> set_instance_assignment -name DPRIO_QUAD_NUM -to <to> -entity <entity name>
```

## DPRIO\_QUAD\_PLL\_NUM

Logical CMU PLL number in a quad

### Type

Integer

### Device Support

Stratix II GX

### Notes

None

### Syntax

```
set_instance_assignment -name DPRIO_QUAD_PLL_NUM -to <to> -entity <entity  
name> <value>
```

## DPRIO\_TX\_PLLO\_REFCLK\_NUM

Logical TX PLL0 Refclk number

### Type

Integer

### Device Support

Stratix II GX

### Notes

None

### Syntax

```
set_instance_assignment -name DPRIO_TX_PLLO_REFCLK_NUM -to <to> -entity  
<entity name> <value>
```

## DPRIO\_TX\_PLL1\_REFCLK\_NUM

Logical TX PLL1 Refclk number

### Type

Integer

### Device Support

Stratix II GX

### Notes

None

### Syntax

```
set_instance_assignment -name DPRIO_TX_PLL1_REFCLK_NUM -to <to> -entity  
<entity name> <value>
```

## DPRIO\_TX\_PLL\_NUM

Logical TX PLL number

### Type

Integer

### Device Support

Stratix II GX

### Notes

None

### Syntax

```
set_instance_assignment -name DPRIO_TX_PLL_NUM -to <to> -entity <entity  
name> <value>
```



## DQSB\_DQS\_PAIR

Specifies the pairing of a DQSn pin to a DQS pin. The I/O pin of a DQS must be placed in the DQS pin location of a DQS group; the I/O pin of a DQSn must be placed in the DQSn pin location of the same DQS group. This option is ignored if is assigned to anything other than an I/O pad, input buffer, or output buffer.

### Type

Boolean

### Device Support

- Arria II GX
- Arria II GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name DQSB_DQS_PAIR -from <from> -to <to> -entity  
<entity name> <value>
```

### Example

```
set_instance_assignment -name DQSB_DQS_PAIR ON -from mem_dqs_n[0] -to  
mem_dqs[0]
```

### See Also

DQ\_GROUP MEMORY\_INTERFACE\_DATA\_PIN\_GROUP

## DQSOUT\_DELAY\_CHAIN

Set the propagation delay on the DQSBUS signal from the DQS pin. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than a DQ pin.

### Type

Integer

### Device Support

- Arria GX
- Arria II GX
- HardCopy II
- Stratix II
- Stratix II GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name DQSOUT_DELAY_CHAIN -to <to> -entity <entity  
name> <value>
```





## DQS\_ENABLE\_DELAY\_CHAIN

Set the propagation delay on the DQS enable signal for the DQS pin. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than a DQS pin.

### Type

Integer

### Device Support

Arria II GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name DQS_ENABLE_DELAY_CHAIN -to <to> -entity  
<entity name> <value>
```

## DQS\_LOCAL\_CLOCK\_DELAY\_CHAIN

Set the propagation delay on the DQS signal to the input register of the target pin. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than a DQ or DQS pin.

### Type

Integer

### Device Support

- Arria GX
- Arria II GX
- HardCopy II
- Stratix II
- Stratix II GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name DQS_LOCAL_CLOCK_DELAY_CHAIN -to <to> -entity  
<entity name> <value>
```

## DQ\_GROUP

Specifies the grouping from a DQS pin to its associated DQ pins and the width (4, 9, 18, or 36) of the group. Setting this option allows the Fitter to view the pins as a DQS/DQ pin group. I/O pins of a DQ pin group must be placed in the DQ pin locations of a single DQS group. This option is ignored if is assigned to anything other than an I/O pad, input buffer, or output buffer.

### Type

Integer

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name DQ_GROUP -from <from> -to <to> -entity  
<entity name> <value>
```

### Example

```
set_instance_assignment -name DQ_GROUP 9 -from mem_dqs[0] -to mem_dq[0..7]
```

### See Also

DQSB\_DQS\_PAIR MEMORY\_INTERFACE\_DATA\_PIN\_GROUP

## DQ\_PIN

Designates the specified pin as a DQ I/O pin.

### Type

Boolean

### Device Support

Cyclone II

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name DQ_PIN -to <to> -entity <entity name> <value>
```



## DUAL\_PURPOSE\_CLOCK\_PIN\_DELAY

Specifies the propagation delay from a dual-purpose clock pin to its fan-out destinations that are routed on the global clock network. Legal integer values range from 0 through 63 for Cyclone and Cyclone II device families and from 0 through 11 for Cyclone III, where 0 is the setting with the least delay and 63 is the setting with the most delay. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin, or if the pin is user assigned to a non-dual-purpose clock pin location.

### Type

Integer

### Device Support

- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- MAX 10

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name DUAL_PURPOSE_CLOCK_PIN_DELAY -to <to> -entity  
<entity name> <value>
```

## DUPLICATE\_ATOM

Directs the Compiler to duplicate the source node, and uses the new duplicate node to fan out to the destination node; the original source node no longer fans out to the destination node. Use the 'Value' field to specify the name of the duplicate node.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

The value of this assignment is case sensitive.

This assignment supports Fitter wildcards.

The value of this assignment must be a node name.

### Syntax

```
set_instance_assignment -name DUPLICATE_ATOM -from <from> -to <to> -entity
```

<entity name> <value>

## DYNAMIC\_OCT\_CONTROL\_GROUP

Assigns a dynamic termination control group number for the specified node. Turning on this option directs the Fitter to view the specified nodes as a dynamic termination control group so as to place them next to each other to share the termination control routing resource. This is only applicable for bidirectional pins.

### Type

String

### Device Support

- Arria II GZ
- Stratix III
- Stratix IV

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name DYNAMIC_OCT_CONTROL_GROUP -to <to> -entity  
<entity name> <value>
```



## ECO\_ALLOW\_ROUTING\_CHANGES

This option controls whether the Fitter will move items in a design to ensure that new ECO signals get routed.

### Type

Boolean

### Device Support

- Cyclone
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name ECO_ALLOW_ROUTING_CHANGES <value>
```

### Default Value

Off

## ECO\_OPTIMIZE\_TIMING

Controls whether the fitter optimizes to meet the user's maximum delay timing requirements (eg. clock cycle time, Tsu, Tco) during ECO compiles. By default, this option is set to off. Turning it on can improve timing performance at the cost of compilation time.

### Type

Enumeration

### Values

- Off
- On

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name ECO_OPTIMIZE_TIMING <value>
```

### Default Value

Off



## ECO\_REGENERATE\_REPORT

Controls whether the fitter report is regenerated during ECO compiles. By default, this option is set to off. Turning it on will regenerate the report at the cost of compilation time.

### Type

Enumeration

### Values

- Off
- On

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name ECO_REGENERATE_REPORT <value>
```

### Default Value

Off

## ENABLE\_ASMI\_FOR\_FLASH\_LOADER

Enables ASMI interface for Flash Loader even before condone goes high.

### Type

Boolean

### Device Support

Cyclone II

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_ASMI_FOR_FLASH_LOADER <value>
```

### Default Value

Off

## ENABLE\_BENEFICIAL\_SKEW\_OPTIMIZATION

Allows the fitter to insert skew on globally routed clock signals to improve the performance of the design.

### Type

Boolean

### Device Support

- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- MAX 10
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name ENABLE_BENEFICIAL_SKEW_OPTIMIZATION <value>  
set_instance_assignment -name ENABLE_BENEFICIAL_SKEW_OPTIMIZATION -to <to> -  
entity <entity name> <value>
```

### Default Value

On

## ENABLE\_BOOT\_SEL\_PIN

Enables CONFIG\_SEL pin in user mode. If this option is turned off, the CONFIG\_SEL pin are disabled when the device operates in user mode and is available as a user I/O pin.

### Type

Boolean

### Device Support

MAX 10

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_BOOT_SEL_PIN <value>
```

### Default Value

On

### Example

```
set_global_assignment -name ENABLE_BOOT_SEL_PIN ON
```



## ENABLE\_BUS\_HOLD\_CIRCUITRY

Enables bus-hold circuitry during device operation. If this option is turned on, a pin will retain its last logic level when it is not driven, and will not go to a high impedance logic level. The 'Enable Bus-Hold Circuitry' option should not be used at the same time as the 'Weak Pull-Up Resistor' option. This option is ignored if it is applied to anything other than a pin.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX7000B
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name ENABLE_BUS_HOLD_CIRCUITRY <value>
set_global_assignment -name ENABLE_BUS_HOLD_CIRCUITRY -entity <entity name>
<value>
set_instance_assignment -name ENABLE_BUS_HOLD_CIRCUITRY -to <to> -entity
<entity name> <value>
```

## Default Value

Off

## Example

```
set_instance_assignment -name ENABLE_BUS_HOLD_CIRCUITRY ON -to pin
```



## ENABLE\_CONFIGURATION\_PINS

Enables major configuration pins, nCONFIG, nSTATUS, and CONF\_DONE pin in user mode. If this option is turned off, the nCONFIG, nSTATUS, and CONF\_DONE pins are disabled when the device operates in user mode and is available as a user I/O pin.

### Type

Boolean

### Device Support

MAX 10

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_CONFIGURATION_PINS <value>
```

### Default Value

On

### Example

```
set_global_assignment -name ENABLE_CONFIGURATION_PINS ON
```

## ENABLE\_CRC\_ERROR\_PIN

Specifies error detection CRC and CRC\_ERROR pin usage for the selected device. If error detection CRC is turned on, the device checks the validity of the programming data in the device. Any changes in the data while the device is in operation generates an error.

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- MAX 10
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_CRC_ERROR_PIN <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name ENABLE_CRC_ERROR_PIN ON
```

### See Also

ERROR\_CHECK\_FREQUENCY\_DIVISOR CRC\_ERROR\_OPEN\_DRAIN

## ENABLE\_CVP\_CONFDONE

Enable the Cvp\_CONFDONE pin, which indicates that the device finished core programming in Configuration via Protocol mode. If this option is turned off, the Cvp\_CONFDONE pin is disabled when the device operates in user mode and is available as a user I/O pin.

### Old Name

ENABLE\_CVPCIE\_CONFDONE

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_CVP_CONFDONE <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name ENABLE_CVP_CONFDONE ON
```

### See Also

CVP\_CONFDONE\_OPEN\_DRAIN

## ENABLE\_DEVICE\_WIDE\_OE

Enables the DEV\_OE pin when the device is in user mode. If this option is turned on, all outputs on the chip operate normally. When the pin is disabled, all outputs are tri-stated. If this option is turned off, the DEV\_OE pin is disabled when the device operates in user mode and is available as a user I/O pin.

### Old Name

ENABLE\_CHIP\_WIDE\_OE

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

None



## Syntax

```
set_global_assignment -name ENABLE_DEVICE_WIDE_OE <value>
```

## Default Value

Off

## Example

```
set_global_assignment -name ENABLE_DEVICE_WIDE_OE ON
```

## ENABLE\_DEVICE\_WIDE\_RESET

Enables the DEV\_CLRn pin, which allows all registers of the device to be reset by an external source. If this option is turned off, the DEV\_CLRn pin is disabled when the device operates in user mode and is available as a user I/O pin.

### Old Name

ENABLE\_CHIP\_WIDE\_RESET

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

None



## Syntax

```
set_global_assignment -name ENABLE_DEVICE_WIDE_RESET <value>
```

## Default Value

Off

## Example

```
set_global_assignment -name ENABLE_DEVICE_WIDE_RESET ON
```

## ENABLE\_HOLD\_BACK\_OFF

Enables the Fitter to successfully fit a design despite infeasible hold constraints.

### Type

Enumeration

### Values

- Off
- On

### Device Support

HardCopy II

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_HOLD_BACK_OFF <value>
```

### Default Value

On





## ENABLE\_INIT\_DONE\_OUTPUT

Enables the INIT\_DONE pin, which allows you to externally monitor when initialization is completed and the device is in user mode. If this option is turned off, the INIT\_DONE pin is disabled when the device operates in user mode and is available as a user I/O pin.

### Old Name

Enable INIT\_DONE Output

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

None

## Syntax

```
set_global_assignment -name ENABLE_INIT_DONE_OUTPUT <value>
```

## Default Value

Off

## Example

```
set_global_assignment -name ENABLE_INIT_DONE_OUTPUT OFF
```

## See Also

INIT\_DONE\_OPEN\_DRAIN

## ENABLE\_JTAG\_BST\_SUPPORT

Enables JTAG boundary-scan test (BST) support.

### Type

Boolean

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_JTAG_BST_SUPPORT <value>
```

### Default Value

Off

## ENABLE\_JTAG\_PIN\_SHARING

Enables JTAG pins sharing feature in user mode. When selected, the JTAGEN pin is used to select JTAG pins (TDO, TCK, TDI, and TMS pins) operation, between JTAG operation (JTAGEN=1) and user I/O operation (JTAGEN=0). If JTAG pin sharing is not enabled the JTAGEN pin acts as a user I/O pin, and the JTAG pins (TDO, TCK, TDI, and TMS pins) are retained as dedicated JTAG pins.

### Type

Boolean

### Device Support

MAX 10

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_JTAG_PIN_SHARING <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name ENABLE_JTAG_PIN_SHARING OFF
```

## ENABLE\_NCEO\_OUTPUT

Enables the nCEO pin. This pin should be connected to the nCE of the succeeding device when multiple devices are being programmed. If this option is turned off, the nCEO pin is disabled when the device operates in user mode and is available as a user I/O pin.

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_NCEO_OUTPUT <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name ENABLE_NCEO_OUTPUT OFF
```

## ENABLE\_NCE\_PIN

Enables nCE pin in user mode. If this option is turned off, the nCE pin are disabled when the device operates in user mode and is available as a user I/O pin.

### Type

Boolean

### Device Support

MAX 10

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_NCE_PIN <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name ENABLE_NCE_PIN ON
```

## ENABLE\_NCONFIG\_FROM\_CORE

Enables the nCONFIG signal from the core. If this option is turned on, you can send the nCONFIG signal from the core or the package pin to the control block to reconfigure the device. If this option is turned off, the nCONFIG signal from the core is disabled and you can only send the nCONFIG signal from the package pin to the control block.

### Type

Boolean

### Device Support

MAX 10

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_NCONFIG_FROM_CORE <value>
```

### Default Value

On

### Example

```
set_global_assignment -name ENABLE_NCONFIG_FROM_CORE ON
```

## ENABLE\_PR\_PINS

Allows you to enable the PR\_REQUEST, PR\_READY, PR\_ERROR, PR\_DONE, DCLK, and DATA[15..0] pins. These pins are needed to support partial reconfiguration (PR) with an external host or external scrubbing. An external host uses the PR\_REQUEST pin to request partial reconfiguration or external scrubbing, the PR\_READY pin to determine if the device is ready to receive programming data, the PR\_ERROR pin to externally monitor programming errors, and the PR\_DONE pin to indicate the device finished programming. If this option is turned off, these pins are not available as PR pins when the device operates in user mode and the dual-purpose programming pins are available as user I/O pins.

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_PR_PINS <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name ENABLE_PR_PINS ON
```

### See Also

PR\_PINS\_OPEN\_DRAIN



## ENABLE\_UNUSED\_RX\_CLOCK\_WORKAROUND

Enable workaround for unused RX clock to preserve its performance over time

### Type

Boolean

### Device Support

Arria 10

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name ENABLE_UNUSED_RX_CLOCK_WORKAROUND <value>
set_instance_assignment -name ENABLE_UNUSED_RX_CLOCK_WORKAROUND -to <to> -
entity <entity name> <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name ENABLE_UNUSED_RX_CLOCK_WORKAROUND ON
set_instance_assignment -name ENABLE_UNUSED_RX_CLOCK_WORKAROUND ON -to AW34
```

## ENABLE\_VREFA\_PIN

Enable the circuitry for input voltage reference pins A.

### Old Name

Enable VREFA pin

### Type

Boolean

### Device Support

MAX7000B

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_VREFA_PIN <value>
```

### Default Value

Off



## ENABLE\_VREFB\_PIN

Enable the circuitry for input voltage reference pins B.

### Old Name

Enable VREFB pin

### Type

Boolean

### Device Support

MAX7000B

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_VREFB_PIN <value>
```

### Default Value

Off

## ERROR\_CHECK\_FREQUENCY\_DIVISOR

Specifies the divide value of the internal clock, which determines the frequency of the CRC. The divide value must be a power of two. Refer to the device handbook to find the frequency of the internal clock for the selected device.

### Type

Integer

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name ERROR_CHECK_FREQUENCY_DIVISOR <value>
```

## Example

```
set_global_assignment -name ERROR_CHECK_FREQUENCY_DIVISOR 16
```

## See Also

CRC\_ERROR\_CHECKING

## EXCLUSIVE\_IO\_GROUP

Assigns an exclusive group number for the specified I/O. I/Os with the different exclusive group number cannot share the same bank.

### Type

Integer

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name EXCLUSIVE_IO_GROUP -to <to> -entity <entity  
name> <value>
```

### Example

```
set_instance_assignment -name "EXCLUSIVE_IO_GROUP" -to pin
```

## EXTERNAL\_LVDS\_RX\_USES\_DPA

Indicates that this LVDS Transmitter pin is connected to an external LVDS Receiver that uses DPA.

### Type

Boolean

### Device Support

Arria II GX

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_instance_assignment -name EXTERNAL_LVDS_RX_USES_DPA -to <to> -entity  
<entity name> <value>
```

## FASTROW\_INTERCONNECT

Uses FastRow interconnect to route the fan-outs of an input or bidirectional pin. Both the pin and its fan-out(s) must also be assigned to the same Fast Region. The FastRow Interconnect option is ignored if it is applied to anything other than a column (vertical) pin that is implemented as an input or bidirectional pin.

### Type

Boolean

### Notes

None

### Syntax

```
set_instance_assignment -name FASTROW_INTERCONNECT -to <to> -entity <entity  
name> <value>
```





## FINAL\_PLACEMENT\_OPTIMIZATION

Specifies whether the Fitter performs final placement optimizations. Performing final placement optimizations may improve timing and routability, but may also require longer compilation time. The default setting of Automatically can be used with the Auto Fit Fitter Effort Level (also the default) to let the fitter decide whether these optimizations should run based on the routability and timing requirements of the design.

### Type

Enumeration

### Values

- Always
- Automatically
- Never

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name FINAL_PLACEMENT_OPTIMIZATION <value>
```

**Default Value**

Automatically



## FITTER\_ADJUST\_HC\_SHORT\_PATH\_GUARDBAND

Allows timing analysis to add extra short path guardband on a specific node during fitting.

### Type

Integer

### Device Support

- HardCopy III
- HardCopy IV

### Notes

None

### Syntax

```
set_global_assignment -name FITTER_ADJUST_HC_SHORT_PATH_GUARDBAND <value>
set_global_assignment -name FITTER_ADJUST_HC_SHORT_PATH_GUARDBAND -entity
<entity name> <value>
set_instance_assignment -name FITTER_ADJUST_HC_SHORT_PATH_GUARDBAND -to
<to> -entity <entity name> <value>
```

## FITTER\_AGGRESSIVE\_ROUTABILITY\_OPTIMIZATION

Specifies whether the Fitter aggressively optimizes for routability. Performing aggressive routability optimizations may decrease design speed, but may also reduce routing wire usage and routing time. The default setting of Automatically lets the fitter decide whether to perform these optimizations based on the routability and timing requirements of the design.

### Type

Enumeration

### Values

- Always
- Automatically
- Never

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

## Syntax

```
<value> set_global_assignment -name FITTER_AGGRESSIVE_ROUTABILITY_OPTIMIZATION
```

## Default Value

Automatically

## FITTER\_AUTO\_EFFORT\_DESIRED\_SLACK\_MARGIN

Specifies the amount of worst-case slack margin the fitter should try to maintain when the Fitter Effort option is set to 'Auto Fit'. If the design is likely to have at least this much slack on every path, the fitter will reduce optimization effort to reduce compilation time. Otherwise, its behavior will be the same as it is with the 'Standard Fit' Fitter Effort setting.

### Type

Time

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name FITTER_AUTO_EFFORT_DESIRED_SLACK_MARGIN <value>
```

Default Value

0ns

## FITTER\_EARLY\_TIMING\_ESTIMATE\_MODE

Controls the type of early timing estimate produced by the Early Timing Estimate feature. Realistic will estimate the average results expected from a Standard Fit compile, Optimistic will estimate the best case final timing and Pessimistic will estimate the worst case final timing.

### Type

Enumeration

### Values

- Optimistic
- Pessimistic
- Realistic

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name FITTER_EARLY_TIMING_ESTIMATE_MODE <value>
```



## Default Value

Realistic



## FITTER\_EFFORT

Controls the fitter's trade-off between performance and compilation speed. Auto Fit adjusts the fitter optimization effort to minimize compilation time, while still achieving the design timing requirements. The Auto Fit Effort Desired Slack Margin option can be used to request that Auto Fit apply sufficient optimization effort to achieve additional timing margin. Standard Fit will use maximum effort regardless of the design's requirements, leading to higher compilation time and more margin on easier designs. For difficult designs, Auto Fit and Standard Fit will both use maximum effort. Fast Fit will decrease optimization effort to reduce compilation time, which may degrade design performance.

### Type

Enumeration

### Values

- Auto Fit
- Fast Fit
- Standard Fit

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Stratix
- Stratix GX
- Stratix II

- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name FITTER_EFFORT <value>
```

### Default Value

Auto Fit

## FIT\_ATTEMPTS\_TO\_SKIP

Controls how many fit attempts the Fitter skips. In subsequent fit attempts, the Fitter uses higher effort to improve design routability at the expense of longer compilation times. Use this setting to force the Fitter directly into a second or third fit attempt, which will save time when it is known that multiple attempts are needed. This setting causes the same amount of additional effort to be applied but does not guarantee an identical result to what would be achieved if all fit attempts were performed. For some families, the Fitter will not perform a third fit attempt automatically due to the long compilation time and possible timing quality degradation. However, a third fit attempt can still be forced to run by setting this value to 2.

### Type

Integer

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### INTEGER\_RANGE

0, 0

### Notes

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name FIT_ATTEMPTS_TO_SKIP <value>
```

## Default Value

0.0

## FIT\_ONLY\_ONE\_ATTEMPT

Controls how many fitting attempts the fitter tries to get a fit. When this option is off (default), the fitter tries a maximum of 2 or 3 placement and routing attempts, with each successive attempt increasing the placement effort and hence increasing compilation times. These additional attempts are used only if previous attempts failed to fit the design. Setting this option restricts the fitter to using only the first of these attempts.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name FIT_ONLY_ONE_ATTEMPT <value>
```

### Default Value

Off

## FLEX10K\_CONFIGURATION\_SCHEME

The method used to load data into the device. Three configuration schemes are available: Passive Parallel Asynchronous (PPA); Passive Parallel Synchronous (PPS); and Passive Serial (PS).

### Type

Enumeration

### Values

- Passive Parallel Asynchronous
- Passive Parallel Synchronous
- Passive Serial

### Device Support

- A
- E

### Notes

None

### Syntax

```
set_global_assignment -name FLEX10K_CONFIGURATION_SCHEME <value>
```

### Default Value

Passive Serial

## FLEX10K\_DECREASE\_INPUT\_DELAY\_TO\_INTERNAL\_CELLS

Decreases the propagation delay from an input or bidirectional pin to logic and embedded cells within the device. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Old Name

Decrease Input Delay to Internal Cells -- FLEX 10KE/ACEX 1K

### Type

Enumeration

### Values

- Off
- On

### Device Support

E

### Notes

None

### Syntax

```
set_instance_assignment -name  
FLEX10K_DECREASE_INPUT_DELAY_TO_INTERNAL_CELLS -to <to> -entity <entity name>  
<value>
```



## FLEX10K\_DEVICE\_IO\_STANDARD

Specifies the default I/O standard to be used for pins on the target device.

### Type

String

### Device Support

- A
- E

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name FLEX10K_DEVICE_IO_STANDARD <value>
```

## FLEX10K\_ENABLE\_LOCK\_OUTPUT

Enables the lock output, which is available in devices with ClockLock phase-locked loop circuitry. The lock output monitors when the digital phase detector locks the input signal. The Enable LOCK output option is provided primarily for backward compatibility with MAX+PLUS II designs. Altera recommends using the MegaWizard Plug-In Manager to instantiate PLLs and to enable the LOCK output in new designs. This option is ignored if it is assigned to a device that does not have the PLL feature.

### Old Name

PLL lock, PLL\_LOCK

### Type

Boolean

### Device Support

- A
- E

### Notes

None

### Syntax

```
set_global_assignment -name FLEX10K_ENABLE_LOCK_OUTPUT <value>
```

### Default Value

Off

## FLEX10K\_MAX\_PERIPHERAL\_OE

Sets the limit on the number of peripheral OE buses that can be used.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name FLEX10K_MAX_PERIPHERAL_OE <value>
```

## FLEX6K\_CONFIGURATION\_SCHEME

The method used to load data into the device. Two configuration schemes are available: Passive Serial (PS) and Passive Serial Asynchronous (PSA).

### Old Name

CONFIGURATION\_SCHEME\_FLEX6K

### Type

Enumeration

### Values

- Passive Serial
- Passive Serial Asynchronous

### Notes

None

### Syntax

```
set_global_assignment -name FLEX6K_CONFIGURATION_SCHEME <value>
```

### Default Value

Passive Serial

## FLEX6K\_DECREASE\_INPUT\_DELAY\_TO\_INTERNAL\_CELLS

Decreases the propagation delay from an input or bidirectional pin to logic and embedded cells within the device. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Old Name

Decrease Input Delay to Internal Cells -- FLEX 6000

### Type

Enumeration

### Values

- Off
- On

### Notes

None

### Syntax

```
set_instance_assignment -name FLEX6K_DECREASE_INPUT_DELAY_TO_INTERNAL_CELLS  
-to <to> -entity <entity name> <value>
```

## FLEX6K\_DEVICE\_IO\_STANDARD

Specifies the default I/O standard to be used for pins on the target device.

### Type

String

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name FLEX6K_DEVICE_IO_STANDARD <value>
```

## FORCE\_CONFIGURATION\_VCCIO

Forces the VCCIO voltage of the configuration pins to be the same as the configuration device I/O voltage.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name FORCE_CONFIGURATION_VCCIO <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name FORCE_CONFIGURATION_VCCIO ON
```

**See Also**

CONFIGURATION\_VCCIO\_LEVEL





## FORCE\_FITTER\_TO\_AVOID\_PERIPHERY\_PLACEMENT\_WARNINGS

Directs the Fitter to treat periphery placement warnings as errors. As a result, the Fitter attempts to find a placement for the design that corrects these warnings. If the Fitter cannot fit the design, an error message is displayed instead of the original warning message.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name  
FORCE_FITTER_TO_AVOID_PERIPHERY_PLACEMENT_WARNINGS <value>
```

## Default Value

Off



## FORCE\_FRACTURED\_MODE\_ALM\_IMPLEMENTATION

Directs the fitter to implement the specified node using the fractured mode of the ALM. This assignment will only be applied to nodes with a specific location assignment.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

This assignment supports wildcards.

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name FORCE_FRACTURED_MODE_ALM_IMPLEMENTATION -to  
<to> -entity <entity name> <value>
```

## FORCE\_MERGE\_PLL

Forces the slave PLL to be merged with the master PLL. This option should be used only for two compatible PLLs driven by the same clock source.

### Type

Boolean

### Device Support

- Arria II GX
- Arria II GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix III
- Stratix IV

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_instance_assignment -name FORCE_MERGE_PLL -from <from> -to <to> -entity  
<entity name> <value>
```

## FORCE\_MERGE\_PLL\_FANOUTS

Forces the fanouts of the slave PLL clock output to be merged into the master PLL clock output. This option should be used only for static PLL clock outputs.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_instance_assignment -name FORCE_MERGE_PLL_FANOUTS -from <from> -to <to>  
-entity <entity name> <value>
```

## FORCE\_NON\_FRACTURED\_MODE\_ALM\_IMPLEMENTATION

Directs the fitter to implement the specified node using the non-fractured mode of the ALM. This assignment will only be applied to nodes with a specific location assignment.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

This assignment supports wildcards.

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name FORCE_NON_FRACTURED_MODE_ALM_IMPLEMENTATION -  
to <to> -entity <entity name> <value>
```

## FORM\_DDR\_CLUSTERING\_CLIQUE

Allows the Fitter to form cluster cliques on a specific DDR logic structure, which may lead to better placement result and improved performance of the design.

### Type

Boolean

### Device Support

- Arria V
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_global_assignment -name FORM_DDR_CLUSTERING_CLIQUE -entity <entity  
name> <value>  
set_instance_assignment -name FORM_DDR_CLUSTERING_CLIQUE -to <to> -entity  
<entity name> <value>  
set_global_assignment -name FORM_DDR_CLUSTERING_CLIQUE <value>
```

### Default Value

Off

## GENERATE\_GXB\_RECONFIG\_MIF

Generates a GXB reconfig MIF file for each used GXB Transmitter and Receiver channel pair (Stratix II GX and Arria GX) or each ALTGX Megafunction instance (Stratix IV, Arria II GX and Cyclone IV GX). Reprogramming using this MIF file reconfigures the GXB channel.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone IV GX
- HardCopy IV
- Stratix II GX
- Stratix IV

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name GENERATE_GXB_RECONFIG_MIF <value>
```

### Default Value

Off



## GENERATE\_GXB\_RECONFIG\_MIF\_WITH\_PLL

Generates a GXB reconfig MIF file with PLL data for each used GXB Transmitter and Receiver channel pair. Reprogramming using this MIF file reconfigures the entire GXB channel.

### Type

Boolean

### Device Support

Stratix II GX

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name GENERATE_GXB_RECONFIG_MIF_WITH_PLL <value>
```

### Default Value

Off

## GLOBAL\_SIGNAL

Specifies whether the signal should be routed using global routing paths. Global signals can be both pin- and logic-driven, and can be any signal in the design. Turning this option on for a pin or a single-output logic function signal is equivalent to feeding the signal through a GLOBAL buffer. Turning this option off for a particular signal will prevent any of the Auto Global options from using the signal as an automatic global signal.

### Type

Enumeration

### Values

- Dual-Fast Regional Clock
- Dual-Regional Clock
- Fast Regional Clock
- Global Clock
- Large Periphery Clock
- Off
- On
- Periphery Clock
- Regional Clock

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- EPC1
- EPC2
- Enhanced Configuration Devices
- A
- B
- E
- FLEX8000
- Flash Memory
- HardCopy II
- HardCopy III

- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- MAX9000
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V
- Virtual JTAG TAP

## Notes

This assignment supports wildcards.

This assignment supports Fitter wildcards.

## Syntax

```
set_instance_assignment -name GLOBAL_SIGNAL -to <to> -entity <entity name>
<value>
set_instance_assignment -name GLOBAL_SIGNAL -from <from> -to <to> -entity
<entity name> <value>
```

## GLOBAL\_SIGNAL\_CLKCTRL\_LOCATION

Specifies the CLKCTRL that the signal should be routed using global routing paths. The value to use is the same as that used for location assignments of Clock Control/Clock Enable Blocks.

### Type

String

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

This assignment supports wildcards.

This assignment is not copied when you create a companion revision for HardCopy II devices.

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name GLOBAL_SIGNAL_CLKCTRL_LOCATION -to <to> -  
entity <entity name> <value>  
set_instance_assignment -name GLOBAL_SIGNAL_CLKCTRL_LOCATION -from <from> -  
to <to> -entity <entity name> <value>
```



## GNDIO\_CURRENT\_1PT8V

For user to override GNDIO current of 1.8-V io standard. Original current is 2mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name GNDIO_CURRENT_1PT8V <value>
```

## GNDIO\_CURRENT\_2PT5V

For user to override GNDIO current of 2.5-V io standard. Original current is 2mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name GNDIO_CURRENT_2PT5V <value>
```



## GNDIO\_CURRENT\_GTL

For user to override GNDIO current of GTL. Not yet supported in MAX7000.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name GNDIO_CURRENT_GTL <value>
```

## GNDIO\_CURRENT\_GTL\_PLUS

For user to override GNDIO current of GTL+. Original current is 50mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name GNDIO_CURRENT_GTL_PLUS <value>
```



## GNDIO\_CURRENT\_LVCMOS

For user to override GNDIO current of LVCMOS. Original current is 2mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name GNDIO_CURRENT_LVCMOS <value>
```

## GNDIO\_CURRENT\_LVTTL

For user to override GNDIO current of LVTTL. Original current is 4mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name GNDIO_CURRENT_LVTTL <value>
```

## GNDIO\_CURRENT\_PCI

For user to override GNDIO current of PCI. Original current is 4mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name GNDIO_CURRENT_PCI <value>
```

## GNDIO\_CURRENT\_SSTL2\_CLASS1

For user to override GNDIO current of SSTL2\_CLASS1. Original current is 14mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name GNDIO_CURRENT_SSTL2_CLASS1 <value>
```



## GNDIO\_CURRENT\_SSTL2\_CLASS2

For user to override GNDIO current of SSTL2\_CLASS2. Original current is 21mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name GNDIO_CURRENT_SSTL2_CLASS2 <value>
```

## GNDIO\_CURRENT\_SSTL3\_CLASS1

For user to override GNDIO current of SSTL3\_CLASS1. Original current is 18mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name GNDIO_CURRENT_SSTL3_CLASS1 <value>
```



## GNDIO\_CURRENT\_SSTL3\_CLASS2

For user to override GNDIO current of SSTL3\_CLASS2. Original current is 25mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name GNDIO_CURRENT_SSTL3_CLASS2 <value>
```

## GUARANTEE\_MIN\_DELAY\_CORNER\_IO\_ZERO\_HOLD\_TIME

Controls whether the fitter tries to achieve a zero hold time for I/O pins that feed globally clocked registers at the fast corner and in stringent operating conditions even if a design does not contain timing assignments. When this option is set to On, the fitter preserves zero hold time for I/O pins feeding globally clocked registers at the fast corner and in stringent operating conditions. This setting may cause violations of tSU or tPD timing constraints. When this option is set to Off, the fitter optimizes a design to meet user timing assignments only. When this option is set to 'When Tsu and Tpd Constraints Permit', the fitter preserves zero hold time for I/O pins feeding globally clocked registers at the fast corner and in stringent operating conditions only if this can be done without violating tSU or tPD timing constraints. This option is useful for automatically meeting I/O hold time requirements in the fast corner without specifying any extra timing constraints.

### Type

Enumeration

### Values

- Off
- On
- When Tsu and Tpd Constraints Permit

### Device Support

- MAX II
- MAX V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name GUARANTEE_MIN_DELAY_CORNER_IO_ZERO_HOLD_TIME  
<value>
```

### Default Value

On



## GXB\_0PPM\_CLOCK\_GROUP

Specifies a group of GXB core clocks that have zero(0) PPM difference. The clock driver source specified in the GXB 0 PPM clock group driver must have a difference of 0 PPM compared with all clocks specified in the GXB 0 PPM clock group. You must connect the specified clock driver to all specified destinations in the GXB 0 PPM clock group. Do not reconfigure the GXB 0 PPM clock group driver differently from other clocks in the GXB 0 PPM clock group and disable the GXB 0 PPM clock group driver source when the destination GXB receiver or transmitter is listening to the signal. Follow the Altera High Speed I/O Applications Technical Support recommendations when using this assignment.

### Type

Integer

### Device Support

- Arria GX
- Stratix II GX

### Notes

This assignment supports Fitter wildcards.

This assignment supports synthesis wildcards.

### Syntax

```
set_instance_assignment -name GXB_0PPM_CLOCK_GROUP -to <to> -entity <entity  
name> <value>
```

## GXB\_0PPM\_CLOCK\_GROUP\_DRIVER

Specifies core clocks that have zero PPM difference. Follow the Altera High Speed I/O Applications Technical Support recommendations when using this assignment.

### Type

Integer

### Device Support

- Arria GX
- Stratix II GX

### Notes

This assignment supports Fitter wildcards.

This assignment supports synthesis wildcards.

### Syntax

```
set_instance_assignment -name GXB_0PPM_CLOCK_GROUP_DRIVER -to <to> -entity  
<entity name> <value>
```

## GXB\_0PPM\_CORECLK

Specifies core clocks that have zero PPM difference. Follow the Altera High Speed I/O Applications Technical Support recommendations when using this assignment.

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name GXB_0PPM_CORECLK -to <to> -entity <entity  
name> <value>
```

## GXB\_0PPM\_CORE\_CLOCK

Specifies two GXB core clocks that have zero (0) PPM difference. The core clock driver for the assignment source GXB must have a difference of 0 PPM compared with the core clock of the assignment destination GXB. Do not reconfigure the GXB 0 PPM clock group driver differently from other clocks it is 0 PPM-linked to and disable the GXB 0 PPM clock source when the destination GXB receiver or transmitter is listening to the signal. Follow the Altera High Speed I/O Applications Technical Support recommendations when using this assignment.

### Type

Boolean

### Device Support

- Arria II GX
- Arria II GZ
- Cyclone IV GX
- HardCopy IV
- Stratix IV

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name GXB_0PPM_CORE_CLOCK -from <from> -to <to> -  
entity <entity name> <value>
```

## GXB\_CLOCK\_GROUP

Specifies GXB core clock groups to be merged after compilation. All specified GXB transmitters in the GXB shared clock group are driven by the clock source specified in the GXB shared clock group driver. All clocks in the GXB shared clock group and GXB clock group driver must be configured in the same manner. When the destination GXB transmitter is listening to a signal such as `gxb_powerdown`, disable the GXB shared clock group driver source. Follow the Altera High Speed I/O Applications Technical Support recommendations when using this assignment.

### Type

Integer

### Device Support

- Arria GX
- Stratix II GX

### Notes

This assignment supports Fitter wildcards.

This assignment supports synthesis wildcards.

### Syntax

```
set_instance_assignment -name GXB_CLOCK_GROUP -to <to> -entity <entity  
name> <value>
```

## GXB\_CLOCK\_GROUP\_DRIVER

Specifies the GXB core clock driver that drives all core clocks in a GXB shared clock group after compilation. All GXB transmitters specified in the GXB shared clock group are driven by the clock source specified in the GXB shared clock group driver. Do not reconfigure the GXB shared clock group driver differently from other clocks in the GXB shared clock group and disable the GXB shared clock group driver source when the destination GXB transmitter is listening to the signal. Follow the Altera High Speed I/O Applications Technical Support recommendations when using this assignment.

### Type

Integer

### Device Support

- Arria GX
- Stratix II GX

### Notes

This assignment supports Fitter wildcards.

This assignment supports synthesis wildcards.

### Syntax

```
set_instance_assignment -name GXB_CLOCK_GROUP_DRIVER -to <to> -entity  
<entity name> <value>
```

## GXB\_RECONFIG\_GROUP

Specifies whether GXB transceiver channels with Dynamic Reconfiguration can be placed in the same physical channel. GXB receivers and transmitters are not placed into the same physical channel when Dynamic Reconfiguration setting is turned ON unless they are in the same reconfig group. GXB receivers and transmitters can be assigned to the same group if the following conditions are met: GXB receiver and transmitter will be dynamically reconfigured at the same time, and the GXB receiver and transmitter will be kept in reset until the dynamic reconfiguration of both is complete.

### Type

Integer

### Device Support

- Arria GX
- Stratix II GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name GXB_RECONFIG_GROUP -to <to> -entity <entity  
name> <value>
```

## GXB\_RECONFIG\_MIF

Specifies the MIF file name to store the GXB reconfig channel data for the entire GXB Receiver or Transmitter channel. This setting can be made on GXB Receiver datain or Transmitter dataout pins. Reprogramming using this MIF file reconfigures the entire GXB channel.

### Type

String

### Device Support

Stratix II GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name GXB_RECONFIG_MIF -to <to> -entity <entity  
name> <value>
```





## GXB\_RECONFIG\_MIF\_PLL

Includes PLL info in the GXB reconfig channel data.

### Type

Boolean

### Device Support

Stratix II GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name GXB_RECONFIG_MIF_PLL -to <to> -entity <entity  
name> <value>
```

## GXB\_REFCLK\_COUPLING\_TERMINATION\_SETTING

Allows the Compiler to configure the AC/DC coupling and on-chip termination (OCT) for a Stratix II GX gigabit transceiver block (GXB) REFCLK input pin. Use DC coupling external termination value only with the HCSL IO standard on the PCI-Express protocol. This option is ignored if it is applied to anything other than an input pin.

### Type

Enumeration

### Values

- DC coupling external termination
- OCT 100 Ohms
- Use as regular IO

### Device Support

- Arria GX
- Stratix II GX

### Notes

This assignment supports Fitter wildcards.

This assignment supports synthesis wildcards.

### Syntax

```
set_instance_assignment -name GXB_REFCLK_COUPLING_TERMINATION_SETTING -to  
<to> -entity <entity name> <value>
```

## GXB\_RESERVED\_TRANSMIT\_CHANNEL

Specifies that a transmitter channel is a reserved transmit channel.

### Type

Boolean

### Device Support

- Arria V
- Cyclone V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name GXB_RESERVED_TRANSMIT_CHANNEL -to <to> -  
entity <entity name> <value>
```

## GXB\_TX\_PLL\_RECONFIG\_GROUP

Specifies whether GXB transceiver channels with Dynamic TX PLL Reconfiguration can be placed in the same physical GXB Quad. If the GXB transceivers have 2 dynamically reconfigured TX PLLs, the GXB transceivers are not placed into the same physical Quad when Dynamic TX PLL Reconfiguration setting is turned ON unless they are in the same TX PLL reconfig group. If the GXB transceivers have 1 dynamically reconfigured TX PLLs, GXB transceivers from 2 TX PLL reconfig groups can be placed into the same physical Quad if the logical number on the TX PLLs are different. GXB transceivers can be assigned to the same group if the following conditions are met: (1) GXB transmitters in the same group can only listen to 2 TX PLLs at one time, (2) the user must maintain proper data rates on TX PLLs according to Altera user guidelines, (3) the user must wait for pll\_locked signal asserted for dynamic PLL reconfiguration completion, and the GXB receiver and transmitter will be kept in reset until the dynamic reconfiguration of both is complete.

### Type

Integer

### Device Support

- Arria II GX
- Arria II GZ
- HardCopy IV
- Stratix II GX
- Stratix IV

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name GXB_TX_PLL_RECONFIG_GROUP -to <to> -entity  
<entity name> <value>
```



## HPS\_IO

Flags an I/O in the user netlist as one that is intended to be owned by a HPS block.

### Type

Boolean

### Device Support

- Arria V
- Cyclone V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name HPS_IO -to <to> -entity <entity name> <value>
```

### Example

```
set_instance_assignment -name HPS_IO ON -to output_pin
```

## IGNORE\_HSSI\_COLUMN\_POWER\_WHEN\_PRESERVING\_UNUSED\_XCVR\_CHANNELS

Ignore the power supply of HSSI column when preserving unused RX/TX channels. By default, any unused RX/TX channels in each HSSI column will be preserved

### Type

Boolean

### Device Support

Arria 10

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name  
IGNORE_HSSI_COLUMN_POWER_WHEN_PRESERVING_UNUSED_XCVR_CHANNELS <value>
```

### Default Value

On

### Example

```
set_global_assignment -name  
IGNORE_HSSI_COLUMN_POWER_WHEN_PRESERVING_UNUSED_XCVR_CHANNELS OFF
```

## IGNORE\_MODE\_FOR\_MERGE

Ignores the mode of the PLL when the Fitter attempts to merge PLLs, therefore allowing PLLs with different modes to be merged.

### Type

Boolean

### Device Support

Cyclone II

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name IGNORE_MODE_FOR_MERGE <value>  
set_global_assignment -name IGNORE_MODE_FOR_MERGE -entity <entity name>  
<value>  
set_instance_assignment -name IGNORE_MODE_FOR_MERGE -to <to> -entity  
<entity name> <value>
```

### Default Value

Off

## IMPLEMENT\_MLAB\_IN\_16\_BIT\_DEEP\_MODE

Allows you to specify the MLAB memory blocks implementation mode. MLAB memory blocks are implemented in 32-bit deep mode or 64-bit deep mode. Turning on this option forces MLAB memory blocks to be implemented in 16-bit deep mode. This leads to significantly shorter delays and may speed up the overall design performance if the MLAB memory block is on the critical path. However, it also requires twice as many MLAB blocks to implement a given logical memory.

### Type

Boolean

### Device Support

- Arria V GZ
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name IMPLEMENT_MLAB_IN_16_BIT_DEEP_MODE -entity  
<entity name> <value>  
set_instance_assignment -name IMPLEMENT_MLAB_IN_16_BIT_DEEP_MODE -to <to> -  
entity <entity name> <value>  
set_global_assignment -name IMPLEMENT_MLAB_IN_16_BIT_DEEP_MODE <value>
```

### Default Value

Off



## INCREASE\_DELAY\_TO\_OUTPUT\_ENABLE\_PIN

Increases the propagation delay to the output enable pin from internal logic or the output enable register implemented in an I/O cell. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an output enable pin.

### Type

Enumeration

### Values

- Off
- On

### Device Support

- Mercury
- Stratix
- Stratix GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name INCREASE_DELAY_TO_OUTPUT_ENABLE_PIN -to <to> -  
entity <entity name> <value>
```

## INCREASE\_DELAY\_TO\_OUTPUT\_PIN

Increases the propagation delay to the output or bidirectional pin from the output register implemented in an I/O cell. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is off by default. This option is ignored if it is applied to anything other than an output or bidirectional pin.

### Type

Enumeration

### Values

- Off
- On

### Device Support

- Cyclone
- Mercury
- Stratix
- Stratix GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name INCREASE_DELAY_TO_OUTPUT_PIN -to <to> -entity  
<entity name> <value>
```

## INCREASE\_INPUT\_CLOCK\_ENABLE\_DELAY

Increases the propagation delay from the interior of the device to the clock enable input of an output register. This is an advanced option that should be used only after you compile a project, check the I/O timing, and determine that the timing is unsatisfactory. This option is ignored if it is applied to anything other than an I/O cell that has an input register with a clock enable signal. For detailed information on how to use this option, refer to the data sheet for the device family, which is available from the Literature section of the Altera web site.

### Type

Enumeration

### Values

- Large
- Off
- On
- Small

### Device Support

- Stratix
- Stratix GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name INCREASE_INPUT_CLOCK_ENABLE_DELAY -to <to> -  
entity <entity name> <value>
```

## INCREASE\_INPUT\_DELAY\_TO\_CE\_IO\_REGISTER

Increases the propagation delay from the interior of the device to the clock enable input of an I/O register. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an I/O cell that has a register that has a clock enable signal.

### Type

Enumeration

### Values

- Large
- Off
- On
- Small

### Notes

None

### Syntax

```
set_instance_assignment -name INCREASE_INPUT_DELAY_TO_CE_IO_REGISTER -to  
<to> -entity <entity name> <value>
```

## INCREASE\_OUTPUT\_CLOCK\_ENABLE\_DELAY

Increases the propagation delay from the interior of the device to the clock enable input of an output register. This is an advanced option that should be used only after you compile a project, check the I/O timing, and determine that the timing is unsatisfactory. This option is ignored if it is applied to anything other than an I/O cell that has an output register with a clock enable signal. For detailed information on how to use this option, refer to the data sheet for the device family, which is available from the Literature section of the Altera web site.

### Type

Enumeration

### Values

- Large
- Off
- On
- Small

### Device Support

- Stratix
- Stratix GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name INCREASE_OUTPUT_CLOCK_ENABLE_DELAY -to <to> -  
entity <entity name> <value>
```

## INCREASE\_OUTPUT\_ENABLE\_CLOCK\_ENABLE\_DELAY

Increases the propagation delay from the interior of the device to the clock enable input of an output enable register. This is an advanced option that should be used only after you compile a project, check the I/O timing, and determine that the timing is unsatisfactory. This option is ignored if it is applied to anything other than an I/O cell that has an output enable register with a clock enable signal. For detailed information on how to use this option, refer to the data sheet for the device family, which is available from the Literature section of the Altera web site.

### Old Name

INCREASE\_OUTPUT\_ENABLE\_CLOCK\_ENABLE\_DELAYR

### Type

Enumeration

### Values

- Large
- Off
- On
- Small

### Device Support

- Stratix
- Stratix GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name INCREASE_OUTPUT_ENABLE_CLOCK_ENABLE_DELAY -to  
<to> -entity <entity name> <value>
```



## INCREASE\_TZX\_DELAY\_TO\_OUTPUT\_PIN

Supports zero bus-turnaround (ZBT) by increasing the propagation delay of the falling edge of the output enable signal. This option allows a device to quickly release control and slowly take control of a bus. Turning the Increase tzx Delay to Output Pin option on prevents bus contention between ZBT SRAM devices. This option is ignored if it is applied to anything other than an output or bidirectional pin.

### Old Name

ZBT\_OE\_FALLING\_EDGE\_DELAY

### Type

Enumeration

### Values

- Off
- On

### Device Support

- Mercury
- Stratix
- Stratix GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name INCREASE_TZX_DELAY_TO_OUTPUT_PIN -to <to> -  
entity <entity name> <value>
```

## INC\_PLC\_MODE

Directs the Quartus Prime software to run in Incremental Placement Mode.

### Type

Boolean

### Device Support

- Cyclone
- MAX II
- MAX V
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name INC_PLC_MODE <value>
```





## INIT\_DONE\_OPEN\_DRAIN

Specify open drain on the INIT\_DONE pin should be enabled or not

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name INIT_DONE_OPEN_DRAIN <value>
```

### Default Value

On

### Example

```
set_global_assignment -name init_done_open_drain on  
set_global_assignment -name init_done_open_drain off
```

### See Also

ENABLE\_INIT\_DONE\_OUTPUT

## INPUT\_DELAY\_CHAIN

Specifies the propagation delay for Input Delay Chain. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Old Name

INPUT\_DELAY

### Type

Integer

### Device Support

- Arria 10

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name INPUT_DELAY_CHAIN -to <to> -entity <entity  
name> <value>  
set_instance_assignment -name INPUT_DELAY_CHAIN -from <from> -to <to> -  
entity <entity name> <value>
```

## INPUT\_REFERENCE

Allows you to specify the VREF pin for the I/O standard being used by an I/O pin. This option is ignored if it is applied to anything other than the I/O standard being used by an I/O pin.

### Type

Enumeration

### Values

- As VREFA
- As VREFB
- Off

### Device Support

MAX7000B

### Notes

None

### Syntax

```
set_instance_assignment -name INPUT_REFERENCE -to <to> -entity <entity  
name> <value>
```

## INPUT\_TERMINATION

Allows the Compiler to configure the on-chip termination (OCT) and impedance matching for an I/O pin. OCT helps to prevent signal reflections and maintain signal integrity. This option is ignored if it is applied to anything other than an I/O pad, input buffer, or output buffer.

### Type

String

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name INPUT_TERMINATION -to <to> -entity <entity  
name> <value>
```

### Example

```
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH  
CALIBRATION" -to pin_name
```

### See Also

IO\_STANDARD OCT\_CONTROL\_BLOCK OUTPUT\_OCT\_VALUE

## INSERT\_ADDITIONAL\_LOGIC\_CELL

Allows the Compiler to insert an additional logic cell after the output(s) of the logic function to which it is applied, provided that the function is implemented as one logic cell. This option allows you to insert logic cells for routing purposes without adding LCELL primitives to the design. If this option is applied to a mega- or macrofunction, it operates on all outputs of the function. This option is ignored if it is applied to a logic function that is not already implemented in a macrocell(s). For example, if it is applied to an AND gate, it does not force the AND gate to be the output of a logic cell.

### Type

Boolean

### Device Support

- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S

### Notes

None

### Syntax

```
set_instance_assignment -name INSERT_ADDITIONAL_LOGIC_CELL -to <to> -entity  
<entity name> <value>
```

## INTERNAL\_FLASH\_UPDATE\_MODE

Specifies the configuration mode used with the configuration scheme for configuring the device.

### Type

Enumeration

### Values

- Dual Images
- Single Comp Image
- Single Comp Image with ERAM
- Single Image
- Single Image with ERAM

### Device Support

MAX 10

### Notes

None

### Syntax

```
set_global_assignment -name INTERNAL_FLASH_UPDATE_MODE <value>
```

### Default Value

Single Image

### Example

```
set_global_assignment -name INTERNAL_FLASH_UPDATE_MODE "Standard"
```

## INTERNAL\_SCRUBBING

Specifies internal scrubbing usage for the selected device. If internal scrubbing is turned on, the device corrects single error or double adjacent error within the core configuration memory while the device is still running.

### Type

Boolean

### Device Support

- Arria 10
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name INTERNAL_SCRUBBING <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name INTERNAL_SCRUBBING ON
```

## IO\_12\_LANE\_INPUT\_DATA\_DELAY\_CHAIN

Specifies the propagation delay for IO\_12\_LANE Input Data Delay Chain. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Old Name

IO\_12\_LANE\_INPUT\_DATA\_DELAY

### Type

Integer

### Device Support

- Arria 10

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name IO_12_LANE_INPUT_DATA_DELAY_CHAIN -to <to> -  
entity <entity name> <value>  
set_instance_assignment -name IO_12_LANE_INPUT_DATA_DELAY_CHAIN -from  
<from> -to <to> -entity <entity name> <value>
```





## IO\_12\_LANE\_INPUT\_STROBE\_DELAY\_CHAIN

Specifies the propagation delay for IO\_12\_LANE Input Strobe Delay Chain. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Old Name

IO\_12\_LANE\_INPUT\_STROBE\_DELAY

### Type

Integer

### Device Support

- Arria 10

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name IO_12_LANE_INPUT_STROBE_DELAY_CHAIN -to <to> -  
entity <entity name> <value>  
set_instance_assignment -name IO_12_LANE_INPUT_STROBE_DELAY_CHAIN -from  
<from> -to <to> -entity <entity name> <value>
```

## IO\_MAXIMUM\_TOGGLE\_RATE

Specifies the toggle rate of this node. You can specify the desired frequency setting. This option is ignored if it is applied to anything other than pins. This option can be used to direct the Fitter in its toggle-rate checking while allowing a single-ended pin to be placed closer to a differential pin. This assignment is used to analyze signal integrity under worst case conditions (highest possible toggle rate). A different assignment, Power Toggle Rate, is used to specify the expected time-averaged toggle rate rather than worst-case toggle rate, and is used by the Power Analyzer to estimate time-averaged power consumption. Use the Synchronizer Toggle Rate if you want to configure the data rates used for Metastability Reporting in the TimeQuest Timing Analyzer.

### Old Name

TOGGLE RATE, TOGGLE\_RATE

### Type

Frequency

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

## Notes

This assignment supports Fitter wildcards.

## Syntax

```
set_instance_assignment -name IO_MAXIMUM_TOGGLE_RATE -to <to> -entity  
<entity name> <value>
```

## IO\_PLACEMENT\_OPTIMIZATION

Specifies whether the Fitter optimizes the location of IOs that do not already have pin locations assigned to them. Performing IO placement optimizations may improve IO timing, fmax, and fitting, but may also require longer compilation time.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name IO_PLACEMENT_OPTIMIZATION <value>
```

Default Value

On

## IO\_STANDARD

Specifies the I/O standard of a pin. Different device families support different I/O standards, and restrictions apply to placing pins with different I/O standards together. For detailed information, refer to the device family data sheet and to Application Note 117 (Using Selectable I/O Standards in Altera Devices). This option is ignored if it is applied to anything other than a pin or a top-level design entity.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX7000B
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment supports synthesis wildcards.

## Syntax

```
<value> set_instance_assignment -name IO_STANDARD -to <to> -entity <entity name>
```

## Example

```
set_instance_assignment -name IO_STANDARD LVDS -to pin
```

## See Also

STRATIX\_DEVICE\_IO\_STANDARD CURRENT\_STRENGTH\_NEW SLEW\_RATE  
OUTPUT\_TERMINATION INPUT\_TERMINATION PROGRAMMABLE\_PREEMPHASIS  
PROGRAMMABLE\_VOD

## LVDS\_DIRECT\_LOOPBACK\_MODE

Enable the LVDS Direct Loop Mode on a True Differential output pin. This assignment should only apply from an input pin to an output pin and both of them should have True Differential I/O standard. When this feature is enabled, data coming in from the adjacent RX pair gets looped back to the TX pair. This feature can be used to verify the Tx and Rx buffer by checking the data transmit and received. This option is ignored if it is applied to anything other than a pin or a top-level design entity.

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_instance_assignment -name LVDS_DIRECT_LOOPBACK_MODE -from <from> -to  
<to> -entity <entity name> <value>
```

### Example

```
set_instance_assignment -name LVDS_DIRECT_LOOPBACK_MODE ON -from  
true_diff_in_pin_p -to true_diff_out_pin_p
```

### See Also

IO\_STANDARD



## LVDS\_RX\_REGISTER

Directs the Compiler to perform special placement and routing of the specified register for LVDS receiver interfaces

### Type

Enumeration

### Values

- High
- Low
- Off

### Device Support

- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- MAX 10

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name LVDS_RX_REGISTER -to <to> -entity <entity  
name> <value>
```

## M144K\_BLOCK\_READ\_CLOCK\_DUTY\_CYCLE\_DEPENDENCY

Allows you to specify whether the M144K memory block read operations depend upon the read clock's duty cycle. When M144K memory blocks are driven by a read clock with a very narrow pulse, they can go into a locked, inactive state. Turning on this option allows the M144K memory blocks to operate dependent upon the read clock's duty cycle to prevent the memory blocks from going into an inactive state; however, turning on this option may degrade the performance of the M144K blocks.

### Type

Enumeration

### Values

- Off
- On

### Device Support

- Arria II GZ
- HardCopy IV
- Stratix IV

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name M144K_BLOCK_READ_CLOCK_DUTY_CYCLE_DEPENDENCY -  
entity <entity name> <value>  
set_instance_assignment -name M144K_BLOCK_READ_CLOCK_DUTY_CYCLE_DEPENDENCY -  
to <to> -entity <entity name> <value>  
set_global_assignment -name M144K_BLOCK_READ_CLOCK_DUTY_CYCLE_DEPENDENCY  
<value>
```

### Default Value

Off

## MACRO\_HEAD

Specifies the head block of a macro.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
<value> set_instance_assignment -name MACRO_HEAD -to <to> -entity <entity name>
```

## MACRO\_MEMBER

Specifies a block to be placed with respect to its macro head.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name MACRO_MEMBER -entity <entity name> <value>
set_instance_assignment -name MACRO_MEMBER -to <to> -entity <entity name>
<value>
set_instance_assignment -name MACRO_MEMBER -from <from> -to <to> -entity
<entity name> <value>
```

## MATCH\_PLL\_COMPENSATION\_CLOCK

Allows you to specify a PLL output clock feeding a clock network as a compensation target for a PLL in NORMAL or SOURCE\_SYNCHRONOUS mode. This configures the PLL to match its feedback path to the target's clock network. This option is ignored if it is applied to anything other than a PLL output clock.

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_instance_assignment -name MATCH_PLL_COMPENSATION_CLOCK -to <to> -entity  
<entity name> <value>
```

## MAX10FPGA\_CONFIGURATION\_SCHEME

The method used to load a design into the device. Only one configuration scheme is available: Internal Configuration (use internal flash).

### Type

Enumeration

### Values

- Active Serial
- Internal Configuration

### Device Support

MAX 10

### Notes

None

### Syntax

```
set_global_assignment -name MAX10FPGA_CONFIGURATION_SCHEME <value>
```

### Default Value

Internal Configuration

### Example

```
set_global_assignment -name MAX10FPGA_CONFIGURATION_SCHEME "Active Serial"
```

### See Also

UPDATE\_MODE\_INTERNAL\_FLASH

## MAX7000B\_VCCIO\_IOBANK1

Specifies the default I/O Bank1 Voltage to be used for pins on the target device.

### Type

String

### Device Support

MAX7000B

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name MAX7000B_VCCIO_IOBANK1 <value>
```

## MAX7000B\_VCCIO\_IOBANK2

Specifies the default I/O Bank2 Voltage to be used for pins on the target device.

### Type

String

### Device Support

MAX7000B

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name MAX7000B_VCCIO_IOBANK2 <value>
```





## MAX7000\_DEVICE\_IO\_STANDARD

Specifies the default I/O standard to be used for pins on the target device.

### Type

String

### Device Support

- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name MAX7000_DEVICE_IO_STANDARD <value>
```

## MAX7000\_ENABLE\_JTAG\_BST\_SUPPORT

Enables JTAG boundary-scan test (BST) support.

### Type

Boolean

### Device Support

- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S

### Notes

None

### Syntax

```
set_global_assignment -name MAX7000_ENABLE_JTAG_BST_SUPPORT <value>
```

### Default Value

On



## MAX7000\_INDIVIDUAL\_TURBO\_BIT

Controls the speed vs. power usage trade-off for a macrocell. If the Turbo Bit is on, the macrocell's speed increases; if it is off, its power consumption decreases.

### Old Name

Turbo Bit -- MAX 7000B/7000AE/3000A/7000S/7000A

### Type

Boolean

### Device Support

- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name MAX7000_INDIVIDUAL_TURBO_BIT -entity <entity  
name> <value>  
set_instance_assignment -name MAX7000_INDIVIDUAL_TURBO_BIT -to <to> -entity  
<entity name> <value>
```

## MAX\_CLOCKS\_ALLOWED

Specifies the maximum number of clocks of any type (e.g. global clock, regional clock) that can be used by the design. A value of -1 means that the fitter can use all the clocks supported by the device.

### Type

Integer

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V GZ
- HardCopy II
- HardCopy III
- HardCopy IV
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name MAX_CLOCKS_ALLOWED <value>
```

### Default Value

-1 (Unlimited)

## MAX\_CONSECUTIVE\_OUTPUTS\_FOR\_ELECTROMIGRATION

Specifies the number of consecutive horizontal output or bidirectional pins considered in the current-density computation for electromigration when the Fitter checks for electromigration violations.

### Type

Integer

### Device Support

- Arria GX
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name MAX_CONSECUTIVE_OUTPUTS_FOR_ELECTROMIGRATION  
<value>
```

## MAX\_CONSECUTIVE\_VIO\_OUTPUTS\_FOR\_ELECTROMIGRATION

Specifies the number of consecutive vertical output or bidirectional pins considered in the current-density computation for electromigration when the Fitter checks for electromigration violations.

### Type

Integer

### Device Support

- Arria GX
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name MAX_CONSECUTIVE_VIO_OUTPUTS_FOR_ELECTROMIGRATION <value>
```

## MAX\_CURRENT\_FOR\_ELECTROMIGRATION

Specifies the maximum amount of DC current, in mA, allowed on horizontal output or bidirectional pins when the Fitter checks for electromigration violations.

### Type

Integer

### Device Support

- Arria GX
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name MAX_CURRENT_FOR_ELECTROMIGRATION <value>
```

## MAX\_CURRENT\_FOR\_VIO\_ELECTROMIGRATION

Specifies the maximum amount of DC current, in mA, allowed on vertical output or bidirectional pins when the Fitter checks for electromigration violations.

### Type

Integer

### Device Support

- Arria GX
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name MAX_CURRENT_FOR_VIO_ELECTROMIGRATION <value>
```



## MAX\_GLOBAL\_CLOCKS\_ALLOWED

Specifies the maximum number of global clocks that can be used by the design. A value of -1 means that the fitter can use all the global clocks supported by the device.

### Type

Integer

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name MAX_GLOBAL_CLOCKS_ALLOWED <value>
```

### Default Value

-1 (Unlimited)

## MAX\_PERIPHERY\_CLOCKS\_ALLOWED

Specifies the maximum number of periphery clocks that can be used by the design. A value of -1 means that the fitter can use all the periphery clocks supported by the device.

### Type

Integer

### Device Support

- Arria II GX
- Arria II GZ
- Arria V GZ
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name MAX_PERIPHERY_CLOCKS_ALLOWED <value>
```

### Default Value

-1 (Unlimited)

## MAX\_REGIONAL\_CLOCKS\_ALLOWED

Specifies the maximum number of regional clocks that can be used by the design. A value of -1 means that the fitter can use all the regional clocks supported by the device.

### Type

Integer

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V GZ
- HardCopy II
- HardCopy III
- HardCopy IV
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name MAX_REGIONAL_CLOCKS_ALLOWED <value>
```

### Default Value

-1 (Unlimited)

## MEMORY\_INTERFACE\_DATA\_PIN\_GROUP

Specifies the group width (4, 9, 18, or 36), and associates a pin with another pin. Turning on this option allows the Fitter to view the pins as part of the same memory interface pin group. I/O pins of this pin group must be placed in the DQ pin locations of a single DQS group. This option is ignored if is assigned to anything other than an I/O pad, input buffer, or output buffer.

### Type

Integer

### Device Support

- Arria II GX
- Arria II GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name MEMORY_INTERFACE_DATA_PIN_GROUP -from <from> -  
to <to> -entity <entity name> <value>
```

### Example

```
set_instance_assignment -name MEMORY_INTERFACE_DATA_PIN_GROUP 4 -from  
mem_clk[0] -to mem_clk_n[0]
```

### See Also

DQSB\_DQS\_PAIR DQ\_GROUP

## MEM\_INTERFACE\_DELAY\_CHAIN\_CONFIG

Changes Quartus Prime Fitter behavior regarding delay chain configurations on memory interface pins. This option is ignored if is assigned to anything other than an I/O pad, input buffer, or output buffer.

### Type

Enumeration

### Values

- Fitter\_optimized
- Flexible\_timing
- Macro\_timing

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name MEM_INTERFACE_DELAY_CHAIN_CONFIG -to <to> -  
entity <entity name> <value>
```

## MERCURY\_CONFIGURATION\_SCHEME

The method used to load data into the device. Three configuration schemes are available: Passive Parallel Asynchronous (PPA); Passive Parallel Synchronous (PPS); and Passive Serial (PS).

### Old Name

CONFIGURATION\_SCHEME\_DALI

### Type

Enumeration

### Values

- Passive Parallel Asynchronous
- Passive Parallel Synchronous
- Passive Serial

### Device Support

Mercury

### Notes

None

### Syntax

```
set_global_assignment -name MERCURY_CONFIGURATION_SCHEME <value>
```

### Default Value

Passive Serial

## MERCURY\_DECREASE\_INPUT\_DELAY\_TO\_INTERNAL\_CELLS

Decreases the propagation delay from an input or bidirectional pin to logic and embedded cells within the device. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Old Name

Decrease Input Delay to Internal Cells -- Mercury

### Type

Enumeration

### Values

- Large
- Medium
- Off
- On
- Small

### Device Support

Mercury

### Notes

None

### Syntax

```
set_instance_assignment -name  
MERCURY_DECREASE_INPUT_DELAY_TO_INTERNAL_CELLS -to <to> -entity <entity name>  
<value>
```

## MERCURY\_DEVICE\_IO\_STANDARD

Specifies the default I/O standard to be used for pins on the target device.

### Type

String

### Device Support

Mercury

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name MERCURY_DEVICE_IO_STANDARD <value>
```





## MERGE\_TX\_PLL\_DRIVEN\_BY\_REGISTERS\_WITH\_SAME\_CLEAR

Allows merging of HSSI TX PLLs if their reset input are driven by registers that have the same asynchronous clear input.

### Type

Boolean

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_instance_assignment -name  
MERGE_TX_PLL_DRIVEN_BY_REGISTERS_WITH_SAME_CLEAR -to <to> -entity <entity name>  
<value>
```

## MIGRATION\_CONSTRAIN\_CORE\_RESOURCES

Limits the compiler to using only those core resources which are also available in the target migration device

### Type

Boolean

### Device Support

- Arria GX
- HardCopy II
- HardCopy III
- HardCopy IV
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name MIGRATION_CONSTRAIN_CORE_RESOURCES <value>
```

### Default Value

On

## MIGRATION\_DEVICES

Shows the selected migration devices for the target device.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name MIGRATION_DEVICES <value>
```

## NCEO\_OPEN\_DRAIN

Specify open drain on the nCEO pin should be enabled or not

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name NCEO_OPEN_DRAIN <value>
```

### Default Value

On

### Example

```
set_global_assignment -name nceo_open_drain on  
set_global_assignment -name nceo_open_drain off
```

### See Also

ENABLE\_NCEO\_OUTPUT

## NDQS\_LOCAL\_CLOCK\_DELAY\_CHAIN

Set the propagation delay on the NDQS signal to the input register of the target pin. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than a DQ or DQS pin.

### Type

Integer

### Device Support

- Arria GX
- Arria II GX
- HardCopy II
- Stratix II
- Stratix II GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name NDQS_LOCAL_CLOCK_DELAY_CHAIN -to <to> -entity  
<entity name> <value>
```

## NORMAL\_LCELL\_INSERT

Directs the Fitter to enable or disable logic cell insertion when the logic cells are not part of a carry or cascade chain. When this option is turned on, the Fitter inserts logic cells where they are needed to improve fitting. When this option is turned off, the Fitter inserts logic cells only to solve deterministic no fits.

### Type

Boolean

### Device Support

- A
- E

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name NORMAL_LCELL_INSERT <value>
set_global_assignment -name NORMAL_LCELL_INSERT -entity <entity name>
<value>
set_instance_assignment -name NORMAL_LCELL_INSERT -to <to> -entity <entity
name> <value>
```

### Default Value

On

## OE\_DELAY\_CHAIN

Specifies the propagation delay for Output Enable Delay Chain. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an output or bidirectional pin.

### Old Name

OE\_DELAY

### Type

Integer

### Device Support

- Arria 10

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name OE_DELAY_CHAIN -to <to> -entity <entity name>
```

## OPTIMIZE\_FOR\_METASTABILITY

This setting improves the reliability of the design by increasing its Mean Time Between Failures (MTBF). When this setting is enabled, the Fitter will aim to increase the output setup slacks of synchronizer registers in the design, which can exponentially increase the design MTBF. This option takes effect only if TimeQuest is being used for timing-driven compilation. Use the TimeQuest `report_metastability` command to review the synchronizers detected in your design and to produce MTBF estimates.

### Type

Enumeration

### Values

- Off
- On

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name OPTIMIZE_FOR_METASTABILITY <value>
```

### Default Value

On



## OPTIMIZE\_HOLD\_TIMING

Allows the Fitter to optimize hold time by adding delay to the appropriate paths. The Optimize Timing option must be turned on in order for this option to work. If you are using the TimeQuest Timing Analyzer, and specify the I/O paths and Minimum tpd Paths setting, all assignments involving I/O pins are optimized. Specifying the All Paths setting directs the Fitter to optimize the hold time of all paths. Turning off this option directs the Fitter not to optimize the hold time of any paths.

### Type

Enumeration

### Values

- All Paths
- IO Paths and Minimum TPD Paths
- Off

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name OPTIMIZE_HOLD_TIMING <value>
```



## OPTIMIZE\_IOC\_REGISTER\_PLACEMENT\_FOR\_TIMING

Controls whether the fitter optimizes I/O pin timing by automatically packing registers into I/Os to minimize I/O -> register and register -> I/O delays. When the 'Normal' option is enabled, the Fitter will opportunistically pack registers into I/Os that should improve I/O timing. When 'Pack All I/O Registers' is enabled, the fitter will aggressively try to pack any registers connected to input, output or output enable pins into I/Os unless prevented by user constraints or other legality restrictions. By default, this option is set to 'Normal'. This option requires the Optimize Timing option to be enabled for it to work.

### Type

Enumeration

### Values

- Normal
- Off
- Pack All IO Registers

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
<value> set_global_assignment -name OPTIMIZE_IOC_REGISTER_PLACEMENT_FOR_TIMING
```

### Default Value

Normal

## OPTIMIZE\_MULTI\_CORNER\_TIMING

Controls whether the Fitter optimizes a design to meet timing requirements at all process corners and operating conditions. The Optimize Timing logic option must be enabled for this option to work. When this setting is turned off, designs are optimized to meet timing only at the slow timing process corner and operating condition. When this option is turned on, designs are optimized to meet timing at all corners and operating conditions; as a result, turning on this option helps create a design implementation that is more robust across process, temperature, and voltage variations. Turning on this option does not enable multi-corner timing analysis. To enable multi-corner timing analysis, see the TimeQuest Timing Analyzer page of the Settings dialog box.

### Old Name

OPTIMIZE\_FAST\_CORNER\_TIMING, Optimize Fast-Corner Timing

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- EPC1
- EPC2
- Enhanced Configuration Devices
- A
- B
- E
- FLEX8000
- Flash Memory
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A



- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- MAX9000
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V
- Virtual JTAG TAP

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name OPTIMIZE_MULTI_CORNER_TIMING <value>
```

## OPTIMIZE\_POWER\_DURING\_FITTING

Controls the power-driven compilation setting of the Fitter. This option determines how aggressively the Fitter optimizes the design for power. If this option is set to 'Off', the Fitter does not perform any power optimizations. If this option is set to 'Normal compilation', the Fitter performs power optimizations which should not impact design performance or increase compile time. When this option is set to 'Extra effort', the Fitter will perform additional power optimizations which may affect design performance and/or increase compile time. For the best results with Extra Effort power optimization during fitting, you should specify a Signal Activity File (SAF file) that lists the toggle rate of each signal in the design. To generate the most accurate Signal Activity File (SAF file) use a gate-level simulation, with glitch filtering, of the compiled design. Specify this SAF file as an input to the Power Analyzer in the PowerPlay Power Analysis Settings, and recompile the design with Extra Effort PowerPlay Power Optimization during fitting. The signal activities (toggle rates) in the SAF file help guide the fitter to reduce power.

### Type

Enumeration

### Values

- Extra effort
- Normal compilation
- Off

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V



## Notes

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name OPTIMIZE_POWER_DURING_FITTING <value>
set_global_assignment -name OPTIMIZE_POWER_DURING_FITTING -entity <entity
name> <value>
set_instance_assignment -name OPTIMIZE_POWER_DURING_FITTING -to <to> -
entity <entity name> <value>
```

## Default Value

Normal compilation

## OPTIMIZE\_SSN

Controls the Simultaneous Switching Noise (SSN) optimization setting of the Fitter. This option determines how aggressively the Fitter optimizes the design for SSN. If this option is set to 'Off', the Fitter does not perform any SSN optimizations. If this option is set to 'Normal compilation', the Fitter performs SSN optimizations which should not impact design performance. When this option is set to 'Extra effort', the Fitter will perform aggressive SSN optimizations which may affect design performance.

### Old Name

OPTIMIZE\_SIGNAL\_INTEGRITY

### Type

Enumeration

### Values

- Extra effort
- Normal compilation
- Off

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name OPTIMIZE_SSN <value>
```





**Default Value**  
Off

## OPTIMIZE\_TIMING

Controls whether the Fitter optimizes to meet the maximum delay timing requirements (for example, clock cycle time). By default, this option is set to Normal compilation. Turning it off can help fit designs that have extremely high interconnect requirements and can also reduce compilation time, although at the expense of significant timing performance (since the fitter will be ignoring the design's timing requirements). If this option is off, other fitter timing optimization options have no effect (such as Optimize Hold Timing).

### Old Name

OPTIMIZE\_INTERNAL\_TIMING, USE\_TIMING\_DRIVEN\_COMPILATION

### Type

Enumeration

### Values

- Normal compilation
- Off

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX



- Stratix III
- Stratix IV
- Stratix V

## Notes

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name OPTIMIZE_TIMING <value>
```

## Default Value

Normal compilation

## OUTPUT\_BUFFER\_DELAY

Specifies the delay value (in ps) for the Programmable Output Buffer Delay. Turning on this feature should improve the output duty cycle at the cost of worse timing across the output buffer.

### Type

Integer

### Device Support

- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone V
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name OUTPUT_BUFFER_DELAY -to <to> -entity <entity  
name> <value>
```

### Example

```
set_instance_assignment -name OUTPUT_BUFFER_DELAY 50 -to pin  
set_instance_assignment -name OUTPUT_BUFFER_DELAY 100 -to pin  
set_instance_assignment -name OUTPUT_BUFFER_DELAY 150 -to pin
```

### See Also

OUTPUT\_BUFFER\_DELAY\_CONTROL

## OUTPUT\_BUFFER\_DELAY\_CONTROL

Sets the Programmable Output Buffer Delay control. Turning on this feature should improve the output duty cycle at the cost of worse timing across the output buffer.

### Old Name

STRATIXII\_OUTPUT\_DUTY\_CYCLE\_CONTROL

### Type

Enumeration

### Values

- Both Edges
- Negative Edge
- Off
- Positive Edge

### Device Support

- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone V
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name OUTPUT_BUFFER_DELAY_CONTROL -to <to> -entity  
<entity name> <value>
```

### Example

```
pin set_instance_assignment -name OUTPUT_BUFFER_DELAY_CONTROL "Both Edges" -to
```

### See Also

OUTPUT\_BUFFER\_DELAY

## OUTPUT\_DELAY\_CHAIN

Specifies the propagation delay for Output Delay Chain. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an output or bidirectional pin.

### Old Name

OUTPUT\_DELAY

### Type

Integer

### Device Support

- Arria 10

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name OUTPUT_DELAY_CHAIN -to <to> -entity <entity  
name> <value>
```

## OUTPUT\_ENABLE\_DELAY

Specifies the propagation delay to the output enable pin from internal logic or the output enable register implemented in an I/O cell. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an output pin or bidirectional pin.

### Type

Integer

### Device Support

- Arria GX
- Arria II GX
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- MAX 10
- Stratix II
- Stratix II GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name OUTPUT_ENABLE_DELAY -to <to> -entity <entity  
name> <value>
```

## OUTPUT\_ENABLE\_GROUP

Assigns an output enable group number for the specified node. Turning on this option directs the Fitter to view the specified nodes as an output enable group so as not to violate the requirements for the maximum number of pins driving out of a VREF group when a voltage-referenced input pin or bidirectional pin is present. For bidirectional pins, the Fitter determines all possible pins that may potentially drive out when any bidirectional pin is driving in by looking at the output enable of all the bidirectional pins in the VREF group. This behavior can result in the VREF group exceeding the maximum number of outputs and result in a no fit. Turning on the 'Output Enable Group' option allows you to specify an output enable group for specific pins, thus allowing you to specify which pins in the design are driving in and out at the same time. The Fitter only considers pins as potential outputs when they are in separate output enable groups or when they are not in an output enable group; by specifying an output enable group, you can lower the total number of outputs in the VREF group when any pin is driving in. As a result, the Fitter does not count all of the potential outputs of the bidirectional pins and the number of outputs in the VREF group remains in the legal range. You should turn on this option when the Fitter cannot detect the output enable group of the pins in the VREF group, for example when the output enables come from a state machine or complex logic. For detailed information on the number of outputs supported by a VREF group, refer to the data sheet for the device family, which is available from the Literature section of the Altera web site.

### Type

Integer

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX



- Stratix III
- Stratix IV
- Stratix V

## Notes

This assignment supports wildcards.

This assignment supports Fitter wildcards.

## Syntax

```
set_instance_assignment -name OUTPUT_ENABLE_GROUP -to <to> -entity <entity  
name> <value>
```

## Example

```
set_instance_assignment -name OUTPUT_ENABLE_GROUP 2 -to output_pin[0]  
set_instance_assignment -name OUTPUT_ENABLE_GROUP 2 -to output_pin[1]
```

## OUTPUT\_ENABLE\_REGISTER\_DUPLICATION

Duplicates a register that feeds to the output enable port of an I/O cell. Turning on this option can help maximize timing performance, for example, by permitting fast clock-to-output times. This option is ignored if it is applied to anything other than an output enable register that feeds to the output enable port of an I/O cell.

### Type

Boolean

### Notes

None

### Syntax

```
set_instance_assignment -name OUTPUT_ENABLE_REGISTER_DUPLICATION -to <to> -  
entity <entity name> <value>
```



## OUTPUT\_ENABLE\_ROUTING

Specifies whether an output enable signal in an I/O cell should be driven by the peripheral bus or the single-pin path. The Single-Pin setting drives the output enable signal with the local interconnect shared by the I/O cell and the adjacent LAB. The Peripheral setting drives the output enable signal with a peripheral control bus. This option is ignored if it is assigned to anything other than a logic function assigned to an I/O cell or the signal that drives the output enable of the I/O cell.

### Type

Enumeration

### Values

- Peripheral
- Single-Pin

### Device Support

- A
- E

### Notes

None

### Syntax

```
set_instance_assignment -name OUTPUT_ENABLE_ROUTING -to <to> -entity  
<entity name> <value>
```

## OUTPUT\_PIN\_LOAD

Specifies the capacitive load, in picofarads (pF), on output pins for each I/O standard. Note: These settings affect FPGA pins only. To specify board trace, termination, and capacitive load parameters for use with Advanced I/O Timing, use the Board Trace Model tab. Capacitive loading is ignored if applied to anything other than an output or bidirectional pin, or if Advanced I/O Timing is enabled.

### Type

Integer

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### INTEGER\_RANGE

0, 10000

### Notes

This assignment is copied to any duplicated nodes.

### Syntax

```
set_instance_assignment -name OUTPUT_PIN_LOAD -to <to> -entity <entity  
name> <value>  
set_global_assignment -name OUTPUT_PIN_LOAD -section_id <section  
identifier> <value>
```



## OUTPUT\_TERMINATION

Allows the Compiler to configure the on-chip termination (OCT) and impedance matching for an I/O pin. OCT helps to prevent signal reflections and maintain signal integrity. This option is ignored if it is applied to anything other than an I/O pad, input buffer, or output buffer.

### Type

String

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name OUTPUT_TERMINATION -to <to> -entity <entity  
name> <value>
```

### Example

```
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH  
CALIBRATION" -to pin_name
```

### See Also

INPUT\_OCT\_VALUE IO\_STANDARD OCT\_CONTROL\_BLOCK

## OVERRIDE\_DEFAULT\_ELECTROMIGRATION\_PARAMETERS

Specifies whether you want the Fitter to use default electromigration values, or if you want to specify maximum consecutive output and maximum current values.

### Type

Boolean

### Device Support

- Arria GX
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- MAX 10
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
<value> set_global_assignment -name OVERRIDE_DEFAULT_ELECTROMIGRATION_PARAMETERS
```

### Default Value

Off



## PAD\_TO\_CORE\_DELAY

Specifies the propagation delay from an input or bidirectional pin to logic and embedded cells within the device. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Type

Integer

### Device Support

- Arria GX
- Arria II GX
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- MAX 10
- MAX II
- MAX V
- Stratix II
- Stratix II GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name PAD_TO_CORE_DELAY -to <to> -entity <entity  
name> <value>  
set_instance_assignment -name PAD_TO_CORE_DELAY -from <from> -to <to> -  
entity <entity name> <value>
```

## PAD\_TO\_DDIO\_REGISTER\_DELAY

Specifies the propagation delay from an input pin to the data input of the DDIO low capture input register in the I/O cell associated with the pin. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin that uses DDIO functionality.

### Type

Integer

### Device Support

Arria II GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name PAD_TO_DDIO_REGISTER_DELAY -to <to> -entity  
<entity name> <value>
```



## PAD\_TO\_INPUT\_REGISTER\_DELAY

Specifies the propagation delay from an input pin to the data input of the input register implemented in the I/O cell associated with the pin. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Type

Integer

### Device Support

- Arria GX
- Arria II GX
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- MAX 10
- Stratix II
- Stratix II GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name PAD_TO_INPUT_REGISTER_DELAY -to <to> -entity  
<entity name> <value>
```

## PCI\_IO

Turns on Peripheral Component Interconnect (PCI) compatibility for a pin. For example, when the VCCIO of an EP20K400 device operates at 3.3 V and PCI I/O is turned on for a pin, the Compiler clamps the pin's signal to the VCCIO value, thus making the pin 3.3-V PCI-compliant. This option is ignored if it is applied to anything other than a pin or a top-level design entity.

### Type

Boolean

### Device Support

- Arria GX
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- A
- E
- HardCopy II
- MAX 10
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name PCI_IO -entity <entity name> <value>
set_instance_assignment -name PCI_IO -to <to> -entity <entity name> <value>
set_global_assignment -name PCI_IO <value>
```

### Default Value

Off

## Example

```
set_instance_assignment -name PCI_IO ON -to pin
```

## PERIPHERY\_TO\_CORE\_PLACEMENT\_AND\_ROUTING\_OPTIMIZATION

Specifies whether the Fitter should perform targeted placement and routing optimization on direct connections between periphery logic and registers in the FPGA core. If this option is set to 'Auto', the Fitter will automatically identify transfers with tight timing windows, place the core registers, and route all connections to or from the periphery. These placement and routing decisions are performed before the rest of core placement and routing, ensuring these timing-critical connections can meet timing, and also avoid routing congestion. If this option is set to 'On', all transfers between the periphery and core registers will be optimized, regardless of timing requirements. Setting this option to 'On' globally is not recommended -- instead it is intended for use in the Assignment Editor to force optimization to a targeted set of nodes or entities.

### Type

Enumeration

### Values

- Auto
- Off
- On

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports wildcards.

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

The value of this assignment must be a node name.

### Syntax

```
set_global_assignment -name  
PERIPHERY_TO_CORE_PLACEMENT_AND_ROUTING_OPTIMIZATION <value>  
set_global_assignment -name  
PERIPHERY_TO_CORE_PLACEMENT_AND_ROUTING_OPTIMIZATION -entity <entity name> <value>  
set_instance_assignment -name  
PERIPHERY_TO_CORE_PLACEMENT_AND_ROUTING_OPTIMIZATION -to <to> -entity <entity name>  
<value>
```

### Default Value

OFF



## PERIPH\_FITTER\_SCRIPT

Specifies the name of the tcl script that will be used to overwrite the default periphery fitter placement script used during a normal compile.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name PERIPH_FITTER_SCRIPT <value>
```

## PERIPH\_REPORT\_SCRIPT

Specifies the name of the tcl script that will be used to overwrite the default periphery fitter report panels created during a normal compile.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name PERIPH_REPORT_SCRIPT <value>
```



## PHYSICAL\_SYNTHESIS\_ASYNCHRONOUS\_SIGNAL\_PIPELINING

Specifies that Quartus Prime should perform automatic insertion of pipeline stages for asynchronous clear and asynchronous load signals during fitting to increase circuit performance. This option is useful for asynchronous signals that are failing recovery and removal timing because they feed registers using a high-speed clock. This feature is not supported in Quartus Prime Pro Edition.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name PHYSICAL_SYNTHESIS_ASYNCHRO-  
NOUS_SIGNAL_PIPELINING <value>  
set_global_assignment -name PHYSICAL_SYNTHESIS_ASYNCHRO-  
NOUS_SIGNAL_PIPELINING -entity <entity name> <value>
```

```
set_instance_assignment -name PHYSICAL_SYNTHESIS_ASYNCHRO-  
NOUS_SIGNAL_PIPELINING -to <to> -entity <entity name> <value>
```

**Default Value**

Off





## PHYSICAL\_SYNTHESIS\_COMBO\_LOGIC

Specifies that Quartus should perform physical synthesis optimizations on combinational logic during synthesis and fitting to increase circuit performance. This feature is not supported in Quartus Prime Pro Edition.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name PHYSICAL_SYNTHESIS_COMBO_LOGIC <value>  
set_global_assignment -name PHYSICAL_SYNTHESIS_COMBO_LOGIC -entity <entity  
name> <value>
```

```
set_instance_assignment -name PHYSICAL_SYNTHESIS_COMBO_LOGIC -to <to> -  
entity <entity name> <value>
```

**Default Value**

Off

## PHYSICAL\_SYNTHESIS\_COMBO\_LOGIC\_FOR\_AREA

Specifies that the Fitter should perform physical synthesis optimizations on combinational logic during fitting to achieve a fit. This feature is not supported in Quartus Prime Pro Edition.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name PHYSICAL_SYNTHESIS_COMBO_LOGIC_FOR_AREA <value>
set_global_assignment -name PHYSICAL_SYNTHESIS_COMBO_LOGIC_FOR_AREA -entity
<entity name> <value>
set_instance_assignment -name PHYSICAL_SYNTHESIS_COMBO_LOGIC_FOR_AREA -to
<to> -entity <entity name> <value>
```

### Default Value

Off



## PHYSICAL\_SYNTHESIS\_EFFORT

Specifies the amount of effort, in terms of compile time, physical synthesis should use. Compared to the Default setting, a setting of Extra will use extra compile time to try to gain extra circuit performance. Conversely, a setting of Fast will use less compile time but may reduce the performance gain that physical synthesis is able to achieve. This feature is not supported in Quartus Prime Pro Edition.

### Old Name

PHYSICAL\_SYNTHESIS\_EXTRA\_EFFORT

### Type

Enumeration

### Values

- Extra
- Fast
- Normal

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

## Notes

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name PHYSICAL_SYNTHESIS_EFFORT <value>
```

## Default Value

Normal

## PHYSICAL\_SYNTHESIS\_LOG\_FILE

Specifies the log file that lists all the FSYN operations performed in a previous compile that need to be reproduced. This log should be generated during a Stratix II compile, with Physical Synthesis on, where a Hardcopy II device is specified for migration. When the design is migrated to HardcopyII, this log file will allow the original Physical Synthesis operations performed on the Stratix II device to be replicated on the Hardcopy II device.

### Type

String

### Device Support

- HardCopy II
- Stratix III

### Notes

### Syntax

```
set_global_assignment -name PHYSICAL_SYNTHESIS_LOG_FILE <value>
```

### Default Value

Off



## PHYSICAL\_SYNTHESIS\_MAP\_LOGIC\_TO\_MEMORY\_FOR\_AREA

Specifies that the Fitter should perform physical synthesis optimizations on logic and registers, specifically allowing the mapping of logic and registers into unused memory blocks during fitting to achieve a fit. This feature is not supported in Quartus Prime Pro Edition.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name PHYSICAL_SYNTHESIS_MAP_LOGIC_TO_MEMORY_FOR_AREA  
<value>  
set_global_assignment -name PHYSICAL_SYNTHESIS_MAP_LOGIC_TO_MEMORY_FOR_AREA  
-entity <entity name> <value>  
set_instance_assignment -name  
PHYSICAL_SYNTHESIS_MAP_LOGIC_TO_MEMORY_FOR_AREA -to <to> -entity <entity name>  
<value>
```

### Default Value

Off

## PHYSICAL\_SYNTHESIS\_REGISTER\_DUPLICATION

Specifies that the Fitter should perform physical synthesis optimizations on registers, specifically allowing register duplication, during fitting to increase circuit performance. This feature is not supported in Quartus Prime Pro Edition.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name PHYSICAL_SYNTHESIS_REGISTER_DUPLICATION <value>
set_global_assignment -name PHYSICAL_SYNTHESIS_REGISTER_DUPLICATION -entity
<entity name> <value>
set_instance_assignment -name PHYSICAL_SYNTHESIS_REGISTER_DUPLICATION -to
```



<to> -entity <entity name> <value>

### Default Value

Off

## PHYSICAL\_SYNTHESIS\_REGISTER\_RETIMING

Specifies that Quartus should perform physical synthesis optimizations on registers, specifically allowing register retiming, during synthesis and fitting to increase circuit performance. This feature is not supported in Quartus Prime Pro Edition.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name PHYSICAL_SYNTHESIS_REGISTER_RETIMING <value>  
set_global_assignment -name PHYSICAL_SYNTHESIS_REGISTER_RETIMING -entity  
<entity name> <value>
```

```
set_instance_assignment -name PHYSICAL_SYNTHESIS_REGISTER_RETIMING -to <to>  
-entity <entity name> <value>
```

### Default Value

Off

## PLACEMENT\_EFFORT\_MULTIPLIER

Controls how much time the fitter spends in placement. The default value is 1.0 and legal values must be greater than 0. Specifying a floating-point number allows you to control the placement effort. A higher value increases CPU time but may improve placement quality. For example, a value of '4' will increase fitting time by approximately 2 to 4 times but may increase quality.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- EPC1
- EPC2
- Enhanced Configuration Devices
- A
- B
- E
- FLEX8000
- Flash Memory
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX9000
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III



- Stratix IV
- Stratix V
- Virtual JTAG TAP

## Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name PLACEMENT_EFFORT_MULTIPLIER <value>
```

## Default Value

1.0

## PLL\_AUTO\_RESET

Causes the PLL to self-reset automatically on loss of lock.

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

This assignment supports synthesis wildcards.

### Syntax

```
<value> set_instance_assignment -name PLL_AUTO_RESET -to <to> -entity <entity name>
```

## PLL\_BANDWIDTH\_PRESET

Specifies the PLL bandwidth preset setting.

### Type

Enumeration

### Values

- Auto
- High
- Low
- Medium

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

This assignment supports synthesis wildcards.

### Syntax

```
set_instance_assignment -name PLL_BANDWIDTH_PRESET -to <to> -entity <entity  
name> <value>
```

## PLL\_CHANNEL\_SPACING

Specifies the PLL channel spacing. The PLL channel spacing is the frequency difference between successive oscillations of the feedback clock into the phase frequency detector.

### Type

Frequency

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_instance_assignment -name PLL_CHANNEL_SPACING -to <to> -entity <entity  
name> <value>
```



## PLL\_COMPENSATE

Allows you to specify an output pin as a compensation target for a PLL in ZERO\_DELAY\_BUFFER or EXTERNAL\_FEEDBACK mode, or an input pin or a group of input pins as compensation targets for a PLL in SOURCE\_SYNCHRONOUS mode. If assigned to an output pin, the pin must be fed by the external clock output port of a PLL in a Stratix, Hardcopy Stratix or Cyclone device, or the compensated clock output port of a PLL in other devices. Any other output pins fed by the same PLL generally are not delay compensated, especially if they have different I/O standards. If assigned to an input pin or a group of input pins, the input pins must drive input registers that are clocked by the compensated clock output port of a PLL in SOURCE\_SYNCHRONOUS mode. This option is ignored if it is applied to anything other than an output or input pin as described previously.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name PLL_COMPENSATE -to <to> -entity <entity name>
```

## PLL\_COMPENSATION\_MODE

Specifies the routing path of the PLL feedback clock and adjusts the delay chains in the PLL.

### Type

Enumeration

### Values

- Direct
- EMIF
- External Feedback
- LVDS
- Normal
- Source Synchronous
- Zero Delay Buffer

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

This assignment supports synthesis wildcards.

### Syntax

```
set_instance_assignment -name PLL_COMPENSATION_MODE -to <to> -entity  
<entity name> <value>
```

## PLL\_ENFORCE\_USER\_PHASE\_SHIFT

Ensures that phase shift requirements are given higher priority.

### Type

Boolean

### Device Support

- Arria II GX
- Arria II GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix III
- Stratix IV

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name PLL_ENFORCE_USER_PHASE_SHIFT -to <to> -entity  
<entity name> <value>
```

## PLL\_FEEDBACK\_CLOCK\_SIGNAL

Allows you to specify whether PLL feedback clock signal should be routed using global or regional routing paths in the PLL conversion code to fractional PLL. Also allows additionally specifying the return path type (near/far).

### Type

Enumeration

### Values

- Far Global Clock
- Far Regional Clock
- Global Clock
- Near Global Clock
- Near Regional Clock
- Regional Clock

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_instance_assignment -name PLL_FEEDBACK_CLOCK_SIGNAL -to <to> -entity  
<entity name> <value>
```



## PLL\_FORCE\_OUTPUT\_COUNTER

Forces which counter to use for a particular PLL clock output. By default the compiler will automatically determine the best counter to use based on clock usage and other routing conflicts, but can be overridden with this option. Using this option can cause clock routing problems, as the clock router cannot rotate counters to resolve conflicts. Also see option PRESERVE\_PLL\_COUNTER\_ORDER.

### Type

Enumeration

### Values

- C0
- C1
- C2
- C3
- C4
- C5
- C6
- C7
- C8
- C9

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

This assignment supports Fitter wildcards.

## Syntax

```
set_instance_assignment -name PLL_FORCE_OUTPUT_COUNTER -to <to> -entity  
<entity name> <value>
```

## PLL\_FORCE\_OUTPUT\_COUNTER\_HARDCOPY\_REPLAY

Forces which counter to use for a particular PLL clock output. By default the compiler will automatically determine the best counter to use based on clock usage and other routing conflicts, but can be overridden with this option. Using this option can cause clock routing problems, as the clock router cannot rotate counters to resolve conflicts. Also see option PRESERVE\_PLL\_COUNTER\_ORDER.

### Type

Enumeration

### Values

- C0
- C1
- C2
- C3
- C4
- C5
- C6
- C7
- C8
- C9

### Device Support

- Arria II GZ
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name PLL_FORCE_OUTPUT_COUNTER_HARDCOPY_REPLAY -to  
<to> -entity <entity name> <value>
```

## PLL\_IGNORE\_MIGRATION\_DEVICES

Forces the compiler to ignore the migration devices when calculating the PLL settings. Normally the PLL is configured to work for all migration devices in addition to the current device. When this option is enabled, the compiler will ignore the PLL constraints for the migration devices, and will only consider the PLL constraints from the current device.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name PLL_IGNORE_MIGRATION_DEVICES -to <to> -entity  
<entity name> <value>
```



## PLL\_OPTIMIZE\_PHASE\_SHIFT\_FOR\_TIMING

Allows the Fitter to set the phase shift of a PLL output counter, and hence the phase shift of its generated clock, to improve timing for all edges affected by this clock. Apply multicyle timing exceptions to paths between the generated clock and other clocks in the design to avoid timing violations.

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_instance_assignment -name PLL_OPTIMIZE_PHASE_SHIFT_FOR_TIMING -to <to> -  
entity <entity name> <value>
```

## PLL\_OUTPUT\_CLOCK\_FREQUENCY

Specifies the output clock frequency of the PLL.

### Type

Frequency

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_instance_assignment -name PLL_OUTPUT_CLOCK_FREQUENCY -to <to> -entity  
<entity name> <value>
```

## PLL\_PFD\_CLOCK\_FREQUENCY

Specifies the phase frequency detector (PFD) clock frequency.

### Type

Frequency

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_instance_assignment -name PLL_PFD_CLOCK_FREQUENCY -to <to> -entity  
<entity name> <value>
```

## PLL\_TYPE

Specifies a specific PLL implementation to target.

### Type

Enumeration

### Values

- ATX
- CMU
- IOPLL
- fPLL

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
<value> set_instance_assignment -name PLL_TYPE -to <to> -entity <entity name>
```

## PLL\_VCO\_CLOCK\_FREQUENCY

Specifies the voltage controlled oscillator (VCO) output clock frequency.

### Type

Frequency

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_instance_assignment -name PLL_VCO_CLOCK_FREQUENCY -to <to> -entity  
<entity name> <value>
```

## PRESERVE\_PLL\_COUNTER\_ORDER

Preserves the order of PLL clock outputs used when selecting corresponding output counters. For example, a clk0 output will use a C0 counter and a clk2 output will use a C2 counter. Turning this option can cause clock routing problems, as the clock router cannot rotate counters to resolve conflicts.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name PRESERVE_PLL_COUNTER_ORDER -to <to> -entity  
<entity name> <value>
```

## PRESERVE\_UNUSED\_XCVR\_CHANNEL

Preserve the performance of unused RX/TX channels over time, if they are intended to be used in future

### Type

Boolean

### Device Support

Arria 10

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name PRESERVE_UNUSED_XCVR_CHANNEL <value>
set_instance_assignment -name PRESERVE_UNUSED_XCVR_CHANNEL -to <to> -entity
<entity name> <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name PRESERVE_UNUSED_XCVR_CHANNEL ON
set_instance_assignment -name PRESERVE_UNUSED_XCVR_CHANNEL ON -to AW34
```

## PROGRAMMABLE\_POWER\_MAXIMUM\_HIGH\_SPEED\_FRACTION\_OF\_USED\_LAB\_TILES

Sets an upper limit on the fraction of the LAB tiles used by your design that can be high-speed. Legal values must be between 0.0 and 1.0. The default value is 1.0. A value of 1.0 means that there is no restriction on the number of high-speed tiles, and the fitter will use the minimum number needed to meet the timing requirements of your design. Specifying a value lower than 1.0 might degrade timing quality, because some timing critical resources might be forced into low-power mode.

### Type

String

### Device Support

- Arria 10
- Arria V GZ
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name PROGRAM-  
MABLE_POWER_MAXIMUM_HIGH_SPEED_FRACTION_OF_USED_LAB_TILES <value>
```

### Default Value

1.0





## PROGRAMMABLE\_POWER\_TECHNOLOGY\_SETTING

Controls how the fitter configures tiles to operate in high-speed mode or low-power mode. Automatic specifies that the fitter should try to minimize power without sacrificing timing performance. Minimize Power Only specifies that the fitter should set the maximum number of tiles to operate in low-power mode. Force All Used Tiles to High Speed specifies that the fitter should set all used tiles to operate in high-speed mode. Force All Tiles with Failing Timing Paths to High Speed specifies that the fitter should ensure that all paths that are failing timing are set to high-speed mode. For designs that meet timing, the behavior of this setting should be similar to the Automatic setting. For designs that fail timing, all paths with negative slack will be put in high-speed mode. Note that this will likely not increase the speed of the design, and it may increase static power consumption, but it may assist in determining which logic paths need to be re-designed in order to close timing.

### Type

Enumeration

### Values

- Automatic
- Force All Tiles with Failing Timing Paths to High Speed
- Force All Used Tiles to High Speed
- Minimize Power Only

### Device Support

- Arria 10
- Arria V GZ
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name PROGRAMMABLE_POWER_TECHNOLOGY_SETTING <value>
```



## PROGRAMMABLE\_PREEMPHASIS

Implements control of programmable pre-emphasis, which helps compensate for high frequency losses. This option is ignored if it is applied to anything other than an output or bidirectional pin, or a top-level design entity containing output or bidirectional pins.

### Type

Integer

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix III
- Stratix IV
- Stratix V

### INTEGER\_RANGE

0, 3

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name PROGRAMMABLE_PREEMPHASIS -entity <entity name>
<value>
set_instance_assignment -name PROGRAMMABLE_PREEMPHASIS -to <to> -entity
<entity name> <value>
set_global_assignment -name PROGRAMMABLE_PREEMPHASIS <value>
```

## Example

```
set_instance_assignment -name PROGRAMMABLE_PREEMPHASIS 0 -to pin
```

## See Also

IO\_STANDARD

## PROGRAMMABLE\_VOD

Implements control of programmable VOD. This option is ignored if it is applied to anything other than an output or bidirectional pin, or a top-level design entity containing output or bidirectional pins.

### Type

Integer

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix III
- Stratix IV
- Stratix V

### INTEGER\_RANGE

0, 3

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name PROGRAMMABLE_VOD -entity <entity name> <value>
set_instance_assignment -name PROGRAMMABLE_VOD -to <to> -entity <entity
name> <value>
set_global_assignment -name PROGRAMMABLE_VOD <value>
```

### Example

```
set_instance_assignment -name PROGRAMMABLE_PREEMPHASIS 0 -to pin
```

### See Also

IO\_STANDARD

## PR\_DONE\_OPEN\_DRAIN

Specify open drain on the PR\_DONE pin should be enabled or not

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name PR_DONE_OPEN_DRAIN <value>
```

### Default Value

On

### Example

```
set_global_assignment -name pr_done_open_drain on  
set_global_assignment -name pr_done_open_drain off
```

### See Also

ENABLE\_PR\_PINS

## PR\_ERROR\_OPEN\_DRAIN

Specify open drain on the PR\_ERROR pin should be enabled or not

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name PR_ERROR_OPEN_DRAIN <value>
```

### Default Value

On

### Example

```
set_global_assignment -name pr_error_open_drain on  
set_global_assignment -name pr_error_open_drain off
```

### See Also

ENABLE\_PR\_PINS

## PR\_PINS\_OPEN\_DRAIN

Specify open drain on the Partial Reconfiguration pins (PR\_READY, PR\_ERROR, and PR\_DONE) should be enabled or not

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name PR_PINS_OPEN_DRAIN <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name pr_pins_open_drain on  
set_global_assignment -name pr_pins_open_drain off
```

### See Also

ENABLE\_PR\_PINS

## PR\_READY\_OPEN\_DRAIN

Specify open drain on the PR\_READY pin should be enabled or not

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name PR_READY_OPEN_DRAIN <value>
```

### Default Value

On

### Example

```
set_global_assignment -name pr_ready_open_drain on  
set_global_assignment -name pr_ready_open_drain off
```

### See Also

ENABLE\_PR\_PINS





## QDR\_D\_PIN\_GROUP

Assigns a quad data rate (QDR) D (data) output pin group number to a specified pin. Turning on this option allows the Fitter to view pins as a QDR D output pin group. I/O pins of a QDR D output pin group must be placed in the DQ pin locations of a single DQS group. This option is ignored if is assigned to anything other than an I/O pin.

### Type

Integer

### Device Support

Cyclone II

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name QDR_D_PIN_GROUP -to <to> -entity <entity  
name> <value>
```

## QII\_AUTO\_PACKED\_REGISTERS

Allows the Compiler to combine a register and a combinational function, or to implement registers using I/O cells, RAM blocks, or DSP blocks instead of logic cells. This option controls how aggressively the Fitter combines registers with other function blocks to reduce the area of the design. Generally, the 'Auto' or 'Sparse Auto' settings should be used for this option. The other options limit the flexibility of the Fitter to combine registers with other function blocks and can result in no fits. When 'Auto', the default setting is selected, the Fitter attempts to achieve the best performance with good area. If necessary, additional logic is combined to reduce the area of the design so that it can fit within the selected device. When this setting is 'Sparse Auto', the Fitter attempts to achieve the highest performance with possibly increased area, but without exceeding the logic capacity of the device. If this option is set to 'Off', the Fitter does not combine registers with other functions. The 'Off' setting severely increases the area of the design and may cause a no fit. If this option is set to 'Sparse', the Fitter combines functions in a way which improves performance for many designs. If this option is set to 'Normal', the Fitter combines functions that are expected to maximize design performance and reduce area. When this option is set to 'Minimize Area', the Fitter aggressively combines unrelated functions to reduce the area required for placing the design, at the expense of performance. When this option is set to 'Minimize Area with Chains', the Fitter even more aggressively combines functions that are part of register cascade chains or can be converted to register cascade chains. If this option is set to any value but 'Off', registers are combined with I/O cells to improve I/O timing (as long as the Optimize IOC Register Placement For Timing option allows it), and with DSP blocks and RAM blocks to reduce the area required for placing the design or to improve timing when possible.

### Old Name

AUTO\_PACKED\_REGISTERS\_ARMSTRONG, AUTO\_PACKED\_REGISTERS\_STRATIXII, Auto Packed Registers -- Stratix II/II GX/III Cyclone II/III Arria GX

### Type

Enumeration

### Values

- Auto
- Minimize Area
- Minimize Area with Chains
- Normal
- Off
- Sparse
- Sparse Auto

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II

- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

## Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name QII_AUTO_PACKED_REGISTERS <value>
set_global_assignment -name QII_AUTO_PACKED_REGISTERS -entity <entity name>
<value>
set_instance_assignment -name QII_AUTO_PACKED_REGISTERS -to <to> -entity
<entity name> <value>
```

## Default Value

Auto

## RELATIVE\_NEUTRON\_FLUX

is the neutron flux rate used by the seu calculator

### Type

Double

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name RELATIVE_NEUTRON_FLUX <value>
```

### Default Value

1.0



## RESERVE\_ALL\_UNUSED\_PINS

Reserves all unused pins on the target device in one of 5 states: as inputs that are tri-stated, as outputs that drive ground, as outputs that drive an unspecified signal, as input tri-stated with bus-hold, or as input tri-stated with weak pull-up.

### Old Name

RESERVED\_ALL\_UNUSED\_PINS

### Type

Enumeration

### Values

- As input tri-stated
- As input tri-stated with bus-hold
- As input tri-stated with weak pull-up
- As output driving an unspecified signal
- As output driving ground

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- A
- E
- HardCopy II
- MAX II
- MAX V
- MAX7000AE
- MAX7000B
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name RESERVE_ALL_UNUSED_PINS <value>
```

**Default Value**

As output driving ground



## RESERVE\_ALL\_UNUSED\_PINS\_WEAK\_PULLUP

Reserves all unused pins on the target device in one of 5 states: as inputs that are tri-stated, as outputs that drive ground, as outputs that drive an unspecified signal, as input tri-stated with bus-hold, or as input tri-stated with weak pull-up.

### Type

Enumeration

### Values

- As input tri-stated
- As input tri-stated with bus-hold
- As input tri-stated with weak pull-up
- As output driving an unspecified signal
- As output driving ground

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name RESERVE_ALL_UNUSED_PINS_WEAK_PULLUP <value>
```

### Default Value

As input tri-stated with weak pull-up

## RESERVE\_ASDO\_AFTER\_CONFIGURATION

Specifies how the ASDO pin should be used when the device is operating in user mode after configuration is complete. Depending on the current device and configuration scheme, the ASDO pin can be reserved as a regular I/O pin, as an input that is tri-stated, as an output that drives ground, or as an output that drives an unspecified signal. If this pin is reserved as a regular I/O pin, the ASDO pin can be used as an ordinary I/O pin after configuration.

### Old Name

RESERVE\_SDO\_AFTER\_CONFIGURATION

### Type

Enumeration

### Values

- As input tri-stated
- Use as regular IO

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name RESERVE_ASDO_AFTER_CONFIGURATION <value>
```

### Example

```
set_global_assignment -name RESERVE_ASDO_AFTER_CONFIGURATION "USE AS  
REGULAR IO"
```



## RESERVE\_DATA0\_AFTER\_CONFIGURATION

Specifies how the Data[0] pin should be used when the device is operating in user mode after configuration is complete. Depending on the current device and configuration scheme, the Data[0] pin can be reserved as a regular I/O pin, as an input that is tri-stated, as an output that drives ground, as an output that drives an unspecified signal, or compiler configured. If the Data[0] pin is reserved as a regular I/O pin, the Data[0] pin can be used as an ordinary I/O pin after configuration. If the Data[0] pin is only used to interface with external memory for configuration, the Data[0] pin should be reserved as compiler configured.

### Type

Enumeration

### Values

- As input tri-stated
- As output driving an unspecified signal
- As output driving ground
- Compiler configured
- Use as regular IO

### Device Support

- Arria 10
- Arria GX
- Arria II GZ
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

None

## Syntax

```
set_global_assignment -name RESERVE_DATA0_AFTER_CONFIGURATION <value>
```

## Default Value

As input tri-stated

## Example

```
set_global_assignment -name RESERVE_DATA0_AFTER_CONFIGURATION "USE AS  
REGULAR IO"
```



## RESERVE\_DATA15\_THROUGH\_DATA8\_AFTER\_CONFIGURATION

Specifies how the Data[15..8] pins should be used when the device is operating in user mode after configuration is complete.

### Type

Enumeration

### Values

- As input tri-stated
- As output driving an unspecified signal
- As output driving ground
- Use as regular IO

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name RESERVE_DATA15_THROUGH_DATA8_AFTER_CONFIGURATION <value>
```

### Default Value

Use as regular IO

### Example

```
set_global_assignment -name RESERVE_DATA15_THROUGH_DATA8_AFTER_CONFIGURATION "USE AS REGULAR IO"
```

## RESERVE\_DATA1\_AFTER\_CONFIGURATION

Specifies how the Data[1]/ASDO pin should be used when the device is operating in user mode after configuration is complete. Depending on the current device and configuration scheme, this pin can be reserved as a regular I/O pin, as an input that is tri-stated, as an output that drives ground, as an output that drives an unspecified signal, or compiler configured. If the Data[1]/ASDO pin is reserved as a regular I/O pin, the Data[1]/ASDO pin can be used as an ordinary I/O pin after configuration. If the Data[1]/ASDO pin is only used to interface with external memory for configuration, the Data[1]/ASDO pin should be reserved as compiler configured.

### Type

Enumeration

### Values

- As input tri-stated
- As output driving an unspecified signal
- As output driving ground
- Compiler configured
- Use as regular IO

### Device Support

- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- MAX 10

### Notes

None

### Syntax

```
set_global_assignment -name RESERVE_DATA1_AFTER_CONFIGURATION <value>
```

### Default Value

As input tri-stated

### Example

```
set_global_assignment -name RESERVE_DATA1_AFTER_CONFIGURATION "USE AS  
REGULAR IO"
```



## RESERVE\_DATA31\_THROUGH\_DATA16\_AFTER\_CONFIGURATION

Specifies how the Data[31..16] pins should be used when the device is operating in user mode after configuration is complete.

### Type

Enumeration

### Values

- As input tri-stated
- As output driving an unspecified signal
- As output driving ground
- Use as regular IO

### Device Support

- Arria 10
- Arria V GZ
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name RESERVE_DATA31_THROUGH_DATA16_AFTER_CONFIGURATION <value>
```

### Default Value

Use as regular IO

### Example

```
set_global_assignment -name RESERVE_DATA31_THROUGH_DATA16_AFTER_CONFIGURATION "USE AS REGULAR IO"
```

## RESERVE\_DATA7\_THROUGH\_DATA1\_AFTER\_CONFIGURATION

Specifies how the Data[7..1] pins should be used when the device is operating in user mode after configuration is complete. Depending on the current device and configuration scheme, these pins can be reserved as regular I/O pins, as inputs that are tri-stated, as outputs that drive ground, or as outputs that drive an unspecified signal. If this pin is reserved as a regular I/O pin, the Data[7..1] pins can be used as ordinary I/O pins after configuration.

### Type

Enumeration

### Values

- As input tri-stated
- As output driving an unspecified signal
- As output driving ground
- Use as regular IO

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V GZ
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name RESERVE_DATA7_THROUGH_DATA1_AFTER_CONFIGURATION  
<value>
```

## Default Value

Use as regular IO

## Example

```
set_global_assignment -name RESERVE_DATA7_THROUGH_DATA1_AFTER_CONFIGURATION  
"USE AS REGULAR IO"
```

## RESERVE\_DATA7\_THROUGH\_DATA2\_AFTER\_CONFIGURATION

Specifies how the Data[7..2] pins should be used when the device is operating in user mode after configuration is complete. Depending on the current device and configuration scheme, these pins can be reserved as regular I/O pins, as inputs that are tri-stated, as outputs that drive ground, as outputs that drive an unspecified signal, or compiler configured. If the Data[7..2] pins are reserved as a regular I/O pins, the Data[7..2] pins can be used as ordinary I/O pins after configuration. If Data[7..2] pins are only used to interface with external memory for configuration, the Data[7..2] pins should be reserved as compiler configured.

### Type

Enumeration

### Values

- As input tri-stated
- As output driving an unspecified signal
- As output driving ground
- Compiler configured
- Use as regular IO

### Device Support

- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX

### Notes

None

### Syntax

```
set_global_assignment -name RESERVE_DATA7_THROUGH_DATA2_AFTER_CONFIGURATION  
<value>
```

### Default Value

Use as regular IO

### Example

```
set_global_assignment -name RESERVE_DATA7_THROUGH_DATA2_AFTER_CONFIGURATION  
"USE AS REGULAR IO"
```



## RESERVE\_DATA7\_THROUGH\_DATA5\_AFTER\_CONFIGURATION

Specifies how the Data[7..5] pins should be used when the device is operating in user mode after configuration is complete. Depending on the current device and configuration scheme, these pins can be reserved as regular I/O pins, as inputs that are tri-stated, as outputs that drive ground, as outputs that drive an unspecified signal. If the Data[7..5] pins are reserved as a regular I/O pins, the Data[7..5] pins can be used as ordinary I/O pins after configuration.

### Type

Enumeration

### Values

- As input tri-stated
- As output driving an unspecified signal
- As output driving ground
- Use as regular IO

### Device Support

- Arria V
- Cyclone V

### Notes

None

### Syntax

```
<value> set_global_assignment -name RESERVE_DATA7_THROUGH_DATA5_AFTER_CONFIGURATION
```

### Default Value

Use as regular IO

### Example

```
set_global_assignment -name RESERVE_DATA7_THROUGH_DATA5_AFTER_CONFIGURATION  
"USE AS REGULAR IO"
```

## RESERVE\_DCLK\_AFTER\_CONFIGURATION

Specifies how the DCLK pin should be used when the device is operating in user mode after configuration is complete. Depending on the current device and configuration scheme, the DCLK pin can be reserved as a regular I/O pin, as a dedicated programming pin, or compiler configured. If this pin is reserved as a regular I/O pin, the DCLK pin can be used as an ordinary output pin after configuration. If the DCLK pin is only used to interface with external memory for configuration, the DCLK pin should be reserved as compiler configured.

### Type

Enumeration

### Values

- Compiler configured
- Use as programming pin
- Use as regular IO

### Device Support

- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- MAX 10

### Notes

None

### Syntax

```
set_global_assignment -name RESERVE_DCLK_AFTER_CONFIGURATION <value>
```

### Default Value

Use as programming pin

### Example

```
set_global_assignment -name RESERVE_DCLK_AFTER_CONFIGURATION "USE AS  
REGULAR IO"
```

## RESERVE\_FLASH\_NCE\_AFTER\_CONFIGURATION

Specifies how the FLASH\_nCE/nCSO pin should be used when the device is operating in user mode after configuration is complete. Depending on the current device and configuration scheme, this pin can be reserved as a regular I/O pin, as an input that is tri-stated, as an output that drives ground, as an output that drives an unspecified signal, or compiler configured. If the FLASH\_nCE/nCSO pin is reserved as a regular I/O pin, the FLASH\_nCE/nCSO pin can be used as an ordinary I/O pin after configuration. If the FLASH\_nCE/nCSO pin is only used to interface with external memory for configuration, the FLASH\_nCE/nCSO pin should be reserved as compiler configured.

### Type

Enumeration

### Values

- As input tri-stated
- As output driving an unspecified signal
- As output driving ground
- Compiler configured
- Use as regular IO

### Device Support

- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- MAX 10

### Notes

None

### Syntax

```
set_global_assignment -name RESERVE_FLASH_NCE_AFTER_CONFIGURATION <value>
```

### Default Value

As input tri-stated

### Example

```
set_global_assignment -name RESERVE_FLASH_NCE_AFTER_CONFIGURATION "USE AS  
REGULAR IO"
```

## RESERVE\_FLEXIBLE\_CLOCK\_NETWORK

Allows you to specify whether this clock should be routed using only flexible section clock network routing. This setting may improve routability for reconfigurable clocks, or clocks that will drive new logic in a later compile.

### Type

Boolean

### Device Support

Arria 10

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name RESERVE_FLEXIBLE_CLOCK_NETWORK -to <to> -  
entity <entity name> <value>
```

## RESERVE\_NCEO\_AFTER\_CONFIGURATION

Specifies how the nCEO pin should be used when the device is operating in user mode after configuration has been completed. The nCEO pin can be reserved as an output that drives ground or as an output that drives an unspecified signal. If this pin is reserved as a regular I/O, the nCEO pin can be used as an ordinary output pin after configuration.

### Type

Enumeration

### Values

- As output driving an unspecified signal
- As output driving ground
- Use as regular IO

### Notes

None

### Syntax

```
set_global_assignment -name RESERVE_NCEO_AFTER_CONFIGURATION <value>
```

### Default Value

Use as regular IO

## RESERVE\_NWS\_NRS\_NCS\_CS\_AFTER\_CONFIGURATION

Specifies how the nWS, nRS, nCS, and CS pins should be used when the device is operating in user mode after configuration is complete. Depending on the current device and configuration scheme, these pins can be reserved as regular I/O pins, as inputs that are tri-stated, as outputs that drive ground, or as outputs that drive an unspecified signal. If this pin is reserved as a regular I/O pin, the nWS, nRS, nCS, and CS pins can be used as ordinary I/O pins after configuration.

### Type

Enumeration

### Values

- As input tri-stated
- As output driving an unspecified signal
- As output driving ground
- Use as regular IO

### Device Support

- Arria GX
- A
- E
- HardCopy II
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name RESERVE_NWS_NRS_NCS_CS_AFTER_CONFIGURATION  
<value>
```

### Default Value

Use as regular IO

## RESERVE\_OTHER\_AP\_PINS\_AFTER\_CONFIGURATION

Specifies how the Data[15..8], PADD[23..0], NRESET, NAVD, NOE and NWE pins should be used when the device is operating in user mode after configuration is complete. Depending on the current device and configuration scheme, these pins can be reserved as regular I/O pins, as inputs that are tri-stated, as outputs that drive ground, as outputs that drive an unspecified signal, or compiler configured. If these pins are reserved as regular I/O pins, they can be used as ordinary I/O pins after configuration. If these pins are only used to interface with external memory for configuration, these pins should be reserved as compiler configured.

### Old Name

RESERVE\_OTHER\_APF\_PINS\_AFTER\_CONFIGURATION

### Type

Enumeration

### Values

- As input tri-stated
- As output driving an unspecified signal
- As output driving ground
- Compiler configured
- Use as regular IO

### Device Support

- Cyclone 10 LP
- Cyclone III
- Cyclone IV E

### Notes

None

### Syntax

```
set_global_assignment -name RESERVE_OTHER_AP_PINS_AFTER_CONFIGURATION  
<value>
```

### Default Value

Use as regular IO

### Example

```
set_global_assignment -name RESERVE_OTHER_AP_PINS_AFTER_CONFIGURATION "USE  
AS REGULAR IO"
```



## RESERVE\_PR\_PINS

Allows you to reserve the PR\_REQUEST, PR\_READY, PR\_ERROR, PR\_DONE, DCLK, and DATA[15..0] pins and prevent other pins from using them. Once these pins are reserved, they could not use to support partial reconfiguration (PR) with an external host as well when the device operates in user mode.

### Type

Boolean

### Device Support

Arria 10

### Notes

None

### Syntax

```
set_global_assignment -name RESERVE_PR_PINS <value>
```

### Default Value

Off

### Example

```
set_global_assignment -name RESERVE_PR_PINS ON
```

### See Also

ENABLE\_PR\_PINS





## RESERVE\_RDYNBUSY\_AFTER\_CONFIGURATION

Specifies how the RDYnBUSY pin should be used when the device is operating in user mode after configuration is complete. Depending on the current device and configuration scheme, the RDYnBUSY pin can be reserved as a regular I/O pin, as an input that is tri-stated, as an output that drives ground, or as an output that drives an unspecified signal. If this pin is reserved as a regular I/O pin, the RDYnBUSY pin can be used as an ordinary I/O pin after configuration.

### Type

Enumeration

### Values

- As input tri-stated
- As output driving an unspecified signal
- As output driving ground
- Use as regular IO

### Device Support

- Arria GX
- A
- E
- HardCopy II
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name RESERVE_RDYNBUSY_AFTER_CONFIGURATION <value>
```

### Default Value

Use as regular IO



## RESERVE\_ROUTING\_OUTPUT\_FLEXIBILITY

Allows you to specify whether the router should reserve output flexibility in this compilation. This setting helps maintain certain routing flexibility for later compilation, but may affect routability in this compilation.

### Type

Boolean

### Device Support

Arria 10

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_global_assignment -name RESERVE_ROUTING_OUTPUT_FLEXIBILITY <value>
```

### Default Value

Off



## ROUTER\_CLOCKING\_TOPOLOGY\_ANALYSIS

Directs the router to perform an analysis of the design's clocking topology and adjust the optimization approach on paths with significant clock skew. Enabling this option may improve hold timing at the cost of increased compile time.

### Type

Boolean

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- MAX 10
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name ROUTER_CLOCKING_TOPOLOGY_ANALYSIS <value>
```

### Default Value

Off

## ROUTER\_EFFORT\_MULTIPLIER

Controls how quickly the router tries to find a valid solution. The default value is 1.0 and legal values must be greater than or equal to 0.25. Values higher than 1.0 may improve routing quality at the expense of run-time on difficult-to-route circuits. Values lower than 1.0 can reduce router run-time, but usually reduces routing quality slightly.

### Type

String

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- EPC1
- EPC2
- Enhanced Configuration Devices
- A
- B
- E
- FLEX8000
- Flash Memory
- MAX 10
- MAX II
- MAX V
- MAX9000
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Virtual JTAG TAP

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name ROUTER_EFFORT_MULTIPLIER <value>
```

## Default Value

1.0

## ROUTER\_LCELL\_INSERTION\_AND\_LOGIC\_DUPLICATION

Allows the Fitter to automatically insert buffer logic cells between two nodes without altering the functionality of the design. Buffer logic cells are created from unused logic cells in the device. This option also allows the Fitter to duplicate a logic cell within a LAB when there are unused logic cells available in a LAB. Using this option can increase compilation time. The default setting of Auto will allow these operations to run when 1) the design requires them to fit the design or 2) the performance of the design can be improved by this optimization with a nominal compilation time increase.

### Type

Enumeration

### Values

- Auto
- Off
- On

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.



## Syntax

```
<value> set_global_assignment -name ROUTER_LCELL_INSERTION_AND_LOGIC_DUPLICATION
```

## Default Value

Auto

## ROUTER\_REGISTER\_DUPLICATION

Allows the Fitter to automatically duplicate registers within a LAB containing empty logic cells. This option does not alter the functionality of the design. The Auto Register Duplication option is also ignored if you select OFF as the setting for the Logic Cell Insertion -- Logic Duplication logic option. Turning on this option can allow the Logic Cell Insertion -- Logic Duplication logic option to improve a design's routability, but can make formal verification of a design more difficult.

### Type

Enumeration

### Values

- Auto
- Off
- On

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.





## Syntax

```
set_global_assignment -name ROUTER_REGISTER_DUPLICATION <value>
```

## Default Value

Auto

## ROUTER\_TIMING\_OPTIMIZATION\_LEVEL

Controls how aggressively the router tries to meet timing requirements. Setting this option to Maximum can increase design speed slightly, at the cost of increased compile time. Setting this option to Minimum can reduce compile time, at the cost of slightly reduced design speed. The default value is Normal.

### Type

Enumeration

### Values

- MAXIMUM
- MINIMUM
- Normal

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- EPC1
- EPC2
- Enhanced Configuration Devices
- A
- B
- E
- FLEX8000
- Flash Memory
- MAX 10
- MAX II
- MAX V
- MAX9000
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III

- Stratix IV
- Stratix V
- Virtual JTAG TAP

## Notes

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name ROUTER_TIMING_OPTIMIZATION_LEVEL <value>
```

## Default Value

Normal

## ROW\_GLOBAL\_SIGNAL

Specifies whether the signal should be available throughout the device on the global routing paths available within each row. Row-global signals can be both pin- and logic-driven. Clock, output enable, and register control signals can be row-global signals. Turning this option on for a pin or a single-output logic function signal is equivalent to feeding the signal through a ROW\_GLOBAL buffer.

### Type

Boolean

### Device Support

Mercury

### Notes

None

### Syntax

```
set_instance_assignment -name ROW_GLOBAL_SIGNAL -to <to> -entity <entity  
name> <value>
```



## RZQ\_GROUP

Specifies an RZQ pin name and an OCT to terminate the given pin. Using the same RZQ pin name instructs the fitter to use the same OCT to terminate the group of pins

### Type

String

### Device Support

- Arria 10

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name RZQ_GROUP -to <to> -entity <entity name>
```

### Example

```
set_instance_assignment -name RZQ_GROUP oct_rzq_in -to output_pin
```

### See Also

OUTPUT\_TERMINATION

## SCE\_PIN

Specifies the SCE configuration pin.

### Type

Boolean

### Device Support

- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- MAX 10

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_instance_assignment -name SCE_PIN -to <to> <value>
```

## SDO\_PIN

Specifies the SDO configuration pin.

### Type

Boolean

### Device Support

- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- MAX 10

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_instance_assignment -name SDO_PIN -to <to> <value>
```

## SEED

Specifies the starting value the Fitter uses when randomly determining the initial placement for the current design. The value can be any non-negative integer value. Changing the starting value may or may not produce better fitting. Specify a starting value only if the Fitter is not meeting timing requirements by a small amount. The Design Space Explorer tool lets you sweep many seed values easily to find the best value for a given project. Modifying the design or Quartus settings even slightly will usually change which seed is best for the design.

### Old Name

INITIAL\_PLACEMENT\_CONFIGURATION

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name SEED <value>
```

### Default Value

1





## SEU\_FIT\_REPORT

determines whether the SEU report is displayed or not

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SEU_FIT_REPORT <value>
```

### Default Value

Off

## SLEW\_RATE

Implements control of low-to-high/high-to-low transitions on output pins to help reduce switching noise. When a large number of output pins switch simultaneously, pins that use the lower Slew Rate option help reduce switching noise. This option is ignored if it is applied to anything other than an output or bidirectional pin, or a top-level design entity containing output or bidirectional pins. Note that using this option may increase the delay for output or bidir pins, which can affect slack on Tco paths for the pins this is applied to.

### Type

Integer

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix III
- Stratix IV
- Stratix V

### INTEGER\_RANGE

0, 3

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name SLEW_RATE -entity <entity name> <value>
set_instance_assignment -name SLEW_RATE -to <to> -entity <entity name>
<value>
set_global_assignment -name SLEW_RATE <value>
```

## Example

```
set_instance_assignment -name SLEW_RATE 0 -to pin
```

## See Also

IO\_STANDARD CURRENT\_STRENGTH\_NEW OUTPUT\_TERMINATION

## SLOW\_SLEW\_RATE

Implements slow low-to-high/high-to-low transitions on output pins to help reduce switching noise.

When a large number of output pins switch simultaneously, pins that use the Slow Slew Rate option help reduce switching noise. This option is ignored if it is applied to anything other than an output or bidirectional pin, or a top-level design entity containing output or bidirectional pins. Note that using this option increases the delay for output or bidir pins, which can affect slack on Tco paths for the pins this is applied to.

### Type

Boolean

### Device Support

- Cyclone
- EPC1
- EPC2
- Enhanced Configuration Devices
- A
- B
- E
- FLEX8000
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- MAX9000
- Mercury
- Stratix
- Stratix GX

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name SLOW_SLEW_RATE -entity <entity name> <value>
set_instance_assignment -name SLOW_SLEW_RATE -to <to> -entity <entity name>
<value>
set_global_assignment -name SLOW_SLEW_RATE <value>
```

### Default Value

Off

## SPECTRAQ\_PHYSICAL\_SYNTHESIS

Enables the Spectra-Q Physical Synthesis engine that includes combinational and sequential optimization during fitting to improve circuit performance.

### Type

Boolean

### Device Support

Arria 10

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name SPECTRAQ_PHYSICAL_SYNTHESIS <value>
```

### Default Value

Off

## STRATIXGX\_ALLOW\_CLOCK\_FANOUT\_WITH\_ANALOG\_RESET

Allows the compiler to enable netlist placements and routing where the dedicated reference clock pad in a Quad, that has a GXB Transmitter PLL with its pll\_reset or pllenable signal connected or has only Receivers which have their rxanalogreset signals connected, to feed other Quads or core logic. Also allows the compiler to enable netlist placements where a GXB Transmitter PLL exists in a Quad that has only Receivers which have their rxanalogreset signals connected.

### Type

Boolean

### Device Support

Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name STRATIXGX_ALLOW_CLOCK_FANOUT_WITH_ANALOG_RESET  
<value>
```

### Default Value

Off

## STRATIXGX\_ALLOW\_GIGE\_IN\_DOUBLE\_DATA\_WIDTH\_MODE

Enables the double data width (channel widths of 16 and 20) GIGE mode operation of GXB Receiver and Transmitter channels

### Type

Boolean

### Device Support

Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name STRATIXGX_ALLOW_GIGE_IN_DOUBLE_DATA_WIDTH_MODE  
<value>
```

### Default Value

Off

## STRATIXGX\_ALLOW\_GIGE\_UNDER\_FULL\_DATARATE\_RANGE

Enables GIGE configurations of GXB Receiver and Transmitter channels to operate at other datarates than 1.25Gbps

### Type

Boolean

### Device Support

Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name STRATIXGX_ALLOW_GIGE_UNDER_FULL_DATARATE_RANGE  
<value>
```

### Default Value

Off



## STRATIXGX\_ALLOW\_GIGE\_WITHOUT\_8B10B

Enables GIGE configurations of GXB Receiver and Transmitter channels where the 8B10B decoder and encoder are not used

### Type

Boolean

### Device Support

Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name STRATIXGX_ALLOW_GIGE_WITHOUT_8B10B <value>
```

### Default Value

Off

## STRATIXGX\_ALLOW\_GIGE\_WITH\_CORECLK\_SELECTED\_AT\_RATE\_MATCHER

Enables GIGE configurations of GXB Receiver channels with the coreclk selected at the rate matching FIFO

### Type

Boolean

### Device Support

Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name  
STRATIXGX_ALLOW_GIGE_WITH_CORECLK_SELECTED_AT_RATE_MATCHER <value>
```

### Default Value

Off



## STRATIXGX\_ALLOW\_GIGE\_WITH\_RX\_CORECLK\_FROM\_NON\_TXPLL\_SOURCE

Allows GIGE configurations of GXB Receiver channels where the coreclk input is fed from another source than the GXB Transmitter PLL in the same Quad

### Type

Boolean

### Device Support

Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name  
STRATIXGX_ALLOW_GIGE_WITH_RX_CORECLK_FROM_NON_TXPLL_SOURCE <value>
```

### Default Value

Off

## STRATIXGX\_ALLOW\_PARALLEL\_LOOPBACK\_IN\_DOUBLE\_DATA\_WIDTH\_MODE

Enables the double data width (channel widths of 16 and 20) parallel loopback mode operation of GXB Receiver and Transmitter channels

### Type

Boolean

### Device Support

Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name  
STRATIXGX_ALLOW_PARALLEL_LOOPBACK_IN_DOUBLE_DATA_WIDTH_MODE <value>
```

### Default Value

Off



## STRATIXGX\_ALLOW\_POST8B10B\_LOOPBACK

Allows Post 8B10B parallel loopback configurations of GXB Receiver and Transmitter channels

### Type

Boolean

### Device Support

Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name STRATIXGX_ALLOW_POST8B10B_LOOPBACK <value>
```

### Default Value

Off

## STRATIXGX\_ALLOW\_REVERSE\_PARALLEL\_LOOPBACK

Allows Reverse parallel loopback configurations of GXB Receiver and Transmitter channels

### Type

Boolean

### Device Support

Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name STRATIXGX_ALLOW_REVERSE_PARALLEL_LOOPBACK  
<value>
```

### Default Value

Off

## STRATIXGX\_ALLOW\_RX\_CORECLK\_FROM\_NON\_RX\_CLKOUT\_SOURCE\_IN\_DOUBLE\_ \_DATA\_WIDTH\_MODE

Enables the GXB Receiver coreclk input to be sourced from a different signal than the clkout output from the same GXB Receiver channel, while in double data width mode (channel widths of 16 or 20)

### Type

Boolean

### Device Support

Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name  
STRATIXGX_ALLOW_RX_CORECLK_FROM_NON_RX_CLKOUT_SOURCE_IN_DOUBLE_DATA_WIDTH_MODE  
<value>
```

### Default Value

Off

## STRATIXGX\_ALLOW\_USE\_OF\_GXB\_COUPLED\_IOS

Directs the compiler to allow the use of I/O pins that couple onto the GXB I/O banks

### Type

Boolean

### Device Support

Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name STRATIXGX_ALLOW_USE_OF_GXB_COUPLED_IOS <value>
```

### Default Value

Off



## STRATIXGX\_ALLOW\_XAUI\_IN\_SINGLE\_DATA\_WIDTH\_MODE

Enables single data width (channel width of 8) XAUI mode operation of GXB Receiver and Transmitter channels

### Type

Boolean

### Device Support

Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name STRATIXGX_ALLOW_XAUI_IN_SINGLE_DATA_WIDTH_MODE  
<value>
```

### Default Value

Off

## STRATIXGX\_ALLOW\_XAUI\_WITH\_CORECLK\_SELECTED\_AT\_RATE\_MATCHER

Enables XAUI configurations of GXB Receiver channels with the coreclk selected at the rate matching FIFO

### Type

Boolean

### Device Support

Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name  
STRATIXGX_ALLOW_XAUI_WITH_CORECLK_SELECTED_AT_RATE_MATCHER <value>
```

### Default Value

Off

## STRATIXGX\_ALLOW\_XAUI\_WITH\_RX\_CORECLK\_FROM\_NON\_TXPLL\_SOURCE

Allows XAUI configurations of GXB Receiver channels where the coreclk input is fed from another source than the GXB Transmitter PLL in the same Quad

### Type

Boolean

### Device Support

Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name  
STRATIXGX_ALLOW_XAUI_WITH_RX_CORECLK_FROM_NON_TXPLL_SOURCE <value>
```

### Default Value

Off

## STRATIXGX\_TERMINATION\_VALUE

Allows the Compiler to configure the on-chip termination (OCT) for a Stratix GX gigabit transceiver block (GXB) receiver channel input pin, GXB transmitter channel output pin, GXB transmitter PLL clock input pin, or GXB receiver channel clock input pin.

### Type

Enumeration

### Values

- OCT 100 Ohms
- OCT 120 Ohms
- OCT 150 Ohms
- Off

### Device Support

Stratix GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name STRATIXGX_TERMINATION_VALUE -to <to> -entity  
<entity name> <value>
```



## STRATIXIIGX\_TERMINATION\_VALUE

Allows the Compiler to configure the on-chip termination (OCT) for a Stratix II GX gigabit transceiver block (GXB) receiver channel input pin or GXB transmitter channel output pin.

### Type

Enumeration

### Values

- OCT 100 Ohms
- OCT 120 Ohms
- OCT 150 Ohms
- Off

### Device Support

- Arria GX
- Stratix II GX

### Notes

This assignment supports Fitter wildcards.

This assignment supports synthesis wildcards.

### Syntax

```
set_instance_assignment -name STRATIXIIGX_TERMINATION_VALUE -to <to> -  
entity <entity name> <value>
```

## STRATIXIII\_CONFIGURATION\_SCHEME

The method used to load data into the device. Three configuration schemes are available: Passive Serial (PS); Fast Passive Parallel (FPP) and Active Serial (AS).

### Old Name

STRATIXIV\_CONFIGURATION\_SCHEME

### Type

Enumeration

### Values

- Active Serial
- Fast Passive Parallel
- Passive Serial

### Device Support

- Arria II GX
- Arria II GZ
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name STRATIXIII_CONFIGURATION_SCHEME <value>
```

### Default Value

Passive Serial

### Example

```
set_global_assignment -name STRATIXIII_CONFIGURATION_SCHEME "Active Serial"
```



## STRATIXIII\_MRAM\_COMPATIBILITY

Direct Quartus Prime software to produce programming files that are compatible with all silicon revisions. Please see the Stratix III Device Handbook for more details.

### Type

Boolean

### Device Support

Stratix III

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name STRATIXIII_MRAM_COMPATIBILITY <value>
```

### Default Value

On

## STRATIXIII\_UPDATE\_MODE

Specifies the configuration mode used with the configuration scheme for configuring the device.

### Type

Enumeration

### Values

- Remote
- Standard

### Device Support

- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name STRATIXIII_UPDATE_MODE <value>
```

### Default Value

Standard

### Example

```
set_global_assignment -name STRATIXIII_UPDATE_MODE REMOTE
```



## STRATIXII\_CONFIGURATION\_SCHEME

The method used to load data into the device. Four configuration schemes are available: Passive Parallel Asynchronous (PPA); Passive Serial (PS); Fast Passive Parallel (FPP) and Active Serial (AS).

### Old Name

STRATIX\_II\_CONFIGURATION\_SCHEME

### Type

Enumeration

### Values

- Active Serial
- Fast Passive Parallel
- Passive Parallel Asynchronous
- Passive Serial

### Device Support

- Arria GX
- HardCopy II
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name STRATIXII_CONFIGURATION_SCHEME <value>
```

### Default Value

Passive Serial

## STRATIXII\_TERMINATION

Allows the Compiler to configure the on-chip termination (OCT) and impedance matching for an I/O pin. OCT helps to prevent signal reflections and maintain signal integrity. This option is ignored if it is applied to anything other than an I/O pin.

### Old Name

Termination -- Stratix II/Stratix II GX/HardCopy II

### Type

Enumeration

### Values

- Differential
- Off
- Parallel 50 Ohms with Calibration
- Series 25 Ohms with Calibration
- Series 25 Ohms without Calibration
- Series 50 Ohms with Calibration
- Series 50 Ohms without Calibration

### Device Support

- Arria GX
- HardCopy II
- Stratix II
- Stratix II GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name STRATIXII_TERMINATION -to <to> -entity  
<entity name> <value>
```

## STRATIXV\_CONFIGURATION\_SCHEME

The method used to configure a device with a design. Available configuration schemes depend on selected device family: Passive Serial (PS), Passive Parallel x8 (PPx8), Passive Parallel x16 (PPx16), Passive Parallel x32 (PPx32), Active Serial x1 (ASx1), Active Serial x4 (ASx4) and AVST x8, x16 and x32.

### Type

Enumeration

### Values

- AVST x16
- AVST x32
- AVST x8
- Active Serial
- Active Serial x1
- Active Serial x4
- Passive Parallel x16
- Passive Parallel x32
- Passive Parallel x8
- Passive Serial

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name STRATIXV_CONFIGURATION_SCHEME <value>
```

### Example

```
set_global_assignment -name STRATIXV_CONFIGURATION_SCHEME "Active Serial"
```



## STRATIX\_CONFIGURATION\_SCHEME

The method used to load data into the device. Three configuration schemes are available: Passive Parallel Asynchronous (PPA); Passive Serial (PS); and Fast Passive Parallel (FPP).

### Type

Enumeration

### Values

- Fast Passive Parallel
- Passive Parallel Asynchronous
- Passive Serial

### Device Support

- MAX II
- MAX V
- Stratix
- Stratix GX

### Notes

None

### Syntax

```
set_global_assignment -name STRATIX_CONFIGURATION_SCHEME <value>
```

### Default Value

Passive Serial



## STRATIX\_DECREASE\_INPUT\_DELAY\_TO\_INTERNAL\_CELLS

Decreases the propagation delay from an input or bidirectional pin to logic and embedded cells within the device. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Old Name

Decrease Input Delay to Internal Cells -- Stratix/Stratix GX/Cyclone,  
YEAGER\_DECREASE\_INPUT\_DELAY\_TO\_INTERNAL\_CELLS

### Type

Enumeration

### Values

- Large
- Medium
- Off
- On
- Small

### Device Support

- Cyclone
- Stratix
- Stratix GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name  
STRATIX_DECREASE_INPUT_DELAY_TO_INTERNAL_CELLS -to <to> -entity <entity name>  
<value>  
set_instance_assignment -name  
STRATIX_DECREASE_INPUT_DELAY_TO_INTERNAL_CELLS -from <from> -to <to> -entity  
<entity name> <value>
```

## STRATIX\_DEVICE\_IO\_STANDARD

Specifies the default I/O standard to be used for pins on the target device.

### Old Name

YEAGER\_DEVICE\_IO\_STANDARD

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.



## Syntax

```
set_global_assignment -name STRATIX_DEVICE_IO_STANDARD <value>
```

## Example

```
set_global_assignment -name STRATIX_DEVICE_IO_STANDARD "1.2 V"
```

## See Also

IO\_STANDARD

## STRATIX\_UPDATE\_MODE

Specifies the configuration mode used with the configuration scheme for configuring the device.

### Old Name

YEAGER\_UPDATE\_MODE

### Type

Enumeration

### Values

- Local
- Remote
- Standard

### Device Support

- Arria GX
- HardCopy II
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name STRATIX_UPDATE_MODE <value>
```

### Default Value

Standard



## SYNCHRONIZER\_IDENTIFICATION

Specifies how the TimeQuest Timing Analyzer identifies registers as being part of a synchronization register chain for metastability analysis. A synchronization register chain is a sequence of registers with the same clock with no fan-out in between, which is driven by a pin or logic from another clock domain. If this option is set to 'Off', the TimeQuest Timing Analyzer does not identify the specified registers, or the registers within the specified entity, as synchronization registers. If the option is set to 'Auto', the TimeQuest Timing Analyzer identifies valid synchronization registers that are part of a chain with more than one register that contains no combinational logic. If this option is set to 'Forced if Asynchronous', the TimeQuest Timing Analyzer identifies synchronization register chains if the software detects an asynchronous signal transfer, even if there is combinational logic or only one register in the chain. If this option is set to 'Forced', then the specified register, or all registers within the specified entity, are identified as synchronizers. The 'Forced' option should not be applied to the entire design, because doing so identifies all registers in the design as synchronizers. Registers that are identified as synchronizers are optimized for improved Mean Time Between Failure (MTBF) as long as the Optimize Design for Metastability option is turned on. If a synchronization register chain is identified with the 'Forced' or 'Forced if Asynchronous' option, then the TimeQuest Timing Analyzer reports the metastability MTBF for the chain. MTBF is not reported for automatically-detected register chains; you can use the 'Auto' setting to generate a report of possible synchronization chains in your design. If a synchronization register chain is identified with the 'Forced' or 'Forced if Asynchronous' option, then the TimeQuest Timing Analyzer reports the metastability MTBF for the chain when it meets the design timing requirements.

### Old Name

ANALYZE\_METASTABILITY

### Type

Enumeration

### Values

- Auto
- Forced
- Forced If Asynchronous
- Off

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III

- HardCopy IV
- MAX 10
- Stratix III
- Stratix IV
- Stratix V

## Notes

This assignment supports wildcards.

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name SYNCHRONIZER_IDENTIFICATION <value>
set_global_assignment -name SYNCHRONIZER_IDENTIFICATION -entity <entity
name> <value>
set_instance_assignment -name SYNCHRONIZER_IDENTIFICATION -to <to> -entity
<entity name> <value>
```

## Default Value

Auto

## SYNCHRONIZER\_TOGGLE\_RATE

Specifies the toggle rate of this register. The units for this value are in transitions per second, and must be positive. This is used when calculating the Mean Time Between Failures (MTBF) of a synchronizer chain in the Metastability Report. This only applies when the TimeQuest Timing Analyzer is used. You can specify the desired frequency setting on the first register of a synchronizer chain, and this will determine the data rate used in the MTBF estimation. There are two other assignments associated with toggle rates. The I/O Maximum Toggle Rate is only used for pins, and specifies the worst-case toggle rates used for signal integrity purposes. The Power Toggle Rate assignment is used to specify the expected time-averaged toggle rate, and is used by the Power Analyzer to estimate time-averaged power consumption.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name SYNCHRONIZER_TOGGLE_RATE -to <to> -entity  
<entity name> <value>
```

## T11\_0\_DELAY

Specifies the propagation delay for the gated T11 delay cell. Use this advanced option only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For more information about using this advanced option, refer to the data sheet for the targeted device family. The software ignores this option if you apply the option to other pins other than an input or bidirectional pin.

### Type

Integer

### Device Support

- Arria V
- Cyclone V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name T11_0_DELAY -to <to> -entity <entity name>
```



## T11\_1\_DELAY

Specifies the propagation delay for the ungated T11 delay cell. Use this advanced option only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For more information about using this option, refer to the data sheet for the device family. The software ignores this option if you apply this option to any pins other than an input or bidirectional pin.

### Type

Integer

### Device Support

- Arria V
- Cyclone V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name T11_1_DELAY -to <to> -entity <entity name>
```

## T11\_DELAY

Specifies the propagation delay for T11 Delay Cell. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Type

Integer

### Device Support

- Arria II GZ
- Arria V GZ
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name T11_DELAY -to <to> -entity <entity name>
```



## T11\_FINE\_DELAY

Enable the fine delay resolution on T11 Delay (DQS post-amble delay cell)

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name T11_FINE_DELAY -to <to> -entity <entity name>
```

&lt;value&gt;





## T4\_DELAY

Specifies the propagation delay for T4 Delay Cell (Output register to switch mux). This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Type

Integer

### Device Support

- Arria II GZ
- Arria V GZ
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name T4_DELAY -to <to> -entity <entity name>
```

## T8\_DELAY0

Specifies the propagation delay for T8 Delay Cell. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Type

Integer

### Device Support

- Arria II GZ
- Arria V GZ
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name T8_DELAY0 -to <to> -entity <entity name>
```

## T8\_DELAY1

Specifies the propagation delay for T8 Delay Cell. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

### Type

Integer

### Device Support

- Arria II GZ
- Arria V GZ
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name T8_DELAY1 -to <to> -entity <entity name>
```

## TERMINATION

Allows the Compiler to configure the on-chip termination (OCT) and impedance matching for an I/O pin. OCT helps to prevent signal reflections and maintain signal integrity. This option is ignored if it is applied to anything other than an I/O pin.

### Old Name

Termination -- Stratix / Stratix GX / HardCopy Stratix / Mercury,  
YEAGER\_OCT\_AND\_IMPEDANCE\_MATCHING

### Type

Enumeration

### Values

- Differential
- Off

### Device Support

- Mercury
- Stratix
- Stratix GX

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name TERMINATION -to <to> -entity <entity name>
```

## TERMINATION\_CONTROL\_BLOCK

Specifies the control block used for calibrated on-chip termination (OCT) and impedance matching for an I/O pin. OCT helps to prevent signal reflections and maintain signal integrity. This option is ignored if it is applied to anything other than an I/O pad, input buffer, or output buffer. This option should only be used on I/O pins which have a calibrated termination assignment.

### Type

String

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone V
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

The value of this assignment is case sensitive.

This assignment is copied to any duplicated nodes.

This assignment supports Fitter wildcards.

The value of this assignment must be a node name.

### Syntax

```
set_instance_assignment -name TERMINATION_CONTROL_BLOCK -to <to> -entity  
<entity name> <value>
```

### Example

```
set_instance_assignment -name TERMINATION_CONTROL_BLOCK "my_oct:inst|  
my_oct_alt_oct_toq:my_oct_alt_oct_toq_component|sdl_a_0" -to pin_name
```

### See Also

INPUT\_OCT\_VALUE IO\_STANDARD OUTPUT\_OCT\_VALUE

## TREAT\_BIDIR\_AS\_OUTPUT

Directs the bidirectional pin to be essentially treated as an output pin meaning that the input path is used for feedback from the output path.

### Type

Boolean

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name TREAT_BIDIR_AS_OUTPUT <value>
set_global_assignment -name TREAT_BIDIR_AS_OUTPUT -entity <entity name>
<value>
set_instance_assignment -name TREAT_BIDIR_AS_OUTPUT -to <to> -entity
<entity name> <value>
```

### Default Value

Off

### Example

```
set_instance_assignment -name TREAT_BIDIR_AS_OUTPUT ON -to bidir_pin
```

## See Also

IO\_STANDARD

## TRI\_STATE\_SPI\_PINS

This option controls Active Configuration Controller to tri-state the Active Configuration pins in user mode. This option would be ignored if the selected configuration scheme is not an Active Configuration scheme.

### Type

Boolean

### Device Support

- Arria 10
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name TRI_STATE_SPI_PINS <value>
```

### Default Value

Off





## TURBO\_BIT

Controls the speed vs. power usage trade-off for a macrocell (that is, for an embedded cell within an Embedded System Block [ESB] that is set to use Product Term mode). If the Turbo Bit is on, the macrocell's speed increases; if it is off, its power consumption decreases. This option is ignored if you select 'ROM' or 'LUT' as the setting for the Technology Mapper option.

### Type

Boolean

### Device Support

Mercury

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name TURBO_BIT <value>  
set_global_assignment -name TURBO_BIT -entity <entity name> <value>  
set_instance_assignment -name TURBO_BIT -to <to> -entity <entity name>  
<value>
```

### Default Value

On

## TXPMA\_SLEW\_RATE

To overwrite TX PMA slew rate to 4 options: Off, Low, Medium, High.

### Type

Enumeration

### Values

- High
- Low
- Medium
- Off

### Device Support

- Arria II GZ
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name TXPMA_SLEW_RATE <value>  
set_instance_assignment -name TXPMA_SLEW_RATE -to <to> <value>
```

### Default Value

Low

## UNFORCE\_MERGE\_PLL

Prevents the specified PLL to be merged with the master PLL. Use this option only for two compatible PLLs driven by the same clock source.

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_instance_assignment -name UNFORCE_MERGE_PLL -to <to> -entity <entity  
name> <value>
```

## UNFORCE\_MERGE\_PLL\_OUTPUT\_COUNTER

Prevents the specified PLL output counter to be merged with the master PLL output counter. Use this option only for two compatible PLLs driven by the same clock source.

### Type

Boolean

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_instance_assignment -name UNFORCE_MERGE_PLL_OUTPUT_COUNTER -to <to> -  
entity <entity name> <value>
```

## UNUSED\_TSD\_PINS\_GND

If this option is turned on, unused temperature sensing diode (TSD) pins, TEMPDIODEp/TEMPDIODEn, on the device are automatically set to GND in the Pin-Out File (.pin) file. By default, the TSD pins are available for connection to an external temperature sensing device; however, you must manually connect the pins to GND if they are not connected. Turning on this option only updates the information in the .pin file, it does not affect FPGA behavior.

### Type

Boolean

### Device Support

- Arria 10
- Arria V GZ
- Stratix IV
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name UNUSED_TSD_PINS_GND <value>
```

### Default Value

Off

## USER\_START\_UP\_CLOCK

Directs the device to use a user-supplied clock on the CLKUSR pin for initialization.

### Old Name

User Specified Start-up clock

### Type

Boolean

### Device Support

- Arria GX
- Arria II GX
- Arria II GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name USER_START_UP_CLOCK <value>
```

### Default Value

Off

## Example

```
set_global_assignment -name USER_START_UP_CLOCK ON  
set_global_assignment -name USER_START_UP_CLOCK OFF
```

## See Also

ACTIVE\_SERIAL\_CLOCK

## VCCIO\_CURRENT\_1PT8V

For user to override VCCIO current of 1.8-V io standard. Original current is 2mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name VCCIO_CURRENT_1PT8V <value>
```



## VCCIO\_CURRENT\_2PT5V

For user to override VCCIO current of 2.5-V io standard. Original current is 2mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name VCCIO_CURRENT_2PT5V <value>
```

## VCCIO\_CURRENT\_GTL

For user to override VCCIO current of GTL. Not yet supported in MAX7000.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name VCCIO_CURRENT_GTL <value>
```



## VCCIO\_CURRENT\_GTL\_PLUS

For user to override VCCIO current of GTL+. Original current is 0mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name VCCIO_CURRENT_GTL_PLUS <value>
```

## VCCIO\_CURRENT\_LVCMOS

For user to override VCCIO current of LVCMOS. Original current is 2mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name VCCIO_CURRENT_LVCMOS <value>
```



## VCCIO\_CURRENT\_LVTTL

For user to override VCCIO current of LVTTL. Original current is 4mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name VCCIO_CURRENT_LVTTL <value>
```

## VCCIO\_CURRENT\_PCI

For user to override VCCIO current of PCI. Original current is 4mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name VCCIO_CURRENT_PCI <value>
```



## VCCIO\_CURRENT\_SSTL2\_CLASS1

For user to override VCCIO current of SSTL2\_CLASS1. Original current is 14mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name VCCIO_CURRENT_SSTL2_CLASS1 <value>
```

## VCCIO\_CURRENT\_SSTL2\_CLASS2

For user to override VCCIO current of SSTL2\_CLASS2. Original current is 21mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name VCCIO_CURRENT_SSTL2_CLASS2 <value>
```





## VCCIO\_CURRENT\_SSTL3\_CLASS1

For user to override VCCIO current of SSTL3\_CLASS1. Original current is 18mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name VCCIO_CURRENT_SSTL3_CLASS1 <value>
```

## VCCIO\_CURRENT\_SSTL3\_CLASS2

For user to override VCCIO current of SSTL3\_CLASS2. Original current is 25mA

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name VCCIO_CURRENT_SSTL3_CLASS2 <value>
```



## VCCPD\_VOLTAGE

Specifies the default I/O Bank VCCPD Voltage to be used for pins on the target device.

### Type

String

### Device Support

- Arria GX
- HardCopy II
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name VCCPD_VOLTAGE -section_id <section identifier>  
<value>
```

### Default Value

3.3V, requires section identifier

## VREF\_MODE

Specifies VREF mode of a pin.

### Type

Enumeration

### Values

- CALIBRATED
- CALIBRATED\_SSTL
- EXTERNAL
- VCCIO\_45
- VCCIO\_50
- VCCIO\_55
- VCCIO\_65
- VCCIO\_70
- VCCIO\_75

### Device Support

- Arria 10

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_global_assignment -name VREF_MODE <value>
set_global_assignment -name VREF_MODE -entity <entity name> <value>
set_instance_assignment -name VREF_MODE -to <to> -entity <entity name>
<value>
```

### Example

```
set_instance_assignment -name VREF_MODE EXTERNAL -to pin
```

### See Also

VREF\_MODE

## WEAK\_PULL\_UP\_RESISTOR

Enables the weak pull-up resistor when the device is operating in user mode. This option pulls a high-impedance bus signal to VCC. The Weak Pull-Up Resistor option should not be used at the same time as the Enable Bus-Hold Circuitry option. This option is ignored if it is applied to anything other than a pin.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX7000B
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name WEAK_PULL_UP_RESISTOR <value>  
set_global_assignment -name WEAK_PULL_UP_RESISTOR -entity <entity name>  
<value>  
set_instance_assignment -name WEAK_PULL_UP_RESISTOR -to <to> -entity  
<entity name> <value>
```

## Default Value

Off

## Example

```
set_instance_assignment -name WEAK_PULL_UP_RESISTOR ON -to pin
```

## XCVR\_A10\_REFCLK\_TERM\_TRISTATE

A logic option that directs the Compiler to enable the internal termination of the dedicated reference clock pin.

### Type

Enumeration

### Values

- TRISTATE\_OFF
- TRISTATE\_ON

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_REFCLK_TERM_TRISTATE -to <to> -  
entity <entity name> <value>
```

## XCVR\_A10\_RX\_ADP\_CTLE\_ACGAIN\_4S

A logic option that allows you to control the amount of AC gain on the equalizer in high gain mode. The amount of AC gain is proportional to the setting where '0' gives the lowest AC gain and '31' gives the largest AC gain. This option is only valid when equalizer operates in manual mode.

### Type

Enumeration

### Values

- RADP\_CTLE\_ACGAIN\_4S\_0
- RADP\_CTLE\_ACGAIN\_4S\_1
- RADP\_CTLE\_ACGAIN\_4S\_10
- RADP\_CTLE\_ACGAIN\_4S\_11
- RADP\_CTLE\_ACGAIN\_4S\_12
- RADP\_CTLE\_ACGAIN\_4S\_13
- RADP\_CTLE\_ACGAIN\_4S\_14
- RADP\_CTLE\_ACGAIN\_4S\_15
- RADP\_CTLE\_ACGAIN\_4S\_16
- RADP\_CTLE\_ACGAIN\_4S\_17
- RADP\_CTLE\_ACGAIN\_4S\_18
- RADP\_CTLE\_ACGAIN\_4S\_19
- RADP\_CTLE\_ACGAIN\_4S\_2
- RADP\_CTLE\_ACGAIN\_4S\_20
- RADP\_CTLE\_ACGAIN\_4S\_21
- RADP\_CTLE\_ACGAIN\_4S\_22
- RADP\_CTLE\_ACGAIN\_4S\_23
- RADP\_CTLE\_ACGAIN\_4S\_24
- RADP\_CTLE\_ACGAIN\_4S\_25
- RADP\_CTLE\_ACGAIN\_4S\_26
- RADP\_CTLE\_ACGAIN\_4S\_27
- RADP\_CTLE\_ACGAIN\_4S\_28
- RADP\_CTLE\_ACGAIN\_4S\_3
- RADP\_CTLE\_ACGAIN\_4S\_4
- RADP\_CTLE\_ACGAIN\_4S\_5
- RADP\_CTLE\_ACGAIN\_4S\_6
- RADP\_CTLE\_ACGAIN\_4S\_7
- RADP\_CTLE\_ACGAIN\_4S\_8
- RADP\_CTLE\_ACGAIN\_4S\_9

### Device Support

- Arria 10



## Notes

## Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_CTLE_ACGAIN_4S -to <to> -  
entity <entity name> <value>
```

## XCVR\_A10\_RX\_ADP\_CTLE\_EQZ\_1S\_SEL

A logic option that allows you to control the amount of AC gain on the one-stage equalizer. The amount of AC gain is proportional to the setting where '0' gives the lowest AC gain and '15' gives the largest AC gain. This option is only valid when equalizer operates in manual mode.

### Type

Enumeration

### Values

- RADP\_CTLE\_EQZ\_1S\_SEL\_0
- RADP\_CTLE\_EQZ\_1S\_SEL\_1
- RADP\_CTLE\_EQZ\_1S\_SEL\_10
- RADP\_CTLE\_EQZ\_1S\_SEL\_11
- RADP\_CTLE\_EQZ\_1S\_SEL\_12
- RADP\_CTLE\_EQZ\_1S\_SEL\_13
- RADP\_CTLE\_EQZ\_1S\_SEL\_14
- RADP\_CTLE\_EQZ\_1S\_SEL\_15
- RADP\_CTLE\_EQZ\_1S\_SEL\_2
- RADP\_CTLE\_EQZ\_1S\_SEL\_3
- RADP\_CTLE\_EQZ\_1S\_SEL\_4
- RADP\_CTLE\_EQZ\_1S\_SEL\_5
- RADP\_CTLE\_EQZ\_1S\_SEL\_6
- RADP\_CTLE\_EQZ\_1S\_SEL\_7
- RADP\_CTLE\_EQZ\_1S\_SEL\_8
- RADP\_CTLE\_EQZ\_1S\_SEL\_9

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_CTLE_EQZ_1S_SEL -to <to> -  
entity <entity name> <value>
```

## XCVR\_A10\_RX\_ADP\_DFE\_FXTAP1

A logic option that allows you to specify the coefficient setting for fix tap one in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP1\_0
- RADP\_DFE\_FXTAP1\_1
- RADP\_DFE\_FXTAP1\_10
- RADP\_DFE\_FXTAP1\_100
- RADP\_DFE\_FXTAP1\_101
- RADP\_DFE\_FXTAP1\_102
- RADP\_DFE\_FXTAP1\_103
- RADP\_DFE\_FXTAP1\_104
- RADP\_DFE\_FXTAP1\_105
- RADP\_DFE\_FXTAP1\_106
- RADP\_DFE\_FXTAP1\_107
- RADP\_DFE\_FXTAP1\_108
- RADP\_DFE\_FXTAP1\_109
- RADP\_DFE\_FXTAP1\_11
- RADP\_DFE\_FXTAP1\_110
- RADP\_DFE\_FXTAP1\_111
- RADP\_DFE\_FXTAP1\_112
- RADP\_DFE\_FXTAP1\_113
- RADP\_DFE\_FXTAP1\_114
- RADP\_DFE\_FXTAP1\_115
- RADP\_DFE\_FXTAP1\_116
- RADP\_DFE\_FXTAP1\_117
- RADP\_DFE\_FXTAP1\_118
- RADP\_DFE\_FXTAP1\_119
- RADP\_DFE\_FXTAP1\_12
- RADP\_DFE\_FXTAP1\_120
- RADP\_DFE\_FXTAP1\_121
- RADP\_DFE\_FXTAP1\_122
- RADP\_DFE\_FXTAP1\_123
- RADP\_DFE\_FXTAP1\_124
- RADP\_DFE\_FXTAP1\_125
- RADP\_DFE\_FXTAP1\_126
- RADP\_DFE\_FXTAP1\_127
- RADP\_DFE\_FXTAP1\_13
- RADP\_DFE\_FXTAP1\_14
- RADP\_DFE\_FXTAP1\_15
- RADP\_DFE\_FXTAP1\_16
- RADP\_DFE\_FXTAP1\_17

- RADP\_DFE\_FXTAP1\_18
- RADP\_DFE\_FXTAP1\_19
- RADP\_DFE\_FXTAP1\_2
- RADP\_DFE\_FXTAP1\_20
- RADP\_DFE\_FXTAP1\_21
- RADP\_DFE\_FXTAP1\_22
- RADP\_DFE\_FXTAP1\_23
- RADP\_DFE\_FXTAP1\_24
- RADP\_DFE\_FXTAP1\_25
- RADP\_DFE\_FXTAP1\_26
- RADP\_DFE\_FXTAP1\_27
- RADP\_DFE\_FXTAP1\_28
- RADP\_DFE\_FXTAP1\_29
- RADP\_DFE\_FXTAP1\_3
- RADP\_DFE\_FXTAP1\_30
- RADP\_DFE\_FXTAP1\_31
- RADP\_DFE\_FXTAP1\_32
- RADP\_DFE\_FXTAP1\_33
- RADP\_DFE\_FXTAP1\_34
- RADP\_DFE\_FXTAP1\_35
- RADP\_DFE\_FXTAP1\_36
- RADP\_DFE\_FXTAP1\_37
- RADP\_DFE\_FXTAP1\_38
- RADP\_DFE\_FXTAP1\_39
- RADP\_DFE\_FXTAP1\_4
- RADP\_DFE\_FXTAP1\_40
- RADP\_DFE\_FXTAP1\_41
- RADP\_DFE\_FXTAP1\_42
- RADP\_DFE\_FXTAP1\_43
- RADP\_DFE\_FXTAP1\_44
- RADP\_DFE\_FXTAP1\_45
- RADP\_DFE\_FXTAP1\_46
- RADP\_DFE\_FXTAP1\_47
- RADP\_DFE\_FXTAP1\_48
- RADP\_DFE\_FXTAP1\_49
- RADP\_DFE\_FXTAP1\_5
- RADP\_DFE\_FXTAP1\_50
- RADP\_DFE\_FXTAP1\_51
- RADP\_DFE\_FXTAP1\_52
- RADP\_DFE\_FXTAP1\_53
- RADP\_DFE\_FXTAP1\_54
- RADP\_DFE\_FXTAP1\_55
- RADP\_DFE\_FXTAP1\_56
- RADP\_DFE\_FXTAP1\_57
- RADP\_DFE\_FXTAP1\_58
- RADP\_DFE\_FXTAP1\_59
- RADP\_DFE\_FXTAP1\_6
- RADP\_DFE\_FXTAP1\_60

- RADP\_DFE\_FXTAP1\_61
- RADP\_DFE\_FXTAP1\_62
- RADP\_DFE\_FXTAP1\_63
- RADP\_DFE\_FXTAP1\_64
- RADP\_DFE\_FXTAP1\_65
- RADP\_DFE\_FXTAP1\_66
- RADP\_DFE\_FXTAP1\_67
- RADP\_DFE\_FXTAP1\_68
- RADP\_DFE\_FXTAP1\_69
- RADP\_DFE\_FXTAP1\_7
- RADP\_DFE\_FXTAP1\_70
- RADP\_DFE\_FXTAP1\_71
- RADP\_DFE\_FXTAP1\_72
- RADP\_DFE\_FXTAP1\_73
- RADP\_DFE\_FXTAP1\_74
- RADP\_DFE\_FXTAP1\_75
- RADP\_DFE\_FXTAP1\_76
- RADP\_DFE\_FXTAP1\_77
- RADP\_DFE\_FXTAP1\_78
- RADP\_DFE\_FXTAP1\_79
- RADP\_DFE\_FXTAP1\_8
- RADP\_DFE\_FXTAP1\_80
- RADP\_DFE\_FXTAP1\_81
- RADP\_DFE\_FXTAP1\_82
- RADP\_DFE\_FXTAP1\_83
- RADP\_DFE\_FXTAP1\_84
- RADP\_DFE\_FXTAP1\_85
- RADP\_DFE\_FXTAP1\_86
- RADP\_DFE\_FXTAP1\_87
- RADP\_DFE\_FXTAP1\_88
- RADP\_DFE\_FXTAP1\_89
- RADP\_DFE\_FXTAP1\_9
- RADP\_DFE\_FXTAP1\_90
- RADP\_DFE\_FXTAP1\_91
- RADP\_DFE\_FXTAP1\_92
- RADP\_DFE\_FXTAP1\_93
- RADP\_DFE\_FXTAP1\_94
- RADP\_DFE\_FXTAP1\_95
- RADP\_DFE\_FXTAP1\_96
- RADP\_DFE\_FXTAP1\_97
- RADP\_DFE\_FXTAP1\_98
- RADP\_DFE\_FXTAP1\_99

## Device Support

- Arria 10

## Notes

## Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP1 -to <to> -entity  
<entity name> <value>
```

## XCVR\_A10\_RX\_ADP\_DFE\_FXTAP10

A logic option that allows you to specify the coefficient setting for fix tap ten in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP10\_0
- RADP\_DFE\_FXTAP10\_1
- RADP\_DFE\_FXTAP10\_10
- RADP\_DFE\_FXTAP10\_11
- RADP\_DFE\_FXTAP10\_12
- RADP\_DFE\_FXTAP10\_13
- RADP\_DFE\_FXTAP10\_14
- RADP\_DFE\_FXTAP10\_15
- RADP\_DFE\_FXTAP10\_16
- RADP\_DFE\_FXTAP10\_17
- RADP\_DFE\_FXTAP10\_18
- RADP\_DFE\_FXTAP10\_19
- RADP\_DFE\_FXTAP10\_2
- RADP\_DFE\_FXTAP10\_20
- RADP\_DFE\_FXTAP10\_21
- RADP\_DFE\_FXTAP10\_22
- RADP\_DFE\_FXTAP10\_23
- RADP\_DFE\_FXTAP10\_24
- RADP\_DFE\_FXTAP10\_25
- RADP\_DFE\_FXTAP10\_26
- RADP\_DFE\_FXTAP10\_27
- RADP\_DFE\_FXTAP10\_28
- RADP\_DFE\_FXTAP10\_29
- RADP\_DFE\_FXTAP10\_3
- RADP\_DFE\_FXTAP10\_30
- RADP\_DFE\_FXTAP10\_31
- RADP\_DFE\_FXTAP10\_32
- RADP\_DFE\_FXTAP10\_33
- RADP\_DFE\_FXTAP10\_34
- RADP\_DFE\_FXTAP10\_35
- RADP\_DFE\_FXTAP10\_36
- RADP\_DFE\_FXTAP10\_37
- RADP\_DFE\_FXTAP10\_38
- RADP\_DFE\_FXTAP10\_39
- RADP\_DFE\_FXTAP10\_4
- RADP\_DFE\_FXTAP10\_40
- RADP\_DFE\_FXTAP10\_41
- RADP\_DFE\_FXTAP10\_42

- RADP\_DFE\_FXTAP10\_43
- RADP\_DFE\_FXTAP10\_44
- RADP\_DFE\_FXTAP10\_45
- RADP\_DFE\_FXTAP10\_46
- RADP\_DFE\_FXTAP10\_47
- RADP\_DFE\_FXTAP10\_48
- RADP\_DFE\_FXTAP10\_49
- RADP\_DFE\_FXTAP10\_5
- RADP\_DFE\_FXTAP10\_50
- RADP\_DFE\_FXTAP10\_51
- RADP\_DFE\_FXTAP10\_52
- RADP\_DFE\_FXTAP10\_53
- RADP\_DFE\_FXTAP10\_54
- RADP\_DFE\_FXTAP10\_55
- RADP\_DFE\_FXTAP10\_56
- RADP\_DFE\_FXTAP10\_57
- RADP\_DFE\_FXTAP10\_58
- RADP\_DFE\_FXTAP10\_59
- RADP\_DFE\_FXTAP10\_6
- RADP\_DFE\_FXTAP10\_60
- RADP\_DFE\_FXTAP10\_61
- RADP\_DFE\_FXTAP10\_62
- RADP\_DFE\_FXTAP10\_63
- RADP\_DFE\_FXTAP10\_7
- RADP\_DFE\_FXTAP10\_8
- RADP\_DFE\_FXTAP10\_9

## Device Support

- Arria 10

## Notes

## Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP10 -to <to> -entity  
<entity name> <value>
```



## XCVR\_A10\_RX\_ADP\_DFE\_FXTAP10\_SGN

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP10\_SGN\_0
- RADP\_DFE\_FXTAP10\_SGN\_1

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP10_SGN -to <to> -  
entity <entity name> <value>
```

## XCVR\_A10\_RX\_ADP\_DFE\_FXTAP11

A logic option that allows you to specify the coefficient setting for fix tap eleven in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP11\_0
- RADP\_DFE\_FXTAP11\_1
- RADP\_DFE\_FXTAP11\_10
- RADP\_DFE\_FXTAP11\_11
- RADP\_DFE\_FXTAP11\_12
- RADP\_DFE\_FXTAP11\_13
- RADP\_DFE\_FXTAP11\_14
- RADP\_DFE\_FXTAP11\_15
- RADP\_DFE\_FXTAP11\_16
- RADP\_DFE\_FXTAP11\_17
- RADP\_DFE\_FXTAP11\_18
- RADP\_DFE\_FXTAP11\_19
- RADP\_DFE\_FXTAP11\_2
- RADP\_DFE\_FXTAP11\_20
- RADP\_DFE\_FXTAP11\_21
- RADP\_DFE\_FXTAP11\_22
- RADP\_DFE\_FXTAP11\_23
- RADP\_DFE\_FXTAP11\_24
- RADP\_DFE\_FXTAP11\_25
- RADP\_DFE\_FXTAP11\_26
- RADP\_DFE\_FXTAP11\_27
- RADP\_DFE\_FXTAP11\_28
- RADP\_DFE\_FXTAP11\_29
- RADP\_DFE\_FXTAP11\_3
- RADP\_DFE\_FXTAP11\_30
- RADP\_DFE\_FXTAP11\_31
- RADP\_DFE\_FXTAP11\_32
- RADP\_DFE\_FXTAP11\_33
- RADP\_DFE\_FXTAP11\_34
- RADP\_DFE\_FXTAP11\_35
- RADP\_DFE\_FXTAP11\_36
- RADP\_DFE\_FXTAP11\_37
- RADP\_DFE\_FXTAP11\_38
- RADP\_DFE\_FXTAP11\_39
- RADP\_DFE\_FXTAP11\_4
- RADP\_DFE\_FXTAP11\_40
- RADP\_DFE\_FXTAP11\_41
- RADP\_DFE\_FXTAP11\_42

- RADP\_DFE\_FXTAP11\_43
- RADP\_DFE\_FXTAP11\_44
- RADP\_DFE\_FXTAP11\_45
- RADP\_DFE\_FXTAP11\_46
- RADP\_DFE\_FXTAP11\_47
- RADP\_DFE\_FXTAP11\_48
- RADP\_DFE\_FXTAP11\_49
- RADP\_DFE\_FXTAP11\_5
- RADP\_DFE\_FXTAP11\_50
- RADP\_DFE\_FXTAP11\_51
- RADP\_DFE\_FXTAP11\_52
- RADP\_DFE\_FXTAP11\_53
- RADP\_DFE\_FXTAP11\_54
- RADP\_DFE\_FXTAP11\_55
- RADP\_DFE\_FXTAP11\_56
- RADP\_DFE\_FXTAP11\_57
- RADP\_DFE\_FXTAP11\_58
- RADP\_DFE\_FXTAP11\_59
- RADP\_DFE\_FXTAP11\_6
- RADP\_DFE\_FXTAP11\_60
- RADP\_DFE\_FXTAP11\_61
- RADP\_DFE\_FXTAP11\_62
- RADP\_DFE\_FXTAP11\_63
- RADP\_DFE\_FXTAP11\_7
- RADP\_DFE\_FXTAP11\_8
- RADP\_DFE\_FXTAP11\_9

## Device Support

- Arria 10

## Notes

## Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP11 -to <to> -entity  
<entity name> <value>
```

## XCVR\_A10\_RX\_ADP\_DFE\_FXTAP11\_SGN

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP11\_SGN\_0
- RADP\_DFE\_FXTAP11\_SGN\_1

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP11_SGN -to <to> -  
entity <entity name> <value>
```



## XCVR\_A10\_RX\_ADP\_DFE\_FXTAP2

A logic option that allows you to specify the coefficient setting for fix tap two in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP2\_0
- RADP\_DFE\_FXTAP2\_1
- RADP\_DFE\_FXTAP2\_10
- RADP\_DFE\_FXTAP2\_100
- RADP\_DFE\_FXTAP2\_101
- RADP\_DFE\_FXTAP2\_102
- RADP\_DFE\_FXTAP2\_103
- RADP\_DFE\_FXTAP2\_104
- RADP\_DFE\_FXTAP2\_105
- RADP\_DFE\_FXTAP2\_106
- RADP\_DFE\_FXTAP2\_107
- RADP\_DFE\_FXTAP2\_108
- RADP\_DFE\_FXTAP2\_109
- RADP\_DFE\_FXTAP2\_11
- RADP\_DFE\_FXTAP2\_110
- RADP\_DFE\_FXTAP2\_111
- RADP\_DFE\_FXTAP2\_112
- RADP\_DFE\_FXTAP2\_113
- RADP\_DFE\_FXTAP2\_114
- RADP\_DFE\_FXTAP2\_115
- RADP\_DFE\_FXTAP2\_116
- RADP\_DFE\_FXTAP2\_117
- RADP\_DFE\_FXTAP2\_118
- RADP\_DFE\_FXTAP2\_119
- RADP\_DFE\_FXTAP2\_12
- RADP\_DFE\_FXTAP2\_120
- RADP\_DFE\_FXTAP2\_121
- RADP\_DFE\_FXTAP2\_122
- RADP\_DFE\_FXTAP2\_123
- RADP\_DFE\_FXTAP2\_124
- RADP\_DFE\_FXTAP2\_125
- RADP\_DFE\_FXTAP2\_126
- RADP\_DFE\_FXTAP2\_127
- RADP\_DFE\_FXTAP2\_13
- RADP\_DFE\_FXTAP2\_14
- RADP\_DFE\_FXTAP2\_15
- RADP\_DFE\_FXTAP2\_16
- RADP\_DFE\_FXTAP2\_17

- RADP\_DFE\_FXTAP2\_18
- RADP\_DFE\_FXTAP2\_19
- RADP\_DFE\_FXTAP2\_2
- RADP\_DFE\_FXTAP2\_20
- RADP\_DFE\_FXTAP2\_21
- RADP\_DFE\_FXTAP2\_22
- RADP\_DFE\_FXTAP2\_23
- RADP\_DFE\_FXTAP2\_24
- RADP\_DFE\_FXTAP2\_25
- RADP\_DFE\_FXTAP2\_26
- RADP\_DFE\_FXTAP2\_27
- RADP\_DFE\_FXTAP2\_28
- RADP\_DFE\_FXTAP2\_29
- RADP\_DFE\_FXTAP2\_3
- RADP\_DFE\_FXTAP2\_30
- RADP\_DFE\_FXTAP2\_31
- RADP\_DFE\_FXTAP2\_32
- RADP\_DFE\_FXTAP2\_33
- RADP\_DFE\_FXTAP2\_34
- RADP\_DFE\_FXTAP2\_35
- RADP\_DFE\_FXTAP2\_36
- RADP\_DFE\_FXTAP2\_37
- RADP\_DFE\_FXTAP2\_38
- RADP\_DFE\_FXTAP2\_39
- RADP\_DFE\_FXTAP2\_4
- RADP\_DFE\_FXTAP2\_40
- RADP\_DFE\_FXTAP2\_41
- RADP\_DFE\_FXTAP2\_42
- RADP\_DFE\_FXTAP2\_43
- RADP\_DFE\_FXTAP2\_44
- RADP\_DFE\_FXTAP2\_45
- RADP\_DFE\_FXTAP2\_46
- RADP\_DFE\_FXTAP2\_47
- RADP\_DFE\_FXTAP2\_48
- RADP\_DFE\_FXTAP2\_49
- RADP\_DFE\_FXTAP2\_5
- RADP\_DFE\_FXTAP2\_50
- RADP\_DFE\_FXTAP2\_51
- RADP\_DFE\_FXTAP2\_52
- RADP\_DFE\_FXTAP2\_53
- RADP\_DFE\_FXTAP2\_54
- RADP\_DFE\_FXTAP2\_55
- RADP\_DFE\_FXTAP2\_56
- RADP\_DFE\_FXTAP2\_57
- RADP\_DFE\_FXTAP2\_58
- RADP\_DFE\_FXTAP2\_59
- RADP\_DFE\_FXTAP2\_6
- RADP\_DFE\_FXTAP2\_60

- RADP\_DFE\_FXTAP2\_61
- RADP\_DFE\_FXTAP2\_62
- RADP\_DFE\_FXTAP2\_63
- RADP\_DFE\_FXTAP2\_64
- RADP\_DFE\_FXTAP2\_65
- RADP\_DFE\_FXTAP2\_66
- RADP\_DFE\_FXTAP2\_67
- RADP\_DFE\_FXTAP2\_68
- RADP\_DFE\_FXTAP2\_69
- RADP\_DFE\_FXTAP2\_7
- RADP\_DFE\_FXTAP2\_70
- RADP\_DFE\_FXTAP2\_71
- RADP\_DFE\_FXTAP2\_72
- RADP\_DFE\_FXTAP2\_73
- RADP\_DFE\_FXTAP2\_74
- RADP\_DFE\_FXTAP2\_75
- RADP\_DFE\_FXTAP2\_76
- RADP\_DFE\_FXTAP2\_77
- RADP\_DFE\_FXTAP2\_78
- RADP\_DFE\_FXTAP2\_79
- RADP\_DFE\_FXTAP2\_8
- RADP\_DFE\_FXTAP2\_80
- RADP\_DFE\_FXTAP2\_81
- RADP\_DFE\_FXTAP2\_82
- RADP\_DFE\_FXTAP2\_83
- RADP\_DFE\_FXTAP2\_84
- RADP\_DFE\_FXTAP2\_85
- RADP\_DFE\_FXTAP2\_86
- RADP\_DFE\_FXTAP2\_87
- RADP\_DFE\_FXTAP2\_88
- RADP\_DFE\_FXTAP2\_89
- RADP\_DFE\_FXTAP2\_9
- RADP\_DFE\_FXTAP2\_90
- RADP\_DFE\_FXTAP2\_91
- RADP\_DFE\_FXTAP2\_92
- RADP\_DFE\_FXTAP2\_93
- RADP\_DFE\_FXTAP2\_94
- RADP\_DFE\_FXTAP2\_95
- RADP\_DFE\_FXTAP2\_96
- RADP\_DFE\_FXTAP2\_97
- RADP\_DFE\_FXTAP2\_98
- RADP\_DFE\_FXTAP2\_99

## Device Support

- Arria 10

## Notes

## Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP2 -to <to> -entity  
<entity name> <value>
```





## XCVR\_A10\_RX\_ADAP\_DFE\_FXTAP2\_SGN

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP2\_SGN\_0
- RADP\_DFE\_FXTAP2\_SGN\_1

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADAP_DFE_FXTAP2_SGN -to <to> -  
entity <entity name> <value>
```

## XCVR\_A10\_RX\_ADP\_DFE\_FXTAP3

A logic option that allows you to specify the coefficient setting for fix tap three in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP3\_0
- RADP\_DFE\_FXTAP3\_1
- RADP\_DFE\_FXTAP3\_10
- RADP\_DFE\_FXTAP3\_100
- RADP\_DFE\_FXTAP3\_101
- RADP\_DFE\_FXTAP3\_102
- RADP\_DFE\_FXTAP3\_103
- RADP\_DFE\_FXTAP3\_104
- RADP\_DFE\_FXTAP3\_105
- RADP\_DFE\_FXTAP3\_106
- RADP\_DFE\_FXTAP3\_107
- RADP\_DFE\_FXTAP3\_108
- RADP\_DFE\_FXTAP3\_109
- RADP\_DFE\_FXTAP3\_11
- RADP\_DFE\_FXTAP3\_110
- RADP\_DFE\_FXTAP3\_111
- RADP\_DFE\_FXTAP3\_112
- RADP\_DFE\_FXTAP3\_113
- RADP\_DFE\_FXTAP3\_114
- RADP\_DFE\_FXTAP3\_115
- RADP\_DFE\_FXTAP3\_116
- RADP\_DFE\_FXTAP3\_117
- RADP\_DFE\_FXTAP3\_118
- RADP\_DFE\_FXTAP3\_119
- RADP\_DFE\_FXTAP3\_12
- RADP\_DFE\_FXTAP3\_120
- RADP\_DFE\_FXTAP3\_121
- RADP\_DFE\_FXTAP3\_122
- RADP\_DFE\_FXTAP3\_123
- RADP\_DFE\_FXTAP3\_124
- RADP\_DFE\_FXTAP3\_125
- RADP\_DFE\_FXTAP3\_126
- RADP\_DFE\_FXTAP3\_127
- RADP\_DFE\_FXTAP3\_13
- RADP\_DFE\_FXTAP3\_14
- RADP\_DFE\_FXTAP3\_15
- RADP\_DFE\_FXTAP3\_16
- RADP\_DFE\_FXTAP3\_17

- RADP\_DFE\_FXTAP3\_18
- RADP\_DFE\_FXTAP3\_19
- RADP\_DFE\_FXTAP3\_2
- RADP\_DFE\_FXTAP3\_20
- RADP\_DFE\_FXTAP3\_21
- RADP\_DFE\_FXTAP3\_22
- RADP\_DFE\_FXTAP3\_23
- RADP\_DFE\_FXTAP3\_24
- RADP\_DFE\_FXTAP3\_25
- RADP\_DFE\_FXTAP3\_26
- RADP\_DFE\_FXTAP3\_27
- RADP\_DFE\_FXTAP3\_28
- RADP\_DFE\_FXTAP3\_29
- RADP\_DFE\_FXTAP3\_3
- RADP\_DFE\_FXTAP3\_30
- RADP\_DFE\_FXTAP3\_31
- RADP\_DFE\_FXTAP3\_32
- RADP\_DFE\_FXTAP3\_33
- RADP\_DFE\_FXTAP3\_34
- RADP\_DFE\_FXTAP3\_35
- RADP\_DFE\_FXTAP3\_36
- RADP\_DFE\_FXTAP3\_37
- RADP\_DFE\_FXTAP3\_38
- RADP\_DFE\_FXTAP3\_39
- RADP\_DFE\_FXTAP3\_4
- RADP\_DFE\_FXTAP3\_40
- RADP\_DFE\_FXTAP3\_41
- RADP\_DFE\_FXTAP3\_42
- RADP\_DFE\_FXTAP3\_43
- RADP\_DFE\_FXTAP3\_44
- RADP\_DFE\_FXTAP3\_45
- RADP\_DFE\_FXTAP3\_46
- RADP\_DFE\_FXTAP3\_47
- RADP\_DFE\_FXTAP3\_48
- RADP\_DFE\_FXTAP3\_49
- RADP\_DFE\_FXTAP3\_5
- RADP\_DFE\_FXTAP3\_50
- RADP\_DFE\_FXTAP3\_51
- RADP\_DFE\_FXTAP3\_52
- RADP\_DFE\_FXTAP3\_53
- RADP\_DFE\_FXTAP3\_54
- RADP\_DFE\_FXTAP3\_55
- RADP\_DFE\_FXTAP3\_56
- RADP\_DFE\_FXTAP3\_57
- RADP\_DFE\_FXTAP3\_58
- RADP\_DFE\_FXTAP3\_59
- RADP\_DFE\_FXTAP3\_6
- RADP\_DFE\_FXTAP3\_60

- RADP\_DFE\_FXTAP3\_61
- RADP\_DFE\_FXTAP3\_62
- RADP\_DFE\_FXTAP3\_63
- RADP\_DFE\_FXTAP3\_64
- RADP\_DFE\_FXTAP3\_65
- RADP\_DFE\_FXTAP3\_66
- RADP\_DFE\_FXTAP3\_67
- RADP\_DFE\_FXTAP3\_68
- RADP\_DFE\_FXTAP3\_69
- RADP\_DFE\_FXTAP3\_7
- RADP\_DFE\_FXTAP3\_70
- RADP\_DFE\_FXTAP3\_71
- RADP\_DFE\_FXTAP3\_72
- RADP\_DFE\_FXTAP3\_73
- RADP\_DFE\_FXTAP3\_74
- RADP\_DFE\_FXTAP3\_75
- RADP\_DFE\_FXTAP3\_76
- RADP\_DFE\_FXTAP3\_77
- RADP\_DFE\_FXTAP3\_78
- RADP\_DFE\_FXTAP3\_79
- RADP\_DFE\_FXTAP3\_8
- RADP\_DFE\_FXTAP3\_80
- RADP\_DFE\_FXTAP3\_81
- RADP\_DFE\_FXTAP3\_82
- RADP\_DFE\_FXTAP3\_83
- RADP\_DFE\_FXTAP3\_84
- RADP\_DFE\_FXTAP3\_85
- RADP\_DFE\_FXTAP3\_86
- RADP\_DFE\_FXTAP3\_87
- RADP\_DFE\_FXTAP3\_88
- RADP\_DFE\_FXTAP3\_89
- RADP\_DFE\_FXTAP3\_9
- RADP\_DFE\_FXTAP3\_90
- RADP\_DFE\_FXTAP3\_91
- RADP\_DFE\_FXTAP3\_92
- RADP\_DFE\_FXTAP3\_93
- RADP\_DFE\_FXTAP3\_94
- RADP\_DFE\_FXTAP3\_95
- RADP\_DFE\_FXTAP3\_96
- RADP\_DFE\_FXTAP3\_97
- RADP\_DFE\_FXTAP3\_98
- RADP\_DFE\_FXTAP3\_99

### Device Support

- Arria 10

## Notes

## Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP3 -to <to> -entity  
<entity name> <value>
```

## XCVR\_A10\_RX\_ADP\_DFE\_FXTAP3\_SGN

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP3\_SGN\_0
- RADP\_DFE\_FXTAP3\_SGN\_1

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP3_SGN -to <to> -  
entity <entity name> <value>
```



## XCVR\_A10\_RX\_ADP\_DFE\_FXTAP4

A logic option that allows you to specify the coefficient setting for floating tap four in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP4\_0
- RADP\_DFE\_FXTAP4\_1
- RADP\_DFE\_FXTAP4\_10
- RADP\_DFE\_FXTAP4\_11
- RADP\_DFE\_FXTAP4\_12
- RADP\_DFE\_FXTAP4\_13
- RADP\_DFE\_FXTAP4\_14
- RADP\_DFE\_FXTAP4\_15
- RADP\_DFE\_FXTAP4\_16
- RADP\_DFE\_FXTAP4\_17
- RADP\_DFE\_FXTAP4\_18
- RADP\_DFE\_FXTAP4\_19
- RADP\_DFE\_FXTAP4\_2
- RADP\_DFE\_FXTAP4\_20
- RADP\_DFE\_FXTAP4\_21
- RADP\_DFE\_FXTAP4\_22
- RADP\_DFE\_FXTAP4\_23
- RADP\_DFE\_FXTAP4\_24
- RADP\_DFE\_FXTAP4\_25
- RADP\_DFE\_FXTAP4\_26
- RADP\_DFE\_FXTAP4\_27
- RADP\_DFE\_FXTAP4\_28
- RADP\_DFE\_FXTAP4\_29
- RADP\_DFE\_FXTAP4\_3
- RADP\_DFE\_FXTAP4\_30
- RADP\_DFE\_FXTAP4\_31
- RADP\_DFE\_FXTAP4\_32
- RADP\_DFE\_FXTAP4\_33
- RADP\_DFE\_FXTAP4\_34
- RADP\_DFE\_FXTAP4\_35
- RADP\_DFE\_FXTAP4\_36
- RADP\_DFE\_FXTAP4\_37
- RADP\_DFE\_FXTAP4\_38
- RADP\_DFE\_FXTAP4\_39
- RADP\_DFE\_FXTAP4\_4
- RADP\_DFE\_FXTAP4\_40
- RADP\_DFE\_FXTAP4\_41
- RADP\_DFE\_FXTAP4\_42

- RADP\_DFE\_FXTAP4\_43
- RADP\_DFE\_FXTAP4\_44
- RADP\_DFE\_FXTAP4\_45
- RADP\_DFE\_FXTAP4\_46
- RADP\_DFE\_FXTAP4\_47
- RADP\_DFE\_FXTAP4\_48
- RADP\_DFE\_FXTAP4\_49
- RADP\_DFE\_FXTAP4\_5
- RADP\_DFE\_FXTAP4\_50
- RADP\_DFE\_FXTAP4\_51
- RADP\_DFE\_FXTAP4\_52
- RADP\_DFE\_FXTAP4\_53
- RADP\_DFE\_FXTAP4\_54
- RADP\_DFE\_FXTAP4\_55
- RADP\_DFE\_FXTAP4\_56
- RADP\_DFE\_FXTAP4\_57
- RADP\_DFE\_FXTAP4\_58
- RADP\_DFE\_FXTAP4\_59
- RADP\_DFE\_FXTAP4\_6
- RADP\_DFE\_FXTAP4\_60
- RADP\_DFE\_FXTAP4\_61
- RADP\_DFE\_FXTAP4\_62
- RADP\_DFE\_FXTAP4\_63
- RADP\_DFE\_FXTAP4\_7
- RADP\_DFE\_FXTAP4\_8
- RADP\_DFE\_FXTAP4\_9

## Device Support

- Arria 10

## Notes

## Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP4 -to <to> -entity  
<entity name> <value>
```



## XCVR\_A10\_RX\_ADAP\_DFE\_FXTAP4\_SGN

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP4\_SGN\_0
- RADP\_DFE\_FXTAP4\_SGN\_1

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADAP_DFE_FXTAP4_SGN -to <to> -  
entity <entity name> <value>
```

## XCVR\_A10\_RX\_ADP\_DFE\_FXTAP5

A logic option that allows you to specify the coefficient setting for fix tap five in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP5\_0
- RADP\_DFE\_FXTAP5\_1
- RADP\_DFE\_FXTAP5\_10
- RADP\_DFE\_FXTAP5\_11
- RADP\_DFE\_FXTAP5\_12
- RADP\_DFE\_FXTAP5\_13
- RADP\_DFE\_FXTAP5\_14
- RADP\_DFE\_FXTAP5\_15
- RADP\_DFE\_FXTAP5\_16
- RADP\_DFE\_FXTAP5\_17
- RADP\_DFE\_FXTAP5\_18
- RADP\_DFE\_FXTAP5\_19
- RADP\_DFE\_FXTAP5\_2
- RADP\_DFE\_FXTAP5\_20
- RADP\_DFE\_FXTAP5\_21
- RADP\_DFE\_FXTAP5\_22
- RADP\_DFE\_FXTAP5\_23
- RADP\_DFE\_FXTAP5\_24
- RADP\_DFE\_FXTAP5\_25
- RADP\_DFE\_FXTAP5\_26
- RADP\_DFE\_FXTAP5\_27
- RADP\_DFE\_FXTAP5\_28
- RADP\_DFE\_FXTAP5\_29
- RADP\_DFE\_FXTAP5\_3
- RADP\_DFE\_FXTAP5\_30
- RADP\_DFE\_FXTAP5\_31
- RADP\_DFE\_FXTAP5\_32
- RADP\_DFE\_FXTAP5\_33
- RADP\_DFE\_FXTAP5\_34
- RADP\_DFE\_FXTAP5\_35
- RADP\_DFE\_FXTAP5\_36
- RADP\_DFE\_FXTAP5\_37
- RADP\_DFE\_FXTAP5\_38
- RADP\_DFE\_FXTAP5\_39
- RADP\_DFE\_FXTAP5\_4
- RADP\_DFE\_FXTAP5\_40
- RADP\_DFE\_FXTAP5\_41
- RADP\_DFE\_FXTAP5\_42

- RADP\_DFE\_FXTAP5\_43
- RADP\_DFE\_FXTAP5\_44
- RADP\_DFE\_FXTAP5\_45
- RADP\_DFE\_FXTAP5\_46
- RADP\_DFE\_FXTAP5\_47
- RADP\_DFE\_FXTAP5\_48
- RADP\_DFE\_FXTAP5\_49
- RADP\_DFE\_FXTAP5\_5
- RADP\_DFE\_FXTAP5\_50
- RADP\_DFE\_FXTAP5\_51
- RADP\_DFE\_FXTAP5\_52
- RADP\_DFE\_FXTAP5\_53
- RADP\_DFE\_FXTAP5\_54
- RADP\_DFE\_FXTAP5\_55
- RADP\_DFE\_FXTAP5\_56
- RADP\_DFE\_FXTAP5\_57
- RADP\_DFE\_FXTAP5\_58
- RADP\_DFE\_FXTAP5\_59
- RADP\_DFE\_FXTAP5\_6
- RADP\_DFE\_FXTAP5\_60
- RADP\_DFE\_FXTAP5\_61
- RADP\_DFE\_FXTAP5\_62
- RADP\_DFE\_FXTAP5\_63
- RADP\_DFE\_FXTAP5\_7
- RADP\_DFE\_FXTAP5\_8
- RADP\_DFE\_FXTAP5\_9

## Device Support

- Arria 10

## Notes

## Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP5 -to <to> -entity  
<entity name> <value>
```

## XCVR\_A10\_RX\_ADP\_DFE\_FXTAP5\_SGN

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP5\_SGN\_0
- RADP\_DFE\_FXTAP5\_SGN\_1

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP5_SGN -to <to> -  
entity <entity name> <value>
```



## XCVR\_A10\_RX\_ADP\_DFE\_FXTAP6

A logic option that allows you to specify the coefficient setting for fix tap six in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP6\_0
- RADP\_DFE\_FXTAP6\_1
- RADP\_DFE\_FXTAP6\_10
- RADP\_DFE\_FXTAP6\_11
- RADP\_DFE\_FXTAP6\_12
- RADP\_DFE\_FXTAP6\_13
- RADP\_DFE\_FXTAP6\_14
- RADP\_DFE\_FXTAP6\_15
- RADP\_DFE\_FXTAP6\_16
- RADP\_DFE\_FXTAP6\_17
- RADP\_DFE\_FXTAP6\_18
- RADP\_DFE\_FXTAP6\_19
- RADP\_DFE\_FXTAP6\_2
- RADP\_DFE\_FXTAP6\_20
- RADP\_DFE\_FXTAP6\_21
- RADP\_DFE\_FXTAP6\_22
- RADP\_DFE\_FXTAP6\_23
- RADP\_DFE\_FXTAP6\_24
- RADP\_DFE\_FXTAP6\_25
- RADP\_DFE\_FXTAP6\_26
- RADP\_DFE\_FXTAP6\_27
- RADP\_DFE\_FXTAP6\_28
- RADP\_DFE\_FXTAP6\_29
- RADP\_DFE\_FXTAP6\_3
- RADP\_DFE\_FXTAP6\_30
- RADP\_DFE\_FXTAP6\_31
- RADP\_DFE\_FXTAP6\_4
- RADP\_DFE\_FXTAP6\_5
- RADP\_DFE\_FXTAP6\_6
- RADP\_DFE\_FXTAP6\_7
- RADP\_DFE\_FXTAP6\_8
- RADP\_DFE\_FXTAP6\_9

### Device Support

- Arria 10

## Notes

## Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP6 -to <to> -entity  
<entity name> <value>
```

## XCVR\_A10\_RX\_ADAP\_DFE\_FXTAP6\_SGN

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP6\_SGN\_0
- RADP\_DFE\_FXTAP6\_SGN\_1

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADAP_DFE_FXTAP6_SGN -to <to> -  
entity <entity name> <value>
```

## XCVR\_A10\_RX\_ADP\_DFE\_FXTAP7

A logic option that allows you to specify the coefficient setting for fix tap seven in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP7\_0
- RADP\_DFE\_FXTAP7\_1
- RADP\_DFE\_FXTAP7\_10
- RADP\_DFE\_FXTAP7\_11
- RADP\_DFE\_FXTAP7\_12
- RADP\_DFE\_FXTAP7\_13
- RADP\_DFE\_FXTAP7\_14
- RADP\_DFE\_FXTAP7\_15
- RADP\_DFE\_FXTAP7\_16
- RADP\_DFE\_FXTAP7\_17
- RADP\_DFE\_FXTAP7\_18
- RADP\_DFE\_FXTAP7\_19
- RADP\_DFE\_FXTAP7\_2
- RADP\_DFE\_FXTAP7\_20
- RADP\_DFE\_FXTAP7\_21
- RADP\_DFE\_FXTAP7\_22
- RADP\_DFE\_FXTAP7\_23
- RADP\_DFE\_FXTAP7\_24
- RADP\_DFE\_FXTAP7\_25
- RADP\_DFE\_FXTAP7\_26
- RADP\_DFE\_FXTAP7\_27
- RADP\_DFE\_FXTAP7\_28
- RADP\_DFE\_FXTAP7\_29
- RADP\_DFE\_FXTAP7\_3
- RADP\_DFE\_FXTAP7\_30
- RADP\_DFE\_FXTAP7\_31
- RADP\_DFE\_FXTAP7\_4
- RADP\_DFE\_FXTAP7\_5
- RADP\_DFE\_FXTAP7\_6
- RADP\_DFE\_FXTAP7\_7
- RADP\_DFE\_FXTAP7\_8
- RADP\_DFE\_FXTAP7\_9

### Device Support

- Arria 10



## Notes

## Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP7 -to <to> -entity  
<entity name> <value>
```



## XCVR\_A10\_RX\_ADP\_DFE\_FXTAP7\_SGN

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP7\_SGN\_0
- RADP\_DFE\_FXTAP7\_SGN\_1

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP7_SGN -to <to> -  
entity <entity name> <value>
```



## XCVR\_A10\_RX\_ADP\_DFE\_FXTAP8

A logic option that allows you to specify the coefficient setting for fix tap eight in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP8\_0
- RADP\_DFE\_FXTAP8\_1
- RADP\_DFE\_FXTAP8\_10
- RADP\_DFE\_FXTAP8\_11
- RADP\_DFE\_FXTAP8\_12
- RADP\_DFE\_FXTAP8\_13
- RADP\_DFE\_FXTAP8\_14
- RADP\_DFE\_FXTAP8\_15
- RADP\_DFE\_FXTAP8\_16
- RADP\_DFE\_FXTAP8\_17
- RADP\_DFE\_FXTAP8\_18
- RADP\_DFE\_FXTAP8\_19
- RADP\_DFE\_FXTAP8\_2
- RADP\_DFE\_FXTAP8\_20
- RADP\_DFE\_FXTAP8\_21
- RADP\_DFE\_FXTAP8\_22
- RADP\_DFE\_FXTAP8\_23
- RADP\_DFE\_FXTAP8\_24
- RADP\_DFE\_FXTAP8\_25
- RADP\_DFE\_FXTAP8\_26
- RADP\_DFE\_FXTAP8\_27
- RADP\_DFE\_FXTAP8\_28
- RADP\_DFE\_FXTAP8\_29
- RADP\_DFE\_FXTAP8\_3
- RADP\_DFE\_FXTAP8\_30
- RADP\_DFE\_FXTAP8\_31
- RADP\_DFE\_FXTAP8\_32
- RADP\_DFE\_FXTAP8\_33
- RADP\_DFE\_FXTAP8\_34
- RADP\_DFE\_FXTAP8\_35
- RADP\_DFE\_FXTAP8\_36
- RADP\_DFE\_FXTAP8\_37
- RADP\_DFE\_FXTAP8\_38
- RADP\_DFE\_FXTAP8\_39
- RADP\_DFE\_FXTAP8\_4
- RADP\_DFE\_FXTAP8\_40
- RADP\_DFE\_FXTAP8\_41
- RADP\_DFE\_FXTAP8\_42

- RADP\_DFE\_FXTAP8\_43
- RADP\_DFE\_FXTAP8\_44
- RADP\_DFE\_FXTAP8\_45
- RADP\_DFE\_FXTAP8\_46
- RADP\_DFE\_FXTAP8\_47
- RADP\_DFE\_FXTAP8\_48
- RADP\_DFE\_FXTAP8\_49
- RADP\_DFE\_FXTAP8\_5
- RADP\_DFE\_FXTAP8\_50
- RADP\_DFE\_FXTAP8\_51
- RADP\_DFE\_FXTAP8\_52
- RADP\_DFE\_FXTAP8\_53
- RADP\_DFE\_FXTAP8\_54
- RADP\_DFE\_FXTAP8\_55
- RADP\_DFE\_FXTAP8\_56
- RADP\_DFE\_FXTAP8\_57
- RADP\_DFE\_FXTAP8\_58
- RADP\_DFE\_FXTAP8\_59
- RADP\_DFE\_FXTAP8\_6
- RADP\_DFE\_FXTAP8\_60
- RADP\_DFE\_FXTAP8\_61
- RADP\_DFE\_FXTAP8\_62
- RADP\_DFE\_FXTAP8\_63
- RADP\_DFE\_FXTAP8\_7
- RADP\_DFE\_FXTAP8\_8
- RADP\_DFE\_FXTAP8\_9

## Device Support

- Arria 10

## Notes

## Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP8 -to <to> -entity  
<entity name> <value>
```

## XCVR\_A10\_RX\_ADAP\_DFE\_FXTAP8\_SGN

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP8\_SGN\_0
- RADP\_DFE\_FXTAP8\_SGN\_1

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADAP_DFE_FXTAP8_SGN -to <to> -  
entity <entity name> <value>
```

## XCVR\_A10\_RX\_ADP\_DFE\_FXTAP9

A logic option that allows you to specify the coefficient setting for fix tap nine in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP9\_0
- RADP\_DFE\_FXTAP9\_1
- RADP\_DFE\_FXTAP9\_10
- RADP\_DFE\_FXTAP9\_11
- RADP\_DFE\_FXTAP9\_12
- RADP\_DFE\_FXTAP9\_13
- RADP\_DFE\_FXTAP9\_14
- RADP\_DFE\_FXTAP9\_15
- RADP\_DFE\_FXTAP9\_16
- RADP\_DFE\_FXTAP9\_17
- RADP\_DFE\_FXTAP9\_18
- RADP\_DFE\_FXTAP9\_19
- RADP\_DFE\_FXTAP9\_2
- RADP\_DFE\_FXTAP9\_20
- RADP\_DFE\_FXTAP9\_21
- RADP\_DFE\_FXTAP9\_22
- RADP\_DFE\_FXTAP9\_23
- RADP\_DFE\_FXTAP9\_24
- RADP\_DFE\_FXTAP9\_25
- RADP\_DFE\_FXTAP9\_26
- RADP\_DFE\_FXTAP9\_27
- RADP\_DFE\_FXTAP9\_28
- RADP\_DFE\_FXTAP9\_29
- RADP\_DFE\_FXTAP9\_3
- RADP\_DFE\_FXTAP9\_30
- RADP\_DFE\_FXTAP9\_31
- RADP\_DFE\_FXTAP9\_32
- RADP\_DFE\_FXTAP9\_33
- RADP\_DFE\_FXTAP9\_34
- RADP\_DFE\_FXTAP9\_35
- RADP\_DFE\_FXTAP9\_36
- RADP\_DFE\_FXTAP9\_37
- RADP\_DFE\_FXTAP9\_38
- RADP\_DFE\_FXTAP9\_39
- RADP\_DFE\_FXTAP9\_4
- RADP\_DFE\_FXTAP9\_40
- RADP\_DFE\_FXTAP9\_41
- RADP\_DFE\_FXTAP9\_42

- RADP\_DFE\_FXTAP9\_43
- RADP\_DFE\_FXTAP9\_44
- RADP\_DFE\_FXTAP9\_45
- RADP\_DFE\_FXTAP9\_46
- RADP\_DFE\_FXTAP9\_47
- RADP\_DFE\_FXTAP9\_48
- RADP\_DFE\_FXTAP9\_49
- RADP\_DFE\_FXTAP9\_5
- RADP\_DFE\_FXTAP9\_50
- RADP\_DFE\_FXTAP9\_51
- RADP\_DFE\_FXTAP9\_52
- RADP\_DFE\_FXTAP9\_53
- RADP\_DFE\_FXTAP9\_54
- RADP\_DFE\_FXTAP9\_55
- RADP\_DFE\_FXTAP9\_56
- RADP\_DFE\_FXTAP9\_57
- RADP\_DFE\_FXTAP9\_58
- RADP\_DFE\_FXTAP9\_59
- RADP\_DFE\_FXTAP9\_6
- RADP\_DFE\_FXTAP9\_60
- RADP\_DFE\_FXTAP9\_61
- RADP\_DFE\_FXTAP9\_62
- RADP\_DFE\_FXTAP9\_63
- RADP\_DFE\_FXTAP9\_7
- RADP\_DFE\_FXTAP9\_8
- RADP\_DFE\_FXTAP9\_9

## Device Support

- Arria 10

## Notes

## Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP9 -to <to> -entity  
<entity name> <value>
```

## XCVR\_A10\_RX\_ADP\_DFE\_FXTAP9\_SGN

### Type

Enumeration

### Values

- RADP\_DFE\_FXTAP9\_SGN\_0
- RADP\_DFE\_FXTAP9\_SGN\_1

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP9_SGN -to <to> -  
entity <entity name> <value>
```



## XCVR\_A10\_RX\_ADP\_VGA\_SEL

A logic option that allows you to controls the amount of output voltage swing on the variable gain amplifier. The amount of voltage swing is propotional to the setting where '0' gives the lowest swing and '7' gives the largest swing. This option is only valid when equalizer operates in manual mode.

### Type

Enumeration

### Values

- RADP\_VGA\_SEL\_0
- RADP\_VGA\_SEL\_1
- RADP\_VGA\_SEL\_2
- RADP\_VGA\_SEL\_3
- RADP\_VGA\_SEL\_4
- RADP\_VGA\_SEL\_5
- RADP\_VGA\_SEL\_6
- RADP\_VGA\_SEL\_7

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_VGA_SEL -to <to> -entity  
<entity name> <value>
```

## XCVR\_A10\_RX\_EQ\_BW\_SEL

### Type

Enumeration

### Values

- EQ\_BW\_1
- EQ\_BW\_2
- EQ\_BW\_3
- EQ\_BW\_4

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_RX_EQ_BW_SEL -to <to> -entity  
<entity name> <value>
```



## XCVR\_A10\_RX\_EQ\_DC\_GAIN\_TRIM

A logic option that allows you to control the amount of DC gain on equalizer in high gain mode. The amount of DC gain is proportional to the setting where '0' gives the lowest DC gain and '28' gives the largest DC gain.

### Type

Enumeration

### Values

- NO\_DC\_GAIN
- STG1\_GAIN7
- STG2\_GAIN7
- STG3\_GAIN7
- STG4\_GAIN7

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_RX_EQ_DC_GAIN_TRIM -to <to> -entity  
<entity name> <value>
```

## XCVR\_A10\_RX\_LINK

A logic option that allows you to specify the type of communication for the receiver link. Quartus Prime will use this option to determine the legal data rate and power mode for the link.

### Type

Enumeration

### Values

- LR
- SR

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_RX_LINK -to <to> -entity <entity  
name> <value>
```



## XCVR\_A10\_RX\_ONE\_STAGE\_ENABLE

### Type

Enumeration

### Values

- NON\_S1\_MODE
- S1\_MODE

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_RX_ONE_STAGE_ENABLE -to <to> -entity  
<entity name> <value>
```

## XCVR\_A10\_RX\_TERM\_SEL

A logic option that allows you to specify the termination value of the receiver pin.

### Type

Enumeration

### Values

- R\_EXT0
- R\_R1
- R\_R2

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_RX_TERM_SEL -to <to> -entity <entity  
name> <value>
```



## XCVR\_A10\_TX\_COMPENSATION\_EN

A logic option that allows you to turn on the compensation for transmitter data rate above 9 Gbps. Turning on this option draws more power on the transmitter buffer.

### Type

Enumeration

### Values

- DISABLE
- ENABLE

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_TX_COMPENSATION_EN -to <to> -entity  
<entity name> <value>
```

## XCVR\_A10\_TX\_LINK

A logic option that allows you to specify the type of communication for the transmitter link. Quartus Prime will use this option to determine the legal data rate and power mode for the link.

### Type

Enumeration

### Values

- LR
- SR

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_TX_LINK -to <to> -entity <entity  
name> <value>
```



## XCVR\_A10\_TX\_PRE\_EMP\_SIGN\_1ST\_POST\_TAP

A logic option that allows you to specify the output polarity of the transmitter pre-emphasis first post-tap.

### Type

Enumeration

### Values

- FIR\_POST\_1T\_NEG
- FIR\_POST\_1T\_POS

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_TX_PRE_EMP_SIGN_1ST_POST_TAP -to  
<to> -entity <entity name> <value>
```

## XCVR\_A10\_TX\_PRE\_EMP\_SIGN\_2ND\_POST\_TAP

A logic option that allows you to specify the output polarity of the transmitter pre-emphasis second post-tap.

### Type

Enumeration

### Values

- FIR\_POST\_2T\_NEG
- FIR\_POST\_2T\_POS

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_TX_PRE_EMP_SIGN_2ND_POST_TAP -to  
<to> -entity <entity name> <value>
```



## XCVR\_A10\_TX\_PRE\_EMP\_SIGN\_PRE\_TAP\_1T

A logic option that allows you to specify the output polarity of the transmitter pre-emphasis first pre-tap.

### Type

Enumeration

### Values

- FIR\_PRE\_1T\_NEG
- FIR\_PRE\_1T\_POS

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_TX_PRE_EMP_SIGN_PRE_TAP_1T -to <to> -  
entity <entity name> <value>
```

## XCVR\_A10\_TX\_PRE\_EMP\_SIGN\_PRE\_TAP\_2T

A logic option that allows you to specify the output polarity of the transmitter pre-emphasis second pre-tap.

### Type

Enumeration

### Values

- FIR\_PRE\_2T\_NEG
- FIR\_PRE\_2T\_POS

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_TX_PRE_EMP_SIGN_PRE_TAP_2T -to <to> -  
entity <entity name> <value>
```



## XCVR\_A10\_TX\_PRE\_EMP\_SWITCHING\_CTRL\_1ST\_POST\_TAP

A logic option that allows you to control the magnitude of transmitter pre-emphasis first post-tap. Legal values are: 0 to 25.

### Type

Integer

### Device Support

- Arria 10

### INTEGER\_RANGE

0, 25

### Notes

### Syntax

```
set_instance_assignment -name  
XCVR_A10_TX_PRE_EMP_SWITCHING_CTRL_1ST_POST_TAP -to <to> -entity <entity name>  
<value>
```

## XCVR\_A10\_TX\_PRE\_EMP\_SWITCHING\_CTRL\_2ND\_POST\_TAP

A logic option that allows you to control the magnitude of transmitter pre-emphasis second post-tap.  
Legal values are: 0 to 12.

### Type

Integer

### Device Support

- Arria 10

### INTEGER\_RANGE

0, 12

### Notes

### Syntax

```
set_instance_assignment -name  
XCVR_A10_TX_PRE_EMP_SWITCHING_CTRL_2ND_POST_TAP -to <to> -entity <entity name>  
<value>
```

## XCVR\_A10\_TX\_PRE\_EMP\_SWITCHING\_CTRL\_PRE\_TAP\_1T

A logic option that allows you to control the magnitude of transmitter pre-emphasis first pre-tap. Legal values are: 0 to 16.

### Type

Integer

### Device Support

- Arria 10

### INTEGER\_RANGE

0, 16

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_TX_PRE_EMP_SWITCHING_CTRL_PRE_TAP_1T  
-to <to> -entity <entity name> <value>
```

## XCVR\_A10\_TX\_PRE\_EMP\_SWITCHING\_CTRL\_PRE\_TAP\_2T

A logic option that allows you to control the magnitude of transmitter pre-emphasis second pre-tap. Legal values are: 0 to 7.

### Type

Integer

### Device Support

- Arria 10

### INTEGER\_RANGE

0, 7

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_TX_PRE_EMP_SWITCHING_CTRL_PRE_TAP_2T  
-to <to> -entity <entity name> <value>
```



## XCVR\_A10\_TX\_SLEW\_RATE\_CTRL

### Type

Enumeration

### Values

- SLEW\_R0
- SLEW\_R1
- SLEW\_R2
- SLEW\_R3
- SLEW\_R4
- SLEW\_R5
- SLEW\_R6
- SLEW\_R7

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_TX_SLEW_RATE_CTRL -to <to> -entity  
<entity name> <value>
```

## XCVR\_A10\_TX\_TERM\_SEL

### Type

Enumeration

### Values

- R\_R1
- R\_R2

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_TX_TERM_SEL -to <to> -entity <entity  
name> <value>
```



## XCVR\_A10\_TX\_VOD\_OUTPUT\_SWING\_CTRL

A logic option that allows you to control the transmitter output swing level. Legal values are: 0 to 31.

### Type

Integer

### Device Support

- Arria 10

### INTEGER\_RANGE

0, 31

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_TX_VOD_OUTPUT_SWING_CTRL -to <to> -  
entity <entity name> <value>
```

## XCVR\_A10\_TX\_XTX\_PATH\_ANALOG\_MODE

### Type

Enumeration

### Values

- CEI\_11100\_LR
- CEI\_11100\_SR
- CEI\_4976\_LR
- CEI\_4976\_SR
- CEI\_6375\_LR
- CEI\_6375\_SR
- CEI\_9950\_LR
- CEI\_9950\_SR
- CPRI\_12500
- CPRI\_E12LVII
- CPRI\_E12LVIII
- CPRI\_E24LVII
- CPRI\_E24LVIII
- CPRI\_E30LVII
- CPRI\_E30LVIII
- CPRI\_E48LVII
- CPRI\_E48LVIII
- CPRI\_E60LVII
- CPRI\_E60LVIII
- CPRI\_E6LVII
- CPRI\_E6LVIII
- CPRI\_E96LVIII
- CPRI\_E99LVIII
- HIGIG\_4062
- HIGIG\_5000
- HIGIG\_6250
- HIGIG\_6562
- IEEE\_10G\_BASE\_CR\_10312
- IEEE\_10G\_KR\_10312
- IEEE\_40G\_BASE\_KR\_10312
- INTERLAKEN\_11100
- INTERLAKEN\_12500
- INTERLAKEN\_6375
- JESD204\_A\_B\_12500
- JESD204\_A\_B\_6375
- QSGMII\_5000
- SERIAL\_LITE\_III\_16400
- SERIAL\_LITE\_III\_17400
- SFI\_S\_6250
- SRIO\_5000\_LR

- SRIO\_5000\_MR
- SRIO\_5000\_SR
- SRIO\_6250\_LR
- SRIO\_6250\_MR
- SRIO\_6250\_SR
- USER\_CUSTOM

### Device Support

- Arria 10

### Notes

### Syntax

```
set_instance_assignment -name XCVR_A10_TX_XTX_PATH_ANALOG_MODE -to <to> -  
entity <entity name> <value>
```

## XCVR\_ANALOG\_SETTINGS\_PROTOCOL

Specify protocol and its variant that are used to determine electrical analog settings for the transceiver.

### Old Name

HSSI\_ANALOG\_SETTINGS\_PROTOCOL

### Type

Enumeration

### Values

- 10G\_KR\_10312
- BASIC
- CEI
- CPRI
- CPRI\_E12HV
- CPRI\_E12LV
- CPRI\_E12LVII
- CPRI\_E24LV
- CPRI\_E24LVII
- CPRI\_E24LVIII
- CPRI\_E30LV
- CPRI\_E30LVII
- CPRI\_E30LVIII
- CPRI\_E48LVII
- CPRI\_E48LVIII
- CPRI\_E60LVII
- CPRI\_E60LVIII
- CPRI\_E6HV
- CPRI\_E6LV
- CPRI\_E6LVII
- CPRI\_E96LVIII
- DP\_1620
- DP\_2700
- DP\_5400
- GBE\_1250
- GIGE
- GPON\_1244
- GPON\_155
- GPON\_2488
- GPON\_622
- INTERLAKEN
- INTERLAKEN\_3125
- INTERLAKEN\_6375
- OBSAI\_1536
- OBSAI\_3072
- OBSAI\_6144

- OBSAI\_768
- PCIE\_CABLE
- PCIE\_GEN1
- PCIE\_GEN1\_3P5DB
- PCIE\_GEN2
- PCIE\_GEN2\_3P5DB
- PCIE\_GEN2\_6DB
- PCIE\_GEN3
- QPI
- QSGMII\_5000
- SATA1\_I
- SATA1\_M
- SATA1\_X
- SATA2\_I
- SATA2\_M
- SATA2\_X
- SDI\_1485\_HD
- SDI\_270\_SD
- SDI\_2970\_3G
- SFIS
- SONET
- SONET\_OC12\_622
- SONET\_OC192\_9953
- SONET\_OC3\_155
- SONET\_OC48\_2488
- SPAUI\_6250
- SRIO
- SRIO\_1250\_LR
- SRIO\_1250\_SR
- SRIO\_2500\_LR
- SRIO\_2500\_SR
- SRIO\_3125\_LR
- SRIO\_3125\_SR
- SRIO\_5000\_LR
- SRIO\_5000\_MR
- SRIO\_5000\_SR
- SRIO\_6250\_LR
- SRIO\_6250\_MR
- SRIO\_6250\_SR
- TENG\_1588
- TENG\_BASER
- TENG\_SDI
- XAUI
- XAUI\_3125

## Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

## Notes

This assignment supports Fitter wildcards.

## Syntax

```
set_instance_assignment -name XCVR_ANALOG_SETTINGS_PROTOCOL -to <to> -  
entity <entity name> <value>
```





## XCVR\_GT\_IO\_PIN\_TERMINATION

Allows the Compiler to configure the GT transceiver termination value.

### Type

Integer

### Device Support

- Arria V GZ
- Stratix V

### INTEGER\_RANGE

0, 15

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_GT_IO_PIN_TERMINATION -to <to> -entity  
<entity name> <value>
```

## XCVR\_GT\_RX\_COMMON\_MODE\_VOLTAGE

GT receiver buffer common-mode voltage.

### Type

Enumeration

### Values

- VTT\_0P35V
- VTT\_0P50V
- VTT\_0P55V
- VTT\_0P60V
- VTT\_0P65V
- VTT\_0P70V
- VTT\_0P75V
- VTT\_0P80V
- VTT\_VCMOFF0
- VTT\_VCMOFF1
- VTT\_VCMOFF2
- VTT\_VCMOFF3
- VTT\_VCMOFF4
- VTT\_VCMOFF5
- VTT\_VCMOFF6
- VTT\_VCMOFF7

### Device Support

- Arria V GZ
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_GT_RX_COMMON_MODE_VOLTAGE -to <to> -  
entity <entity name> <value>
```

## XCVR\_GT\_RX\_CTLE

Static control for the continuous time equalizer in the receiver buffer.

### Type

Integer

### Device Support

- Arria V GZ
- Stratix V

### INTEGER\_RANGE

0, 8

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_GT_RX_CTLE -to <to> -entity <entity  
name> <value>
```

## XCVR\_GT\_RX\_DC\_GAIN

Controls the amount of a stage receive-buffer DC gain.

### Type

Integer

### Device Support

- Arria V GZ
- Stratix V

### INTEGER\_RANGE

0, 19

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_GT_RX_DC_GAIN -to <to> -entity <entity  
name> <value>
```

## XCVR\_GT\_TX\_COMMON\_MODE\_VOLTAGE

GT Transmitter common-mode driver voltage

### Type

Enumeration

### Values

- GROUNDED
- PULL\_DN
- PULL\_UP
- PULL\_UP\_TO\_VCCELA
- TRISTATED1
- VOLT\_0P35V
- VOLT\_0P50V
- VOLT\_0P55V
- VOLT\_0P60V
- VOLT\_0P65V
- VOLT\_0P70V
- VOLT\_0P75V
- VOLT\_0P80V

### Device Support

- Arria V GZ
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_GT_TX_COMMON_MODE_VOLTAGE -to <to> -  
entity <entity name> <value>
```

## XCVR\_GT\_TX\_PRE\_EMP\_1ST\_POST\_TAP

Specifies the GT transmitter preemphasis first post-tap setting value.

### Type

Integer

### Device Support

- Arria V GZ
- Stratix V

### INTEGER\_RANGE

0, 31

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_GT_TX_PRE_EMP_1ST_POST_TAP -to <to> -  
entity <entity name> <value>
```



## XCVR\_GT\_TX\_PRE\_EMP\_INV\_PRE\_TAP

Inverts the GT transmitter preemphasis pre-tap setting value.

### Type

Boolean

### Device Support

- Arria V GZ
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_GT_TX_PRE_EMP_INV_PRE_TAP -to <to> -  
entity <entity name> <value>
```

## XCVR\_GT\_TX\_PRE\_EMP\_PRE\_TAP

Specifies the GT transmitter preemphasis pre-tap setting value.

### Type

Integer

### Device Support

- Arria V GZ
- Stratix V

### INTEGER\_RANGE

0, 31

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_GT_TX_PRE_EMP_PRE_TAP -to <to> -entity  
<entity name> <value>
```



## XCVR\_GT\_TX\_VOD\_MAIN\_TAP

Differential output voltage setting for GT.

### Type

Integer

### Device Support

- Arria V GZ
- Stratix V

### INTEGER\_RANGE

0, 5

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_GT_TX_VOD_MAIN_TAP -to <to> -entity  
<entity name> <value>
```

## XCVR\_IO\_PIN\_TERMINATION

Allows the Compiler to configure the Transceiver Termination value for a GXB I/O pin. It specifies the intended Transceiver Termination value for the specified GXB I/O pin.

### Old Name

GXB\_IO\_PIN\_TERMINATION

### Type

Enumeration

### Values

- 100\_OHMS
- 120\_OHMS
- 150\_OHMS
- 85\_OHMS
- EXTERNAL\_RESISTOR

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_IO_PIN_TERMINATION -to <to> -entity  
<entity name> <value>
```

## XCVR\_RECONFIG\_GROUP

Assigns the node you specify to a transceiver Avalon Memory-Mapped interface group. The Avalon Memory-Mapped interfaces of an RX-only channel and a TX-only channel, or a CDR PLL and a TX-only channel, can be merged and placed into one transceiver channel. You can assign this option to the instance names of the transceiver Avalon Memory-Mapped interfaces you want the Fitter to merge. You can also assign this to option to a CDR PLL instance name and the transceiver TX (or RX) positive pin name of a TX-only (or RX-only) channel, instead of the corresponding transceiver Avalon Memory-Mapped interface instance name. Assigning this option to two nodes directs the Fitter to view the specified nodes as single group. The Fitter does not automatically merge the transceiver Avalon Memory-Mapped interfaces; by default a CDR PLL, RX-only channel, and a TX-only channel map to three different transceiver channels. If the Avalon Memory-Mapped interfaces of the transceiver channels can be merged into one Avalon Memory-Mapped interface, the Fitter merges and places them in the same transceiver channel. If the Fitter cannot merge the transceiver channels, your compilation will result in an error.

### Type

String

### Device Support

- Arria 10

### Notes

This assignment supports wildcards.

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_RECONFIG_GROUP -to <to> -entity <entity  
name> <value>
```

### Example

```
set_instance_assignment -name XCVR_RECONFIG_GROUP myChannel -to  
output_pin[0]  
set_instance_assignment -name XCVR_RECONFIG_GROUP myChannel -to input_pin[1]
```

## XCVR\_REFCLK\_PIN\_TERMINATION

Allows the Compiler to configure the Termination value for a dedicated refclk pin. It specifies the intended Termination value for the specified refclk pin.

### Old Name

GXB\_REFCLK\_PIN\_TERMINATION

### Type

Enumeration

### Values

- AC\_COUPLING
- DC\_COUPLING\_EXTERNAL\_RESISTOR
- DC\_COUPLING\_INTERNAL\_100\_OHMS

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_REFCLK_PIN_TERMINATION -to <to> -entity  
<entity name> <value>
```

## XCVR\_RX\_ACGAIN\_A

Sets reference voltage on EQA

### Type

Enumeration

### Values

- AREF\_VOLT\_0
- AREF\_VOLT\_0P5
- AREF\_VOLT\_0P75
- AREF\_VOLT\_1P0

### Device Support

- Arria V
- Cyclone V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_RX_ACGAIN_A -to <to> -entity <entity  
name> <value>
```

## XCVR\_RX\_ACGAIN\_V

Sets reference voltage on EQV

### Type

Enumeration

### Values

- VREF\_VOLT\_0
- VREF\_VOLT\_0P5
- VREF\_VOLT\_0P75
- VREF\_VOLT\_1P0

### Device Support

- Arria V
- Cyclone V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_RX_ACGAIN_V -to <to> -entity <entity  
name> <value>
```



## XCVR\_RX\_BYPASS\_EQ\_STAGES\_234

Bypasses continuous time equalizer stages 2, 3, and 4 to save power. This assignment eliminates significant AC gain on the equalizer and is appropriate for chip-to-chip short range communication on a PCB.

### Type

Enumeration

### Values

- ALL\_STAGES\_ENABLED
- BYPASS\_STAGES\_234

### Device Support

- Arria V GZ
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_RX_BYPASS_EQ_STAGES_234 -to <to> -entity  
<entity name> <value>
```

## XCVR\_RX\_COMMON\_MODE\_VOLTAGE

Receiver buffer common-mode voltage.

### Type

Enumeration

### Values

- TRISTATE1
- VTT\_0P35V
- VTT\_0P50V
- VTT\_0P55V
- VTT\_0P60V
- VTT\_0P65V
- VTT\_0P70V
- VTT\_0P75V
- VTT\_0P80V
- VTT\_PDN\_STRONG
- VTT\_PDN\_WEAK
- VTT\_PUP\_STRONG
- VTT\_PUP\_WEAK

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_RX_COMMON_MODE_VOLTAGE -to <to> -entity  
<entity name> <value>
```





## XCVR\_RX\_DC\_GAIN

Controls the amount of a stage receive-buffer DC gain.

### Type

Integer

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### INTEGER\_RANGE

0, 19

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_RX_DC_GAIN -to <to> -entity <entity  
name> <value>
```

## XCVR\_RX\_ENABLE\_LINEAR\_EQUALIZER\_PCIEMODE

If enabled, equalizer gain control is driven by the PCS block for PCI Express. If disabled, equalizer gain control is determined by the XCVR\_RX\_LINEAR\_EQUALIZER\_SETTING assignment.

### Type

Boolean

### Device Support

- Arria V GZ
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_RX_ENABLE_LINEAR_EQUALIZER_PCIEMODE -to  
<to> -entity <entity name> <value>
```

## XCVR\_RX\_EQ\_BW\_SEL

Sets the gain peaking frequency for the equalizer. For data-rates of less than 6.5Gbps, set to HALF. For higher data-rates, set to FULL.

### Type

Enumeration

### Values

- BW\_FULL\_12P5
- BW\_HALF\_6P5

### Device Support

- Arria V GZ
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_RX_EQ_BW_SEL -to <to> -entity <entity  
name> <value>
```

## XCVR\_RX\_INPUT\_VCM\_SEL

When set to LOW\_VCM, this assignment enables PMOS equalizer on stage 1 of the input buffer and disables the NMOS stage for QPI and other modes in which the DC coupled connection common voltage is at approximately 0.25 V.

### Type

Enumeration

### Values

- HIGH\_VCM
- LOW\_VCM

### Device Support

- Arria V
- Arria V GZ
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_RX_INPUT_VCM_SEL -to <to> -entity  
<entity name> <value>
```

## XCVR\_RX\_LINEAR\_EQUALIZER\_CONTROL

Static control for the continuous time equalizer in the receiver buffer. Higher values of equalizer settings correspond to increasing AC gain.

### Type

Integer

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### INTEGER\_RANGE

1, 16

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_RX_LINEAR_EQUALIZER_CONTROL -to <to> -  
entity <entity name> <value>
```

## XCVR\_RX\_SD\_ENABLE

Enables or disables the receiver signal detection unit.

### Type

Boolean

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_RX_SD_ENABLE -to <to> -entity <entity  
name> <value>
```



## XCVR\_RX\_SD\_OFF

Number of parallel cycles to wait before the signal detect block declares loss of signal.

### Type

Integer

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### INTEGER\_RANGE

0, 29

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name XCVR_RX_SD_OFF -to <to> -entity <entity name>
```

## XCVR\_RX\_SD\_ON

Number of parallel cycles to wait before the signal detect block declares presence of signal.

### Type

Integer

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### INTEGER\_RANGE

0, 16

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name XCVR_RX_SD_ON -to <to> -entity <entity name>
```



## XCVR\_RX\_SD\_THRESHOLD

Specifies signal detection voltage threshold level.

### Type

Integer

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### INTEGER\_RANGE

0, 7

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_RX_SD_THRESHOLD -to <to> -entity <entity  
name> <value>
```

## XCVR\_RX\_SEL\_HALF\_BW

Enable half bandwidth mode. For BW=3.25GHZ, select FULL\_BW. For BW=1.5GHz, select HALF\_BW

### Type

Enumeration

### Values

- FULL\_BW
- HALF\_BW

### Device Support

- Arria V
- Cyclone V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_RX_SEL_HALF_BW -to <to> -entity <entity  
name> <value>
```

## XCVR\_TX\_COMMON\_MODE\_VOLTAGE

Transmitter common-mode driver voltage

### Type

Enumeration

### Values

- GROUNDED
- PULL\_DN
- PULL\_UP
- PULL\_UP\_TO\_VCCELA
- TRISTATED1
- VOLT\_0P35V
- VOLT\_0P50V
- VOLT\_0P55V
- VOLT\_0P60V
- VOLT\_0P65V
- VOLT\_0P70V
- VOLT\_0P75V
- VOLT\_0P80V

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_TX_COMMON_MODE_VOLTAGE -to <to> -entity  
<entity name> <value>
```

## XCVR\_TX\_PLL\_RECONFIG\_GROUP

Specifies whether XCVR channels with Dynamic TX PLL Reconfiguration can be merged.

### Type

Integer

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_TX_PLL_RECONFIG_GROUP -to <to> -entity  
<entity name> <value>
```

## XCVR\_TX\_PRE\_EMP\_1ST\_POST\_TAP

Specifies the transmitter preemphasis first post-tap setting value.

### Type

Integer

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### INTEGER\_RANGE

0, 31

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_TX_PRE_EMP_1ST_POST_TAP -to <to> -entity  
<entity name> <value>
```

## XCVR\_TX\_PRE\_EMP\_2ND\_POST\_TAP

Specifies the transmitter preemphasis second post-tap setting value.

### Type

Integer

### Device Support

- Arria V GZ
- Stratix V

### INTEGER\_RANGE

0, 15

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_TX_PRE_EMP_2ND_POST_TAP -to <to> -entity  
<entity name> <value>
```

## XCVR\_TX\_PRE\_EMP\_2ND\_POST\_TAP\_USER

Specifies the transmitter preemphasis second post-tap setting value, including inversion.

### Type

Integer

### Device Support

- Arria V GZ
- Stratix V

### INTEGER\_RANGE

0, 31

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_TX_PRE_EMP_2ND_POST_TAP_USER -to <to> -  
entity <entity name> <value>
```

## XCVR\_TX\_PRE\_EMP\_INV\_2ND\_TAP

Inverts the transmitter preemphasis second post-tap setting value.

### Type

Boolean

### Device Support

- Arria V GZ
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_TX_PRE_EMP_INV_2ND_TAP -to <to> -entity  
<entity name> <value>
```





## XCVR\_TX\_PRE\_EMP\_INV\_PRE\_TAP

Inverts the transmitter preemphasis pre-tap setting value.

### Type

Boolean

### Device Support

- Arria V GZ
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_TX_PRE_EMP_INV_PRE_TAP -to <to> -entity  
<entity name> <value>
```

## XCVR\_TX\_PRE\_EMP\_PRE\_TAP

Specifies the transmitter preemphasis pre-tap setting value.

### Type

Integer

### Device Support

- Arria V GZ
- Stratix V

### INTEGER\_RANGE

0, 15

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_TX_PRE_EMP_PRE_TAP -to <to> -entity  
<entity name> <value>
```



## XCVR\_TX\_PRE\_EMP\_PRE\_TAP\_USER

Specifies the transmitter preemphasis pre-tap setting value, including inversion.

### Type

Integer

### Device Support

- Arria V GZ
- Stratix V

### INTEGER\_RANGE

0, 31

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_TX_PRE_EMP_PRE_TAP_USER -to <to> -entity  
<entity name> <value>
```

## XCVR\_TX\_RX\_DET\_ENABLE

Enables or disables the receiver detector circuit at the transmitter.

### Type

Boolean

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_TX_RX_DET_ENABLE -to <to> -entity  
<entity name> <value>
```

## XCVR\_TX\_RX\_DET\_MODE

Sets the mode for the receiver detect block function.

### Type

Integer

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### INTEGER\_RANGE

0, 15

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_TX_RX_DET_MODE -to <to> -entity <entity  
name> <value>
```

## XCVR\_TX\_RX\_DET\_OUTPUT\_SEL

Determines QPI or PCI Express mode for the Receiver Detect block.

### Type

Enumeration

### Values

- RX\_DET\_PCIE\_OUT
- RX\_DET\_QPI\_OUT

### Device Support

- Arria V GZ
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_TX_RX_DET_OUTPUT_SEL -to <to> -entity  
<entity name> <value>
```



## XCVR\_TX\_SLEW\_RATE\_CTRL

Specifies the slew rate of the output signal. The valid values span from the slowest rate to fastest rate.

### Type

Integer

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### INTEGER\_RANGE

1, 5

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_TX_SLEW_RATE_CTRL -to <to> -entity  
<entity name> <value>
```

## XCVR\_TX\_VCM\_CTRL\_SRC

Controls the VCM driver (pulldown/pullup) dynamically from user signals when you set this assignment to DYNAMIC\_CTL for QPI protocol. The default setting (RAM\_CTL) causes the XCVR\_TX\_COMMON\_MODE\_VOLTAGE assignment to determine the state of the VCM driver.

### Type

Enumeration

### Values

- DYNAMIC\_CTL
- RAM\_CTL

### Device Support

- Arria V
- Arria V GZ
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_TX_VCM_CTRL_SRC -to <to> -entity <entity  
name> <value>
```





## XCVR\_TX\_VOD

Differential output voltage setting. The values are monotonically increasing with the driver main tap current strength.

### Type

Integer

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### INTEGER\_RANGE

0, 63

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
<value> set_instance_assignment -name XCVR_TX_VOD -to <to> -entity <entity name>
```

## XCVR\_TX\_VOD\_PRE\_EMP\_CTRL\_SRC

When you set this assignment to DYNAMIC\_CTL for PCI Express, the PCS block controls the VOD and preemphasis coefficients. When you set this assignment to RAM\_CTL, the VOD and preemphasis are controlled by other assignments (for example, XCVR\_TX\_PRE\_EMP\_1ST\_POST\_TAP).

### Type

Enumeration

### Values

- DYNAMIC\_CTL
- RAM\_CTL

### Device Support

- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_TX_VOD_PRE_EMP_CTRL_SRC -to <to> -entity  
<entity name> <value>
```

## XCVR\_VCCA\_VOLTAGE

Configure the VCCA\_GXB voltage for a GXB I/O pin by specifying the intended VCCA\_GXB voltage for a GXB I/O pin. If you do not set this option, the Compiler automatically sets the correct VCCA\_GXB voltage.

### Old Name

GXB\_VCCA\_VOLTAGE

### Type

Enumeration

### Values

- 2\_5V
- 3\_0V

### Device Support

- Arria V
- Arria V GZ
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_VCCA_VOLTAGE -to <to> -entity <entity  
name> <value>
```

## XCVR\_VCCR\_VCCT\_VOLTAGE

Configure the VCCR\_GXB and VCCT\_GXB voltage for an GXB I/O pin by specifying the intended supply voltages for a GXB I/O pin. If this is not set, the compiler automatically sets the correct VCCR\_GXB and VCCT\_GXB voltage.

### Old Name

GXB\_VCCR\_VCCT\_VOLTAGE

### Type

Enumeration

### Values

- 0\_85V
- 0\_9V
- 1\_0V
- 1\_15V
- 1\_1V
- 1\_2V

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name XCVR_VCCR_VCCT_VOLTAGE -to <to> -entity  
<entity name> <value>
```

## XSTL\_INPUT\_ALLOW\_SE\_BUFFER

Allows the pin with a Differential-XSTL IO-standard to be used with a single-ended input buffer.

### Type

Boolean

### Device Support

- Arria II GX
- Arria II GZ
- Cyclone 10 LP
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix III
- Stratix IV

### Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name XSTL_INPUT_ALLOW_SE_BUFFER <value>
set_global_assignment -name XSTL_INPUT_ALLOW_SE_BUFFER -entity <entity
name> <value>
set_instance_assignment -name XSTL_INPUT_ALLOW_SE_BUFFER -to <to> -entity
<entity name> <value>
```

### Default Value

Off

### Example

```
set_instance_assignment -name XSTL_INPUT_ALLOW_SE_BUFFER ON -to pin
```

### See Also

IO\_STANDARD

# Incremental Compilation Assignments

## ABSORB\_PATHS\_FROM\_OUTPUTS\_TO\_INPUTS

Allows the Compiler to optimize connections from a partition's outputs to its inputs by making the path internal to the partition. You must also enable the cross-boundary optimizations feature for this partition using the CROSS\_BOUNDARY\_OPTIMIZATIONS assignment.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name ABSORB_PATHS_FROM_OUTPUTS_TO_INPUTS -entity  
<entity name> -section_id <section identifier> <value>  
set_instance_assignment -name ABSORB_PATHS_FROM_OUTPUTS_TO_INPUTS -to <to> -  
entity <entity name> -section_id <section identifier> <value>
```

### Default Value

On, requires section identifier and entity name



## ALLOW\_MULTIPLE\_PERSONAS

Specifies if this partition represents a reconfigurable part of the design that can have multiple personas (implementations)

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name ALLOW_MULTIPLE_PERSONAS -entity <entity name> -  
section_id <section identifier> <value>  
set_instance_assignment -name ALLOW_MULTIPLE_PERSONAS -to <to> -entity  
<entity name> -section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier and entity name

## AUTO\_EXPORT\_INCREMENTAL\_COMPILATION

Automatically exports the project as a design partition

### Type

Boolean

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name AUTO_EXPORT_INCREMENTAL_COMPILATION <value>
```

### Default Value

Off





## CROSS\_BOUNDARY\_OPTIMIZATIONS

This setting specifies whether the Compiler should optimize across the partition's boundary. If enabled, the Compiler may be able to optimize the logic inside the partition by applying various cross-boundary optimizations, such as constant propagation and dangling logic removal. Specific cross-boundary optimizations are enabled by individual assignments.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name CROSS_BOUNDARY_OPTIMIZATIONS -entity <entity
name> -section_id <section identifier> <value>
set_instance_assignment -name CROSS_BOUNDARY_OPTIMIZATIONS -to <to> -entity
<entity name> -section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier and entity name

## ENABLE\_LAB\_SHARING\_WITH\_PARENT\_PARTITION

Allows logic from the target partition to share LAB resources with the immediate parent partition.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

### Syntax

```
set_instance_assignment -name ENABLE_LAB_SHARING_WITH_PARENT_PARTITION -to  
<to> -entity <entity name> -section_id <section identifier> <value>
```

## ENABLE\_STRICT\_PRESERVATION

Specifies whether IO pin belong to a strictly preserved safety IP. Setting defaults to off.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_STRICT_PRESERVATION -entity <entity  
name> -section_id <section identifier> <value>  
set_instance_assignment -name ENABLE_STRICT_PRESERVATION -to <to> -entity  
<entity name> -section_id <section identifier> <value>
```

## EXTENDS\_TOP\_BLOCK

Specifies a top-level block to extend. This currently instructs the fitter to use the post-map compiler results from the given VLNV, and to override the original QSF settings with those given in the current revision before running the fitter.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EXTENDS_TOP_BLOCK <value>
```



## IGNORE\_PARTITIONS

Specifies whether the compiler should ignore partition assignments in the project.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name IGNORE_PARTITIONS <value>
```

### Default Value

Off

## IMPORT\_BLOCK

Specifies a block in the form of VLNV+Snapshot to be imported for the specified partition.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
<value> set_instance_assignment -name IMPORT_BLOCK -to <to> -entity <entity name>
```

## INCREMENTAL\_COMPILATION\_EXPORT\_FILE

Specifies the path to the exported file. The file must have a QXP file extension

### Type

File name

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

The value of this assignment is case sensitive.

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name INCREMENTAL_COMPILATION_EXPORT_FILE <value>
```

## INCREMENTAL\_COMPILATION\_EXPORT\_FLATTEN

Specifies whether the netlist exported to the QXP file should flatten sub-partitions

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name INCREMENTAL_COMPILATION_EXPORT_FLATTEN <value>
```





## INCREMENTAL\_COMPILATION\_EXPORT\_PARTITION\_NAME

Specifies the name of the partition that contains the design hierarchy to be exported. The root partition will be exported if this assignment is not specified.

### Type

String

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

The value of this assignment is case sensitive.

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
<value> set_global_assignment -name INCREMENTAL_COMPILATION_EXPORT_PARTITION_NAME
```

## INCREMENTAL\_COMPILATION\_EXPORT\_POST\_FIT

Specifies whether the exported QXP file contains the post-fit netlist

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name INCREMENTAL_COMPILATION_EXPORT_POST_FIT <value>
```



## INCREMENTAL\_COMPILATION\_EXPORT\_POST\_SYNTH

Specifies whether the exported QXP file contains the post-synthesis netlist

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
<value> set_global_assignment -name INCREMENTAL_COMPILATION_EXPORT_POST_SYNTH
```

## INCREMENTAL\_COMPILATION\_EXPORT\_ROUTING

Specifies whether the post-fit netlist exported to the QXP file contains routing information

### Type

Boolean

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name INCREMENTAL_COMPILATION_EXPORT_ROUTING <value>
```

## INPUT\_PERSONA

Specifies the input Persona file to use for this partition.

### Type

File name

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

The value of this assignment is case sensitive.

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name INPUT_PERSONA -entity <entity name> -section_id  
<section identifier> <value>  
set_instance_assignment -name INPUT_PERSONA -to <to> -entity <entity name> -  
section_id <section identifier> <value>
```

## INSERT\_BOUNDARY\_WIRE\_LUTS

Enables wire lut insertion for boundary ports in the given partition (the partition is named by hierarchy path). This ensures that the inputs and outputs can have their locations preserved, which is useful for partial reconfiguration and compiling a design containing a blackbox.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

### Syntax

```
set_instance_assignment -name INSERT_BOUNDARY_WIRE_LUTS -to <to> -entity  
<entity name> <value>
```



## MERGE\_EQUIVALENT\_BIDIRS

Allows the Compiler to merge electrically equivalent bidirectional inputs. You must also enable the cross-boundary optimizations feature for this partition using the CROSS\_BOUNDARY\_OPTIMIZATIONS assignment.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name MERGE_EQUIVALENT_BIDIRS -entity <entity name> -  
section_id <section identifier> <value>  
set_instance_assignment -name MERGE_EQUIVALENT_BIDIRS -to <to> -entity  
<entity name> -section_id <section identifier> <value>
```

### Default Value

On, requires section identifier and entity name

## MERGE\_EQUIVALENT\_INPUTS

Allows the Compiler to merge inputs connected to the same source. You must also enable the cross-boundary optimizations feature for this partition using the CROSS\_BOUNDARY\_OPTIMIZATIONS assignment.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name MERGE_EQUIVALENT_INPUTS -entity <entity name> -  
section_id <section identifier> <value>  
set_instance_assignment -name MERGE_EQUIVALENT_INPUTS -to <to> -entity  
<entity name> -section_id <section identifier> <value>
```

### Default Value

On, requires section identifier and entity name



## PARTIAL\_RECONFIGURATION\_PARTITION

Specifies if this partition in the design is partially reconfigurable.

### Old Name

PR\_PARTITION

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

### Syntax

```
set_instance_assignment -name PARTIAL_RECONFIGURATION_PARTITION -to <to> -  
entity <entity name> <value>
```

## PARTITION

Creates a partition rooted at the specified instance. When an instance is defined as a partition, its hierarchical boundaries are fixed, allowing it to be independently exported or imported in many cases. The value of this assignment is the name of the design block that contains the implementation for the partition. The partition name must be unique in the complete design across all hierarchies. \n\nPartitions are an advanced feature and require significant up-front planning to use successfully. See the documentation for more information.

### Type

String

### Device Support

- Arria 10

### Notes

The value of this assignment is case sensitive.

### Syntax

```
<value> set_instance_assignment -name PARTITION -to <to> -entity <entity name>
```



## PARTITION\_ALWAYS\_USE\_QXP\_NETLIST

Specifies whether to always use the netlist in the QXP file associated with the partition, either because the QXP file is imported into the partition, or is specified as a source file for the partition. Setting defaults to off.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name PARTITION_ALWAYS_USE_QXP_NETLIST -entity  
<entity name> -section_id <section identifier> <value>  
set_instance_assignment -name PARTITION_ALWAYS_USE_QXP_NETLIST -to <to> -  
entity <entity name> -section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier and entity name

## PARTITION\_ASD\_REGION

Specifies the advanced SEU detection region assignment for this partition.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

### Syntax

```
set_instance_assignment -name PARTITION_ASD_REGION -to <to> -entity <entity  
name> <value>
```



## PARTITION\_ASD\_REGION\_ID

Indicates the advanced sensitivity detection region assignment for this partition.

### Type

Integer

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name PARTITION_ASD_REGION_ID -entity <entity name> -  
section_id <section identifier> <value>  
set_instance_assignment -name PARTITION_ASD_REGION_ID -to <to> -entity  
<entity name> -section_id <section identifier> <value>
```

### Default Value

1, requires section identifier and entity name

## PARTITION\_ENABLE\_STRICT\_PRESERVATION

Specifies whether partition is a strictly preserved safety IP. Setting defaults to off.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name PARTITION_ENABLE_STRICT_PRESERVATION -entity  
<entity name> -section_id <section identifier> <value>  
set_instance_assignment -name PARTITION_ENABLE_STRICT_PRESERVATION -to <to>  
-entity <entity name> -section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier and entity name

## PARTITION\_FITTER\_PRESERVATION\_LEVEL

Specifies the amount of data to reuse when you specify to reuse the post-fit netlist of this partition

### Type

Enumeration

### Values

- COMPATIBLE\_PLACEMENT
- COMPATIBLE\_PLACEMENT\_AND\_ROUTING
- NETLIST\_ONLY
- PLACEMENT
- PLACEMENT\_AND\_ROUTING
- PLACEMENT\_AND\_ROUTING\_AND\_HIGH\_SPEED\_TILES

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name PARTITION_FITTER_PRESERVATION_LEVEL -entity  
<entity name> -section_id <section identifier> <value>  
set_instance_assignment -name PARTITION_FITTER_PRESERVATION_LEVEL -to <to> -  
entity <entity name> -section_id <section identifier> <value>
```

## PARTITION\_HIERARCHY

The target of the assignment specifies the hierarchy path of the entity instance for the partition. The value of the assignment specifies the base output filename for writing intermediary atom netlists. It is strongly recommended that you rely on the default output filenames generated by Quartus Prime. If you decide to provide your own filenames, you must ensure their uniqueness among partitions.

### Old Name

INCREMENTAL\_DESIGN\_PARTITION

### Type

File name

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name PARTITION_HIERARCHY -entity <entity name> -  
section_id <section identifier> <value>  
set_instance_assignment -name PARTITION_HIERARCHY -to <to> -entity <entity  
name> -section_id <section identifier> <value>  
set_global_assignment -name PARTITION_HIERARCHY -entity <entity name>  
<value>  
set_instance_assignment -name PARTITION_HIERARCHY -to <to> -entity <entity  
name> <value>
```



## PARTITION\_IGNORE\_SOURCE\_FILE\_CHANGES

Specifies whether to use the requested post-synthesis or post-fit netlist when it is available, even when source file changes are present. Setting defaults to off.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name PARTITION_IGNORE_SOURCE_FILE_CHANGES -entity  
<entity name> -section_id <section identifier> <value>  
set_instance_assignment -name PARTITION_IGNORE_SOURCE_FILE_CHANGES -to <to>  
-entity <entity name> -section_id <section identifier> <value>
```

### Default Value

Off, requires section identifier and entity name

## PARTITION\_IMPORT\_ASSIGNMENTS

Specifies whether assignments (LogicLock or non-LogicLock) should be imported. If set to FALSE, only the netlist will be imported.

### Type

Boolean

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name PARTITION_IMPORT_ASSIGNMENTS -entity <entity
name> -section_id <section identifier> <value>
set_instance_assignment -name PARTITION_IMPORT_ASSIGNMENTS -to <to> -entity
<entity name> -section_id <section identifier> <value>
```

### Default Value

On, requires section identifier and entity name

## PARTITION\_IMPORT\_EXISTING\_ASSIGNMENTS

Specifies the way existing and conflicting non-LogicLock region assignments should be handled during import

### Type

Enumeration

### Values

- REPLACE\_CONFLICTING
- SKIP\_CONFLICTING

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name PARTITION_IMPORT_EXISTING_ASSIGNMENTS -entity  
<entity name> -section_id <section identifier> <value>  
set_instance_assignment -name PARTITION_IMPORT_EXISTING_ASSIGNMENTS -to  
<to> -entity <entity name> -section_id <section identifier> <value>
```

### Default Value

REPLACE\_CONFLICTING, requires section identifier and entity name

## PARTITION\_IMPORT\_EXISTING\_LOGICLOCK\_REGIONS

Specifies the way existing and conflicting LogicLock region assignments should be handled during import

### Type

Enumeration

### Values

- REPLACE\_CONFLICTING
- SKIP\_CONFLICTING
- UPDATE\_CONFLICTING

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name PARTITION_IMPORT_EXISTING_LOGICLOCK_REGIONS -  
entity <entity name> -section_id <section identifier> <value>  
set_instance_assignment -name PARTITION_IMPORT_EXISTING_LOGICLOCK_REGIONS -  
to <to> -entity <entity name> -section_id <section identifier> <value>
```

### Default Value

UPDATE\_CONFLICTING, requires section identifier and entity name

## PARTITION\_IMPORT\_FILE

Specifies the name of the file from which to import the contents for the partition. This setting is only used during importation.

### Type

File name

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

The value of this assignment is case sensitive.

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name PARTITION_IMPORT_FILE -entity <entity name> -  
section_id <section identifier> <value>  
set_instance_assignment -name PARTITION_IMPORT_FILE -to <to> -entity  
<entity name> -section_id <section identifier> <value>
```

## PARTITION\_IMPORT\_PROMOTE\_ASSIGNMENTS

Specifies whether assignments should be promoted to all instances of the imported entity

### Type

Boolean

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name PARTITION_IMPORT_PROMOTE_ASSIGNMENTS -entity  
<entity name> -section_id <section identifier> <value>  
set_instance_assignment -name PARTITION_IMPORT_PROMOTE_ASSIGNMENTS -to <to>  
-entity <entity name> -section_id <section identifier> <value>
```

### Default Value

On, requires section identifier and entity name

## PARTITION\_LAST\_IMPORTED\_FILE

Specifies the name of the file from which the partition was last imported. This assignment is for purely informational purpose only.

### Type

File name

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

The value of this assignment is case sensitive.

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name PARTITION_LAST_IMPORTED_FILE -entity <entity
name> -section_id <section identifier> <value>
set_instance_assignment -name PARTITION_LAST_IMPORTED_FILE -to <to> -entity
<entity name> -section_id <section identifier> <value>
```

## PARTITION\_NETLIST\_TYPE

Specifies the type of netlist to use for this partition during the next compilation

### Type

Enumeration

### Values

- Auto
- EMPTY
- IMPORTED
- IMPORT\_BASED\_POST\_FIT
- POST\_FIT
- POST\_FIT\_WITH\_ROUTING
- POST\_SYNT
- RR\_HYBRID
- SOURCE
- STRICT\_POST\_FIT

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name PARTITION_NETLIST_TYPE -entity <entity name> -  
section_id <section identifier> <value>  
set_instance_assignment -name PARTITION_NETLIST_TYPE -to <to> -entity  
<entity name> -section_id <section identifier> <value>
```



## PARTITION\_PRESERVE\_HIGH\_SPEED\_TILES

Specifies whether to preserve the high-speed tiles in the post-fit netlist, if applicable.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name PARTITION_PRESERVE_HIGH_SPEED_TILES -entity  
<entity name> -section_id <section identifier> <value>  
set_instance_assignment -name PARTITION_PRESERVE_HIGH_SPEED_TILES -to <to> -  
entity <entity name> -section_id <section identifier> <value>
```

### Default Value

On, requires section identifier and entity name

## PRESERVE

Directs the compiler to preserve the existing results of a partition. The value of this assignment is the snapshot to preserve, such as \"final\" or \"placed.\" If the specified snapshot does not exist, the compiler will exit with an error message. By default, the partition's results will not be preserved unless the only results available for the partition are later than the stage currently being compiled. For example, if the only snapshot for a partition is the \"placed\" snapshot, the Fitter will preserve the partition until the end of placement, and will not attempt to preserve it during routing.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
<value> set_instance_assignment -name PRESERVE -to <to> -entity <entity name>
```



## PROPAGATE\_CONSTANTS\_ON\_INPUTS

Allows the Compiler to use constants on a partition input to optimize the logic in the partition. You must also enable the cross-boundary optimizations feature for the partition using the CROSS\_BOUNDARY\_OPTIMIZATIONS assignment.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name PROPAGATE_CONSTANTS_ON_INPUTS -entity <entity  
name> -section_id <section identifier> <value>  
set_instance_assignment -name PROPAGATE_CONSTANTS_ON_INPUTS -to <to> -  
entity <entity name> -section_id <section identifier> <value>
```

### Default Value

On, requires section identifier and entity name

## PROPAGATE\_INVERSIONS\_ON\_INPUTS

Specifies that the Compiler should push inversions into partition inputs when possible. This cross-boundary optimization is especially important when inverted clock or asynchronous signals are connected to a partition input. Without this optimization, the Compiler may need to implement the inversion with a logic cell, introducing skew on the clock or reset path. The partition must also have enabled cross-boundary optimizations with the CROSS\_BOUNDARY\_OPTIMIZATIONS assignment.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name PROPAGATE_INVERSIONS_ON_INPUTS -entity <entity
name> -section_id <section identifier> <value>
set_instance_assignment -name PROPAGATE_INVERSIONS_ON_INPUTS -to <to> -
entity <entity name> -section_id <section identifier> <value>
```

### Default Value

On, requires section identifier and entity name

## QDB\_PATH

Specify path to read and write compiler generated database to a directory other than project directory.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name QDB_PATH <value>
```

## RAPID\_RECOMPILE\_ASSIGNMENT\_CHECKING

Specifies whether to check if assignments have changed when running Rapid Recompile. Turning off this option will bypass assignment change errors.

### Type

Boolean

### Device Support

- Arria V
- Cyclone V
- Stratix V

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name RAPID_RECOMPILE_ASSIGNMENT_CHECKING <value>
```

### Default Value

On



## REMOVE\_LOGIC\_ON\_UNCONNECTED\_OUTPUTS

Allows the Compiler to remove logic connected to dangling partitions outputs. You must also enable the cross-boundary optimizations feature for this partition using the CROSS\_BOUNDARY\_OPTIMIZATIONS assignment.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name REMOVE_LOGIC_ON_UNCONNECTED_OUTPUTS -entity  
<entity name> -section_id <section identifier> <value>  
set_instance_assignment -name REMOVE_LOGIC_ON_UNCONNECTED_OUTPUTS -to <to> -  
entity <entity name> -section_id <section identifier> <value>
```

### Default Value

On, requires section identifier and entity name

## LogicLock Region Assignments

### CORE\_ONLY\_PLACE\_REGION

Specifies if the placement region only applies to core logic.

#### Type

Boolean

#### Device Support

This setting can be used in projects targeting any Altera device family.

#### Notes

#### Syntax

```
set_instance_assignment -name CORE_ONLY_PLACE_REGION -to <to> -entity  
<entity name> <value>
```





## LL\_AUTO\_SIZE

Specifies whether the LogicLock region is auto-sized. The Compiler determines an appropriate size for auto-sized regions during compilation. If this keyword is set to 'On,' LL\_STATE must be set to 'Floating.'

### Type

Enumeration

### Values

- Off
- On

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name LL_AUTO_SIZE -entity <entity name> -section_id  
<section identifier> <value>
```

## LL\_CORE\_ONLY

If set to ON, the setting allows non-core tiles in the region.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name LL_CORE_ONLY -entity <entity name> -section_id  
<section identifier> <value>
```



## LL\_ENABLED

Specifies whether the region is enabled.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name LL_ENABLED -entity <entity name> -section_id  
<section identifier> <value>
```

## LL\_HEIGHT

Specifies the height of the LogicLock region in rows.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name LL_HEIGHT -entity <entity name> -section_id  
<section identifier> <value>
```

## LL\_MEMBER\_EXCEPTIONS

If specified, the Fitter assigns all nodes under the target design entity or path to be members of the LogicLock region, except for nodes of the specified types.

### Old Name

LL\_MEMBER\_RESOURCE\_EXCLUDE

### Type

String

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

The value of this assignment is case sensitive.

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name LL_MEMBER_EXCEPTIONS -entity <entity name> -  
section_id <section identifier> <value>  
set_instance_assignment -name LL_MEMBER_EXCEPTIONS -to <to> -entity <entity  
name> -section_id <section identifier> <value>  
set_instance_assignment -name LL_MEMBER_EXCEPTIONS -from <from> -to <to> -  
entity <entity name> -section_id <section identifier> <value>
```

## LL\_MEMBER\_OF

Assigns the current node(s) to a LogicLock region.

### Type

String

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

The value of this assignment is case sensitive.

This assignment is not copied when you create a companion revision for HardCopy II devices.

This assignment supports Fitter wildcards.

This assignment supports synthesis wildcards.

The value of this assignment must be a node name.

### Syntax

```
set_global_assignment -name LL_MEMBER_OF -entity <entity name> -section_id
<section identifier> <value>
set_instance_assignment -name LL_MEMBER_OF -to <to> -entity <entity name> -
section_id <section identifier> <value>
set_instance_assignment -name LL_MEMBER_OF -from <from> -to <to> -entity
<entity name> -section_id <section identifier> <value>
```

## LL\_MEMBER\_OF\_SECURITY\_ROUTING\_INTERFACE

Assigns the current signal to a security routing interface.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is not copied when you create a companion revision for HardCopy II devices.

The value of this assignment must be a node name.

### Syntax

```
set_instance_assignment -name LL_MEMBER_OF_SECURITY_ROUTING_INTERFACE -to  
<to> -entity <entity name> -section_id <section identifier> <value>
```

## LL\_ORIGIN

Specifies the location of the LogicLock region's origin. For APEX 20K and APEX II devices, the origin is the top left corner of the region. For newer devices, the origin is the bottom left corner of the region. A LogicLock region's origin is specified as an absolute location on the device, regardless of whether the region is a top-level LogicLock region or a child LogicLock region. However, if the region is a child LogicLock region, the Quartus Prime software interprets the origin as a relative offset from the parent region's origin. If LL\_STATE is set to 'Locked,' the Compiler places the LogicLock region at this location. If LL\_STATE is set to 'Floating,' the Compiler is free to determine an appropriate location for the region during compilation.

### Type

Location

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name LL_ORIGIN -entity <entity name> -section_id  
<section identifier> <value>
```



## LL\_PARENT

Specifies the name of the LogicLock region's parent LogicLock region.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name LL_PARENT -entity <entity name> -section_id  
<section identifier> <value>
```

## LL\_PRIORITY

Indicates the priority of a wildcard or path-based LL\_MEMBER\_OF assignment relative to other wildcard or path-based LL\_MEMBER\_OF assignments. If a node matches more than one wildcard or path-based LL\_MEMBER\_OF assignment target, the assignment whose target has the highest LL\_PRIORITY value wins

### Type

Integer

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

This assignment supports Fitter wildcards.

This assignment supports synthesis wildcards.

### Syntax

```
set_instance_assignment -name LL_PRIORITY -to <to> -entity <entity name> -  
section_id <section identifier> <value>  
set_instance_assignment -name LL_PRIORITY -from <from> -to <to> -entity  
<entity name> -section_id <section identifier> <value>
```

## LL\_RESERVED

If set to ON, the setting prevents the Fitter from placing non-member logic in the region.

### Old Name

LL\_RESERVE

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name LL_RESERVED -entity <entity name> -section_id  
<section identifier> <value>
```

## LL\_ROOT\_REGION

Indicates that the LogicLock region is a root region.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name LL_ROOT_REGION -entity <entity name> -  
section_id <section identifier> <value>
```

## LL\_STATE

Specifies whether the location of the LogicLock region is locked or floating. The Compiler determines an appropriate location for floating regions during compilation. If this keyword is set to 'Locked', LL\_AUTO\_SIZE must be set to 'Off'.

### Type

Enumeration

### Values

- Floating
- Locked
- Soft

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name LL_STATE -entity <entity name> -section_id  
<section identifier> <value>
```

## LL\_WIDTH

Specifies the width of the LogicLock region in LABs/ESBs.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name LL_WIDTH -entity <entity name> -section_id  
<section identifier> <value>
```

## PLACE\_REGION

Specifies the target and bounding boxes of a placement region.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

### Syntax

```
<value> set_instance_assignment -name PLACE_REGION -to <to> -entity <entity name>
```

## RESERVE\_PLACE\_REGION

Specifies if the placement region excludes other logic from being placed in that region.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

### Syntax

```
set_instance_assignment -name RESERVE_PLACE_REGION -to <to> -entity <entity  
name> <value>
```



## ROUTE\_REGION

Specifies the target and bounding boxes of a routing region.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

### Syntax

```
<value> set_instance_assignment -name ROUTE_REGION -to <to> -entity <entity name>
```

# Migration Assignments

## MIGRATION\_AUTO\_PACKED\_REGISTERS

Register Packings that have been performed on a prototype device and that must be reproduced on the target migration device

### Type

String

### Device Support

- Arria GX
- HardCopy II
- HardCopy III
- HardCopy IV
- Stratix II
- Stratix II GX
- Stratix III

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_instance_assignment -name MIGRATION_AUTO_PACKED_REGISTERS -to <to> -  
entity <entity name> <value>  
set_instance_assignment -name MIGRATION_AUTO_PACKED_REGISTERS -from <from> -  
to <to> -entity <entity name> <value>
```

## MIGRATION\_AUTO\_PORT\_SWAP

Port Swappings that have been performed on a prototype device and that must be reproduced on the target migration device

### Type

String

### Device Support

- Arria GX
- HardCopy II
- HardCopy III
- HardCopy IV
- Stratix II
- Stratix II GX
- Stratix III

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_instance_assignment -name MIGRATION_AUTO_PORT_SWAP -to <to> -entity  
<entity name> <value>
```

## MIGRATION\_RAM\_INFORMATION

RAMs that have been created on a prototype device and that must be reproduced on the target migration device

### Type

String

### Device Support

- Arria GX
- HardCopy II
- HardCopy III
- HardCopy IV
- Stratix II
- Stratix II GX
- Stratix III

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_instance_assignment -name MIGRATION_RAM_INFORMATION -to <to> -entity  
<entity name> <value>
```

# Netlist Viewer Assignments

## RTL\_V\_GROUP\_COMB\_LOGIC\_IN\_CLOUD

Allow RTL Viewer to group combinational logic in logic cloud

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name RTL_V_GROUP_COMB_LOGIC_IN_CLOUD <value>
```

### Default Value

Off

## RTL\_V\_GROUP\_COMB\_LOGIC\_IN\_CLOUD\_TMV

Allow Technology Map Viewer to group combinational logic in logic cloud

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name RTL_V_GROUP_COMB_LOGIC_IN_CLOUD_TMV <value>
```

### Default Value

Off

## RTL\_V\_GROUP\_RELATED\_NODES

Allow RTL Viewer to group all related nodes into a single bus node

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name RTL_V_GROUP_RELATED_NODES <value>
```

### Default Value

On

## RTL\_V\_GROUP\_RELATED\_NODES\_TMV

Allow Technology Map Viewer to group all related nodes into a single bus node

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name RTL_V_GROUP_RELATED_NODES_TMV <value>
```

### Default Value

On





## RTL\_V\_REMOVE\_FANOUT\_FREE\_REGISTERS

Allow RTL Viewer to remove fanout free registers

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name RTL_V_REMOVE_FANOUT_FREE_REGISTERS <value>
```

### Default Value

On

## RTL\_V\_SIMPLIFIED\_LOGIC

Allow RTL Viewer to remove wire nodes and merge chain of equivalent combinatorial gates

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name RTL_V_SIMPLIFIED_LOGIC <value>
```

### Default Value

On



## Pin & Location Assignments

### APEX20K\_CLIQUE\_TYPE

Specifies the type of a clique.

#### Old Name

CLIQUE\_TYPE

#### Type

Enumeration

#### Values

LAB

#### Notes

None

#### Syntax

```
set_global_assignment -name APEX20K_CLIQUE_TYPE -entity <entity name> -  
section_id <section identifier> <value>
```

#### Default Value

LAB, requires section identifier and entity name

## APEX20K\_LOCAL\_ROUTING\_SOURCE

Specifies that the fan-out(s) of an input pin connected to logic elements, or the fan-out(s) of a logic element connected to output pin(s), should be fed via shared local interconnect lines. If the Local Routing Source assignment is turned on for a pin, local routing occurs only for the cells placed in adjacent LABs to which local routing is possible. If the Local Routing Source assignment is turned on for a logic element, local routing occurs only for the output pins that are adjacent to the LAB containing the logic element. Altera recommends that you make an explicit location assignment to the cells (input, output, logic element) to guarantee they are placed in a suitable location for local routing. You can connect logic on a speed-critical path using local routing to maximize the project performance.

### Old Name

USE\_LOCAL

### Type

Boolean

### Notes

None

### Syntax

```
set_instance_assignment -name APEX20K_LOCAL_ROUTING_SOURCE -to <to> -entity  
<entity name> <value>
```

## FAST\_INPUT\_REGISTER

Implements an input register in a cell that has a fast, direct connection from an I/O pin. If such a fast, direct connection from the I/O pin is not available on the I/O cell hardware, this option instructs the Fitter to lock the input register in the LAB adjacent to the I/O cell feeding it. Turning on the Fast Input Register option can help maximize I/O timing performance, for example, by permitting fast setup times. Turning this option off for a particular signal prevents the Fitter from implementing the signal automatically in an I/O cell or locking down the input register in the LAB adjacent to the I/O cell. This option is ignored if it is applied to anything other than a register or an input or bidirectional pin that feeds a register.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

## Notes

This assignment supports Fitter wildcards.

## Syntax

```
set_instance_assignment -name FAST_INPUT_REGISTER -to <to> -entity <entity  
name> <value>
```



## FAST\_OCT\_REGISTER

Implements an OCT register in a cell that has a fast, direct connection to an I/O pin. Turning on the Fast OCT Register option can help maximize I/O timing performance, for example, by permitting fast clock-to-output times. Turning this option off for a particular signal prevents the Fitter from implementing the signal automatically in an I/O cell. This option is ignored if it is applied to anything other than a register or an output or bidirectional pin fed by a register.

### Type

Boolean

### Device Support

- Arria II GX
- Arria II GZ
- Arria V GZ
- HardCopy III
- HardCopy IV
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_instance_assignment -name FAST_OCT_REGISTER -to <to> -entity <entity  
name> <value>
```

## FAST\_OUTPUT\_ENABLE\_REGISTER

Implements an output enable register in a cell that has a fast, direct connection to an I/O pin. If such a fast, direct connection to the I/O pin is not available in the I/O cell hardware, this option instructs the Fitter to lock the output enable register in the LAB adjacent to the I/O cell it is feeding. Turning on the Fast Output Enable Register option can help maximize I/O timing performance, for example, by permitting fast clock-to-output times. Turning this option off for a particular signal prevents the Fitter from implementing the signal automatically in an I/O cell or locking down the output enable register in the LAB adjacent to the I/O cell. This option is ignored if it is applied to anything other than a register or an output or bidirectional pin fed by a register.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports Fitter wildcards.





## Syntax

```
set_instance_assignment -name FAST_OUTPUT_ENABLE_REGISTER -to <to> -entity  
<entity name> <value>
```

## FAST\_OUTPUT\_REGISTER

Implements an output register in a cell that has a fast, direct connection to an I/O pin. If such a fast, direct connection to the I/O pin is not available in the I/O cell hardware, this option instructs the Fitter to lock the output register in the LAB adjacent to the I/O cell it is feeding. Turning on the Fast Output Register option can help maximize I/O timing performance, for example, by permitting fast clock-to-output times. Turning this option off for a particular signal prevents the Fitter from implementing the signal automatically in an I/O cell or locking down the output register in the LAB adjacent to the I/O cell. This option is ignored if it is applied to anything other than a register or an output or bidirectional pin fed by a register.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

## Notes

This assignment supports Fitter wildcards.

## Syntax

```
set_instance_assignment -name FAST_OUTPUT_REGISTER -to <to> -entity <entity  
name> <value>
```

## FLEX10K\_CLIQUE\_TYPE

Specifies the type of a clique.

### Type

Enumeration

### Values

LAB

### Device Support

- A
- E

### Notes

None

### Syntax

```
set_global_assignment -name FLEX10K_CLIQUE_TYPE -entity <entity name> -  
section_id <section identifier> <value>
```

### Default Value

LAB, requires section identifier and entity name

## FLEX6K\_CLIQUE\_TYPE

Specifies the type of a clique.

### Type

Enumeration

### Values

- Best
- Half Row
- LAB
- Row

### Notes

None

### Syntax

```
set_global_assignment -name FLEX6K_CLIQUE_TYPE -entity <entity name> -  
section_id <section identifier> <value>
```

### Default Value

LAB, requires section identifier and entity name

## FLEX6K\_LOCAL\_ROUTING\_SOURCE

Specifies that the fan-out(s) of an input pin connected to logic elements, or the fan-out(s) of a logic element connected to output pin(s), should be fed via shared local interconnect lines. If the Local Routing Source assignment is turned on for a pin, local routing occurs only for the cells placed in adjacent LABs to which local routing is possible. If the Local Routing Source assignment is turned on for a logic element, local routing occurs only for the output pins that are adjacent to the LAB containing the logic element. Altera recommends that you make an explicit location assignment to the cells (input, output, logic element) to guarantee they are placed in a suitable location for local routing. You can connect logic on a speed-critical path using local routing to maximize the project performance.

### Old Name

FLEX6K\_LOCAL\_ROUTING\_DESTINATION

### Type

Boolean

### Notes

None

### Syntax

```
set_instance_assignment -name FLEX6K_LOCAL_ROUTING_SOURCE -to <to> -entity  
<entity name> <value>
```



## IP\_DEBUG\_VISIBLE

When assigned to an Encrypted IP node this option directs Quartus Prime to display the node in the Node Finder.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_instance_assignment -name IP_DEBUG_VISIBLE -to <to> -entity <entity  
name> <value>
```

## LL\_IGNORE\_IO\_PIN\_SECURITY\_CONSTRAINT

Allows the specified I/O pin to ignore security constraints.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is not copied when you create a companion revision for HardCopy II devices.

The value of this assignment must be a node name.

### Syntax

```
set_instance_assignment -name LL_IGNORE_IO_PIN_SECURITY_CONSTRAINT -to <to>  
-entity <entity name> <value>
```





## LOCATION

Assigns a location on the device for the current node(s) and/or pin(s).

### Type

Location

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports Fitter wildcards.

### Syntax

```
set_location_assignment -to <to> <value>
```

## MAX7K\_CLIQUE\_TYPE

Specifies the type of a clique.

### Type

Enumeration

### Values

LAB

### Device Support

- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S

### Notes

None

### Syntax

```
set_global_assignment -name MAX7K_CLIQUE_TYPE -entity <entity name> -  
section_id <section identifier> <value>
```

### Default Value

LAB, requires section identifier and entity name

## MEMBER\_OF

Assigns one or more currently selected nodes and/or entities to a clique, which is a group of functions that the Compiler attempts to place together in the same area. You must also assign a name to the clique. A clique assignment allows you to group all logic on a speed-critical path to help achieve optimum performance.

### Type

String

### Device Support

- A
- E
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Mercury

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_instance_assignment -name MEMBER_OF -to <to> -entity <entity name> -  
section_id <section identifier> <value>
```

## MERCURY\_CLIQUE\_TYPE

Specifies the type of a clique.

### Type

Enumeration

### Values

LAB

### Device Support

Mercury

### Notes

None

### Syntax

```
set_global_assignment -name MERCURY_CLIQUE_TYPE -entity <entity name> -  
section_id <section identifier> <value>
```

### Default Value

LAB, requires section identifier and entity name

## PIN\_CONNECT\_FROM\_NODE

Directs the Compiler to generate a device pin with the specified name and connect the device pin to an internal signal.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_instance_assignment -name PIN_CONNECT_FROM_NODE -to <to> <value>
```

## RESERVE\_PIN

Reserves the pin in one of seven states: as an input that is tri-stated; as an output that drives ground; as an output that drives VCC; as an output that drives an unspecified signal; as SignalProbe output; as a voltage reference (VREF); or as bidirectional. Note: The 'As VREF' setting is not appropriate for all device families. Please refer to the device data sheet for information on VREF support.

### Old Name

RESERVED\_PIN

### Type

Enumeration

### Values

- As SignalProbe output
- As VREF
- As bidirectional
- As input tri-stated
- As output driving VCC
- As output driving an unspecified signal
- As output driving ground

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_instance_assignment -name RESERVE_PIN -to <to> <value>  
set_global_assignment -name RESERVE_PIN <value>
```



## SUBCLIQUE\_OF

Specifies that the current clique is a member of another clique.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_instance_assignment -name SUBCLIQUE_OF -to <to> -entity <entity name> -  
section_id <section identifier> <value>
```

## VIRTUAL\_PIN

Specifies whether an I/O element in a lower-level design entity can be temporarily mapped to a logic element and not to a pin during compilation. The virtual pin is then implemented as a LUT. This option should be specified only for I/O elements that become nodes when imported to the top-level design.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment supports synthesis wildcards.

### Syntax

```
set_instance_assignment -name VIRTUAL_PIN -to <to> -entity <entity name>  
<value>
```



## Power Estimation Assignments

### ENABLE\_SMART\_VOLTAGE\_ID

Specifies whether smart voltage ID feature is used.

#### Type

Boolean

#### Device Support

- Arria 10

#### Notes

This assignment is included in the Fitter report.

#### Syntax

```
set_global_assignment -name ENABLE_SMART_VOLTAGE_ID <value>
```

#### Default Value

Off

## POWER\_AUTO\_COMPUTE\_TJ

Specifies whether the junction temperature is auto-computed during power estimation. If the junction temperature is not auto-computed, you must specify the junction temperature.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_AUTO_COMPUTE_TJ <value>
```

### Default Value

On



## POWER\_BOARD\_TEMPERATURE

Specifies the board temperature, in degrees Celsius, used during power estimation.

### Type

Integer

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_BOARD_TEMPERATURE <value>
```

### Default Value

25

## POWER\_BOARD\_THERMAL\_MODEL

Specifies the board thermal model used during power estimation.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_BOARD_THERMAL_MODEL <value>
```



## POWER\_DEFAULT\_INPUT\_IO\_TOGGLE\_RATE

Specifies the default toggle rate to be used on input I/O pins during power estimation. This value is only used if a toggle rate has not been specified for a node either through a Signal Activity File, VCD file or user assignment.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name POWER_DEFAULT_INPUT_IO_TOGGLE_RATE <value>
```

## Default Value

12.5%

## POWER\_DEFAULT\_TOGGLE\_RATE

Specifies the default toggle rate to be used on all nodes except input I/O pins during power estimation. This value is only used if a toggle rate has not been specified for a node either through a Signal Activity File, VCD file or user assignment.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name POWER_DEFAULT_TOGGLE_RATE <value>
```

## Default Value

12.5%





## POWER\_EXT\_SUPPLY\_VOLTAGE\_TO\_REGULATOR

Specifies the external supply voltage applied to the on-chip voltage regulator. This option applies only to devices which have an on-chip voltage regulator.

### Type

String

### Device Support

- MAX II
- MAX V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_EXT_SUPPLY_VOLTAGE_TO_REGULATOR <value>
```

## POWER\_GLITCH\_FACTOR

Specifies the multiplication factor to the toggle rates used for power estimation for part of design hierarchy. This is useful to adjust toggle rates of parts of the design with high number of glitches. The value must be positive.

### Type

Double

### Device Support

- Arria 10

### Notes

None

### Syntax

```
set_global_assignment -name POWER_GLITCH_FACTOR -entity <entity name>  
<value>  
set_instance_assignment -name POWER_GLITCH_FACTOR -to <to> -entity <entity  
name> <value>
```

## POWER\_HPS\_DYNAMIC\_POWER\_DUAL

Dynamic Power of dual processor core when HPS is active.

### Type

String

### Device Support

- Arria 10
- Arria V
- Cyclone V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_HPS_DYNAMIC_POWER_DUAL <value>
```

## POWER\_HPS\_DYNAMIC\_POWER\_SINGLE

Dynamic power of single processor core when HPS is active.

### Type

String

### Device Support

- Arria 10
- Arria V
- Cyclone V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_HPS_DYNAMIC_POWER_SINGLE <value>
```

## POWER\_HPS\_ENABLE

Specifies whether or not you must include the HPS processor subsystem for SoC power estimation.

### Type

Boolean

### Device Support

- Arria 10
- Arria V
- Cyclone V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_HPS_ENABLE <value>
```

### Default Value

Off

## POWER\_HPS\_JUNCTION\_TEMPERATURE

Junction Temperature when HPS is active.

### Type

String

### Device Support

- Arria 10
- Arria V
- Cyclone V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_HPS_JUNCTION_TEMPERATURE <value>
```

## POWER\_HPS\_PROC\_FREQ

Specifies the processor frequency of the HPS assumed by power estimation. The units for this value are MHz and the value must be positive. The value provided should be within 0 to 1000.

### Type

Double

### Device Support

- Arria 10
- Arria V
- Cyclone V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_HPS_PROC_FREQ <value>
```

### Default Value

0.0

## POWER\_HPS\_STATIC\_POWER

Static Power when HPS is active.

### Type

String

### Device Support

- Arria 10
- Arria V
- Cyclone V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_HPS_STATIC_POWER <value>
```





## POWER\_HPS\_TOTAL\_POWER

Total power when HPS is active.

### Type

String

### Device Support

- Arria 10
- Arria V
- Cyclone V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_HPS_TOTAL_POWER <value>
```

## POWER\_HSSI

If the transceivers are unused, setting this option to \"Opportunistically power off\" directs the Quartus Prime software to consider the transceivers as powered down. Setting this option to \"Power on\" directs the Quartus Prime software to consider the transceivers powered regardless of their use. This setting affects the VCCA, VCCH\_GXB, and VCCL\_GXB power rails.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_HSSI <value>
```



## POWER\_HSSI\_LEFT

If the transceivers on the left side of the device are unused, setting this option to \"Opportunistically power off\" directs the Quartus Prime software to consider the transceivers on the left side of the device powered down. Setting this option to \"Power on\" directs the Quartus Prime software to consider the transceivers on the left side powered regardless of their use. This setting affects the VCCA\_L, VCCH\_GXBL, VCCL\_GXBL, VCCR\_L, and VCCT\_L power rails.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_HSSI_LEFT <value>
```

## POWER\_HSSI\_RIGHT

If the transceivers on the right side of the device are unused, setting this option to \"Opportunistically power off\" directs the Quartus Prime software to consider the transceivers on the right side of the device powered down. Setting this option to \"Power on\" directs the Quartus Prime software to consider the transceivers on the right side powered regardless of their use. This setting affects the VCCA\_R, VCCH\_GXBR, VCCL\_GXBR, VCCR\_R, and VCCT\_R power rails.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_HSSI_RIGHT <value>
```



## POWER\_HSSI\_VCCHIP\_LEFT

If the PCI Express hard IP blocks on the left side of the device are unused, setting this option to \"Opportunistically power off\" directs the Quartus Prime software to consider the PCI Express hard IP blocks on the left side of the device powered down. Setting this option to \"Power on\" directs the Quartus Prime software to consider the PCI Express hard IP blocks on the left side powered regardless of their use.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_HSSI_VCCHIP_LEFT <value>
```

## POWER\_HSSI\_VCCHIP\_RIGHT

If the PCI Express hard IP blocks on the right side of the device are unused, setting this option to \"Opportunistically power off\" directs the Quartus Prime software to consider the PCI Express hard IP blocks on the right side of the device powered down. Setting this option to \"Power on\" directs the Quartus Prime software to consider the PCI Express hard IP blocks on the right side powered regardless of their use.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_HSSI_VCCHIP_RIGHT <value>
```



## POWER\_INPUT\_FILE\_NAME

Specifies the name of the VCD File or Signal Activity File which should be used to initialize the toggle rates and static probabilities that will be used during power estimation.

### Type

File name

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name POWER_INPUT_FILE_NAME -entity <entity name> -
```

```
section_id <section identifier> <value>
```





## POWER\_INPUT\_FILE\_TYPE

Specifies whether the input power file is a VCD file or SAF file.

### Type

Enumeration

### Values

- SAF
- VCD

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

None

## Syntax

```
set_global_assignment -name POWER_INPUT_FILE_TYPE -entity <entity name> -  
section_id <section identifier> <value>
```

## POWER\_INPUT\_SAF\_NAME

Specifies the name of the Signal Activity File which should be used to initialize the toggle rates and static probabilities that will be used during power estimation.

### Type

File name

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name POWER_INPUT_SAF_NAME <value>
```

## POWER\_INPUT\_VCD\_FILE\_NAME

Specifies the names of the VCD files which should be used to initialize the toggle rates and static probabilities that will be used during power estimation.

### Type

File name

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name POWER_INPUT_VCD_FILE_NAME <value>
```



## POWER\_OCS\_VALUE

Specifies the case-to-heat sink thermal resistance, in degrees Celsius per Watt, used during power estimation.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_OCS_VALUE <value>
```

## POWER\_OJB\_VALUE

Specifies the junction-to-board thermal resistance, in degrees Celsius per Watt, used during power estimation.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_OJB_VALUE <value>
```

## POWER\_OJC\_VALUE

Specifies the junction-to-case-sink thermal resistance, in degrees Celsius per Watt, used during power estimation.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_OJC_VALUE <value>
```

## POWER\_OSA\_VALUE

Specifies the heat sink-to-ambient thermal resistance, in degrees Celsius per Watt, used during power estimation.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_OSA_VALUE <value>
```



## POWER\_OUTPUT\_SAF\_NAME

Specifies the name the Signal Activity File should be written to containing the toggle rates and static probabilities used during power estimation.

### Type

File name

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name POWER_OUTPUT_SAF_NAME <value>
```



## POWER\_PRESET\_COOLING\_SOLUTION

Specifies the preset cooling solution used during power estimation.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_PRESET_COOLING_SOLUTION <value>
```

## POWER\_READ\_INPUT\_FILE

Assigns user-defined power input file characteristics to an entity. To specify a power input file, you must define a named group of 'power input file settings' and assign them to an entity with this option. You can create these settings using the PowerPlay Power Analyzer Settings page.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_instance_assignment -name POWER_READ_INPUT_FILE -to <to> -entity
```



<entity name> <value>

## POWER\_REPORT\_POWER DISSIPATION

Specifies whether the PowerPlay Power Analyzer should report the thermal power dissipation calculated during power analysis in the Thermal Power Dissipation By Block report panel.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_REPORT_POWER DISSIPATION <value>  
set_instance_assignment -name POWER_REPORT_POWER DISSIPATION -to <to> -
```

entity <entity name> <value>

Default Value

Off

## POWER\_REPORT\_SIGNAL\_ACTIVITY

Specifies whether the PowerPlay Power Analyzer should report the signal activities assumed for power analysis, and the sources for those activities. Signal activity consists of both the static probability and the toggle rate for the signals generated by the node or entity.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_REPORT_SIGNAL_ACTIVITY <value>
```





```
set_instance_assignment -name POWER_REPORT_SIGNAL_ACTIVITY -to <to> -entity  
<entity name> <value>
```

### Default Value

Off

## POWER\_SIGNAL\_ACTIVITY\_END\_TIME

Specifies the time at which toggle rates and static probabilities should stop being calculated for the output signals contained in the VCD files.

### Type

Time

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name POWER_SIGNAL_ACTIVITY_END_TIME <value>
```

## POWER\_SIGNAL\_ACTIVITY\_START\_TIME

Specifies the time at which toggle rates and static probabilities should start to be calculated for the output signals contained in the VCD files.

### Type

Time

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name POWER_SIGNAL_ACTIVITY_START_TIME <value>
```

## POWER\_STATIC\_PROBABILITY

Specifies the fraction of time the signals generated by the node or entity are expected to be at VCC. Allowable values range from and include 0.0 through 1.0.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

None

### Syntax

```
set_instance_assignment -name POWER_STATIC_PROBABILITY -to <to> <value>
```

## POWER\_TJ\_VALUE

Specifies the junction temperature value, in degrees Celsius, used during power estimation.

### Type

Integer

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_TJ_VALUE <value>
```

### Default Value

25

## POWER\_TOGGLE\_RATE

Specifies the toggle rate assumed by power estimation for the signals generated by this node or entity. The units for this value are transitions per second and the value must be positive. The value provided should be the expected time-averaged toggle rate, rather than worst case (highest possible) toggle rate. A different assignment, Toggle Rate, applies to I/O pins only and is used by the Fitter and by I/O Assignment Analysis to verify signal integrity under worst case conditions (highest possible toggle rate). Use the Synchronizer Toggle Rate if you want to configure the data rates used for Metastability Reporting in the TimeQuest Timing Analyzer.

### Type

Double

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

None



## Syntax

```
set_instance_assignment -name POWER_TOGGLE_RATE -to <to> <value>
```

## POWER\_TOGGLE\_RATE\_PERCENTAGE

Specifies the toggle rate, as a percentage of clock domain frequency, assumed by power estimation for the signals generated by this node or entity. This percentage acts as a multiplier for the clock domain frequency of the given node. For example, a toggle rate percentage of 12.5 on a node with a clock domain frequency of 96 MHz would result in a toggle rate of 12 million transitions per second. The percentage value must be positive and can take on values greater than 100. The value provided should be representative of the expected time-averaged toggle rate, rather than worst case (highest possible) toggle rate.

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

None



## Syntax

```
set_instance_assignment -name POWER_TOGGLE_RATE_PERCENTAGE -to <to> <value>
```



## POWER\_USE\_CUSTOM\_COOLING\_SOLUTION

Specifies whether a custom cooling solution is used during power estimation. For a custom cooling solution, you must specify the case-to-heat sink, junction-to-case and heat sink-to-ambient thermal resistances.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_USE_CUSTOM_COOLING_SOLUTION <value>
```

### Default Value

Off

## POWER\_USE\_DEVICE\_CHARACTERISTICS

Specifies the device characteristics to be used during power estimation. Estimates are based on average power consumed by typical silicon at nominal operating conditions. For FPGA board power supply design, change to MAXIMUM to get worst-case values.

### Type

Enumeration

### Values

- MAXIMUM
- TYPICAL

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_USE_DEVICE_CHARACTERISTICS <value>
```

**Default Value**

TYPICAL



## POWER\_USE\_INPUT\_FILE

Specifies whether or not Signal Activity Files or VCD files should be used to initialize the toggle rates and static probabilities that will be used during power estimation.

### Type

Enumeration

### Values

- No File
- Signal Activity File
- VCD File

### Device Support

- Arria GX
- Cyclone
- Cyclone II
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX

### Notes

None

### Syntax

```
set_global_assignment -name POWER_USE_INPUT_FILE <value>
```

### Default Value

No File

## POWER\_USE\_INPUT\_FILES

Specifies whether or not Signal Activity Files or VCD files should be used to initialize the toggle rates and static probabilities that will be used during power estimation.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_USE_INPUT_FILES <value>
```

**Default Value**  
Off

## POWER\_USE\_PVA

Specifies whether or not Power Vectorless Activity should be used to fill in undefined toggle rates and static probabilities.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_USE_PVA <value>
```

### Default Value

On



## POWER\_USE\_TA\_VALUE

Specifies the ambient temperature value, in degrees Celsius, used during power estimation.

### Type

Integer

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_USE_TA_VALUE <value>
```

### Default Value

25

## POWER\_VCCAUX\_USER\_OPTION

Allows you to specify settings for the VCCAUX power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCCAUX_USER_OPTION <value>
```



## POWER\_VCCA\_GXBL\_USER\_OPTION

Allows you to specify settings for the VCCA\_GXBL power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCCA_GXBL_USER_OPTION <value>
```

## POWER\_VCCA\_GXBR\_USER\_OPTION

Allows you to specify settings for the VCCA\_GXBR power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCCA_GXBR_USER_OPTION <value>
```



## POWER\_VCCA\_GXB\_USER\_OPTION

Allows you to specify settings for the VCCA\_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCCA_GXB_USER_OPTION <value>
```

## POWER\_VCCA\_L\_USER\_OPTION

Allows you to specify settings for the VCCA\_L power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCCA_L_USER_OPTION <value>
```



## POWER\_VCCA\_R\_USER\_OPTION

Allows you to specify settings for the VCCA\_R power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCCA_R_USER_OPTION <value>
```

## POWER\_VCCCB\_USER\_OPTION

Allows you to specify settings for the VCCCB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCCCB_USER_OPTION <value>
```





## POWER\_VCCH\_GXBL\_USER\_OPTION

Allows you to specify settings for the VCCH\_GXBL power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCCH_GXBL_USER_OPTION <value>
```

## POWER\_VCCH\_GXBR\_USER\_OPTION

Allows you to specify settings for the VCCH\_GXBR power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCCH_GXBR_USER_OPTION <value>
```



## POWER\_VCCH\_GXB\_USER\_OPTION

Allows you to specify settings for the VCCH\_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCCH_GXB_USER_OPTION <value>
```

## POWER\_VCCIO\_USER\_OPTION

Allows you to specify settings for the VCCIO power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCCIO_USER_OPTION <value>
```



## POWER\_VCCL\_GXB\_USER\_OPTION

Allows you to specify settings for the VCCL\_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCCL_GXB_USER_OPTION <value>
```

## POWER\_VCCPD\_USER\_OPTION

Allows you to specify settings for the VCCPD power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCCPD_USER_OPTION <value>
```



## POWER\_VCCR\_GXBL\_USER\_OPTION

Allows you to specify settings for the VCCR\_GXBL power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCCR_GXBL_USER_OPTION <value>
```

## POWER\_VCCR\_GXBR\_USER\_OPTION

Allows you to specify settings for the VCCR\_GXBR power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCCR_GXBR_USER_OPTION <value>
```





## POWER\_VCCR\_GXB\_USER\_OPTION

Allows you to specify settings for the VCCR\_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCCR_GXB_USER_OPTION <value>
```

## POWER\_VCCT\_GXBL\_USER\_OPTION

Allows you to specify settings for the VCCT\_GXBL power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCCT_GXBL_USER_OPTION <value>
```



## POWER\_VCCT\_GXBR\_USER\_OPTION

Allows you to specify settings for the VCCT\_GXBR power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCCT_GXBR_USER_OPTION <value>
```

## POWER\_VCCT\_GXB\_USER\_OPTION

Allows you to specify settings for the VCCT\_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCCT_GXB_USER_OPTION <value>
```



## POWER\_VCD\_FILE\_END\_TIME

Specifies the time at which toggle rates and static probabilities should stop being calculated for the output signals contained in the VCD files.

### Type

Time

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name POWER_VCD_FILE_END_TIME -entity <entity name> -
```

```
section_id <section identifier> <value>
```

## POWER\_VCD\_FILE\_START\_TIME

Specifies the time at which toggle rates and static probabilities should start to be calculated for the output signals contained in the VCD files.

### Type

Time

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name POWER_VCD_FILE_START_TIME -entity <entity name>
```

-section\_id <section identifier> <value>





## POWER\_VCD\_FILTER\_GLITCHES

Specifies whether or not glitch filtering should be used when reading in VCD files.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name POWER_VCD_FILTER_GLITCHES <value>
```

### Default Value

On

## VCCAUX\_SHARED\_USER\_VOLTAGE

Specifies the voltage of the VCCAUX\_SHARED power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCAUX_SHARED_USER_VOLTAGE <value>
```



## VCCAUX\_USER\_VOLTAGE

Specifies the voltage of the VCCAUX power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCAUX_USER_VOLTAGE <value>
```

## VCCA\_FPLL\_USER\_VOLTAGE

Specifies the voltage of the VCCA\_FPLL power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCA_FPLL_USER_VOLTAGE <value>
```



## VCCA\_GTBR\_USER\_VOLTAGE

Specifies the voltage of the VCCA\_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCA_GTBR_USER_VOLTAGE <value>
```

## VCCA\_GTB\_USER\_VOLTAGE

Specifies the voltage of the VCCA\_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCA_GTB_USER_VOLTAGE <value>
```



## VCCA\_GXBL\_USER\_VOLTAGE

Specifies the voltage of the VCCA\_GXBL power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCA_GXBL_USER_VOLTAGE <value>
```

## VCCA\_GXBR\_USER\_VOLTAGE

Specifies the voltage of the VCCA\_GXBR power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCA_GXBR_USER_VOLTAGE <value>
```



## VCCA\_GXB\_USER\_VOLTAGE

Specifies the voltage of the VCCA\_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCA_GXB_USER_VOLTAGE <value>
```

## VCCA\_L\_USER\_VOLTAGE

Specifies the default voltage of the VCCA\_L power rail supply, which is applied if all transceivers on the left side of the device are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCA_L_USER_VOLTAGE <value>
```



## VCCA\_PLL\_USER\_VOLTAGE

Specifies the voltage of the VCCA\_PLL power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCA_PLL_USER_VOLTAGE <value>
```

## VCCA\_R\_USER\_VOLTAGE

Specifies the default voltage of the VCCA\_R power rail supply, which is applied if all transceivers on the right side of the device are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCA_R_USER_VOLTAGE <value>
```

## VCCA\_USER\_VOLTAGE

Specifies the voltage of the VCCA power rail supply. For devices in the Arria II family, this voltage is applied if the transceivers are powered. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCA_USER_VOLTAGE <value>
```

## VCCBAT\_USER\_VOLTAGE

Specifies the voltage of the VCCBAT power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCBAT_USER_VOLTAGE <value>
```



## VCCCB\_USER\_VOLTAGE

Specifies the voltage of the VCCCB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCCB_USER_VOLTAGE <value>
```

## VCCD\_FPLL\_USER\_VOLTAGE

Specifies the voltage of the VCCD\_FPLL power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCD_FPLL_USER_VOLTAGE <value>
```





## VCCD\_PLL\_USER\_VOLTAGE

Specifies the voltage of the VCCD\_PLL power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCD_PLL_USER_VOLTAGE <value>
```

## VCCD\_USER\_VOLTAGE

Specifies the voltage of the VCCD power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCD_USER_VOLTAGE <value>
```



## VCCEH\_GXBL\_USER\_VOLTAGE

Specifies the default voltage of the VCCEH\_GXBL power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCEH_GXBL_USER_VOLTAGE <value>
```

## VCCEH\_GXBR\_USER\_VOLTAGE

Specifies the default voltage of the VCCEH\_GXBR power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCEH_GXBR_USER_VOLTAGE <value>
```



## VCCEH\_GXB\_USER\_VOLTAGE

Specifies the default voltage of the VCCEH\_GXB power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCEH_GXB_USER_VOLTAGE <value>
```

## VCCERAM\_USER\_VOLTAGE

Specifies the voltage of the VCCERAM power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCERAM_USER_VOLTAGE <value>
```



## VCCE\_GXBL\_USER\_VOLTAGE

Specifies the default voltage of the VCCE\_GXBL power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCE_GXBL_USER_VOLTAGE <value>
```

## VCCE\_GXBR\_USER\_VOLTAGE

Specifies the default voltage of the VCCE\_GXBR power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCE_GXBR_USER_VOLTAGE <value>
```





## VCCE\_GXB\_USER\_VOLTAGE

Specifies the default voltage of the VCCE\_GXB power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCE_GXB_USER_VOLTAGE <value>
```

## VCCE\_USER\_VOLTAGE

Specifies the voltage of the VCCE power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCE_USER_VOLTAGE <value>
```



## VCCHIP\_L\_USER\_VOLTAGE

Specifies the voltage of the VCCHIP\_L power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCHIP_L_USER_VOLTAGE <value>
```

## VCCHIP\_R\_USER\_VOLTAGE

Specifies the voltage of the VCCHIP\_R power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCHIP_R_USER_VOLTAGE <value>
```



## VCCHIP\_USER\_VOLTAGE

Specifies the voltage of the VCCHIP power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCHIP_USER_VOLTAGE <value>
```

## VCCHSSI\_L\_USER\_VOLTAGE

Specifies the voltage of the VCCHSSI\_L power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCHSSI_L_USER_VOLTAGE <value>
```



## VCCHSSI\_R\_USER\_VOLTAGE

Specifies the voltage of the VCCHSSI\_R power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCHSSI_R_USER_VOLTAGE <value>
```

## VCCH\_GTBR\_USER\_VOLTAGE

Specifies the voltage of the VCCH\_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCH_GTBR_USER_VOLTAGE <value>
```



## VCCH\_GTB\_USER\_VOLTAGE

Specifies the voltage of the VCCH\_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCH_GTB_USER_VOLTAGE <value>
```

## VCCH\_GXBL\_USER\_VOLTAGE

Specifies the default voltage of the VCCH\_GXBL power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCH_GXBL_USER_VOLTAGE <value>
```



## VCCH\_GXBR\_USER\_VOLTAGE

Specifies the default voltage of the VCCH\_GXBR power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCH_GXBR_USER_VOLTAGE <value>
```

## VCCH\_GXB\_USER\_VOLTAGE

Specifies the voltage of the VCCH\_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCH_GXB_USER_VOLTAGE <value>
```



## VCCH\_L\_USER\_VOLTAGE

Specifies the default voltage of the VCCH\_L power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCH_L_USER_VOLTAGE <value>
```

## VCCH\_R\_USER\_VOLTAGE

Specifies the default voltage of the VCCH\_R power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCH_R_USER_VOLTAGE <value>
```

## VCCINT\_USER\_VOLTAGE

Specifies the voltage of the VCCINT power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCINT_USER_VOLTAGE <value>
```

## VCCIOREF\_HPS\_USER\_VOLTAGE

Specifies the voltage of the VCCIOREF\_HPS power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCIOREF_HPS_USER_VOLTAGE <value>
```





## VCCIO\_HPS\_USER\_VOLTAGE

Specifies the voltage of the VCCIO\_HPS power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCIO_HPS_USER_VOLTAGE <value>
```

## VCCIO\_USER\_VOLTAGE

Specifies the voltage of the VCCIO power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCIO_USER_VOLTAGE <value>
```



## VCCL\_GTBL\_USER\_VOLTAGE

Specifies the voltage of the VCCL\_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCL_GTBL_USER_VOLTAGE <value>
```

## VCCL\_GTBR\_USER\_VOLTAGE

Specifies the voltage of the VCCL\_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCL_GTBR_USER_VOLTAGE <value>
```



## VCCL\_GTB\_USER\_VOLTAGE

Specifies the voltage of the VCCL\_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCL_GTB_USER_VOLTAGE <value>
```

## VCCL\_GXBL\_USER\_VOLTAGE

Specifies the voltage of the VCCL\_GXBL power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCL_GXBL_USER_VOLTAGE <value>
```



## VCCL\_GXBR\_USER\_VOLTAGE

Specifies the voltage of the VCCL\_GXBR power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCL_GXBR_USER_VOLTAGE <value>
```

## VCCL\_GXB\_USER\_VOLTAGE

Specifies the voltage of the VCCL\_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCL_GXB_USER_VOLTAGE <value>
```





## VCCL\_HPS\_USER\_VOLTAGE

Specifies the voltage of the VCCL\_HPS power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCL_HPS_USER_VOLTAGE <value>
```

## VCCL\_USER\_VOLTAGE

Specifies the voltage of the VCCL power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCL_USER_VOLTAGE <value>
```



## VCCPD\_USER\_VOLTAGE

Specifies the voltage of the VCCPD power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCPD_USER_VOLTAGE <value>
```

## VCCPGM\_USER\_VOLTAGE

Specifies the voltage of the VCCPGM power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCPGM_USER_VOLTAGE <value>
```



## VCCPLL\_HPS\_USER\_VOLTAGE

Specifies the voltage of the VCCPLL\_HPS power rail supply. For more information, refer to the respective device datasheet.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCPLL_HPS_USER_VOLTAGE <value>
```

## VCCPT\_USER\_VOLTAGE

Specifies the voltage of the VCCPT power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCPT_USER_VOLTAGE <value>
```



## VCCP\_USER\_VOLTAGE

Specifies the voltage of the VCCP power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCP_USER_VOLTAGE <value>
```

## VCCRSTCLK\_HPS\_USER\_VOLTAGE

Specifies the voltage of the VCCRSTCLK\_HPS power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCRSTCLK_HPS_USER_VOLTAGE <value>
```





## VCCR\_GTBL\_USER\_VOLTAGE

Specifies the voltage of the VCCR\_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCR_GTBL_USER_VOLTAGE <value>
```

## VCCR\_GTBR\_USER\_VOLTAGE

Specifies the voltage of the VCCR\_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCR_GTBR_USER_VOLTAGE <value>
```



## VCCR\_GTB\_USER\_VOLTAGE

Specifies the voltage of the VCCR\_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCR_GTB_USER_VOLTAGE <value>
```

## VCCR\_GXBL\_USER\_VOLTAGE

Specifies the voltage of the VCCR\_GXBL power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCR_GXBL_USER_VOLTAGE <value>
```



## VCCR\_GXBR\_USER\_VOLTAGE

Specifies the voltage of the VCCR\_GXBR power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCR_GXBR_USER_VOLTAGE <value>
```

## VCCR\_GXB\_USER\_VOLTAGE

Specifies the voltage of the VCCR\_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCR_GXB_USER_VOLTAGE <value>
```



## VCCR\_L\_USER\_VOLTAGE

Specifies the voltage of the VCCR\_L power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCR_L_USER_VOLTAGE <value>
```

## VCCR\_R\_USER\_VOLTAGE

Specifies the voltage of the VCCR\_R power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCR_R_USER_VOLTAGE <value>
```





## VCCR\_USER\_VOLTAGE

Specifies the voltage of the VCCR power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCR_USER_VOLTAGE <value>
```

## VCCT\_GTBL\_USER\_VOLTAGE

Specifies the voltage of the VCCT\_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCT_GTBL_USER_VOLTAGE <value>
```



## VCCT\_GTBR\_USER\_VOLTAGE

Specifies the voltage of the VCCT\_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCT_GTBR_USER_VOLTAGE <value>
```

## VCCT\_GTB\_USER\_VOLTAGE

Specifies the voltage of the VCCT\_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCT_GTB_USER_VOLTAGE <value>
```



## VCCT\_GXBL\_USER\_VOLTAGE

Specifies the voltage of the VCCT\_GXBL power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCT_GXBL_USER_VOLTAGE <value>
```

## VCCT\_GXBR\_USER\_VOLTAGE

Specifies the voltage of the VCCT\_GXBR power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCT_GXBR_USER_VOLTAGE <value>
```

## VCCT\_GXB\_USER\_VOLTAGE

Specifies the voltage of the VCCT\_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCT_GXB_USER_VOLTAGE <value>
```

## VCCT\_L\_USER\_VOLTAGE

Specifies the voltage of the VCCT\_L power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCT_L_USER_VOLTAGE <value>
```





## VCCT\_R\_USER\_VOLTAGE

Specifies the voltage of the VCCT\_R power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCT_R_USER_VOLTAGE <value>
```

## VCCT\_USER\_VOLTAGE

Specifies the voltage of the VCCT power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCCT_USER_VOLTAGE <value>
```



## VCC\_HPS\_USER\_VOLTAGE

Specifies the voltage of the VCC\_HPS power rail supply. For more information, refer to the respective device datasheet.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCC_HPS_USER_VOLTAGE <value>
```

## VCC\_USER\_VOLTAGE

Specifies the voltage of the VCC power rail supply. Refer to the device datasheet for the current device family for more details.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name VCC_USER_VOLTAGE <value>
```



## Programmer Assignments

### GENERATE\_CONFIG\_HEXOUT\_FILE

Generates a Hexadecimal (Intel-format) Output File (.hexout) containing configuration data that can be programmed into a parallel data source, such as an EPROM or a mass storage device, which then in turn configures the target device.

#### Type

Boolean

#### Device Support

Enhanced Configuration Devices

#### Notes

This assignment is included in the Fitter report.

#### Syntax

```
set_global_assignment -name GENERATE_CONFIG_HEXOUT_FILE <value>
```

#### Default Value

Off

## GENERATE\_CONFIG\_ISC\_FILE

Generates an In System Configuration File (.isc) containing configuration data that an intelligent external controller can use to configure the target device.

### Type

Boolean

### Device Support

Enhanced Configuration Devices

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name GENERATE_CONFIG_ISC_FILE <value>
```

### Default Value

Off



## GENERATE\_CONFIG\_JAM\_FILE

Generate a JEDEC STAPL Format File (.jam) containing configuration data that an intelligent external controller can use to configure the target device.

### Type

Boolean

### Device Support

- EPC2
- Enhanced Configuration Devices

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name GENERATE_CONFIG_JAM_FILE <value>
```

### Default Value

Off

## GENERATE\_CONFIG\_JBC\_FILE

Generate a compressed Jam STAPL Byte Code 2.0 File (.jbc) containing configuration data that an intelligent external controller can use to configure the target device.

### Type

Boolean

### Device Support

- EPC2
- Enhanced Configuration Devices

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name GENERATE_CONFIG_JBC_FILE <value>
```

### Default Value

Off



## GENERATE\_CONFIG\_JBC\_FILE\_COMPRESSED

Generate a compressed Jam STAPL Byte Code 2.0 File (.jbc) containing configuration data that an intelligent external controller can use to configure the target device.

### Type

Boolean

### Device Support

- EPC2
- Enhanced Configuration Devices

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name GENERATE_CONFIG_JBC_FILE_COMPRESSED <value>
```

### Default Value

On

## GENERATE\_CONFIG\_SVF\_FILE

Generates a Serial Vector Format File (.svf) containing configuration data that an intelligent external controller can use to configure the target device.

### Type

Boolean

### Device Support

- EPC2
- Enhanced Configuration Devices

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name GENERATE_CONFIG_SVF_FILE <value>
```

### Default Value

Off



## GENERATE\_ISC\_FILE

Directs the programmer to generate an In System Configuration File (.isc) containing configuration data that an intelligent external controller can use to configure the target device.

### Type

Boolean

### Device Support

- MAX3000A
- MAX7000AE
- MAX7000B

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name GENERATE_ISC_FILE <value>
```

### Default Value

Off

## GENERATE\_JAM\_FILE

Directs the programmer to generate a JEDEC JESD71 STAPL Format File (.jam) containing configuration data that an intelligent external controller can use to configure the target device.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name GENERATE_JAM_FILE <value>
```

## Default Value

Off

## GENERATE\_JBC\_FILE

Directs the programmer to generate a compressed JAM Byte Code File (.jbc) containing configuration data that an intelligent external controller can use to configure the target device.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name GENERATE_JBC_FILE <value>
```

## Default Value

Off

## GENERATE\_JBC\_FILE\_COMPRESSED

Generate a compressed JAM Byte Code File (.jbc) containing configuration data that an intelligent external controller can use to configure the target device.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.





## Syntax

```
set_global_assignment -name GENERATE_JBC_FILE_COMPRESSED <value>
```

## Default Value

On

## GENERATE\_SVF\_FILE

Directs the programmer to generate a Serial Vector Format File (.svf) containing configuration data that an intelligent external controller can use to configure the target device.

### Type

Boolean

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- A
- E
- MAX 10
- MAX II
- MAX V
- MAX3000A
- MAX7000A
- MAX7000AE
- MAX7000B
- MAX7000S
- Mercury
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name GENERATE_SVF_FILE <value>
```

## Default Value

Off

## HPS\_EARLY\_IO\_RELEASE

Release the HPS shared I/O bank after the IOCSR programming

### Type

Boolean

### Device Support

Arria 10

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name HPS_EARLY_IO_RELEASE <value>
```

### Default Value

Off

## ISP\_CLAMP\_STATE

Specifies the pin state during in-system programming. This option is ignored if it is assigned to anything other than pins.

### Type

Enumeration

### Values

- High
- Low
- Sample and Sustain
- Tri-state

### Device Support

- MAX 10
- MAX II
- MAX V
- MAX7000B

### Notes

None

### Syntax

```
set_instance_assignment -name ISP_CLAMP_STATE -to <to> -entity <entity  
name> <value>
```

## ISP\_CLAMP\_STATE\_DEFAULT

For used pins that do not have an in-system programming clamp state assignment, this option allows you to specify the state that the pins take during in-system programming. Unused pins and dedicated inputs must always be tri-stated for in-system programming.

### Type

Enumeration

### Values

- High
- Low
- Sample and Sustain
- Tri-state

### Device Support

- MAX 10
- MAX II
- MAX V
- MAX7000B

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name ISP_CLAMP_STATE_DEFAULT <value>
```

### Default Value

Tri-state



## MERGE\_HEX\_FILE

Uses the Hexadecimal (Intel-Format) File (.hex) and the programmable logic Partial SRAM Object File (.psof) to create passive programming files.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name MERGE_HEX_FILE <value>
```

### Default Value

Off

## Project-Wide Assignments

### AGGREGATE\_REVISION

Specifies an AGGREGATE revision type.

#### Type

String

#### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

#### Notes

The value of this assignment is case sensitive.

#### Syntax

```
set_global_assignment -name AGGREGATE_REVISION <value>
```





## AHDL\_FILE

Associates an AHDL source file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name AHDL_FILE <value>
```

## AHDL\_TEXT\_DESIGN\_OUTPUT\_FILE

Associates an AHDL Text Design Output File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name AHDL_TEXT_DESIGN_OUTPUT_FILE <value>
```



## ASM\_FILE

Associates an Assembly source file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name ASM_FILE <value>
```

## AUTO\_EXPORT\_VER\_COMPATIBLE\_DB

Automatically exports version-compatible database files when compilation completes.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name AUTO_EXPORT_VER_COMPATIBLE_DB <value>
```

### Default Value

Off



## BASE\_REVISION

Specifies a BASE revision type.

### Type

String

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name BASE_REVISION <value>
```

## BASE\_REVISION\_PROJECT\_OUTPUT\_DIRECTORY

Specifies the directory where project output files such as the Text-Format Report Files (.rpt) and Equation Files (.eqn) were saved for the base revision. By default, all project output files are saved in the project directory.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name BASE_REVISION_PROJECT_OUTPUT_DIRECTORY <value>
```

## BDF\_FILE

Associates a Block Design File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name BDF_FILE <value>
```

## BINARY\_FILE

Associates a binary file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name BINARY_FILE <value>
```





## BSF\_FILE

Associates a Block Symbol File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name BSF_FILE <value>
```

## CDF\_FILE

Associates a Chain Description File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name CDF_FILE <value>
```



## COMMAND\_MACRO\_FILE

Associates a script file or ModelSim Macro File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name COMMAND_MACRO_FILE <value>
```

## CPP\_FILE

Associates a C++ source file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name CPP_FILE <value>
```



## CPP\_INCLUDE\_FILE

Associates a C++ include file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name CPP_INCLUDE_FILE <value>
```

## CUSP\_FILE

Associates a C++ source file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name CUSP_FILE <value>
```



## CVP\_REVISION

Specifies a CVP revision type.

### Type

String

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name CVP_REVISION <value>
```

## C\_FILE

Associates a C source file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name C_FILE <value>
```





## DEPENDENCY\_FILE

Associates a Dependency file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name DEPENDENCY_FILE <value>
```

## DSPBUILDER\_FILE

Associates a DSPBuilder source file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name DSPBUILDER_FILE <value>
```



## EDIF\_FILE

Associates an EDIF source file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDIF_FILE <value>
```

## ELF\_FILE

Associates an ELF file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name ELF_FILE <value>
```



## ENABLE\_COMPACT\_REPORT\_TABLE

Allows you to view the report table in compact format.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name ENABLE_COMPACT_REPORT_TABLE <value>
```

### Default Value

Off

## ENABLE\_REDUCED\_MEMORY\_MODE

Determines whether to enable compiler to run in reduced memory mode. This assignment controls a small number of memory-intensive fitter optimizations. Therefore, enabling the reduced memory mode may slightly impact the performance of your design.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name ENABLE_REDUCED_MEMORY_MODE <value>
```

### Default Value

Off



## EQUATION\_FILE

Associates an Equation File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EQUATION_FILE <value>
```

## FLOW\_DISABLE\_ASSEMBLER

Allows you to turn on or turn off the Assembler during compilation.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name FLOW_DISABLE_ASSEMBLER <value>
```

### Default Value

Off





## FLOW\_ENABLE\_HC\_COMPARE

Enable HardCopy Compare during compilation

### Type

Boolean

### Device Support

- HardCopy II
- HardCopy III
- HardCopy IV

### Notes

None

### Syntax

```
set_global_assignment -name FLOW_ENABLE_HC_COMPARE <value>
```

### Default Value

Off

## FLOW\_ENABLE\_IO\_ASSIGNMENT\_ANALYSIS

Allows you to run I/O assignment analysis before compilation

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name FLOW_ENABLE_IO_ASSIGNMENT_ANALYSIS <value>
```

### Default Value

Off

## FLOW\_ENABLE\_PARALLEL\_MODULES

Allows you to run Assembler and TimeQuest Timing Analyzer in parallel during compilation.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name FLOW_ENABLE_PARALLEL_MODULES <value>
```

### Default Value

On

## FLOW\_ENABLE\_POWER\_ANALYZER

Allows you to turn on or turn off the Power Analyzer during compilation.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name FLOW_ENABLE_POWER_ANALYZER <value>
```

### Default Value

Off



## FLOW\_ENABLE\_RTL\_VIEWER

Allows the RTL Viewer to process the schematic during design compilation. Turning on this option also allows you to open the RTL Viewer after the Analysis & Synthesis portion of design compilation completes, rather than waiting for the full compilation to complete.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name FLOW_ENABLE_RTL_VIEWER <value>
```

### Default Value

Off

## FLOW\_HARDCOPY\_DESIGN\_READINESS\_CHECK

Allows you to turn on or turn off the HardCopy Design Readiness Check during compilation.

### Type

Boolean

### Device Support

- Arria II GZ
- HardCopy II
- HardCopy III
- HardCopy IV
- Stratix II
- Stratix III
- Stratix IV

### Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name FLOW_HARDCOPY_DESIGN_READINESS_CHECK <value>
```

### Default Value

On

## GDF\_FILE

Associates a GDF source file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name GDF_FILE <value>
```

## HC\_OUTPUT\_DIR

Specifies the directory to which HardCopy handoff files should be generated

### Type

File name

### Device Support

- HardCopy II
- HardCopy III
- HardCopy IV

### Notes

The value of this assignment is case sensitive.

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name HC_OUTPUT_DIR <value>
```

### Default Value

hc\_output





## HEX\_FILE

Associates a Hexadecimal source file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name HEX_FILE <value>
```

## HEX\_OUTPUT\_FILE

Associates a Hexadecimal Output File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name HEX_OUTPUT_FILE <value>
```



## HPS\_ISW\_FILE

Associates a hard processor system (HPS) initial software configuration file with an HPS entity.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name HPS_ISW_FILE -entity <entity name> <value>  
set_instance_assignment -name HPS_ISW_FILE -to <to> -entity <entity name>  
<value>
```

## HTML\_FILE

Associates an HTML file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name HTML_FILE <value>
```



## HTML\_REPORT\_FILE

Associates an HTML Report File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name HTML_REPORT_FILE <value>
```

## INCLUDE\_FILE

Associates an Include File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name INCLUDE_FILE <value>
```



## IPA\_FILE

Associates an IP Advisor file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IPA_FILE <value>
```

## IPX\_FILE

Associates a Quartus Prime IP-XACT description file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IPX_FILE <value>
```





## IP\_COMPONENT\_AUTHOR

Specifies the IP component author

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IP_COMPONENT_AUTHOR <value>
set_global_assignment -name IP_COMPONENT_AUTHOR -entity <entity name>
<value>
set_instance_assignment -name IP_COMPONENT_AUTHOR -to <to> -entity <entity
name> <value>
```

## IP\_COMPONENT\_DESCRIPTION

Specifies the IP component description

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IP_COMPONENT_DESCRIPTION <value>
set_global_assignment -name IP_COMPONENT_DESCRIPTION -entity <entity name>
<value>
set_instance_assignment -name IP_COMPONENT_DESCRIPTION -to <to> -entity
<entity name> <value>
```



## IP\_COMPONENT\_DISPLAY\_NAME

Specifies the IP component display name

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IP_COMPONENT_DISPLAY_NAME <value>
set_global_assignment -name IP_COMPONENT_DISPLAY_NAME -entity <entity name>
<value>
set_instance_assignment -name IP_COMPONENT_DISPLAY_NAME -to <to> -entity
<entity name> <value>
```

## IP\_COMPONENT\_DOCUMENTATION\_LINK

Specifies a documentation link for the IP component

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IP_COMPONENT_DOCUMENTATION_LINK <value>
set_global_assignment -name IP_COMPONENT_DOCUMENTATION_LINK -entity <entity
name> <value>
set_instance_assignment -name IP_COMPONENT_DOCUMENTATION_LINK -to <to> -
entity <entity name> <value>
```

## IP\_COMPONENT\_GROUP

Specifies the group in the Component Library that includes this IP component

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IP_COMPONENT_GROUP <value>
set_global_assignment -name IP_COMPONENT_GROUP -entity <entity name> <value>
set_instance_assignment -name IP_COMPONENT_GROUP -to <to> -entity <entity
name> <value>
```

## IP\_COMPONENT\_INTERNAL

Specifies the if the IP is an internal component.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

### Syntax

```
set_global_assignment -name IP_COMPONENT_INTERNAL <value>
set_global_assignment -name IP_COMPONENT_INTERNAL -entity <entity name>
<value>
set_instance_assignment -name IP_COMPONENT_INTERNAL -to <to> -entity
<entity name> <value>
```

### Default Value

Off

## IP\_COMPONENT\_NAME

Specifies the IP component name

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IP_COMPONENT_NAME <value>
set_global_assignment -name IP_COMPONENT_NAME -entity <entity name> <value>
set_instance_assignment -name IP_COMPONENT_NAME -to <to> -entity <entity
name> <value>
```

## IP\_COMPONENT\_PARAMETER

Specifies the parameter, value, and display name of an IP component parameter

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IP_COMPONENT_PARAMETER <value>
set_global_assignment -name IP_COMPONENT_PARAMETER -entity <entity name>
<value>
set_instance_assignment -name IP_COMPONENT_PARAMETER -to <to> -entity
<entity name> <value>
```



## IP\_COMPONENT\_REPORT\_HIERARCHY

Specifies the if the IP component should report its hierarchy

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

### Syntax

```
set_global_assignment -name IP_COMPONENT_REPORT_HIERARCHY <value>
set_global_assignment -name IP_COMPONENT_REPORT_HIERARCHY -entity <entity
name> <value>
set_instance_assignment -name IP_COMPONENT_REPORT_HIERARCHY -to <to> -
entity <entity name> <value>
```

### Default Value

Off

## IP\_COMPONENT\_VERSION

Specifies the IP component version

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IP_COMPONENT_VERSION <value>
set_global_assignment -name IP_COMPONENT_VERSION -entity <entity name>
<value>
set_instance_assignment -name IP_COMPONENT_VERSION -to <to> -entity <entity
name> <value>
```

## IP\_FILE

Associates a Qsys IP file (.ip) with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IP_FILE <value>
```

## IP\_GENERATED\_DEVICE\_FAMILY

Specifies the device families for which the IP core was generated for.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IP_GENERATED_DEVICE_FAMILY <value>
set_global_assignment -name IP_GENERATED_DEVICE_FAMILY -entity <entity
name> <value>
set_instance_assignment -name IP_GENERATED_DEVICE_FAMILY -to <to> -entity
<entity name> <value>
```

## IP\_QSYS\_MODE

Mode used to generate a QIP

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IP_QSYS_MODE <value>  
set_global_assignment -name IP_QSYS_MODE -entity <entity name> <value>  
set_instance_assignment -name IP_QSYS_MODE -to <to> -entity <entity name>  
<value>
```

## IP\_TARGETED\_DEVICE\_FAMILY

Specifies the device family for which the IP core was targeted.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IP_TARGETED_DEVICE_FAMILY <value>
set_global_assignment -name IP_TARGETED_DEVICE_FAMILY -entity <entity name>
<value>
set_instance_assignment -name IP_TARGETED_DEVICE_FAMILY -to <to> -entity
<entity name> <value>
```



## IP\_TARGETED\_PART\_TRAIT

Specifies a part trait for which IP core was targeted.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IP_TARGETED_PART_TRAIT <value>
set_global_assignment -name IP_TARGETED_PART_TRAIT -entity <entity name>
<value>
set_instance_assignment -name IP_TARGETED_PART_TRAIT -to <to> -entity
<entity name> <value>
```

## IP\_TOOL\_ENV

Specifies the tool which generated the IP core.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IP_TOOL_ENV <value>
set_global_assignment -name IP_TOOL_ENV -entity <entity name> <value>
set_instance_assignment -name IP_TOOL_ENV -to <to> -entity <entity name>
<value>
```



## IP\_TOOL\_HIERARCHY\_LEVELS

Specifies the number of levels of hierarchy from the IP root.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IP_TOOL_HIERARCHY_LEVELS <value>
set_global_assignment -name IP_TOOL_HIERARCHY_LEVELS -entity <entity name>
<value>
set_instance_assignment -name IP_TOOL_HIERARCHY_LEVELS -to <to> -entity
<entity name> <value>
```

## IP\_TOOL\_NAME

Specifies the IP core name.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IP_TOOL_NAME <value>
set_global_assignment -name IP_TOOL_NAME -entity <entity name> <value>
set_instance_assignment -name IP_TOOL_NAME -to <to> -entity <entity name>
<value>
```

## IP\_TOOL\_VERSION

Specifies the IP core version

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IP_TOOL_VERSION <value>
set_global_assignment -name IP_TOOL_VERSION -entity <entity name> <value>
set_instance_assignment -name IP_TOOL_VERSION -to <to> -entity <entity
name> <value>
```

## ISC\_FILE

IEEE 1532 file

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name ISC_FILE <value>
```



## JAM\_FILE

Associates a Jam File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name JAM_FILE <value>
```

## JBC\_FILE

Associates a Jam Byte-Code File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name JBC_FILE <value>
```



## LICENSE\_FILE

Associates a License File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name LICENSE_FILE <value>
```

## LMF\_FILE

Associates a Library Mapping File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name LMF_FILE <value>
```





## LOGIC\_ANALYZER\_INTERFACE\_FILE

Associates a Logic Analyzer Interface file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name LOGIC_ANALYZER_INTERFACE_FILE <value>
```

## MAP\_FILE

EPC16 addresses used

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name MAP_FILE <value>
```



## MASK\_REVISION

Specifies a MASK revision type.

### Type

String

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name MASK_REVISION <value>
```

## MESSAGE\_DISABLE

Tells the compiler to suppress the specified user message(s).

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports Fitter wildcards.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name MESSAGE_DISABLE <value>
set_global_assignment -name MESSAGE_DISABLE -entity <entity name> <value>
set_instance_assignment -name MESSAGE_DISABLE -to <to> -entity <entity
name> <value>
```



## MESSAGE\_ENABLE

Tells the compiler to enable the specified user message(s).

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports Fitter wildcards.

This assignment supports synthesis wildcards.

### Syntax

```
set_global_assignment -name MESSAGE_ENABLE <value>  
set_global_assignment -name MESSAGE_ENABLE -entity <entity name> <value>  
set_instance_assignment -name MESSAGE_ENABLE -to <to> -entity <entity name>  
<value>
```

## MIF\_FILE

Associates a Memory Initialization File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name MIF_FILE <value>
```



## MIGRATION\_DIFFERENT\_SOURCE\_FILE

Specifies a HDL source file that will be different in the companion revision. This is used to allow setting differences between the current and companion revision. The companion revision will have a different source file than the one specified here.

### Type

File name

### Device Support

- HardCopy II
- HardCopy III
- HardCopy IV
- Stratix II

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name MIGRATION_DIFFERENT_SOURCE_FILE <value>
```

## MISC\_FILE

Associates a file with this project. Files assigned to this assignment will be archived by the Project Archive command if the 'Project source and settings files' file subset is selected.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name MISC_FILE <value>
```





## NUM\_PARALLEL\_PROCESSORS

Specifies the maximum number of processors allocated for parallel compilation on a single machine. For parallel compilation you can use all available processors on your machine, or specify the number of processors you want to use. For example, if you have a quad-core processor machine and want to leave one processor free for other tasks, you specify '3' as the setting of this option. A setting of '1' disables parallel compilation.

### Old Name

MAX\_PROCESSORS\_USED\_FOR\_MULTITHREADING

### Type

String

### Device Support

- Arria 10
- Arria GX
- Arria II GX
- Arria II GZ
- Arria V
- Arria V GZ
- Cyclone
- Cyclone 10 LP
- Cyclone II
- Cyclone III
- Cyclone III LS
- Cyclone IV E
- Cyclone IV GX
- Cyclone V
- HardCopy II
- HardCopy III
- HardCopy IV
- MAX 10
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV
- Stratix V

### Notes

This assignment is included in the Fitter report.

## Syntax

```
set_global_assignment -name NUM_PARALLEL_PROCESSORS <value>
```



## OBJECT\_FILE

Associates an Object file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name OBJECT_FILE <value>
```

## OCP\_FILE

Specifies the OpenCore core plus file generated by the MegaWizard. This file is used by Quartus to allow compilation and sof generation of the core without a license.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name OCP_FILE <value>
```



## PARTIAL\_SRAM\_OBJECT\_FILE

Associates a Partial SRAM Object File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name PARTIAL_SRAM_OBJECT_FILE <value>
```

## PDC\_FILE

Associates a Physical Design Constraint File (.pdc) with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name PDC_FILE <value>
```



## PERSONA\_FILE

Associates a Quartus Prime Persona with this project as a source file.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name PERSONA_FILE <value>
```

## PIN\_FILE

Associates a Pin-Out File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name PIN_FILE <value>
```





## POWER\_INPUT\_FILE

Associates a Power Input File (.pwf) with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name POWER_INPUT_FILE <value>
```

## PPF\_FILE

Specifies the name of the MegaWizard generated .ppf file containing core specific pin assignments. This file will be loaded by Pin Planner.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name PPF_FILE <value>
```



## PROGRAMMER\_OBJECT\_FILE

Associates a Programmer Object File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name PROGRAMMER_OBJECT_FILE <value>
```

## PROJECT\_OUTPUT\_DIRECTORY

Specifies the directory in which to save all project output files such as the Text-Format Report Files (.rpt) and Equation Files (.eqn). By default, all project output files are saved in the project directory.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name PROJECT_OUTPUT_DIRECTORY <value>
```

## PROJECT\_SHOW\_ENTITY\_NAME

Determines whether to display the entity name for node names

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

### Syntax

```
set_global_assignment -name PROJECT_SHOW_ENTITY_NAME <value>
```

### Default Value

On

## PROJECT\_USE\_SIMPLIFIED\_NAMES

Determines whether to use the simplified naming scheme.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name PROJECT_USE_SIMPLIFIED_NAMES <value>
```

### Default Value

Off



## QARLOG\_FILE

Associates an Archive Log file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name QARLOG_FILE <value>
```

## QAR\_FILE

Associates an Archive file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name QAR_FILE <value>
```





## QDB\_FILE

Associates a QDB archive as a source file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name QDB_FILE <value>
```

## QIP\_FILE

Associates a Quartus Prime IP file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name QIP_FILE <value>
```



## QSYS\_FILE

Associates a Qsys file (.qsys) with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name QSYS_FILE <value>
```

## QUARTUS\_PTF\_FILE

Associates a Peripheral Template File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name QUARTUS_PTF_FILE <value>
```



## QUARTUS\_SBD\_FILE

Associates a Quartus Prime System Build Descriptor File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name QUARTUS_SBD_FILE <value>
```

## QUARTUS\_STANDARD\_DELAY\_FILE

Associates a Quartus Prime Standard Delay Format File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name QUARTUS_STANDARD_DELAY_FILE <value>
```



## QVAR\_FILE

Associates a Quartus Prime IP variation file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name QVAR_FILE <value>
```

## QXP\_FILE

Associates a Quartus Prime Exported Partition (QXP) with this project as a source file

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name QXP_FILE <value>
```





## RAW\_BINARY\_FILE

Associates a Raw Binary File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name RAW_BINARY_FILE <value>
```

## READ\_OR\_WRITE\_IN\_BYTE\_ADDRESS

Determines whether to read or write Hexadecimal(.hex) File in byte addressable mode for this project.

### Type

Enumeration

### Values

- Off
- On
- Use global settings

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name READ_OR_WRITE_IN_BYTE_ADDRESS <value>
```

### Default Value

Use global settings

## RECONFIGURABLE\_REVISION

Specifies a RECONFIGURABLE revision type.

### Type

String

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name RECONFIGURABLE_REVISION <value>
```

## REVISION\_TYPE

Describes the type of revision. The possible revision types are BASE, RECONFIGURABLE, AGGREGATE, CVP, and MASK. The default type is BASE.

### Type

Enumeration

### Values

- Aggregate
- Base
- CVP
- Mask
- PR\_Base
- PR\_Impl
- PR\_Syn
- Reconfigurable

### Device Support

- Arria 10
- Arria V
- Arria V GZ
- Cyclone V
- Stratix V

### Notes

None

### Syntax

```
set_global_assignment -name REVISION_TYPE <value>
```

## RUN\_FULL\_COMPILE\_ON\_DEVICE\_CHANGE

Run Full Compilation when the device changes

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name RUN_FULL_COMPILE_ON_DEVICE_CHANGE <value>
```

### Default Value

On

## SAVE\_MIGRATION\_INFO\_DURING\_COMPILATION

Option to save out migration information during compilation

### Old Name

HARDCOPYII\_SAVE\_MIGRATION\_INFO\_DURING\_COMPILATION

### Type

Boolean

### Device Support

- HardCopy II
- HardCopy III
- HardCopy IV
- Stratix II

### Notes

None

### Syntax

```
set_global_assignment -name SAVE_MIGRATION_INFO_DURING_COMPILATION <value>
```

### Default Value

Off

## SBI\_FILE

Associates a Slave Binary Image File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SBI_FILE <value>
```

## SDC\_ENTITY\_FILE

Associates a Synopsys Design Constraint File (.sdc) with an entity.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SDC_ENTITY_FILE -entity <entity name> <value>
set_instance_assignment -name SDC_ENTITY_FILE -to <to> -entity <entity
name> <value>
set_global_assignment -name SDC_ENTITY_FILE <value>
```



## SDC\_ENTITY\_HELPER\_FILE

Associates a file \"sourced\" into a Synopsys Design Constraint File (.sdc) with an entity. Helper files are usually TCL (.tcl) files.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SDC_ENTITY_HELPER_FILE -entity <entity name>
<value>
set_instance_assignment -name SDC_ENTITY_HELPER_FILE -to <to> -entity
<entity name> <value>
set_global_assignment -name SDC_ENTITY_HELPER_FILE <value>
```

## SDC\_FILE

Associates a Synopsys Design Constraint File (.sdc) with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SDC_FILE <value>
```



## SDF\_OUTPUT\_FILE

Associates a Standard Delay Format Output File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SDF_OUTPUT_FILE <value>
```

## SERIAL\_BITSTREAM\_FILE

Associates a Serial Bitstream File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SERIAL_BITSTREAM_FILE <value>
```



## SIGNALTAP\_FILE

Associates a SignalTap II file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SIGNALTAP_FILE <value>
```

## SIP\_FILE

Associates a Simulation IP File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SIP_FILE <value>
```



## SLD\_FILE

Associates a file with this project. Files assigned to this assignment will be archived by the Project Archive command if the 'Project source and settings files' file subset is selected.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SLD_FILE <value>
```

## SMF\_FILE

Associates a State Machine file (.smf) with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SMF_FILE <value>
```





## SOFTWARE\_LIBRARY\_FILE

Associates a Software library file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SOFTWARE_LIBRARY_FILE <value>
```

## SOPCINFO\_FILE

Associates a Qsys or SOPC Builder report file with this project. If you select the Project source and settings files option, the Project Archive command will archive the files assigned to this assignment.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SOPCINFO_FILE <value>
```



## SOPC\_FILE

Associates a SOPC Builder file (.sopc) with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SOPC_FILE <value>
```

## SOURCE\_TCL\_SCRIPT\_FILE

Runs Tcl script file. This assignment has the same effect as 'source <filename>'.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SOURCE_TCL_SCRIPT_FILE <value>
```



## SPD\_FILE

Associates a Simulation Package Descriptor File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SPD_FILE <value>
```

## SRAM\_OBJECT\_FILE

Associates an SRAM Object File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SRAM_OBJECT_FILE <value>
```



## SRECORDS\_FILE

Associates a Motorola S-Record file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SRECORDS_FILE <value>
```

## SVF\_FILE

Associates a Serial Vector Format File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SVF_FILE <value>
```





## SYM\_FILE

Associates a Symbol File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SYM_FILE <value>
```

## SYNTHESIS\_ONLY\_QIP

Determines whether a Quartus Prime IP File is not for simulation.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SYNTHESIS_ONLY_QIP <value>
```

## SYSTEMVERILOG\_FILE

Associates a SystemVerilog HDL source file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SYSTEMVERILOG_FILE <value>
```

## TCL\_ENTITY\_FILE

Associates a TCL File (.tcl) with an entity. These files are often \"sourced\" into Synopsys Design Constraint Files (.sdc) that were also associated with the same entity .

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name TCL_ENTITY_FILE -entity <entity name> <value>
set_instance_assignment -name TCL_ENTITY_FILE -to <to> -entity <entity
name> <value>
set_global_assignment -name TCL_ENTITY_FILE <value>
```



## TCL\_SCRIPT\_FILE

Associates a Tcl script file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name TCL_SCRIPT_FILE <value>
```

## TEMPLATE\_FILE

Associates a Template File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name TEMPLATE_FILE <value>
```



## TEXT\_FILE

Associates a text file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name TEXT_FILE <value>
```

## TEXT\_FORMAT\_REPORT\_FILE

Associates a text-format Report File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name TEXT_FORMAT_REPORT_FILE <value>
```





## TIMING\_ANALYSIS\_OUTPUT\_FILE

Associates a Timing Analysis Output File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name TIMING_ANALYSIS_OUTPUT_FILE <value>
```

## VCD\_FILE

Associates a Verilog Value Change Dump File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name VCD_FILE <value>
```

## VECTOR\_TABLE\_OUTPUT\_FILE

Associates a Vector Table Output File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name VECTOR_TABLE_OUTPUT_FILE <value>
```

## VECTOR\_TEXT\_FILE

Associates a text-format Vector File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name VECTOR_TEXT_FILE <value>
```



## VECTOR\_WAVEFORM\_FILE

Associates a Vector Waveform File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name VECTOR_WAVEFORM_FILE <value>
```

## VERILOG\_FILE

Associates a Verilog HDL source file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name VERILOG_FILE <value>
```



## VERILOG\_INCLUDE\_FILE

Associates a Verilog Include file with this project.

### Old Name

VERILOG\_VH\_FILE

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name VERILOG_INCLUDE_FILE <value>
```

## VERILOG\_OUTPUT\_FILE

Associates a Verilog Output File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name VERILOG_OUTPUT_FILE <value>
```





## VERILOG\_TEST\_BENCH\_FILE

Associates a Verilog HDL Test Bench File (.vt) with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name VERILOG_TEST_BENCH_FILE <value>
```

## VER\_COMPATIBLE\_DB\_DIR

Specifies the directory to which version-compatible database files should be saved

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is not copied when you create a companion revision for HardCopy II devices.

### Syntax

```
set_global_assignment -name VER_COMPATIBLE_DB_DIR <value>
```

### Default Value

export\_db

## VHDL\_FILE

Associates a VHDL source file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name VHDL_FILE <value>
```

## VHDL\_OUTPUT\_FILE

Associates a VHDL Output File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name VHDL_OUTPUT_FILE <value>
```



## VHDL\_TEST\_BENCH\_FILE

Associates a VHDL Test Bench File (.vht) with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name VHDL_TEST_BENCH_FILE <value>
```

## VQM\_FILE

Associates a structural Verilog HDL source file with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name VQM_FILE <value>
```



## ZIP\_VECTOR\_WAVEFORM\_FILE

Associates a Compressed Vector Waveform File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name ZIP_VECTOR_WAVEFORM_FILE <value>
```

## SignalProbe Assignments

### SIGNALPROBE\_ALLOW\_OVERUSE

This option controls whether the Quartus Prime Fitter will move nodes in a design in order to ensure that signalprobe signals get routed to the appropriate pin.

#### Type

Boolean

#### Notes

None

#### Syntax

```
set_global_assignment -name SIGNALPROBE_ALLOW_OVERUSE <value>
```

#### Default Value

Off



## SIGNALPROBE\_CLOCK

Registers the output of the SignalProbe node and assigns the specified clock to this register.

### Type

String

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_instance_assignment -name SIGNALPROBE_CLOCK -to <to> <value>
```

## SIGNALPROBE\_DURING\_NORMAL\_COMPILATION

When enabled, SignalProbe signals will be routed during normal compilation.

### Type

Boolean

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name SIGNALPROBE_DURING_NORMAL_COMPILATION <value>
```

### Default Value

Off

## SIGNALPROBE\_ENABLE

Selects whether SignalProbe routing is enabled for current node.

### Type

Boolean

### Notes

None

### Syntax

```
set_instance_assignment -name SIGNALPROBE_ENABLE -to <to> <value>
```

## SIGNALPROBE\_NUM\_REGISTERS

Specifies the number of registers to insert before the output of the SignalProbe pin.

### Type

Integer

### Notes

None

### Syntax

```
set_instance_assignment -name SIGNALPROBE_NUM_REGISTERS -to <to> <value>
```

## SIGNALPROBE\_SOURCE

Assigns the source of the signal to be routed to the specified SignalProbe node.

### Type

String

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_instance_assignment -name SIGNALPROBE_SOURCE -to <to> <value>
```

## SignalTap II Assignments

### ENABLE\_LOGIC\_ANALYZER\_INTERFACE

Enables Logic Analyzer Interface for compilation

#### Type

Boolean

#### Device Support

This setting can be used in projects targeting any Altera device family.

#### Notes

This assignment is included in the Fitter report.

#### Syntax

```
set_global_assignment -name ENABLE_LOGIC_ANALYZER_INTERFACE <value>
```



## ENABLE\_SIGNALTAP

Enables the SignalTap II Logic Analyzer for compilation

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name ENABLE_SIGNALTAP <value>
```

## STP\_FILE

Associates a SignalTap II Logic Analyzer File with this project.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name STP_FILE <value>
```





## USE\_LOGIC\_ANALYZER\_INTERFACE\_FILE

Specifies the Logic Analyzer Interface File to be used for compilation.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name USE_LOGIC_ANALYZER_INTERFACE_FILE <value>
```

## USE\_SIGNALTAP\_FILE

Specifies the SignalTap II Logic Analyzer File to be used for compilation.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

### Syntax

```
set_global_assignment -name USE_SIGNALTAP_FILE <value>
```



# Simulator Assignments

## ACTION

Specifies the breakpoint's action when triggered.

### Type

Enumeration

### Values

- Give Error
- Give Info
- Give Warning
- Stop

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name ACTION -section_id <section identifier> <value>
```

## ADD\_DEFAULT\_PINS\_TO\_SIMULATION\_OUTPUT\_WAVEFORMS

Adds output pins to the simulation vector output waveforms automatically.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name ADD_DEFAULT_PINS_TO_SIMULATION_OUTPUT_WAVEFORMS  
<value>
```

### Default Value

On



## ADD\_TO\_SIMULATION\_OUTPUT\_WAVEFORMS

Adds the signal to the list of signals for which output waveforms are shown in the simulation report. This option makes a node observable during simulation.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_instance_assignment -name ADD_TO_SIMULATION_OUTPUT_WAVEFORMS -to <to> -  
entity <entity name> <value>
```

## ALIAS

Specifies an alias for the full hierarchical name of the node.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_instance_assignment -name ALIAS -to <to> -entity <entity name> <value>
```



## AUTO\_USE\_SIMULATION\_PDB\_NETLIST

Automatically saves/loads simulation netlist to/from external file

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name AUTO_USE_SIMULATION_PDB_NETLIST <value>
```

### Default Value

Off

## BREAKPOINT\_STATE

Specifies the state of a breakpoint as either enabled or disabled.

### Type

Enumeration

### Values

- Disabled
- Enabled

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name BREAKPOINT_STATE -section_id <section  
identifier> <value>
```



## CHECK\_OUTPUTS

Checks expected outputs vs. actual outputs in the simulation report.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name CHECK_OUTPUTS <value>
```

### Default Value

Off

## END\_TIME

Specifies the end time for simulation.

### Type

Time

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name END_TIME <value>
```



## EXTERNAL\_PIN\_CONNECTION

Specifies an external pin connection between an output pin and an input pin. This option is used during simulations only.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_instance_assignment -name EXTERNAL_PIN_CONNECTION -to <to> -entity  
<entity name> <value>
```

## GLITCH\_DETECTION

Monitors the design for user-defined glitches (spikes).

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name GLITCH_DETECTION <value>
```

### Default Value

Off



## GLITCH\_INTERVAL

Allows you to detect glitches and specify the time interval that defines a glitch. If two logic level transitions occur in a period shorter than the specified time period, the resulting glitch is detected and reported in the Processing tab of the Messages window.

### Type

Time

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name GLITCH_INTERVAL <value>
```

### Default Value

1ns

## IMMEDIATE\_ASSERTION\_FAIL\_ACTION

Specifies the immediate assertion's action when the assertion fails.

### Type

Enumeration

### Values

- Give Error
- Give Info
- Give Warning
- Stop

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name IMMEDIATE_ASSERTION_FAIL_ACTION -section_id  
<section identifier> <value>
```

## IMMEDIATE\_ASSERTION\_FAIL\_MESSAGE

Specifies the immediate assertion's message when the assertion fails.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IMMEDIATE_ASSERTION_FAIL_MESSAGE -section_id  
<section identifier> <value>
```

## IMMEDIATE\_ASSERTION\_PASS\_MESSAGE

Specifies the immediate assertion's message when the assertion passes.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IMMEDIATE_ASSERTION_PASS_MESSAGE -section_id  
<section identifier> <value>
```





## IMMEDIATE\_ASSERTION\_STATE

Specifies the state of an immediate assertion as either enabled or disabled.

### Type

Enumeration

### Values

- Disabled
- Enabled

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name IMMEDIATE_ASSERTION_STATE -section_id <section  
identifier> <value>
```

## IMMEDIATE\_ASSERTION\_TEST\_CONDITION

Specifies the immediate assertion's test condition.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name IMMEDIATE_ASSERTION_TEST_CONDITION -section_id  
<section identifier> <value>
```

## INCREMENTAL\_VECTOR\_INPUT\_SOURCE

Specifies the source of input vectors to be used for simulation.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name INCREMENTAL_VECTOR_INPUT_SOURCE <value>
```

## PASSIVE\_RESISTOR

Specifies whether an output or bidirectional pin has a pull-up or pull-down resistor. This option is used in functional simulations only.

### Type

Enumeration

### Values

- Pull-down
- Pull-up

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_instance_assignment -name PASSIVE_RESISTOR -to <to> -entity <entity  
name> <value>
```

## SETUP\_HOLD\_DETECTION

Detects setup and hold time violations.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name SETUP_HOLD_DETECTION <value>
```

### Default Value

Off

## SETUP\_HOLD\_DETECTION\_INPUT\_REGISTERS\_BIDIR\_PINS\_DISABLED

Disables setup and hold time violations detection in input registers of bi-directional pins.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name  
SETUP_HOLD_DETECTION_INPUT_REGISTERS_BIDIR_PINS_DISABLED <value>
```

### Default Value

Off

## SETUP\_HOLD\_TIME\_VIOLATION\_DETECTION

Enables setup and hold time violation detection during simulation.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_instance_assignment -name SETUP_HOLD_TIME_VIOLATION_DETECTION -to <to> -  
entity <entity name> <value>
```

## SIMULATION\_BUS\_CHANNEL\_GROUPING

Automatically groups bus channels in the output waveforms which are shown in the simulation report.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIMULATION_BUS_CHANNEL_GROUPING <value>
```

### Default Value

Off



## SIMULATION\_CELL\_DELAY\_MODEL\_TYPE

Specifies the type of delay model to be used for cell delays : transport or inertial

### Type

Enumeration

### Values

- Inertial
- Transport

### Device Support

- Arria II GZ
- Cyclone III
- Cyclone III LS
- Stratix III
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name SIMULATION_CELL_DELAY_MODEL_TYPE <value>
```

### Default Value

TRANSPORT

## SIMULATION\_COMPARE\_SIGNAL

Specifies the signal to be compared in a waveform comparison.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_instance_assignment -name SIMULATION_COMPARE_SIGNAL -to <to> -entity  
<entity name> <value>
```

## SIMULATION\_COMPLETE\_COVERAGE\_REPORT\_PANEL

Display report on output ports that toggle between 1 and 0 during simulation.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
<value> set_global_assignment -name SIMULATION_COMPLETE_COVERAGE_REPORT_PANEL
```

### Default Value

On

## SIMULATION\_COVERAGE

Reports 'coverage,' that is, the ratio of output ports that toggle between 1 and 0 during simulation, compared to the total number of output ports present in the netlist, expressed as a percentage.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIMULATION_COVERAGE <value>
```

### Default Value

On

## SIMULATION\_DEFAULT\_VECTOR\_COMPARE\_TOLERANCE

Specifies the default comparison timing tolerance to be used in a waveform comparison.

### Type

Time

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIMULATION_DEFAULT_VECTOR_COMPARE_TOLERANCE  
<value>
```

## SIMULATION\_INTERCONNECT\_DELAY\_MODEL\_TYPE

Specifies the type of delay model to be used for interconnect delays : transport or inertial

### Type

Enumeration

### Values

- Inertial
- Transport

### Device Support

- Arria II GZ
- Cyclone III
- Cyclone III LS
- Stratix III
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name SIMULATION_INTERCONNECT_DELAY_MODEL_TYPE <value>
```

### Default Value

TRANSPORT

## SIMULATION\_MISSING\_0\_VALUE\_COVERAGE\_REPORT\_PANEL

Display report on output ports that do not toggle to 0 during simulation.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name  
SIMULATION_MISSING_0_VALUE_COVERAGE_REPORT_PANEL <value>
```

### Default Value

On

## SIMULATION\_MISSING\_1\_VALUE\_COVERAGE\_REPORT\_PANEL

Display report on output ports that do not toggle to 1 during simulation.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name  
SIMULATION_MISSING_1_VALUE_COVERAGE_REPORT_PANEL <value>
```

### Default Value

On



## SIMULATION\_MODE

Specifies the type of simulation to perform for the current Simulation focus.

### Type

Enumeration

### Values

- Functional
- Timing
- Timing using Fast Timing Model

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name SIMULATION_MODE <value>
```

### Default Value

TIMING

## SIMULATION\_NETLIST\_VIEWER

Enables the Simulation Netlist Viewer.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIMULATION_NETLIST_VIEWER <value>
```

### Default Value

Off



## SIMULATION\_SIGNAL\_COMPARE\_TOLERANCE

Specifies the comparison timing tolerance to be used for each signal in a waveform comparison.

### Type

Time

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_instance_assignment -name SIMULATION_SIGNAL_COMPARE_TOLERANCE -to <to> -  
entity <entity name> <value>
```

## SIMULATION\_VDB\_RESULT\_FLUSH

Flushes signal transitions from memory to disk for memory optimization

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

None

### Syntax

```
set_global_assignment -name SIMULATION_VDB_RESULT_FLUSH <value>
```

### Default Value

On



## SIMULATION\_VECTOR\_COMPARE\_BEGIN\_TIME

Specifies the begin time at which waveform comparison on simulation results should start.

### Type

Time

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIMULATION_VECTOR_COMPARE_BEGIN_TIME <value>
```

## SIMULATION\_VECTOR\_COMPARE\_END\_TIME

Specifies the end time at which waveform comparison on simulation results should stop.

### Type

Time

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIMULATION_VECTOR_COMPARE_END_TIME <value>
```

## SIMULATION\_VECTOR\_COMPARE\_RULE\_FOR\_0

Specifies vector values that match with expected strong low value (0) in the waveform file

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIMULATION_VECTOR_COMPARE_RULE_FOR_0 <value>
```

## SIMULATION\_VECTOR\_COMPARE\_RULE\_FOR\_1

Specifies vector values that match with expected strong high value (1) in the waveform file

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIMULATION_VECTOR_COMPARE_RULE_FOR_1 <value>
```





## SIMULATION\_VECTOR\_COMPARE\_RULE\_FOR\_DC

Specifies vector values that match with expected don't care value (DC) in the waveform file

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIMULATION_VECTOR_COMPARE_RULE_FOR_DC <value>
```

## SIMULATION\_VECTOR\_COMPARE\_RULE\_FOR\_H

Specifies vector values that match with expected weak high value (H) in the waveform file

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIMULATION_VECTOR_COMPARE_RULE_FOR_H <value>
```

## SIMULATION\_VECTOR\_COMPARE\_RULE\_FOR\_L

Specifies vector values that match with expected weak low value (L) in the waveform file

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIMULATION_VECTOR_COMPARE_RULE_FOR_L <value>
```

## SIMULATION\_VECTOR\_COMPARE\_RULE\_FOR\_U

Specifies vector values that match with expected uninitialized value (U) in the waveform file

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIMULATION_VECTOR_COMPARE_RULE_FOR_U <value>
```

## SIMULATION\_VECTOR\_COMPARE\_RULE\_FOR\_W

Specifies vector values that match with expected weak unknown value (W) in the waveform file

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIMULATION_VECTOR_COMPARE_RULE_FOR_W <value>
```

## SIMULATION\_VECTOR\_COMPARE\_RULE\_FOR\_X

Specifies vector values that match with expected unknown value (X) in the waveform file

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIMULATION_VECTOR_COMPARE_RULE_FOR_X <value>
```



## SIMULATION\_VECTOR\_COMPARE\_RULE\_FOR\_Z

Specifies vector values that match with expected high impedance value (Z) in the waveform file

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIMULATION_VECTOR_COMPARE_RULE_FOR_Z <value>
```

## SIMULATION\_WITH\_AUTO\_GLITCH\_FILTERING

Specifies whether or not glitch filtering should be performed during Timing Simulation.

### Type

Enumeration

### Values

- Always
- Auto
- Never

### Device Support

- Arria GX
- Arria II GZ
- Cyclone
- Cyclone II
- Cyclone III
- Cyclone III LS
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name SIMULATION_WITH_AUTO_GLITCH_FILTERING <value>
```

### Default Value

AUTO



## SIMULATION\_WITH\_GLITCH\_FILTERING\_IN\_NORMAL\_FLOW

Specifies whether or not glitch filtering should be used when Generate Signal Activity File and Generate VCD File for PowerPlay Power Analyzer are turned off.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GZ
- Cyclone
- Cyclone II
- Cyclone III
- Cyclone III LS
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name SIMULATION_WITH_GLITCH_FILTERING_IN_NORMAL_FLOW  
<value>
```

## SIMULATION\_WITH\_GLITCH\_FILTERING\_WHEN\_GENERATING\_SAF

Specifies whether or not glitch filtering should be used when generating the Signal Activity File or VCD File for PowerPlay Power Analyzer.

### Old Name

SIMULATION\_WITH\_GLITCH\_FILTERING

### Type

Boolean

### Device Support

- Arria GX
- Arria II GZ
- Cyclone
- Cyclone II
- Cyclone III
- Cyclone III LS
- HardCopy II
- MAX II
- MAX V
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name  
SIMULATION_WITH_GLITCH_FILTERING_WHEN_GENERATING_SAF <value>
```

### Default Value

On



## SIMULATOR\_GENERATE\_POWERPLAY\_VCD\_FILE

Specifies whether or not a VCD File for PowerPlay Power Analyzer should be written out.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GZ
- Cyclone
- Cyclone II
- Cyclone III
- Cyclone III LS
- HardCopy II
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name SIMULATOR_GENERATE_POWERPLAY_VCD_FILE <value>
```

### Default Value

Off

## SIMULATOR\_GENERATE\_SIGNAL\_ACTIVITY\_FILE

Specifies whether or not a Signal Activity File should be written out.

### Type

Boolean

### Device Support

- Arria GX
- Arria II GZ
- Cyclone
- Cyclone II
- Cyclone III
- Cyclone III LS
- HardCopy II
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name SIMULATOR_GENERATE_SIGNAL_ACTIVITY_FILE <value>
```

### Default Value

Off



## SIMULATOR\_POWERPLAY\_VCD\_FILE\_END\_TIME

Specifies the end time for the PowerPlay Power Analyzer VCD file.

### Type

Time

### Device Support

- Arria GX
- Arria II GZ
- Cyclone
- Cyclone II
- Cyclone III
- Cyclone III LS
- HardCopy II
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name SIMULATOR_POWERPLAY_VCD_FILE_END_TIME <value>
```

## SIMULATOR\_POWERPLAY\_VCD\_FILE\_OUTPUT\_DESTINATION

Specifies the name the VCD File for PowerPlay Power Analyzer should be written to.

### Type

File name

### Device Support

- Arria GX
- Arria II GZ
- Cyclone
- Cyclone II
- Cyclone III
- Cyclone III LS
- HardCopy II
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SIMULATOR_POWERPLAY_VCD_FILE_OUTPUT_DESTINATION  
<value>
```



## SIMULATOR\_POWERPLAY\_VCD\_FILE\_START\_TIME

Specifies the start time for the PowerPlay Power Analyzer VCD file.

### Type

Time

### Device Support

- Arria GX
- Arria II GZ
- Cyclone
- Cyclone II
- Cyclone III
- Cyclone III LS
- HardCopy II
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name SIMULATOR_POWERPLAY_VCD_FILE_START_TIME <value>
```

## SIMULATOR\_PVT\_TIMING\_MODEL\_TYPE

Specifies the type of PVT Timing Model to use for the current Simulation focus.

### Type

Enumeration

### Values

- Auto
- Model\_1
- Model\_2
- Model\_3

### Device Support

- Arria II GZ
- Cyclone III
- Cyclone III LS
- Stratix III
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name SIMULATOR_PVT_TIMING_MODEL_TYPE <value>
```

### Default Value

AUTO



## SIMULATOR\_SIGNAL\_ACTIVITY\_FILE\_END\_TIME

Specifies the time at which toggle rates and static probabilities should stop being calculated.

### Type

Time

### Device Support

- Arria GX
- Arria II GZ
- Cyclone
- Cyclone II
- Cyclone III
- Cyclone III LS
- HardCopy II
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name SIMULATOR_SIGNAL_ACTIVITY_FILE_END_TIME <value>
```

## SIMULATOR\_SIGNAL\_ACTIVITY\_FILE\_OUTPUT\_DESTINATION

Specifies the name the Signal Activity File should be written to.

### Type

File name

### Device Support

- Arria GX
- Arria II GZ
- Cyclone
- Cyclone II
- Cyclone III
- Cyclone III LS
- HardCopy II
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name SIMULATOR_SIGNAL_ACTIVITY_FILE_OUTPUT_DESTINATION <value>
```

## SIMULATOR\_SIGNAL\_ACTIVITY\_FILE\_START\_TIME

Specifies the time at which toggle rates and static probabilities should start to be calculated.

### Type

Time

### Device Support

- Arria GX
- Arria II GZ
- Cyclone
- Cyclone II
- Cyclone III
- Cyclone III LS
- HardCopy II
- MAX II
- MAX V
- MAX3000A
- MAX7000AE
- MAX7000B
- Stratix
- Stratix GX
- Stratix II
- Stratix II GX
- Stratix III
- Stratix IV

### Notes

None

### Syntax

```
set_global_assignment -name SIMULATOR_SIGNAL_ACTIVITY_FILE_START_TIME  
<value>
```

## SIM\_BEHAVIOR\_SIMULATION

Perform QUASAR Behavior simulation to simulate a verilog design

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIM_BEHAVIOR_SIMULATION <value>
```



## SIM\_COMPILE\_HDL\_FILES

Collect a list of HDL files for compilation in QUASAR

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIM_COMPILE_HDL_FILES <value>
```

## SIM\_HDL\_TOP\_MODULE\_NAME

Top level module name provided from user to determine starting point of simulation

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIM_HDL_TOP_MODULE_NAME <value>
```

## SIM\_OVERWRITE\_WAVEFORM\_INPUTS

Overwrite simulation input file with simulation results.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIM_OVERWRITE_WAVEFORM_INPUTS <value>
```

## SIM\_TAP\_REGISTER\_D\_Q\_PORTS

Adds the D and Q ports of a register node to the list of signals for which output waveforms are shown in the simulation report. This option makes the D and Q ports of a register node observable during Functional Simulation.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_instance_assignment -name SIM_TAP_REGISTER_D_Q_PORTS -to <to> -entity  
<entity name> <value>
```



## SIM\_VECTOR\_COMPARED\_CLOCK\_DUTY\_CYCLE

Specifies the duty cycle of compared clock used to trigger waveform comparison.

### Type

Integer

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIM_VECTOR_COMPARED_CLOCK_DUTY_CYCLE -  
section_id <section identifier> <value>
```

### Default Value

50, requires section identifier

## SIM\_VECTOR\_COMPARED\_CLOCK\_OFFSET

Specifies the offset of compared clock used to trigger waveform comparison.

### Type

Time

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIM_VECTOR_COMPARED_CLOCK_OFFSET -section_id  
<section identifier> <value>
```

### Default Value

0ns, requires section identifier

## SIM\_VECTOR\_COMPARED\_CLOCK\_PERIOD

Specifies the period of compared clock used to trigger waveform comparison.

### Type

Time

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name SIM_VECTOR_COMPARED_CLOCK_PERIOD -section_id  
<section identifier> <value>
```

## START\_TIME

Specifies the start time for simulation.

### Type

Time

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name START_TIME <value>
```

### Default Value

0ns



## TRIGGER\_EQUATION

Specifies the breakpoint's trigger equation.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name TRIGGER_EQUATION -section_id <section  
identifier> <value>
```

## TRIGGER\_VECTOR\_COMPARE\_ON\_SIGNAL

Trigger vector comparison with the specified signal.

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_instance_assignment -name TRIGGER_VECTOR_COMPARE_ON_SIGNAL -to <to> -  
entity <entity name> <value>
```

## USER\_MESSAGE

Specifies the breakpoint's message when triggered.

### Type

String

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
<value> set_global_assignment -name USER_MESSAGE -section_id <section identifier>
```

## VECTOR\_COMPARE\_TRIGGER\_MODE

Specifies the comparison mode to trigger vector comparison.

### Type

Enumeration

### Values

- ALL\_EDGE
- INPUT\_EDGE
- SELECTED\_EDGE

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name VECTOR_COMPARE_TRIGGER_MODE <value>
```

### Default Value

INPUT\_EDGE





## VECTOR\_INPUT\_SOURCE

Specifies the source of input vectors to be used for simulation.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name VECTOR_INPUT_SOURCE <value>
```

## VECTOR\_OUTPUT\_DESTINATION

Specifies the output vector file for the current simulation.

### Type

File name

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name VECTOR_OUTPUT_DESTINATION <value>
```



## VECTOR\_OUTPUT\_FORMAT

Specifies the format of simulation results.

### Type

Enumeration

### Values

- CVWF
- VCD
- VWF

### Device Support

This setting can be used in projects targeting any Altera device family.

### Syntax

```
set_global_assignment -name VECTOR_OUTPUT_FORMAT <value>
```

## X\_ON\_VIOLATION\_OPTION

Gives user the option to see 'X' or valid data at the output of registers in the event of a timing violation during simulation..

### Type

Boolean

### Device Support

This setting can be used in projects targeting any Altera device family.

### Notes

This assignment supports wildcards.

### Syntax

```
set_instance_assignment -name X_ON_VIOLATION_OPTION -to <to> -entity  
<entity name> <value>
```