Contents

   1.1. Advanced I/O Timing Assignments ................................................................. 25
       1.1.1. BOARD_MODEL_EBD_FAR_END................................................................. 25
       1.1.2. BOARD_MODEL_EBD_FILE_NAME............................................................. 26
       1.1.3. BOARD_MODEL_EBD_SIGNAL_NAME......................................................... 27
       1.1.4. BOARD_MODEL_FAR_C............................................................................. 28
       1.1.5. BOARD_MODEL_FAR_DIFFERENTIAL_R....................................................... 29
       1.1.6. BOARD_MODEL_FAR_PULLDOWN_R........................................................... 30
       1.1.7. BOARD_MODEL_FAR_PULLUP_R................................................................. 31
       1.1.8. BOARD_MODEL_FAR_SERIES_R................................................................. 32
       1.1.9. BOARD_MODEL_NEAR_C.......................................................................... 33
       1.1.10. BOARD_MODEL_NEAR_DIFFERENTIAL_R.................................................... 34
       1.1.11. BOARD_MODEL_NEAR_PULLDOWN_R........................................................ 35
       1.1.12. BOARD_MODEL_NEAR_PULLUP_R............................................................. 36
       1.1.13. BOARD_MODEL_NEAR_SERIES_R............................................................. 37
       1.1.14. BOARD_MODEL_NEAR_TLINE_C_PER_LENGTH.......................................... 38
       1.1.15. BOARD_MODEL_NEAR_TLINE_LENGTH..................................................... 39
       1.1.16. BOARD_MODEL_NEAR_TLINE_L_PER_LENGTH.......................................... 40
       1.1.17. BOARD_MODEL_TERMINATION_V............................................................ 41
       1.1.18. BOARD_MODEL_TLINE_C_PER_LENGTH................................................. 42
       1.1.19. BOARD_MODEL_TLINE_LENGTH............................................................. 43
       1.1.20. BOARD_MODEL_TLINE_L_PER_LENGTH................................................... 44
       1.1.21. OUTPUT_IO_TIMING_ENDPOINT............................................................ 45
       1.1.22. OUTPUT_IO_TIMING_FAR_END_VMEAS.................................................. 46
       1.1.23. OUTPUT_IO_TIMING_NEAR_END_VMEAS.............................................. 47
   1.2. Analysis & Synthesis Assignments ........................................................................ 48
       1.2.1. ADV_NETLIST_OPT_ALLOWED................................................................ 48
       1.2.2. ADV_NETLIST_OPT_SYNTH_WYSIWYG_REMAP............................................ 49
       1.2.3. AGGRESSIVE_MUX_AREA_OPTIMIZATION............................................... 50
       1.2.4. ALLOW_ANY_RAM_SIZE_FOR_RECOGNITION............................................. 51
       1.2.5. ALLOW_ANY_ROM_SIZE_FOR_RECOGNITION............................................. 52
       1.2.6. ALLOW_ANY_SHIFT_REGISTER_SIZE_FOR_RECOGNITION............................ 53
       1.2.7. ALLOW_CHILD_PARTITIONS.................................................................... 54
       1.2.8. ALLOW_POWER_UP_DONT_CARE.............................................................. 55
       1.2.9. ALLOW_SHIFT_REGISTER_MERGING_ACROSS_HIERARCHIES........................ 56
       1.2.10. ALLOW_SYNCH_CTRL_USAGE................................................................. 57
       1.2.11. ALTERA_A10_IOPLL_BOOTSTRAP.......................................................... 58
       1.2.12. AUTO_CLOCK_ENABLE_RECOGNITION.................................................... 59
       1.2.13. AUTO_DSP_RECOGNITION.................................................................... 60
       1.2.14. AUTO_ENABLE_SMART_COMPILE........................................................... 61
       1.2.15. AUTO_OPEN_DRAIN_PINS..................................................................... 62
       1.2.16. AUTO_PARALLEL_SYNTHESIS................................................................ 63
       1.2.17. AUTO_RAM_RECOGNITION.................................................................... 64
       1.2.18. AUTO_RESOURCE_SHARING.................................................................... 65
       1.2.19. AUTO_ROM_RECOGNITION..................................................................... 66
       1.2.20. AUTO_SHIFT_REGISTER_RECOGNITION................................................... 67
       1.2.21. BARRELSHIFTER_CARRY_CHAIN_PACKING............................................. 68
<table>
<thead>
<tr>
<th>Section</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.2.22. BLOCK_DESIGN_NAMING</td>
<td>69</td>
</tr>
<tr>
<td>1.2.23. BOARD</td>
<td>70</td>
</tr>
<tr>
<td>1.2.24. DEVICE_FILTER_PACKAGE</td>
<td>71</td>
</tr>
<tr>
<td>1.2.25. DEVICE_FILTER_PIN_COUNT</td>
<td>72</td>
</tr>
<tr>
<td>1.2.26. DEVICE_FILTER_SPEED_GRADE</td>
<td>73</td>
</tr>
<tr>
<td>1.2.27. DEVICE_FILTER_VOLTAGE</td>
<td>74</td>
</tr>
<tr>
<td>1.2.28. DISABLE_DSP_NEGATE_INFERENCING</td>
<td>75</td>
</tr>
<tr>
<td>1.2.29. DISABLE_REGISTER_MERGING_ACROSS_HIERARCHIES</td>
<td>76</td>
</tr>
<tr>
<td>1.2.30. DISABLE_REGISTER_POWER_UP_INITIALIZATION</td>
<td>77</td>
</tr>
<tr>
<td>1.2.31. DONT_MERGE_REGISTER</td>
<td>78</td>
</tr>
<tr>
<td>1.2.32. DSE_SYNTH_EXTRA_EFFORT_MODE</td>
<td>79</td>
</tr>
<tr>
<td>1.2.33. DSP_BLOCK_BALANCING</td>
<td>80</td>
</tr>
<tr>
<td>1.2.34. DUPLICATE_HIERARCHY_DEPTH</td>
<td>81</td>
</tr>
<tr>
<td>1.2.35. EDA_DESIGN_ENTRY_SYNTHESIS_TOOL</td>
<td>82</td>
</tr>
<tr>
<td>1.2.36. EDA_INPUT_DATA_FORMAT</td>
<td>83</td>
</tr>
<tr>
<td>1.2.37. EDA_INPUT_GND_NAME</td>
<td>84</td>
</tr>
<tr>
<td>1.2.38. EDA_INPUT_VCC_NAME</td>
<td>85</td>
</tr>
<tr>
<td>1.2.39. EDA_LMF_FILE</td>
<td>86</td>
</tr>
<tr>
<td>1.2.40. EDA_RUN_TOOL_AUTOMATICALLY</td>
<td>87</td>
</tr>
<tr>
<td>1.2.41. EDA_SHOW_LMF_MAPPING_MESSAGES</td>
<td>88</td>
</tr>
<tr>
<td>1.2.42. EDA_VHDL_LIBRARY</td>
<td>89</td>
</tr>
<tr>
<td>1.2.43. ENABLE_FORMAL_VERIFICATION</td>
<td>90</td>
</tr>
<tr>
<td>1.2.44. ENABLE_FPGA_TAMPER_DETECTION</td>
<td>91</td>
</tr>
<tr>
<td>1.2.45. ENABLE_STATE_MACHINE_INERENCE</td>
<td>92</td>
</tr>
<tr>
<td>1.2.46. ENABLE_SV_STATIC_ASSERTIONS</td>
<td>93</td>
</tr>
<tr>
<td>1.2.47. ENABLE_VHDL_STATIC_ASSERTIONS</td>
<td>94</td>
</tr>
<tr>
<td>1.2.48. FAMILY</td>
<td>95</td>
</tr>
<tr>
<td>1.2.49. FORCE_CLOCK_ENABLE_INFERENCE</td>
<td>96</td>
</tr>
<tr>
<td>1.2.50. FORCE_SYNCH_CLEAR</td>
<td>97</td>
</tr>
<tr>
<td>1.2.51. FRACTAL_SYNTHESIS</td>
<td>98</td>
</tr>
<tr>
<td>1.2.52. HDL_INITIAL_FANOUT_LIMIT</td>
<td>99</td>
</tr>
<tr>
<td>1.2.53. HDL_MESSAGE_LEVEL</td>
<td>100</td>
</tr>
<tr>
<td>1.2.54. HDL_MESSAGE_OFF</td>
<td>101</td>
</tr>
<tr>
<td>1.2.55. HDL_MESSAGE_ON</td>
<td>102</td>
</tr>
<tr>
<td>1.2.56. HPS_PARTITION</td>
<td>103</td>
</tr>
<tr>
<td>1.2.57. IGNORE_GLOBAL_BUFFERS</td>
<td>104</td>
</tr>
<tr>
<td>1.2.58. IGNORE_LCELL_BUFFERS</td>
<td>105</td>
</tr>
<tr>
<td>1.2.59. IGNORE_MAX_FANOUT_ASSIGNMENTS</td>
<td>106</td>
</tr>
<tr>
<td>1.2.60. IGNORE_REGISTER_POWER_UP_INITIALIZATION</td>
<td>107</td>
</tr>
<tr>
<td>1.2.61. IGNORE_SOFT_BUFFERS</td>
<td>108</td>
</tr>
<tr>
<td>1.2.62. IGNORE_TRANSLATE_OFF_AND_SYNTHESIS_OFF</td>
<td>109</td>
</tr>
<tr>
<td>1.2.63. IMPLEMENT_AS_CLOCK_ENABLE</td>
<td>110</td>
</tr>
<tr>
<td>1.2.64. IMPLEMENT_AS_OUTPUT_OF_LOGIC_CELL</td>
<td>111</td>
</tr>
<tr>
<td>1.2.65. INFER_RAMS_FROM_RAW_LOGIC</td>
<td>112</td>
</tr>
<tr>
<td>1.2.66. IP_SEARCH_PATHS</td>
<td>113</td>
</tr>
<tr>
<td>1.2.67. MAX_BALANCING_DSP_BLOCKS</td>
<td>114</td>
</tr>
<tr>
<td>1.2.68. MAX_FANOUT</td>
<td>115</td>
</tr>
<tr>
<td>1.2.69. MAX_FANOUT_FOR_SYNCH_CTRL</td>
<td>116</td>
</tr>
<tr>
<td>1.2.70. MAX_LABS</td>
<td>117</td>
</tr>
<tr>
<td>1.2.71. MAX_NUMBER_OF_REGISTERS_FROM_UNINFERRLED_RAMS</td>
<td>118</td>
</tr>
<tr>
<td>1.2.72. MAX_RAM_BLOCKS_M4K</td>
<td>119</td>
</tr>
</tbody>
</table>
Contents

1.2.123. SYNTH_GATED_CLOCK_CONVERSION_BASE_CLOCK............................... 170
1.2.124. SYNTH_MESSAGE_LEVEL.................................................................... 171
1.2.125. SYNTH_PROTECT_SDC_CONSTRAINT.................................................... 172
1.2.126. SYNTH_RESOURCE_AWARE_INFERENC_FOR_BLOCK_RAM......................173
1.2.127. SYNTH_TIMING_DRIVEN_SYNTHESIS.................................................... 174
1.2.128. TOP_LEVEL_ENTITY............................................................................ 175
1.2.129. UNCONNECTED_OUTPUT_PORT_MESSAGE_LEVEL...................................176
1.2.130. USER_LIBRARIES............................................................................... 177
1.2.131. USE_GENERATED_PHYSICAL_CONSTRAINTS..........................................178
1.2.132. VERILOG_CONSTANT_LOOP_LIMIT....................................................... 179
1.2.133. VERILOG_INPUT_VERSION.................................................................. 180
1.2.134. VERILOG_LMF_FILE............................................................................ 181
1.2.135. VERILOG_MACRO............................................................................... 182
1.2.136. VERILOG_NON_CONSTANT_LOOP_LIMIT............................................... 183
1.2.137. VERILOG_SHOW_LMF_MAPPING_MESSAGES..........................................184
1.2.138. VHDL_INPUT_LIBRARY........................................................................ 185
1.2.139. VHDL_INPUT_VERSION....................................................................... 186
1.2.140. VHDL_LMF_FILE................................................................................. 187
1.2.141. VHDL_SHOW_LMF_MAPPING_MESSAGES...............................................188
1.3.  Assembler Assignments .................................................................................... 189
1.3.1. ANTI_TAMPER_RESPONSE.......................................................................189
1.3.2. ATTESTATION_ALT_NAME_MANUFACTURER............................................... 190
1.3.3. ATTESTATION_ALT_NAME_PRODUCT.........................................................191
1.3.4. ATTESTATION_CRL_DISTRIBUTION_POINT.............................................192
1.3.5. ATTESTATION_MODEL_INFO....................................................................193
1.3.6. ATTESTATION_RIM_URI_PREFIX...............................................................194
1.3.7. ATTESTATION_RIM_URI_SUFFIX..............................................................195
1.3.8. ATTESTATION_VENDOR_INFO..................................................................196
1.3.9. AUTO_RESTART_CONFIGURATION............................................................197
1.3.10. CLOCK_SOURCE..................................................................................198
1.3.11. COMPRESSION_MODE...........................................................................199
1.3.12. CONFIGURATION_CLOCK_DIVISOR.......................................................200
1.3.13. CONFIGURATION_CLOCK_FREQUENCY...................................................201
1.3.14. ENABLE_ADV_SEU_DETECTION..............................................................202
1.3.15. ENABLE_AUTONOMOUS_PCIE_HIP..........................................................203
1.3.16. ENABLE_FPGA_TAMPER_DEVICE_SELF_KILL..........................................204
1.3.17. ENABLE_FREQUENCY_TAMPER_DETECTION.............................................205
1.3.18. ENABLE_FREQUENCY_TAMPER_DEVICE_SELF_KILL...................................206
1.3.19. ENABLE_MULTI_AUTHORITY..................................................................207
1.3.20. ENABLE_OCT_DONE.............................................................................208
1.3.21. ENABLE_PARTIAL_RECONFIGURATION_BITSTREAM_ENCRYPTION...............209
1.3.22. ENABLE_PR_POF_ID.............................................................................210
1.3.23. ENABLE_S10_ATTESTATION_COMMANDS.................................................211
1.3.24. ENABLE_TEMPERATURE_TAMPER_DETECTION........................................212
1.3.25. ENABLE_TEMPERATURE_TAMPER_DEVICE_SELF_KILL..............................213
1.3.26. ENABLE_VCCL_SDM_VOLTAGE_TAMPER_DETECTION................................ 214
1.3.27. ENABLE_VCCL_VOLTAGE_TAMPER_DETECTION.........................................215
1.3.28. ENABLE_VOLTAGE_TAMPER_DETECTION.................................................216
1.3.29. ENABLE_VOLTAGE_TAMPER_DEVICE_SELF_KILL.......................................217
1.3.30. ENCRYPT_PROGRAMMING_BITSTREAM...................................................218
1.3.31. EPROM_USE_CHECKSUM_AS_USERCODE................................................219
1.3.83. RSU_MAX_RETRY_COUNT ................................................................. 271
1.3.84. RUN_CONFIG_CPU_FROM_INT_OSC .................................................. 272
1.3.85. SECU_OPTION_DISABLE_ENCRYPTION_KEY_IN_BBRAM .......................... 273
1.3.86. SECU_OPTION_DISABLE_ENCRYPTION_KEY_IN_EFUSES .............................. 274
1.3.87. SECU_OPTION_DISABLE_HPS_DEBUG ............................................. 275
1.3.88. SECU_OPTION_DISABLE_JTAG ...................................................... 276
1.3.89. SECU_OPTION_DISABLE_PUF_WRAPPED_ENCRYPTION_KEY ...................... 277
1.3.90. SECU_OPTION_DISABLE_VIRTUAL_EFUSES ........................................ 278
1.3.91. SECU_OPTION_FORCE_ENCRYPTION_KEY_UPDATE ................................ 279
1.3.92. SECU_OPTION_FORCE_SDM_CLOCK_TO_INT_OSC .................................. 280
1.3.93. SECU_OPTION_LOCK_SECURITY_EFUSES .......................................... 281
1.3.94. STRATIXII_CONFIGURATION_DEVICE ............................................. 282
1.3.95. STRATIX_JTAG_USER_CODE ..................................................... 283
1.3.96. TEMPERATURE_TAMPER_LOWER_BOUND ....................................... 284
1.3.97. TEMPERATURE_TAMPER_UPPER_BOUND .......................................... 285
1.3.98. UNINITIALIZED_RAM_CONTENT_PATTERN ....................................... 286
1.3.99. USE_ALIAS_L1 ............................................................................ 287
1.3.100. USE_CHECKSUM_AS_USERCODE ................................................... 288
1.3.101. USE_CONFIGURATION_DEVICE .................................................... 289
1.3.102. VCCL_SDM_VOLTAGE_DIFFERENCE_TRIGGER .................................... 290
1.3.103. VCCL_VOLTAGE_DIFFERENCE_TRIGGER ........................................ 291
1.3.104. VOLTAGE_TAMPER_DETECTION_TRIGGER ...................................... 292

1.4. Classic Timing Assignments .................................................................................. 293
1.4.1. ANALYZE_LATCHES_AS_SYNCHRONOUS_ELEMENTS .................................. 293
1.4.2. CUT_OFF_IO_PIN_FEEDBACK .......................................................... 294
1.4.3. CUT_OFF_PATHS_BETWEEN_CLOCK_DOMAINS ..................................... 295
1.4.4. CUT_OFF_READ_DURING_WRITE_PATHS ............................................. 296
1.4.5. DEFAULT_HOLD_MULTICYCLE .......................................................... 297
1.4.6. EMIF_SOC_PHYCLK_ADVANCE_MODELING ........................................ 298
1.4.7. ENABLE_HPS_INTERNAL_TIMING ...................................................... 299
1.4.8. FLOW_ENABLE_TIMING_ANALYZER_AFTER_PLAN_STAGE ......................... 300
1.4.9. IMPLEMENTS_FREE_RUNNING_CLOCK .............................................. 301
1.4.10. INPUT_TRANSITION_TIME ............................................................ 302
1.4.11. MAX_CORE_JUNCTION_TEMP ....................................................... 303
1.4.12. MIN_CORE_JUNCTION_TEMP .......................................................... 304
1.4.13. MIN_MTBF_REQUIREMENT .............................................................. 305
1.4.14. NOMINAL_CORE_SUPPLY_VOLTAGE ............................................... 306
1.4.15. PACKAGE_SKEW_COMPENSATION ................................................... 307
1.4.16. PLL_EXTERNAL_FEEDBACK_BOARD_DELAY ...................................... 308
1.4.17. SDC_STATEMENT ........................................................................... 309
1.4.18. STA_AUTO_REPORT_SETUP_SUMMARY .................................................. 310
1.4.19. STA_AUTO_UPDATE_TIMING_NETLIST .............................................. 311
1.4.20. TDC_AGGRESSIVE_HOLD_CLOSURE_EFFORT .................................... 312
1.4.21. TIMING_ANALYZER_DO_CCPP_REMOVAL .......................................... 313
1.4.22. TIMING_ANALYZER_DO_REPORT_CDC_VIEWER .................................. 314
1.4.23. TIMING_ANALYZER_DO_REPORT_TIMING ........................................ 315
1.4.24. TIMING_ANALYZER_MULTICORNER_ANALYSIS .................................. 316
1.4.25. TIMING_ANALYZER_REPORT_NUM_WORST_CASE_TIMING_PATHS .......... 317
1.4.26. TIMING_ANALYZER_REPORT_SCRIPT ............................................... 318
1.4.27. TIMING_ANALYZER_REPORT_SCRIPT_INCLUDE_DEFAULT_ANALYSIS ........ 319
1.4.28. TIMING_ANALYZER_REPORT_WORST_CASE_TIMING_PATHS .................. 320
1.4.29. TIMING_ANALYZER_SIMULTANEOUS_MULTICORNER_ANALYSIS..................321
1.4.30. TIMING_ANALYZER_REPORT_WORST_CASE_TIMING_PATHS_SHOW_ROUT             ..... 322
1.4.31. USE_DLL_FREQUENCY_FOR_DQS_DELAY_CHAIN..................................... 323

1.5.  Compiler Assignments ........................................................................... 324
1.5.1. ALLOW_REGISTER_DUPLICATION.............................................................324
1.5.2. ALLOW_REGISTER_MERGING.................................................................. 325
1.5.3. ALLOW_REGISTER RETIMING..................................................................326
1.5.4. OPTIMIZATION_MODE........................................................................... 327

1.6.  Design Assistant Assignments ................................................................. 329
1.6.1. CLK_RULE_CLKNET_CLKSPINES_THRESHOLD............................................329
1.6.2. DA_CUSTOM_RULE_FILE.........................................................................330
1.6.3. DESIGN_ASSISTANT_EXCLUDE................................................................331
1.6.4. DESIGN_ASSISTANT_INCLUDE................................................................332
1.6.5. DRC_DEADLOCK_STATE_LIMIT..............................................................333
1.6.6. DRC_DETAIL_MESSAGE_LIMIT...............................................................334
1.6.7. DRC_FANOUT_EXCEEDING.......................................................................335
1.6.8. DRC_GATED_CLOCK_FEED.....................................................................336
1.6.9. DRC_REPORT_FANOUT_EXCEEDING.......................................................337
1.6.10. DRC_REPORT_TOP_FANOUT.................................................................338
1.6.11. DRC_TOP_FANOUT...............................................................................339
1.6.12. DRC_VIOLATION_MESSAGE_LIMIT.......................................................340
1.6.13. HARDCOPY_FLOW_AUTOMATION..........................................................341
1.6.14. HARDCOPY_NEW_PROJECT_PATH..........................................................342
1.6.15. HCPY_CAT...........................................................................................343
1.6.16. HCPY_PLL_MULTIPLE_CLK_NETWORK_TYPES...........................................344
1.6.17. HCPY_VREF_PINS...............................................................................345

1.7.  Design Partition Assignments .................................................................. 346
1.7.1. ABSORB_PATHS_FROM_OUTPUTS_TO_INPUTS...........................................346
1.7.2. AUTOMATIC_DANGLING_PORT_TIEOFF....................................................347
1.7.3. CROSS_BOUNDARY_OPTIMIZATIONS.......................................................348
1.7.4. EMPTY..................................................................................................349
1.7.5. ENABLE_LAB_SHARING_WITH_PARENT_PARTITION.................................350
1.7.6. ENTITY_REBINDING...............................................................................351
1.7.7. EXPORT_BLOCK_NAME_OBFUSCATION....................................................352
1.7.8. IGNORE_PARTITIONS..............................................................................353
1.7.9. INCREMENTAL_COMPILATION_EXPORT_FLATTEN....................................354
1.7.10. INCREMENTAL_COMPILATION_EXPORT_POST_FIT....................................355
1.7.11. INCREMENTAL_COMPILATION_EXPORT_POST_SYNTH.............................356
1.7.12. INSERT_BOUNDARY_WIRE_LUTS..........................................................357
1.7.13. MERGE_EQUIVALENT_BIDIRS..............................................................358
1.7.14. MERGE_EQUIVALENT_INPUTS...............................................................359
1.7.15. PARTIAL_RECONFIGURATION_PARTITION..............................................360
1.7.16. PARTITION...........................................................................................361
1.7.17. PARTITION_ALWAYS_USE_QXP_NETLIST..............................................362
1.7.18. PARTITION_ASD_REGION.....................................................................363
1.7.19. PARTITION_ASD_REGION_ID.................................................................364
1.7.20. PARTITION_IGNORE_SOURCE_FILE_CHANGES.......................................365
1.7.21. PARTITION_PRESERVE_HIGH_SPEED_TILES..........................................366
1.7.22. PRESERVE...........................................................................................367
1.7.23. PROPAGATE_CONSTANTS_ON_INPUTS................................................368
1.7.24. PROPAGATE_INVERSIONS_ON_INPUTS................................................... 369
1.7.25. QDB_FILE_PARTITION......................................................................... 370
1.7.26. QDB_PATH......................................................................................... 371
1.7.27. REMOVE_LOGIC_ON_UNCONNECTED_OUTPUTS.................................... 372
1.7.28. RESERVED_CORE............................................................................. 373
1.7.29. RTL_PARAMETER.............................................................................. 374
1.8.  EDA Netlist Writer Assignments ............................................................. 375
1.8.1. EDA_BOARD_BOUNDARY_SCAN_OPERATION....................................... 375
1.8.2. EDA_BOARD_DESIGN_BOUNDARY_SCAN_TOOL.................................... 376
1.8.3. EDA_BOARD_DESIGN_SIGNAL_INTEGRITY_TOOL.................................. 377
1.8.4. EDA_BOARD_DESIGN_SYMBOL_TOOL.................................................. 378
1.8.5. EDA_BOARD_DESIGN_TIMING_TOOL................................................... 379
1.8.6. EDA_BOARD_DESIGN_TOOL.................................................................. 380
1.8.7. EDA_DESIGN_EXTRA_ALTERA_SIM_LIB............................................. 381
1.8.8. EDA_ENABLE_GLITCH_FILTERING...................................................... 382
1.8.9. EDA_ENABLE_IPUTF_MODE.................................................................. 383
1.8.10. EDA_EXTRA_ELAB_OPTION.............................................................. 384
1.8.11. EDA_FLATTEN_BUSES....................................................................... 385
1.8.12. EDA_FORCE_GATE_LEVEL_REG_INIT_X............................................. 386
1.8.13. EDA_GENERATE_POWER_INPUT_FILE............................................... 387
1.8.14. EDA_GENERATE_SDF_FOR_POWER................................................... 388
1.8.15. EDA_GENERATE_TIMING_CLOSURE_DATA......................................... 389
1.8.16. EDA_IBIS_EXTENDED_MODEL_SELECTOR.......................................... 390
1.8.17. EDA_IBIS_MODEL_SELECTOR............................................................ 391
1.8.18. EDA_IBIS_MUTUAL_COUPLING....................................................... 392
1.8.19. EDA_IBIS_SPECIFICATION_VERSION............................................... 393
1.8.20. EDA_IBIS_EXTENDED_MODEL_SELECTOR......................................... 394
1.8.21. EDA_IBIS_MODEL_SELECTOR............................................................. 395
1.8.22. EDA_IBIS_MUTUAL_COUPLING........................................................ 396
1.8.23. EDA_IBIS_SPECIFICATION_VERSION............................................... 397
1.8.24. EDA_IPFS_FILE................................................................................. 398
1.8.25. EDA_LAUNCH_CMD_LINE_TOOL....................................................... 399
1.8.26. EDA_MAP_ILLEGAL_CHARACTERS.................................................... 400
1.8.27. EDA_NATIVE_LINK_GENERATE_SCRIPT_ONLY...................................... 401
1.8.28. EDA_NATIVE_LINK_PORTABLE_FILE_PATHS...................................... 402
1.8.29. EDA_NATIVE_LINK_SIMULATION_SETUP_SCRIPT.................................. 403
1.8.30. EDA_NATIVE_LINK_SIMULATION_TEST_BENCH.................................. 404
1.8.31. EDA_NETLIST_WRITER_OUTPUT_DIR............................................... 405
1.8.32. EDA_RESYNTHESIS_TOOL.................................................................. 406
1.8.33. EDA_RTL_SIMULATION_RUN_SCRIPT............................................... 407
1.8.34. EDA_RTL_SIM_MODE....................................................................... 408
1.8.35. EDA_RTL_TEST_BENCH_FILE_NAME............................................... 409
1.8.36. EDA_RTL_TEST_BENCH_NAME.......................................................... 410
1.8.37. EDA_RTL_TEST_BENCH_RUN FOR.................................................. 411
1.8.38. EDA_SDC_FILE_NAME....................................................................... 412
1.8.39. EDA_SIMULATION_RUN_SCRIPT...................................................... 413
1.8.40. EDA_SIMULATION_TOOL................................................................... 414
1.8.41. EDA_TEST_BENCH_DESIGN_INSTANCE_NAME.................................... 415
1.8.42. EDA_TEST_BENCH_ENABLE_STATUS............................................... 416
1.8.43. EDA_TEST_BENCH_ENTITY_MODULE_NAME....................................... 417
1.8.44. EDA_TEST_BENCH_EXTRA_ALTERA_SIM_LIB.................................... 418
1.8.45. EDA_TEST_BENCH_FILE........................................................................419
1.8.46. EDA_TEST_BENCH_FILE_NAME................................................................420
1.8.47. EDA_TEST_BENCH_GATE_LEVEL_NETLIST_LIBRARY........................................421
1.8.48. EDA_TEST_BENCH_MODULE_NAME........................................................422
1.8.49. EDA_TEST_BENCH_NAME......................................................................423
1.8.50. EDA_TEST_BENCH_RUN_FOR................................................................424
1.8.51. EDA_TEST_BENCH_RUN_SIM_FOR.........................................................425
1.8.52. EDA_TIME_SCALE................................................................................426
1.8.53. EDA_TIMING_ANALYSIS_TOOL..............................................................427
1.8.54. EDA_TRUNCATE_LONG_HIERARCHY_PATHS................................................428
1.8.55. EDA_USER_COMPILED_SIMULATION_LIBRARY_DIRECTORY..........................429
1.8.56. EDA_VHDL_ARCH_NAME.......................................................................430
1.8.57. EDA_WAIT_FOR_GUI_TOOL_COMPLETION................................................431
1.8.58. EDA_WRITER_DONT_WRITE_TOP_ENTITY................................................432
1.8.59. EDA_WRITEDEVICE_CONTROL_PORTS..................................................433
1.8.60. EDA_WRITE_NODES_FOR_POWER_ESTIMATION.............................................434
1.9. Equivalence Checker Assignments ................................................................435
1.9.1. EQC_AUTO_BREAK_CONE.......................................................................435
1.9.2. EQC_AUTO_COMP_LOOP_CUT..................................................................436
1.9.3. EQC_AUTO_INVERSION..........................................................................437
1.9.4. EQC_AUTO_PORTSWAP...........................................................................438
1.9.5. EQC_AUTO_TERMINATE..........................................................................439
1.9.6. EQC_BBOX_MERGE................................................................................440
1.9.7. EQC_CONSTANT_DFF_DETECTION...........................................................441
1.9.8. EQC_DETECT_DONT_CARES....................................................................442
1.9.9. EQC_DFF_SS_EMULATION.......................................................................443
1.9.10. EQC_DUPLICATE_DFF_DETECTION.........................................................444
1.9.11. EQC_LVDS_MERGE...............................................................................445
1.9.12. EQC_MAC_REGISTER_UNPACK...............................................................446
1.9.13. EQC_PARAMETER_CHECK......................................................................447
1.9.14. EQC_POWER_UP_COMPARE...................................................................448
1.9.15. EQC_RAM_REGISTER_UNPACK...............................................................449
1.9.16. EQC_RAM_UNMERGING........................................................................450
1.9.17. EQC_RENAMING_RULES......................................................................451
1.9.18. EQC_RENAMING_RULES_LIST...............................................................452
1.9.19. EQC_SET_PARTITION_BB_TO_VCC_GND................................................453
1.9.20. EQC_SHOW_ALL_MAPPED_POINTS.........................................................454
1.9.21. EQC_STRUCTURE_MATCHING................................................................455
1.9.22. EQC_SUB_CONE_REPORT......................................................................456
1.10. Fitter Assignments ..................................................................................457
1.10.1. ACTIVE_SERIAL_CLOCK........................................................................457
1.10.2. ALLOW_ROUTING_TO_PERIPHERY_THROUGH_GLOBAL_NETWORK...............459
1.10.3. ALLOW_SEU_FAULT_INJECTION.............................................................460
1.10.4. ALLOW_VCCR_VCCT_PER_BANK...........................................................461
1.10.5. ALM_REGISTER_PACKING_EFFORT.........................................................462
1.10.6. ANTI_TAMPER_RESPONSE_FAILED..........................................................463
1.10.7. AUTO_ANALYZE_METASTABILITY............................................................464
1.10.8. AUTO_DELAY_CHAINS...........................................................................465
1.10.9. AUTO_DELAY_CHAINS_FOR_HIGH_FANOUT_INPUT_PINS..........................466
1.10.10. AUTO_GLOBAL_CLOCK......................................................................467
1.10.11. AUTO_GLOBAL_REGISTER_CONTROLS..................................................468
1.10.12. AUTO_RESERVE_CLKUSR_FOR_CALIBRATION ........................................ 469
1.10.13. BASE_PIN_OUT_FILE_ON_SAMEFRAME_DEVICE .................................. 470
1.10.14. BLOCK_RAM_AND_MLAB_EQUIVALENT_PAUSED_READ_CAPABILITIES ...... 471
1.10.15. BLOCK_RAM_AND_MLAB_EQUIVALENT_POWER_UP_CONDITIONS .......... 472
1.10.16. BLOCK_RAM_TO_MLAB_CELL_CONVERSION ..................................... 473
1.10.17. CDR_BANDWIDTH_PRESET ................................................................ 474
1.10.18. CKN_CK_PAIR .................................................................................. 475
1.10.19. CLOCK_REGION ............................................................................... 476
1.10.20. CLOCK_SPINE .................................................................................. 478
1.10.21. CONFIGURATION_VCCIO_LEVEL ..................................................... 479
1.10.22. CONVERT_PR_WARNINGS_TO_ERRORS ............................................ 480
1.10.23. CRC_ERROR_OPEN_DRAIN ............................................................... 481
1.10.24. CURRENT_STRENGTH_NEW .............................................................. 482
1.10.25. CVP_CONFDONE_OPEN_DRAIN ......................................................... 483
1.10.26. CVP_MODE ....................................................................................... 484
1.10.27. DEVICE ............................................................................................ 485
1.10.28. DEVICE_INITIALIZATION_CLOCK .................................................... 486
1.10.29. DEVICE_IO_STANDARD_ALL ............................................................... 487
1.10.30. DEVICE_MIGRATION_LIST ............................................................... 488
1.10.31. DEVICE_TECHNOLOGY_MIGRATION_LIST ........................................ 489
1.10.32. DQ_GROUP ....................................................................................... 490
1.10.33. DSP_REGISTER_PACKING .................................................................. 491
1.10.34. DSP_REGISTER_PACKING_LEVEL ....................................................... 492
1.10.35. DUPLICATE_ATOM ............................................................................ 493
1.10.36. DUPLICATE_REGISTER ...................................................................... 494
1.10.37. ENABLE_BUS_HOLD_CIRCUITRY ....................................................... 495
1.10.38. ENABLE_CRC_ERROR_PIN ................................................................. 496
1.10.39. ENABLE_CVP_CONFDONE ................................................................. 497
1.10.40. ENABLE_DEVICE_WIDE_OE ............................................................... 498
1.10.41. ENABLE_DEVICE_WIDE_RESET ......................................................... 499
1.10.42. ENABLE_DSP_REGISTER_UNPACKING .............................................. 500
1.10.43. ENABLE_ED_CRC_CHECK ................................................................... 501
1.10.44. ENABLE_INFERRED_SHIFT_REG_COUNTER_DUPLICATION .................. 502
1.10.45. ENABLE_INIT_DONE_OUTPUT ............................................................. 503
1.10.46. ENABLE_INTERMEDIATE_SNAPSHOTS .............................................. 504
1.10.47. ENABLE_NCEO_OUTPUT .................................................................... 505
1.10.48. ENABLE_PR_PINS ............................................................................. 506
1.10.49. ENABLE_TIME_BORROWING_OPTIMIZATION .................................... 507
1.10.50. ENABLE_UNUSED_RX_CLOCK_WORKAROUND .................................... 508
1.10.51. ERROR_CHECK_FREQUENCY_DIVISOR ............................................. 509
1.10.52. EXCLUSIVE_IO_GROUP .................................................................... 510
1.10.53. FINAL_PLACEMENT_OPTIMIZATION ............................................... 511
1.10.54. FITTER_AGGRESSIVE_ROUTABILITY_OPTIMIZATION ......................... 512
1.10.55. FITTER_AUTO_EFFORT_DESIRED_SLACK_MARGIN ......................... 513
1.10.56. FITTER_DENSITY_PACKING_EFFORT .............................................. 514
1.10.57. FITTER_EARLY_RETIMING ............................................................... 515
1.10.58. FITTER_EFFORT .............................................................................. 516
1.10.59. FLEX10K_MAX_PERIPHERAL_OE ................................................... 517
1.10.60. FORCE_CONFIGURATION_VCCIO ..................................................... 518
1.10.61. GLOBAL_PLACEMENT_EFFORT ....................................................... 519
1.10.62. GLOBAL_SIGNAL ........................................................................... 520
<table>
<thead>
<tr>
<th>Setting Name</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.10.63. GNDIO_CURRENT_1PT8V</td>
<td>522</td>
</tr>
<tr>
<td>1.10.64. GNDIO_CURRENT_2PT5V</td>
<td>523</td>
</tr>
<tr>
<td>1.10.65. GNDIO_CURRENT_GTL</td>
<td>524</td>
</tr>
<tr>
<td>1.10.66. GNDIO_CURRENT_GTL_PLUS</td>
<td>525</td>
</tr>
<tr>
<td>1.10.67. GNDIO_CURRENT_LVCMOS</td>
<td>526</td>
</tr>
<tr>
<td>1.10.68. GNDIO_CURRENT_LVTTL</td>
<td>527</td>
</tr>
<tr>
<td>1.10.69. GNDIO_CURRENT_PCI</td>
<td>528</td>
</tr>
<tr>
<td>1.10.70. GNDIO_CURRENT_SSTL2_CLASS1</td>
<td>529</td>
</tr>
<tr>
<td>1.10.71. GNDIO_CURRENT_SSTL2_CLASS2</td>
<td>530</td>
</tr>
<tr>
<td>1.10.72. GNDIO_CURRENT_SSTL3_CLASS1</td>
<td>531</td>
</tr>
<tr>
<td>1.10.73. GNDIO_CURRENT_SSTL3_CLASS2</td>
<td>532</td>
</tr>
<tr>
<td>1.10.74. GXB_0PPM_CORECLK</td>
<td>533</td>
</tr>
<tr>
<td>1.10.75. HPS_COLD_RESET_PIN_MODE</td>
<td>534</td>
</tr>
<tr>
<td>1.10.76. HPS_WARM_RESET_PIN_MODE</td>
<td>535</td>
</tr>
<tr>
<td>1.10.77. HSSI_PARAMETER</td>
<td>536</td>
</tr>
<tr>
<td>1.10.78. IGNORE_HSSI_COLUMN_POWER_WHEN_PRESERVING_UNUSED_XCVR_CHANNELS</td>
<td>537</td>
</tr>
<tr>
<td>1.10.79. INIT_DONE_OPEN_DRAIN</td>
<td>538</td>
</tr>
<tr>
<td>1.10.80. INPUT_DELAYCHAIN</td>
<td>539</td>
</tr>
<tr>
<td>1.10.81. INPUT_TERMINATION</td>
<td>540</td>
</tr>
<tr>
<td>1.10.82. INTERNAL_SCRUBBING</td>
<td>541</td>
</tr>
<tr>
<td>1.10.83. IO_12_LANE_INPUT_DATA_DELAY_CHAIN</td>
<td>542</td>
</tr>
<tr>
<td>1.10.84. IO_12_LANE_INPUT_STROBE_DELAYCHAIN</td>
<td>543</td>
</tr>
<tr>
<td>1.10.85. IO_MAXIMUM_TOGGLE_RATE</td>
<td>544</td>
</tr>
<tr>
<td>1.10.86. IO_PARTITION_PLACEMENT</td>
<td>545</td>
</tr>
<tr>
<td>1.10.87. IO_STANDARD</td>
<td>546</td>
</tr>
<tr>
<td>1.10.88. IP_BB_LOCATION</td>
<td>547</td>
</tr>
<tr>
<td>1.10.89. IP_COLOCATE</td>
<td>548</td>
</tr>
<tr>
<td>1.10.90. IP_RECONFIG_GROUP_MASTER_CLOCK_CHANNEL</td>
<td>549</td>
</tr>
<tr>
<td>1.10.91. IP_RECONFIG_GROUP_PARENT</td>
<td>550</td>
</tr>
<tr>
<td>1.10.92. IP_RECONFIG_GROUP_SHARED_SIP</td>
<td>551</td>
</tr>
<tr>
<td>1.10.93. IP_RECONFIG_ID</td>
<td>552</td>
</tr>
<tr>
<td>1.10.94. IP_TILE_ASSIGNMENT</td>
<td>553</td>
</tr>
<tr>
<td>1.10.95. IP_TILE_SETTING</td>
<td>554</td>
</tr>
<tr>
<td>1.10.96. LVDS_DIRECT_LOOPBACK_MODE</td>
<td>555</td>
</tr>
<tr>
<td>1.10.97. MACRO_HEAD</td>
<td>556</td>
</tr>
<tr>
<td>1.10.98. MACRO_MEMBER</td>
<td>557</td>
</tr>
<tr>
<td>1.10.99. MATCH_PLL_COMPENSATION_CLOCK</td>
<td>558</td>
</tr>
<tr>
<td>1.10.100. MIGRATION_DEVICES</td>
<td>559</td>
</tr>
<tr>
<td>1.10.101. MINIMUM_SEU_INTERVAL</td>
<td>560</td>
</tr>
<tr>
<td>1.10.102. MODULE_BLOATING_FACTOR</td>
<td>561</td>
</tr>
<tr>
<td>1.10.103. NCEO_OPEN_DRAIN</td>
<td>562</td>
</tr>
<tr>
<td>1.10.104. NUMBER_OFEXAMPLE_NODES_REPORTED</td>
<td>563</td>
</tr>
<tr>
<td>1.10.105. OE_DELAY_CHAIN</td>
<td>564</td>
</tr>
<tr>
<td>1.10.106. OPTIMIZE_FOR_METASTABILITY</td>
<td>565</td>
</tr>
<tr>
<td>1.10.107. OPTIMIZE_HOLD_TIMING</td>
<td>566</td>
</tr>
<tr>
<td>1.10.108. OPTIMIZE_IOC_REGISTER_PLACEMENT_FOR_TIMING</td>
<td>567</td>
</tr>
<tr>
<td>1.10.109. OPTIMIZE_MULTI_CORNER_TIMING</td>
<td>568</td>
</tr>
<tr>
<td>1.10.110. OPTIMIZE_PERSONA_ROUTABILITY</td>
<td>569</td>
</tr>
<tr>
<td>1.10.111. OPTIMIZE_POWER_DURING_FITTING</td>
<td>570</td>
</tr>
<tr>
<td>1.10.112. OPTIMIZE_TIMING</td>
<td>571</td>
</tr>
</tbody>
</table>
1.10.13. OUTPUT_DELAY_CHAIN. ................................................................. 572
1.10.14. OUTPUT_PIN_LOAD. ....................................................................... 573
1.10.15. OUTPUT_TERMINATION. ................................................................. 574
1.10.16. PERIPHERY_TO_CORE_PLACEMENT_AND_ROUTING_OPTIMIZATION. ... 575
1.10.17. PERIPH_FITTER_SCRIPT. ................................................................. 576
1.10.18. PERIPH_REPORT_SCRIPT. .............................................................. 577
1.10.19. PHYSICAL_RAM_RPT_MAX_ROW. .................................................... 578
1.10.20. PHYSICAL_SYNTHESIS. ................................................................. 579
1.10.21. PLACEMENT_EFFORT_MULTIPLIER. .............................................. 580
1.10.22. PLL_AUTO_RESET. .......................................................................... 581
1.10.23. PLL_BANDWIDTH_PRESET. ............................................................ 582
1.10.24. PLL_COMPENSATION_MODE. ......................................................... 583
1.10.25. PLL_OPTIMIZE_PHASE_SHIFT_FOR_TIMING. .................................... 584
1.10.26. PRESERVEUNUSED_XCVR_CHANNEL. .......................................... 585
1.10.27. PRIORITY_SEU_AREA. ..................................................................... 586
1.10.28. PROGRAMMABLE_DEEMPHASIS. ..................................................... 587
1.10.29. PROGRAMMABLE_POWER_MAXIMUM_HIGH_SPEED_FRACTION_OF_US... 588
     ED_LAB_TILES. ................................................................................... 588
1.10.30. PROGRAMMABLE_POWER_TECHNOLOGY_SETTING. ......................... 589
1.10.31. PROGRAMMABLE_PRE_EMPHASIS. ................................................. 590
1.10.32. PROGRAMMABLE_VOD. .................................................................. 591
1.10.33. PR_DONE_OPEN_DRAIN. ................................................................. 592
1.10.34. PR_ERROR_OPEN_DRAIN. ............................................................... 593
1.10.35. PR_PINS_OPEN_DRAIN. ................................................................. 594
1.10.36. PR_READY_OPEN_DRAIN. ............................................................... 595
1.10.37. PR_SECURITY_VALIDATION. ............................................................. 596
1.10.38. PUD_CTRL. .................................................................................... 597
1.10.39. QII_AUTO_PACKED_REGISTERS. ..................................................... 598
1.10.40. RELATIVE_NEUTRON_FLUX. .......................................................... 600
1.10.41. RESERVE_ALL_UNUSED_PINS_WEAK_PULLUP. ............................... 601
1.10.42. RESERVE_AVST_CLK_AFTER_CONFIGURATION. ............................... 602
1.10.43. RESERVE_AVST_DATA15_THROUGH_DATA0_AFTER_CONFIGURATION. .... 603
1.10.44. RESERVE_AVST_DATA31_THROUGH_DATA16_AFTER_CONFIGURATION. .... 604
1.10.45. RESERVE_AVST_DATA0_AFTER_CONFIGURATION. ............................. 605
1.10.46. RESERVE_AVST_DATA8_AFTER_CONFIGURATION. ............................ 606
1.10.47. RESERVE_AVST_DATA15_THROUGH_DATA8_AFTER_CONFIGURATION. .... 607
1.10.48. RESERVE_AVST_DATA31_THROUGH_DATA16_AFTER_CONFIGURATION. .... 608
1.10.49. RESERVE_AVST_DATA7_THROUGH_DATA1_AFTER_CONFIGURATION. .... 609
1.10.50. RESERVE_FLEXIBLE_CLOCK_NETWORK. ......................................... 610
1.10.51. RESERVE_PR_PINS. ........................................................................ 611
1.10.52. RESERVE_ROUTING_OUTPUT_FLEXIBILITY. ................................. 612
1.10.53. ROUTER_CLOCKING_TOPOLOGY_ANALYSIS. ................................. 613
1.10.54. ROUTER_EFFORT_MULTIPLIER. ..................................................... 614
1.10.55. ROUTER_LCELL_INSERTION_AND_LOGIC_DUPLICATION. ................. 615
1.10.56. ROUTER_REGISTER_DUPLICATION. .............................................. 616
1.10.57. ROUTER_TIMING_OPTIMIZATION_LEVEL. ....................................... 617
1.10.58. RZQ_GROUP. ............................................................................... 618
1.10.59. SCHMITT_TRIGGER. ...................................................................... 619
1.10.60. SDM_DIRECT_TO_FACTORY_IMAGE. ............................................... 620
1.10.61. SDM_PCIE_CALIB_START. ............................................................... 621
1.10.62. SEED. .......................................................................................... 622
1.10.163. SEU_FIT_REPORT................................................................. 623
1.10.164. SLEW_RATE................................................................. 624
1.10.165. SLOW_SLEW_RATE................................................................. 625
1.10.166. STRATIXV_CONFIGURATIONS_SCHEME......................... 626
1.10.167. SYNCHRONIZER_IDENTIFICATION................................. 627
1.10.168. SYNCHRONIZER_TOGGLE_RATE........................................ 629
1.10.169. TERMINATION_CONTROL_BLOCK.................................. 630
1.10.170. TREAT_BIDIR_AS_OUTPUT................................................ 631
1.10.171. TRI_STATE_SPI_PINS............................................................. 632
1.10.172. UNFORCE_MERGE_PLL....................................................... 633
1.10.173. UNUSED_IO_BANK_VOLTAGE......................................... 634
1.10.174. UNUSED_TSD_PINS_GND..................................................... 635
1.10.175. USE_ANTI_TAMPER.......................................................... 636
1.10.176. USE_AS_3V_GPIO.............................................................. 637
1.10.177. USE_CONF_DONE............................................................... 638
1.10.178. USE_CVP_CONF_DONE...................................................... 639
1.10.179. USE_DATA_UNLOCK.......................................................... 640
1.10.180. USE_HPS_COLD_RESET...................................................... 641
1.10.181. USE_HPS_WARM_RESET.................................................... 642
1.10.182. USE_INIT_DONE............................................................... 643
1.10.183. USE_NCATTRIP................................................................. 644
1.10.184. USE_PWRMGT_ALERT....................................................... 645
1.10.185. USE_PWRMGT_PWM0......................................................... 646
1.10.186. USE_PWRMGT_SCL............................................................. 647
1.10.187. USE_PWRMGT_SDA............................................................. 648
1.10.188. USE_SEU_ERROR............................................................... 649
1.10.189. USE_TAMPER_DETECT....................................................... 650
1.10.190. USE_UIB_CATTRIP............................................................ 651
1.10.191. VCCIO_CURRENT_1PT8V................................................ 652
1.10.192. VCCIO_CURRENT_2PT5V................................................ 653
1.10.193. VCCIO_CURRENT_GTL....................................................... 654
1.10.194. VCCIO_CURRENT_GTL_PLUS........................................... 655
1.10.195. VCCIO_CURRENT_LVCMOS................................................ 656
1.10.196. VCCIO_CURRENT_LVTTL.................................................... 657
1.10.197. VCCIO_CURRENT_PCI........................................................ 658
1.10.198. VCCIO_CURRENT_SSTL2_CLASS1..................................... 659
1.10.199. VCCIO_CURRENT_SSTL2_CLASS2..................................... 660
1.10.200. VCCIO_CURRENT_SSTL3_CLASS1..................................... 661
1.10.201. VCCIO_CURRENT_SSTL3_CLASS2..................................... 662
1.10.202. VID_OPERATION_MODE...................................................... 663
1.10.203. VREF_MODE.................................................................. 664
1.10.204. WEAK_PULL_UP_DN_SEL................................................... 665
1.10.205. WEAK_PULL_UP_RESISTOR.............................................. 666
1.10.206. WIRELUT_REMOVAL_HOLD_GUARD_BAND......................... 667
1.10.207. WIRELUT_REMOVAL_SETUP_GUARD_BAND......................... 668
1.10.208. XCVR_A10_REFCLK_TERM_TRISTATE...................................... 669
1.10.209. XCVR_A10_RX_ADPACTLE_ACGAIN_4S................................ 670
1.10.210. XCVR_A10_RX_ADPACTLE_EQZ_1S_SEL............................ 672
1.10.211. XCVR_A10_RX_ADPACTLE_FXTAP1..................................... 673
1.10.212. XCVR_A10_RX_ADPACTLE_FXTAP10.................................... 677
1.10.213. XCVR_A10_RX_ADPACTLE_FXTAP10_SGN............................ 680
<table>
<thead>
<tr>
<th>Section</th>
<th>Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.13.49</td>
<td>POWER_VCCA_GXBL_USER_OPTION</td>
<td>875</td>
</tr>
<tr>
<td>1.13.50</td>
<td>POWER_VCCA_GXBR_USER_OPTION</td>
<td>876</td>
</tr>
<tr>
<td>1.13.51</td>
<td>POWER_VCCA_GXB_USER_OPTION</td>
<td>877</td>
</tr>
<tr>
<td>1.13.52</td>
<td>POWER_VCCA_L_USER_OPTION</td>
<td>878</td>
</tr>
<tr>
<td>1.13.53</td>
<td>POWER_VCCA_R_USER_OPTION</td>
<td>879</td>
</tr>
<tr>
<td>1.13.54</td>
<td>POWER_VCCCB_USER_OPTION</td>
<td>880</td>
</tr>
<tr>
<td>1.13.55</td>
<td>POWER_VCCH_GXBL_USER_OPTION</td>
<td>881</td>
</tr>
<tr>
<td>1.13.56</td>
<td>POWER_VCCH_GXBR_USER_OPTION</td>
<td>882</td>
</tr>
<tr>
<td>1.13.57</td>
<td>POWER_VCCH_GXB_USER_OPTION</td>
<td>883</td>
</tr>
<tr>
<td>1.13.58</td>
<td>POWER_VCCIO_USER_OPTION</td>
<td>884</td>
</tr>
<tr>
<td>1.13.59</td>
<td>POWER_VCCL_GXB_USER_OPTION</td>
<td>885</td>
</tr>
<tr>
<td>1.13.60</td>
<td>POWER_VCCPD_USER_OPTION</td>
<td>886</td>
</tr>
<tr>
<td>1.13.61</td>
<td>POWER_VCCR_GXBL_USER_OPTION</td>
<td>887</td>
</tr>
<tr>
<td>1.13.62</td>
<td>POWER_VCCR_GXBR_USER_OPTION</td>
<td>888</td>
</tr>
<tr>
<td>1.13.63</td>
<td>POWER_VCCR_GXB_USER_OPTION</td>
<td>889</td>
</tr>
<tr>
<td>1.13.64</td>
<td>POWER_VCCT_GXBL_USER_OPTION</td>
<td>890</td>
</tr>
<tr>
<td>1.13.65</td>
<td>POWER_VCCT_GXBR_USER_OPTION</td>
<td>891</td>
</tr>
<tr>
<td>1.13.66</td>
<td>POWER_VCCT_GXB_USER_OPTION</td>
<td>892</td>
</tr>
<tr>
<td>1.13.67</td>
<td>POWER_VCD_FILE_END_TIME</td>
<td>893</td>
</tr>
<tr>
<td>1.13.68</td>
<td>POWER_VCD_FILE_START_TIME</td>
<td>894</td>
</tr>
<tr>
<td>1.13.69</td>
<td>POWER_VCD_FILTER_GLITCHES</td>
<td>895</td>
</tr>
<tr>
<td>1.13.70</td>
<td>VCCE_AUX_SHARED_USER_VOLTAGE</td>
<td>896</td>
</tr>
<tr>
<td>1.13.71</td>
<td>VCCE_AUX_USER_VOLTAGE</td>
<td>897</td>
</tr>
<tr>
<td>1.13.72</td>
<td>VCCA_FPLL_USER_VOLTAGE</td>
<td>898</td>
</tr>
<tr>
<td>1.13.73</td>
<td>VCCA_GTBR_USER_VOLTAGE</td>
<td>899</td>
</tr>
<tr>
<td>1.13.74</td>
<td>VCCA_GTB_USER_VOLTAGE</td>
<td>900</td>
</tr>
<tr>
<td>1.13.75</td>
<td>VCCA_GXBL_USER_VOLTAGE</td>
<td>901</td>
</tr>
<tr>
<td>1.13.76</td>
<td>VCCA_GXBR_USER_VOLTAGE</td>
<td>902</td>
</tr>
<tr>
<td>1.13.77</td>
<td>VCCA_GXB_USER_VOLTAGE</td>
<td>903</td>
</tr>
<tr>
<td>1.13.78</td>
<td>VCCA_L_USER_VOLTAGE</td>
<td>904</td>
</tr>
<tr>
<td>1.13.79</td>
<td>VCCA_PLL_USER_VOLTAGE</td>
<td>905</td>
</tr>
<tr>
<td>1.13.80</td>
<td>VCCA_R_USER_VOLTAGE</td>
<td>906</td>
</tr>
<tr>
<td>1.13.81</td>
<td>VCCA_USER_VOLTAGE</td>
<td>907</td>
</tr>
<tr>
<td>1.13.82</td>
<td>VCCBAT_USER_VOLTAGE</td>
<td>908</td>
</tr>
<tr>
<td>1.13.83</td>
<td>VCCCB_USER_VOLTAGE</td>
<td>909</td>
</tr>
<tr>
<td>1.13.84</td>
<td>VCCD_FPLL_USER_VOLTAGE</td>
<td>910</td>
</tr>
<tr>
<td>1.13.85</td>
<td>VCCD_PLL_USER_VOLTAGE</td>
<td>911</td>
</tr>
<tr>
<td>1.13.86</td>
<td>VCCD_USER_VOLTAGE</td>
<td>912</td>
</tr>
<tr>
<td>1.13.87</td>
<td>VCCEH_GXBL_USER_VOLTAGE</td>
<td>913</td>
</tr>
<tr>
<td>1.13.88</td>
<td>VCCEH_GXBR_USER_VOLTAGE</td>
<td>914</td>
</tr>
<tr>
<td>1.13.89</td>
<td>VCCEH_GXB_USER_VOLTAGE</td>
<td>915</td>
</tr>
<tr>
<td>1.13.90</td>
<td>VCCEMERAM_USER_VOLTAGE</td>
<td>916</td>
</tr>
<tr>
<td>1.13.91</td>
<td>VCCE_GXBL_USER_VOLTAGE</td>
<td>917</td>
</tr>
<tr>
<td>1.13.92</td>
<td>VCCE_GXBR_USER_VOLTAGE</td>
<td>918</td>
</tr>
<tr>
<td>1.13.93</td>
<td>VCCE_GXB_USER_VOLTAGE</td>
<td>919</td>
</tr>
<tr>
<td>1.13.94</td>
<td>VCCE_USER_VOLTAGE</td>
<td>920</td>
</tr>
<tr>
<td>1.13.95</td>
<td>VCCHIP_L_USER_VOLTAGE</td>
<td>921</td>
</tr>
<tr>
<td>1.13.96</td>
<td>VCCHIP_R_USER_VOLTAGE</td>
<td>922</td>
</tr>
<tr>
<td>1.13.97</td>
<td>VCCHIP_USER_VOLTAGE</td>
<td>923</td>
</tr>
<tr>
<td>1.13.98</td>
<td>VCCHIP_L_USER_VOLTAGE</td>
<td>924</td>
</tr>
<tr>
<td>1.13.99</td>
<td>VCCHIP_R_USER_VOLTAGE</td>
<td>925</td>
</tr>
</tbody>
</table>
1.13.100. VCCH_GTBR_USER_VOLTAGE............................................................. 926
1.13.101. VCCH_GTB_USER_VOLTAGE................................................................ 927
1.13.102. VCCH_GXBL_USER_VOLTAGE............................................................. 928
1.13.103. VCCH_GXBR_USER_VOLTAGE............................................................. 929
1.13.104. VCCH_GXB_USER_VOLTAGE............................................................... 930
1.13.105. VCCH_L_USER_VOLTAGE.................................................................... 931
1.13.106. VCCH_R_USER_VOLTAGE................................................................... 932
1.13.107. VCCINT_USER_VOLTAGE................................................................... 933
1.13.108. VCCIOREF_HPS_USER_VOLTAGE..................................................... 934
1.13.109. VCCI0_HPS_USER_VOLTAGE.............................................................. 935
1.13.110. VCCI0_USER_VOLTAGE...................................................................... 936
1.13.111. VCCL_GTBL_USER_VOLTAGE.............................................................. 937
1.13.112. VCCL_GTBR_USER_VOLTAGE.............................................................. 938
1.13.113. VCCL_GTB_USER_VOLTAGE............................................................... 939
1.13.114. VCCL_GXBL_USER_VOLTAGE.............................................................. 940
1.13.115. VCCL_GXBR_USER_VOLTAGE.............................................................. 941
1.13.116. VCCL_GXB_USER_VOLTAGE............................................................... 942
1.13.117. VCCL_HPS_USER_VOLTAGE............................................................... 943
1.13.118. VCCL_USER_VOLTAGE...................................................................... 944
1.13.119. VCCPD_USER_VOLTAGE.................................................................... 945
1.13.120. VCCPGM_USER_VOLTAGE................................................................. 946
1.13.121. VCCPL_HPS_USER_VOLTAGE............................................................ 947
1.13.122. VCCPT_USER_VOLTAGE..................................................................... 948
1.13.123. VCCP_USER_VOLTAGE....................................................................... 949
1.13.124. VCCRSTCLK_HPS_USER_VOLTAGE................................................... 950
1.13.125. VCCR_GTBL_USER_VOLTAGE.............................................................. 951
1.13.126. VCCR_GTBR_USER_VOLTAGE............................................................. 952
1.13.127. VCCR_GTB_USER_VOLTAGE............................................................... 953
1.13.128. VCCR_GXBL_USER_VOLTAGE.............................................................. 954
1.13.129. VCCR_GXBR_USER_VOLTAGE............................................................. 955
1.13.130. VCCR_GXB_USER_VOLTAGE............................................................... 956
1.13.131. VCCR_L_USER_VOLTAGE.................................................................... 957
1.13.132. VCCR_R_USER_VOLTAGE................................................................... 958
1.13.133. VCCR_USER_VOLTAGE...................................................................... 959
1.13.134. VCCT_GTBL_USER_VOLTAGE.............................................................. 960
1.13.135. VCCT_GTBR_USER_VOLTAGE............................................................. 961
1.13.136. VCCT_GTB_USER_VOLTAGE............................................................... 962
1.13.137. VCCT_GXBL_USER_VOLTAGE.............................................................. 963
1.13.138. VCCT_GXBR_USER_VOLTAGE............................................................. 964
1.13.139. VCCT_GXB_USER_VOLTAGE............................................................... 965
1.13.140. VCCT_L_USER_VOLTAGE.................................................................... 966
1.13.141. VCCT_R_USER_VOLTAGE................................................................... 967
1.13.142. VCCT_USER_VOLTAGE...................................................................... 968
1.13.143. VCC_HPS_USER_VOLTAGE................................................................. 969
1.13.144. VCC_USER_VOLTAGE...................................................................... 970

1.14. Programmer Assignments ........................................................................ 971
1.14.1. GENERATE_CONFIG_HEXOUT_FILE................................................... 971
1.14.2. GENERATE_CONFIG_ISC_FILE............................................................. 972
1.14.3. GENERATE_CONFIG_JAM_FILE.......................................................... 973
1.14.4. GENERATE_CONFIG_JBC_FILE............................................................ 974
1.14.5. GENERATE_CONFIG_JBC_FILE_COMPRESSED...................................... 975
1.14.6. GENERATE_CONFIG_SVF_FILE........................................................................................................ 976
1.14.7. GENERATE_JAM_FILE...................................................................................................................... 977
1.14.8. GENERATE_JBC_FILE........................................................................................................................ 978
1.14.9. GENERATE_JBC_FILE_COMPRESSED.................................................................................................. 979
1.14.10. GENERATE_SVF_FILE...................................................................................................................... 980
1.14.11. HPS_EARLY_IO_RELEASE ............................................................................................................... 981
1.14.12. MERGE_HEX_FILE........................................................................................................................... 982

1.15. Project-Wide Assignments ...................................................................................................................... 983
1.15.1. AHDL_FILE......................................................................................................................................... 983
1.15.2. AHDL_TEXT_DESIGN_OUTPUT_FILE.................................................................................................. 984
1.15.3. ALLOW_DSP_RETIMING ................................................................................................................... 985
1.15.4. ALLOW_RAM_RETIMING .................................................................................................................. 986
1.15.5. ASM_FILE......................................................................................................................................... 987
1.15.6. AUTO_EXPORT_VER_COMPATIBLE_DB ............................................................................................ 988
1.15.7. BASE_REVISION_PROJECT_OUTPUT_DIRECTORY .................................................................................. 989
1.15.8. BDF_FILE......................................................................................................................................... 990
1.15.9. BINARY_FILE.................................................................................................................................... 991
1.15.10. BSF_FILE....................................................................................................................................... 992
1.15.11. CDC_MISC_FILE............................................................................................................................ 993
1.15.12. CDC_SYSTEMVERILOG_FILE .......................................................................................................... 994
1.15.13. CDC_VERILOG_FILE...................................................................................................................... 995
1.15.14. CDF_FILE........................................................................................................................................ 996
1.15.15. COMMAND_MACRO_FILE.............................................................................................................. 997
1.15.16. CPP_FILE....................................................................................................................................... 998
1.15.17. CPP_INCLUDE_FILE........................................................................................................................ 999
1.15.18. CUSP_FILE...................................................................................................................................... 1000
1.15.19. C_FILE.......................................................................................................................................... 1001
1.15.20. DEPENDENCY_FILE........................................................................................................................ 1002
1.15.21. DESIGN_ASSISTANT_INCLUDE_IP_BLOCKS ................................................................................... 1003
1.15.22. DESIGN_ASSISTANT_MAX_VIOLATIONS_PER_RULE........................................................................ 1004
1.15.23. DESIGN_ASSISTANT_WAIVER_FILE................................................................................................ 1005
1.15.24. DRC_RAM_INFERENCE_HIGH_FANOUT_NET_THRESHOLD................................................................. 1006
1.15.25. DSPBUILDER_FILE........................................................................................................................ 1007
1.15.26. EDIF_FILE....................................................................................................................................... 1008
1.15.27. ELF_FILE....................................................................................................................................... 1009
1.15.28. ENABLE_COMPACT_REPORT_TABLE............................................................................................... 1010
1.15.29. ENABLE_FIT_RPTRESOURCE_BY_ENTITY....................................................................................... 1011
1.15.30. ENABLE_REDUCED_MEMORY_MODE.................................................................................................. 1012
1.15.31. EQUATION_FILE............................................................................................................................ 1013
1.15.32. ERROR_ON_INVALID_ENTITY_NAME ............................................................................................... 1014
1.15.33. EXPORT_PARTITION_SNAPSHOT_FINAL....................................................................................... 1015
1.15.34. EXPORT_PARTITION_SNAPSHOT_SYNTHESIZED........................................................................... 1016
1.15.35. FLOW_DISABLE_ASSEMBLER......................................................................................................... 1017
1.15.36. FLOW_ENABLE_DESIGN_ASSISTANT............................................................................................... 1018
1.15.37. FLOW_ENABLE_EDA_NETLIST_WRITER........................................................................................... 1019
1.15.38. FLOW_ENABLE_INTERACTIVE_TIMING_ANALYZER......................................................................... 1020
1.15.39. FLOW_ENABLE_IO_ASSIGNMENT_ANALYSIS................................................................................... 1021
1.15.40. FLOW_ENABLE_PARALLEL_MODULES............................................................................................ 1022
1.15.41. FLOW_ENABLE_POWER_ANALYZER.................................................................................................. 1023
1.15.42. FLOW_ENABLE_RTL_VIEWER.......................................................................................................... 1024
1.15.43. GDF_FILE....................................................................................................................................... 1025
### Contents

1.15.44. HEX_FILE.........................................................................................1026  
1.15.45. HEX_OUTPUT_FILE............................................................................1027  
1.15.46. HPS_ISW_DATA................................................................................1028  
1.15.47. HPS_ISW_EMIF................................................................................1029  
1.15.48. HPS_ISW_FILE................................................................................1030  
1.15.49. HTML_FILE.......................................................................................1031  
1.15.50. HTML_REPORT_FILE........................................................................1032  
1.15.51. INCLUDE_FILE..................................................................................1033  
1.15.52. INVALID_DESIGN_SOURCE................................................................1034  
1.15.53. IPX_FILE..........................................................................................1035  
1.15.54. IP_COMPONENT_AUTHOR..................................................................1036  
1.15.55. IP_COMPONENT_DESCRIPTION..........................................................1037  
1.15.56. IP_COMPONENT_DISPLAY_NAME........................................................1038  
1.15.57. IP_COMPONENT_DOCUMENTATION_LINK.............................................1039  
1.15.58. IP_COMPONENT_GROUP....................................................................1040  
1.15.59. IP_COMPONENT_INTERNAL................................................................1041  
1.15.60. IP_COMPONENT_NAME......................................................................1042  
1.15.61. IP_COMPONENT_PARAMETER.............................................................1043  
1.15.62. IP_COMPONENT_REPORT_HIERARCHY.................................................1044  
1.15.63. IP_COMPONENT_VERSION.................................................................1045  
1.15.64. IP_FILE...........................................................................................1046  
1.15.65. IP_GENERATED_DEVICE_FAMILY.........................................................1047  
1.15.66. IP_QSYS_MODE................................................................................1048  
1.15.67. IP_TARGETED_DEVICE_FAMILY...........................................................1049  
1.15.68. IP_TARGETED_PART_TRAIT................................................................1050  
1.15.69. IP_TOOL_ENV...................................................................................1051  
1.15.70. IP_TOOL_HIERARCHY_LEVELS............................................................1052  
1.15.71. IP_TOOL_NAME................................................................................1053  
1.15.72. IP_TOOL_VENDOR_NAME...................................................................1054  
1.15.73. IP_TOOL_VERSION...........................................................................1055  
1.15.74. IP_TOOL_VERSION_CREATED.............................................................1056  
1.15.75. IP_TOP_LEVEL_COMPONENT_NAME.....................................................1057  
1.15.76. IP_TOP_LEVEL_ENTITY_NAME............................................................1058  
1.15.77. JAM_FILE.........................................................................................1059  
1.15.78. JBC_FILE.........................................................................................1060  
1.15.79. LICENSE_FILE..................................................................................1061  
1.15.80. LMF_FILE.........................................................................................1062  
1.15.81. LOGIC_ANALYZER_INTERFACE_FILE....................................................1063  
1.15.82. MAP_FILE........................................................................................1064  
1.15.83. MAX_IGNORED_ASGN_MSG...............................................................1065  
1.15.84. MESSAGE_DISABLE...........................................................................1066  
1.15.85. MESSAGE_ENABLE............................................................................1067  
1.15.86. MIF_FILE.........................................................................................1068  
1.15.87. MISC_FILE.......................................................................................1069  
1.15.88. NUM_PARALLEL_PROCESSORS...........................................................1070  
1.15.89. OBJECT_FILE....................................................................................1071  
1.15.90. OCP_FILE........................................................................................1072  
1.15.91. PARTIAL_SRAM_OBJECT_FILE..........................................................1073  
1.15.92. PIN_FILE.........................................................................................1074  
1.15.93. POWER_INPUT_FILE..........................................................................1075  
1.15.94. PPF_FILE........................................................................................1076
1.15.146. VERILOG_INCLUDE_FILE.................................................................1128
1.15.147. VERILOG_OUTPUT_FILE................................................................1129
1.15.148. VERILOG_TEST_BENCH_FILE.......................................................1130
1.15.149. VER_COMPATIBLE_DB_DIR............................................................1131
1.15.150. VHDL_FILE..................................................................................1132
1.15.151. VHDL_OUTPUT_FILE.................................................................1133
1.15.152. VHDL_TEST_BENCH_FILE.............................................................1134
1.15.153. VQM_FILE..................................................................................1135
1.15.154. ZIP_VECTOR_WAVEFORM_FILE..................................................1136

1.16. Retimer Assignments ...........................................................................1137
   1.16.1. HYPER_RETIMER_ADD_PIPELINING.............................................1137
   1.16.2. HYPER_RETIMER_ADD_PIPELINING_GROUP....................................1138
   1.16.3. HYPER_RETIMER_ENABLE_ADD_PIPELINING...................................1139
   1.16.4. HYPER_RETIMER_FAST_FORWARD_ADD_PIPELINING_MAX.................1140
   1.16.5. HYPER_RETIMER_FAST_FORWARDASYNCH_CLEAR.............................1141
   1.16.6. HYPER_RETIMER_FAST_FORWARD_DSP_BLOCKS...............................1142
   1.16.7. HYPER_RETIMER_FAST_FORWARD_RAM_BLOCKS...............................1143
   1.16.8. HYPER_RETIMER_FAST_FORWARD_USER_PRESERVE_RESTRICTION........1144

1.17. Retimer Fast Forward Assignments .....................................................1145
   1.17.1. CRITICAL_CHAIN_VIEWER.........................................................1145
   1.17.2. FLOW_ENABLE_HYPER_RETIMER_FAST_FORWARD............................1146
   1.17.3. HYPER_RETIMER_FAST_FORWARD_CUT_ALL_CLOCK_TRANSFERS........1147
   1.17.4. HYPER_RETIMER_FAST_FORWARD_ON_HIERARCHY..........................1148

1.18. Signal Tap Assignments .....................................................................1149
   1.18.1. CREATE_PARTITION_BOUNDARY_PORTS.......................................1149
   1.18.2. ENABLE_LOGIC_ANALYZER_INTERFACE.........................................1150
   1.18.3. ENABLE_SIGNALTAP.....................................................................1151
   1.18.4. PRESERVE_FOR_DEBUG................................................................1152
   1.18.5. PRESERVE_FOR_DEBUG_ENABLE..................................................1153
   1.18.6. STP_FILE.....................................................................................1154
   1.18.7. USE_LOGIC_ANALYZER_INTERFACE_FILE......................................1155
   1.18.8. USE_SIGNALTAP_FILE.................................................................1156

1.19. Simulator Assignments .................................................................1157
   1.19.1. ACTION.....................................................................................1157
   1.19.2. ADD_DEFAULT_PINS_TO_SIMULATION_OUTPUT_WAVEFORMS........1158
   1.19.3. ADD_TO_SIMULATION_OUTPUT_WAVEFORMS...............................1159
   1.19.4. ALIAS.......................................................................................1160
   1.19.5. AUTO_USE_SIMULATION_PDB_NETLIST.......................................1161
   1.19.6. BREAKPOINT_STATE..................................................................1162
   1.19.7. CHECK_OUTPUTS.......................................................................1163
   1.19.8. END_TIME...............................................................................1164
   1.19.9. EXTERNAL_PIN_CONNECTION.....................................................1165
   1.19.10. GLITCH_DETECTION.................................................................1166
   1.19.11. GLITCH_INTERVAL....................................................................1167
   1.19.12. IMMEDIATE_ASSERTION_FAIL_ACTION.......................................1168
   1.19.13. IMMEDIATE_ASSERTION_FAIL_MESSAGE....................................1169
   1.19.14. IMMEDIATE_ASSERTION_PASS_MESSAGE....................................1170
   1.19.15. IMMEDIATE_ASSERTION_STATE.................................................1171
   1.19.16. IMMEDIATE_ASSERTION_TEST_CONDITION..................................1172
   1.19.17. INCREMENTAL_VECTOR_INPUT_SOURCE.....................................1173
   1.19.18. PASSIVE_RESISTOR.................................................................1174
1.19.19. SETUP_HOLD_DETECTION ................................................................. 1175
1.19.20. SETUP_HOLD_DETECTION_INPUT_REGISTERS_BIDIR_PINS_DISABLED... 1176
1.19.21. SETUP_HOLD_TIME_VIOLATION_DETECTION ....................................... 1177
1.19.22. SIMULATION_BUS_CHANNEL_GROUPING ............................................. 1178
1.19.23. SIMULATION_COMPARE_SIGNAL ......................................................... 1179
1.19.24. SIMULATION_COMPLETE_COVERAGE_REPORT_PANEL ........................... 1180
1.19.25. SIMULATION_COVERAGE ................................................................... 1181
1.19.26. SIMULATION_DEFAULT_VECTOR_COMPARE_TOLERANCE .................... 1182
1.19.27. SIMULATION_MISSING_0_VALUE_COVERAGE_REPORT_PANEL ............... 1183
1.19.28. SIMULATION_MISSING_1_VALUE_COVERAGE_REPORT_PANEL ............... 1184
1.19.29. SIMULATION_MODE .......................................................................... 1185
1.19.30. SIMULATION_NETLIST_VIEWER .......................................................... 1186
1.19.31. SIMULATION_SIGNAL_COMPARE_TOLERANCE ..................................... 1187
1.19.32. SIMULATION_VDB_RESULT_FLUSH ..................................................... 1188
1.19.33. SIMULATION_VECTOR_COMPARE_BEGIN_TIME .................................... 1189
1.19.34. SIMULATION_VECTOR_COMPARE_END_TIME ....................................... 1190
1.19.35. SIMULATION_VECTOR_COMPARE_RULE_FOR_0 .................................. 1191
1.19.36. SIMULATION_VECTOR_COMPARE_RULE_FOR_1 .................................. 1192
1.19.37. SIMULATION_VECTOR_COMPARE_RULE_FOR_DC ................................ 1193
1.19.38. SIMULATION_VECTOR_COMPARE_RULE_FOR_H .................................. 1194
1.19.39. SIMULATION_VECTOR_COMPARE_RULE_FOR_L .................................. 1195
1.19.40. SIMULATION_VECTOR_COMPARE_RULE_FOR_U .................................. 1196
1.19.41. SIMULATION_VECTOR_COMPARE_RULE_FOR_W .................................. 1197
1.19.42. SIMULATION_VECTOR_COMPARE_RULE_FOR_X .................................. 1198
1.19.43. SIMULATION_VECTOR_COMPARE_RULE_FOR_Z .................................. 1199
1.19.44. SIM_BEHAVIOR_SIMULATION ............................................................. 1200
1.19.45. SIM_COMPILE_HDL_FILES ................................................................. 1201
1.19.46. SIM_HDL_TOP_MODULE_NAME ............................................................ 1202
1.19.47. SIM_OVERWRITE_WAVEFORM_INPUTS ............................................... 1203
1.19.48. SIM_TAP_REGISTER_D_Q_PORTS ....................................................... 1204
1.19.49. SIM_VECTOR_COMPARED_CLOCK_DUTY_CYCLE ................................ 1205
1.19.50. SIM_VECTOR_COMPARED_CLOCK_OFFSET .......................................... 1206
1.19.51. SIM_VECTOR_COMPARED_CLOCK_PERIOD ......................................... 1207
1.19.52. START_TIME ..................................................................................... 1208
1.19.53. TRIGGER_EQUATION ...................................................................... 1209
1.19.54. TRIGGER_VECTOR_COMPARE_ON_SIGNAL ......................................... 1210
1.19.55. USER_MESSAGE .............................................................................. 1211
1.19.56. VECTOR_COMPARE_TRIGGER_MODE ............................................... 1212
1.19.57. VECTOR_INPUT_SOURCE ................................................................. 1213
1.19.58. VECTOR_OUTPUT_DESTINATION ......................................................... 1214
1.19.59. VECTOR_OUTPUT_FORMAT ................................................................. 1215
1.19.60. X_ON_VIOLATION_OPTION ............................................................... 1216

1.1. Advanced I/O Timing Assignments

1.1.1. BOARD_MODEL_EBD_FAR_END

Specifies the far-end node to be used in the Electronic Board Description (EBD) path description.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_instance_assignment -name BOARD_MODEL_EBD_FAR_END -to <to> -entity <entity name> <value>
```
1.1.2. BOARD_MODEL_EBD_FILE_NAME

Specifies the Electronic Board Description (EBD) file that contains the path description for an I/O pin.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment supports wildcards.

The value of this assignment is case sensitive.

**Syntax**

```
set_instance_assignment -name BOARD_MODEL_EBD_FILE_NAME -to <to> -entity <entity name> <value>
```
1.1.3. BOARD_MODEL_EBD_SIGNAL_NAME

Specifies the Electronic Board Description (EBD) path description to be used with an I/O pin. You must specify the EBD file name.

Type

String

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Notes

The value of this assignment is case sensitive.

Syntax

```plaintext
set_instance_assignment -name BOARD_MODEL_EBD_SIGNAL_NAME -to <to> -entity <entity name> <value>
```
1.1.4. BOARD_MODEL_FAR_C

Specifies, in farads, the board trace model far capacitance.

Type
String

Device Support
- Intel® Agilex™
- Intel Arria® 10
- Intel Cyclone® 10 GX
- Intel Stratix® 10

Notes
This assignment supports wildcards.

Syntax

```bash
set_instance_assignment -name BOARD_MODEL_FAR_C -to <to> -entity <entity name> <value>
set_global_assignment -name BOARD_MODEL_FAR_C -section_id <section identifier> <value>
```
1.1.5. BOARD_MODEL_FAR_DIFFERENTIAL_R

Specifies, in ohms, the board trace model far differential resistance.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports wildcards.

**Syntax**

```
set_instance_assignment -name BOARD_MODEL_FAR_DIFFERENTIAL_R -to <to> -entity <entity name> <value>
set_global_assignment -name BOARD_MODEL_FAR_DIFFERENTIAL_R -section_id <section identifier> <value>
```
1.1.6. BOARD_MODEL_FAR_PULLDOWN_R

Specifies, in ohms, the board trace model far pull-down resistance.

Type
String

Device Support
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes
This assignment supports wildcards.

Syntax

```bash
set_instance_assignment -name BOARD_MODEL_FAR_PULLDOWN_R -to <to> -entity <entity name> <value>
set_global_assignment -name BOARD_MODEL_FAR_PULLDOWN_R -section_id <section identifier> <value>
```
1.1.7. BOARD_MODEL_FAR_PULLUP_R

Specifies, in ohms, the board trace model far pull-up resistance.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports wildcards.

**Syntax**

```
set_instance_assignment -name BOARD_MODEL_FAR_PULLUP_R -to <to> -entity <entity name> <value>
set_global_assignment -name BOARD_MODEL_FAR_PULLUP_R -section_id <section identifier> <value>
```
1.1.8. BOARD_MODEL_FAR_SERIES_R

Specifies, in ohms, the board trace model far series resistance.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports wildcards.

**Syntax**

```
set_instance_assignment -name BOARD_MODEL_FAR_SERIES_R -to <to> -entity <entity name> <value>
set_global_assignment -name BOARD_MODEL_FAR_SERIES_R -section_id <section identifier> <value>
```
1.1.9. BOARD_MODEL_NEAR_C

Specifies, in farads, the board trace model near capacitance.

Type
String

Device Support
• Intel Agilex
• Intel Arria 10
• Intel Cyclone 10 GX
• Intel Stratix 10

Notes
This assignment supports wildcards.

Syntax

```
set_instance_assignment -name BOARD_MODEL_NEAR_C -to <to> -entity <entity name> <value>
set_global_assignment -name BOARD_MODEL_NEAR_C -section_id <section identifier> <value>
```
1.1.10. BOARD_MODEL_NEAR_DIFFERENTIAL_R

Specifies, in ohms, the board trace model near differential resistance.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports wildcards.

**Syntax**

```
set_instance_assignment -name BOARD_MODEL_NEAR_DIFFERENTIAL_R -to <to> -entity <entity name> <value>
set_global_assignment -name BOARD_MODEL_NEAR_DIFFERENTIAL_R -section_id <section identifier> <value>
```
1.1.11. BOARD_MODEL_NEAR_PULLDOWN_R

Specifies, in ohms, the board trace model near pull-down resistance.

Type
String

Device Support
• Intel Agilex
• Intel Arria 10
• Intel Cyclone 10 GX
• Intel Stratix 10

Notes
This assignment supports wildcards.

Syntax

set_instance_assignment -name BOARD_MODEL_NEAR_PULLDOWN_R -to <to> -entity <entity name> <value>
set_global_assignment -name BOARD_MODEL_NEAR_PULLDOWN_R -section_id <section identifier> <value>
1.1.12. BOARD_MODEL_NEAR_PULLUP_R

Specifies, in ohms, the board trace model near pull-up resistance.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports wildcards.

**Syntax**

```plaintext
set_instance_assignment -name BOARD_MODEL_NEAR_PULLUP_R -to <to> -entity <entity name> <value>
set_global_assignment -name BOARD_MODEL_NEAR_PULLUP_R -section_id <section identifier> <value>
```
1.1.13. BOARD_MODEL_NEAR_SERIES_R

Specifies, in ohms, the board trace model near series resistance.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports wildcards.

**Syntax**

```
set_instance_assignment -name BOARD_MODEL_NEAR_SERIES_R -to <to> -entity <entity name> <value>
set_global_assignment -name BOARD_MODEL_NEAR_SERIES_R -section_id <section identifier> <value>
```
1.1.14. BOARD_MODEL_NEAR_TLINE_C_PER_LENGTH

Specifies, in farads/inch, the board trace model near transmission line distributed capacitance.

**Type**
String

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**
This assignment supports wildcards.

**Syntax**

```plaintext
set_instance_assignment -name BOARD_MODEL_NEAR_TLINE_C_PER_LENGTH -to <to> -entity <entity name> <value>
set_global_assignment -name BOARD_MODEL_NEAR_TLINE_C_PER_LENGTH -section_id <section identifier> <value>
```
1.1.15. BOARD_MODEL_NEAR_TLINE_LENGTH

Specifies, in inches, the board trace model near transmission line length.

Type
String

Device Support
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes
This assignment supports wildcards.

Syntax

```plaintext
set_instance_assignment -name BOARD_MODEL_NEAR_TLINE_LENGTH -to <to> -entity <entity name> <value>
set_global_assignment -name BOARD_MODEL_NEAR_TLINE_LENGTH -section_id <section identifier> <value>
```
1.1.16. BOARD_MODEL_NEAR_TLINE_L_PER_LENGTH

Specifies, in henrys/inch, the board trace model near transmission line distributed inductance.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports wildcards.

**Syntax**

```plaintext
set_instance_assignment -name BOARD_MODEL_NEAR_TLINE_L_PER_LENGTH -to <to> -entity <entity name> <value>
set_global_assignment -name BOARD_MODEL_NEAR_TLINE_L_PER_LENGTH -section_id <section identifier> <value>
```
1.1.17. BOARD_MODEL_TERMINATION_V

Specifies, in volts, the board trace model termination voltage.

**Type**
String

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**
This assignment supports wildcards.

**Syntax**

```plaintext
set_instance_assignment -name BOARD_MODEL_TERMINATION_V -to <to> -entity <entity name> <value>
set_global_assignment -name BOARD_MODEL_TERMINATION_V -section_id <section identifier> <value>
```
1.1.18. BOARD_MODEL_TLINE_C_PER_LENGTH

Specifies, in farads/inch, the board trace model far transmission line distributed capacitance.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports wildcards.

**Syntax**

```
set_instance_assignment -name BOARD_MODEL_TLINE_C_PER_LENGTH -to <to> -entity <entity name> <value>
set_global_assignment -name BOARD_MODEL_TLINE_C_PER_LENGTH -section_id <section identifier> <value>
```
1.1.19. BOARD_MODEL_TLINE_LENGTH

Specifies, in inches, the board trace model for transmission line length.

**Type**
String

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**
This assignment supports wildcards.

**Syntax**

```
set_instance_assignment -name BOARD_MODEL_TLINE_LENGTH -to <to> -entity <entity name> <value>
set_global_assignment -name BOARD_MODEL_TLINE_LENGTH -section_id <section identifier> <value>
```
1.1.20. BOARD_MODEL_TLINE_L_PER_LENGTH

Specifies, in henrys/inch, the board trace model for transmission line distributed inductance.

**Type**
String

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**
This assignment supports wildcards.

**Syntax**

```plaintext
set_instance_assignment -name BOARD_MODEL_TLINE_L_PER_LENGTH -to <to> -entity <entity name> <value>
set_global_assignment -name BOARD_MODEL_TLINE_L_PER_LENGTH -section_id <section identifier> <value>
```
1.1.21. OUTPUT_IO_TIMING_ENDPOINT

Specifies the node at which output I/O Timing ends.

**Type**

Enumeration

**Values**

- Far End
- Near End

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports wildcards.

**Syntax**

```
set_instance_assignment -name OUTPUT_IO_TIMING_ENDPOINT -to <to> -entity <entity name> <value>
set_global_assignment -name OUTPUT_IO_TIMING_ENDPOINT -entity <entity name> <value>
set_global_assignment -name OUTPUT_IO_TIMING_ENDPOINT <value>
```

**Default Value**

Near End
1.1.22. OUTPUT_IO_TIMING_FAR_END_VMEAS

Specifies, in volts, the measurement voltage at the far-end.

**Type**
String

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**
This assignment supports wildcards.

**Syntax**

```text
set_instance_assignment -name OUTPUT_IO_TIMING_FAR_END_VMEAS -to <to> -entity <entity name> <value>
set_global_assignment -name OUTPUT_IO_TIMING_FAR_END_VMEAS -section_id <section identifier> <value>
set_global_assignment -name OUTPUT_IO_TIMING_FAR_END_VMEAS <value>
```
1.1.23. OUTPUT_IO_TIMING_NEAR_END_VMEAS

Specifies, in volts, the measurement voltage at the near-end.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports wildcards.

**Syntax**

```
set_instance_assignment -name OUTPUT_IO_TIMING_NEAR_END_VMEAS -to <to> -entity <entity name> <value>
set_global_assignment -name OUTPUT_IO_TIMING_NEAR_END_VMEAS -section_id <section identifier> <value>
set_global_assignment -name OUTPUT_IO_TIMING_NEAR_END_VMEAS <value>
```
1.2. Analysis & Synthesis Assignments

1.2.1. ADV_NETLIST_OPT_ALLOWED

Specifies whether the Compiler should perform advanced netlist optimizations, such as gate-level retiming or physical synthesis, on the specified node or entity. If this option is set to 'Default', the Compiler duplicates, moves, or changes the synthesis of the node or entity, or allows register retiming during netlist optimization, only if doing so does not negatively affect the timing or performance of the design. If this option is set to 'Always Allow', the Compiler can alter the node or entity, even if doing so affects the timing or performance of the design. Intel does not recommend using this setting. If this option is set to 'Never Allow' the Compiler cannot alter the node or entity.

Type
Enumeration

Values
- Always Allow
- Default
- Never Allow

Device Support
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes
This assignment supports synthesis wildcards.

Syntax

```
set_global_assignment -name ADV_NETLIST_OPT_ALLOWED -entity <entity name> <value>
set_instance_assignment -name ADV_NETLIST_OPT_ALLOWED -to <to> -entity <entity name> <value>
```

Example

```
set_instance_assignment -name adv_netlist_opt_allowed "always allow" -to reg
```
1.2.2. ADV_NETLIST_OPT_SYNTH_WYSIWYG_REMAP

Specifies whether to perform WYSIWYG primitive resynthesis during synthesis. This option uses the setting specified in the Optimization Technique logic option.

Type
Boolean

Device Support
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes
This assignment is included in the Fitter report.
This assignment supports synthesis wildcards.

Syntax

```
set_global_assignment -name ADV_NETLIST_OPT_SYNTH_WYSIWYG_REMAP <value>
set_instance_assignment -name ADV_NETLIST_OPT_SYNTH_WYSIWYG_REMAP -to <to> -
entity <entity name> <value>
```

Default Value
Off

Example

```
set_global_assignment -name adv_netlist_opt_synth_wysiwyg_remap on
set_instance_assignment -name adv_netlist_opt_synth_wysiwyg_remap on -to foo
```

See Also
Optimization Technique
1.2.3. AGGRESSIVE_MUX_AREA_OPTIMIZATION

Performs aggressive area optimization on multiplexers.

**Type**

Enumeration

**Values**

- Auto
- Off
- On

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name AGGRESSIVE_MUX_AREA_OPTIMIZATION <value>
set_global_assignment -name AGGRESSIVE_MUX_AREA_OPTIMIZATION -entity <entity name> <value>
set_instance_assignment -name AGGRESSIVE_MUX_AREA_OPTIMIZATION -to <to> -entity <entity name> <value>
```

**Default Value**

Auto

**Example**

```
set_global_assignment -name aggressive_mux_area_optimization off
set_instance_assignment -name aggressive_mux_area_optimization on -to accel
```
1.2.4. ALLOW_ANY_RAM_SIZE_FOR_RECOGNITION

Allows the Compiler to infer RAMs of any size, even if they don't meet the current minimum requirements.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name ALLOW_ANY_RAM_SIZE_FOR_RECOGNITION <value>
set_global_assignment -name ALLOW_ANY_RAM_SIZE_FOR_RECOGNITION -entity <entity name> <value>
set_instance_assignment -name ALLOW_ANY_RAM_SIZE_FOR_RECOGNITION -to <to> -entity <entity name> <value>
```

**Default Value**

Off

**Example**

```
set_global_assignment -name allow_any_ram_size_for_recognition off
set_instance_assignment -name allow_any_ram_size_for_recognition off -to foo
```
1.2.5. ALLOW_ANY_ROM_SIZE_FOR_RECOGNITION

Allows the Compiler to infer ROMs of any size even if the ROMs do not meet the design's current minimum size requirements.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```plaintext
set_global_assignment -name ALLOW_ANY_ROM_SIZE_FOR_RECOGNITION <value>
set_global_assignment -name ALLOW_ANY_ROM_SIZE_FOR_RECOGNITION -entity <entity name> <value>
set_instance_assignment -name ALLOW_ANY_ROM_SIZE_FOR_RECOGNITION -to <to> -entity <entity name> <value>
```

**Default Value**

Off

**Example**

```plaintext
set_global_assignment -name allow_any_rom_size_for_recognition off
set_instance_assignment -name allow_any_rom_size_for_recognition off -to foo
```
1.2.6. ALLOW_ANY_SHIFT_REGISTER_SIZE_FOR_RECOGNITION

Allows the Compiler to infer shift registers of any size even if they do not meet the design's current minimum size requirements.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

- `set_global_assignment -name ALLOW_ANY_SHIFT_REGISTER_SIZE_FOR_RECOGNITION <value>`
- `set_global_assignment -name ALLOW_ANY_SHIFT_REGISTER_SIZE_FOR_RECOGNITION -entity <entity name> <value>`
- `set_instance_assignment -name ALLOW_ANY_SHIFT_REGISTER_SIZE_FOR_RECOGNITION -to <to> -entity <entity name> <value>`

**Default Value**

Off

**Example**

- `set_global_assignment -name allow_any_shift_register_size_for_recognition off`
- `set_instance_assignment -name allow_any_shift_register_size_for_recognition off -to foo`
1.2.7. ALLOW_CHILD_PARTITIONS

Specifies whether or not an instance or a section of design hierarchy can contain user partitions.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment supports synthesis wildcards.

**Syntax**

```bash
set_global_assignment -name ALLOW_CHILD_PARTITIONS -entity <entity name> <value>
set_instance_assignment -name ALLOW_CHILD_PARTITIONS -to <to> -entity <entity name> <value>
```

**Example**

```bash
set_global_assignment -name allow_child_partitions off
set_instance_assignment -name allow_child_partitions off -to "sub:inst"
```
1.2.8. ALLOW_POWER_UP_DONT_CARE

Causes registers that do not have a Power-Up Level logic option setting to power up with a don't care logic level (X). A don't care setting allows the Compiler to change the power-up level of a register to minimize the area of the design.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name ALLOW_POWER_UP_DONT_CARE <value>
```

**Default Value**

On

**Example**

```
set_global_assignment -name allow_power_up_dont_care off
```

**See Also**

Power-Up Level
1.2.9. ALLOW SHIFT REGISTER MERGING ACROSS HIERARCHIES

Allows the Compiler to take shift registers from different hierarchies of the design and put them in the same RAM.

**Type**

Enumeration

**Values**

- Always
- Auto
- Off

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name ALLOW_SHIFT_REGISTER_MERGING_ACROSS_HIERARCHIES <value>
set_global_assignment -name ALLOW_SHIFT_REGISTER_MERGING_ACROSS_HIERARCHIES -entity <entity name> <value>
set_instance_assignment -name ALLOW SHIFT REGISTER MERGING ACROSS HIERARCHIES -to <to> -entity <entity name> <value>
```

**Default Value**

Auto

**Example**

```
set_global_assignment -name allow_shift_register_merging_across_hierarchies off
set_instance_assignment -name allow_shift_register_merging_across_hierarchies -to foo
```

**See Also**

Auto Shift Register Replacement
1.2.10. ALLOW_SYNCH_CTRL_USAGE

Allows the Compiler to utilize synchronous clear and/or synchronous load signals in normal mode logic cells. Turning on this option helps to reduce the total number of logic cells used in the design, but might negatively impact the fitting since synchronous control signals are shared by all the logic cells in a LAB.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name ALLOW_SYNCH_CTRL_USAGE <value>
set_global_assignment -name ALLOW_SYNCH_CTRLUSAGE -entity <entity name> <value>
set_instance_assignment -name ALLOW_SYNCH_CTRL_USAGE -to <to> -entity <entity name> <value>
```

**Default Value**

On

**Example**

```
set_global_assignment -name allow_synch_ctrl_usage off
set_instance_assignment -name allow_synch_ctrl_usage off -to foo
```

**See Also**

Force Use of Synchronous Clear Signals
1.2.11. ALTERA_A10_IOPLL_BOOTSTRAP

Turns on the A10 IOPLL bootstrap fix

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```plaintext
set_global_assignment -name ALTERA_A10_IOPLL_BOOTSTRAP <value>
```
1.2.12. AUTO_CLOCK_ENABLE_RECOGNITION

Allows the Compiler to find logic that feeds a register and move the logic to the register's clock enable input port.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name AUTO_CLOCK_ENABLE_RECOGNITION <value>
set_global_assignment -name AUTO_CLOCK_ENABLE_RECOGNITION -entity <entity name> <value>
set_instance_assignment -name AUTO_CLOCK_ENABLE_RECOGNITION -to <to> -entity <entity name> <value>
```

**Default Value**

On

**Example**

```
set_global_assignment -name auto_clock_enable_replacement off
set_instance_assignment -name auto_clock_enable_replacement off -to reg
```
1.2.13. AUTO_DSP_RECOGNITION

Allows the Compiler to find a multiply-accumulate function or a multiply-add function that can be replaced with a DSP block.

Type

Boolean

Device Support

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

Syntax

```plaintext
set_global_assignment -name AUTO_DSP_RECOGNITION <value>
set_global_assignment -name AUTO_DSP_RECOGNITION -entity <entity name> <value>
set_instance_assignment -name AUTO_DSP_RECOGNITION -to <to> -entity <entity name> <value>
```

Default Value

On

Example

```plaintext
set_global_assignment -name auto_dsp_recognition off
set_instance_assignment -name auto_dsp_recognition off -to foo
```
1.2.14. AUTO_ENABLE_SMART_COMPILE

Specifies whether the Signal Tap Logic Analyzer should perform a smart compilation if conditions exist in which Signal Tap with incremental routing is used.

Type
Boolean

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```
set_global_assignment -name AUTO_ENABLE_SMART_COMPILE <value>
```
1.2.15. AUTO_OPEN_DRAIN_PINS

Allows the Compiler to automatically convert a tri-state buffer with a strong low data input into the equivalent open-drain buffer.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```plaintext
set_global_assignment -name AUTO_OPEN_DRAIN_PINS <value>
set_global_assignment -name AUTO_OPEN_DRAIN_PINS -entity <entity name> <value>
set_instance_assignment -name AUTO_OPEN_DRAIN_PINS -to <to> -entity <entity name> <value>
```

**Default Value**

On

**Example**

```plaintext
set_global_assignment -name auto_open_drain_pins off
set_instance_assignment -name auto_open_drain_pins off -to foo
```
1.2.16. AUTO_PARALLEL_SYNTHESIS

Option to enable/disable automatic parallel synthesis. This option can be used to speed up synthesis compile time by using multiple processors when available.

**Type**
Boolean

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**
This assignment is included in the Analysis & Synthesis report.

**Syntax**

```plaintext
set_global_assignment -name AUTO_PARALLEL_SYNTHESIS <value>
```

**Default Value**
On

**Example**

```plaintext
set_global_assignment -name auto_parallel_synthesis on
```
1.2.17. AUTO_RAM_RECOGNITION

 Allows the Compiler to find a set of registers and logic that can be replaced with the altsyncram or the lpm_ram_dp megafuction. Turning on this option may change the functionality of the design.

 Type
 Boolean

 Device Support
 • Intel Agilex
 • Intel Arria 10
 • Intel Cyclone 10 GX
 • Intel Stratix 10

 Notes
 This assignment is included in the Analysis & Synthesis report.
 This assignment supports synthesis wildcards.

 Syntax

 set_global_assignment -name AUTO_RAM_RECOGNITION <value>
 set_global_assignment -name AUTO_RAM_RECOGNITION -entity <entity name> <value>
 set_instance_assignment -name AUTO_RAM_RECOGNITION -to <to> -entity <entity name> <value>

 Default Value
 On

 Example

 set_global_assignment -name auto_ram_recognition off
 set_instance_assignment -name auto_ram_recognition off -to foo
1.2.18. AUTO_RESOURCE_SHARING

Allows the Compiler to share hardware resources among many similar, but mutually exclusive, operations in your HDL source code. If you enable this option, the Compiler will merge compatible addition, subtraction, and multiplication operations. By merging operations, this may reduce the area required by your design. Because resource sharing introduces extra muxing and control logic on each shared resource, it may negatively impact the final fmax of your design.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

<table>
<thead>
<tr>
<th>Syntax</th>
</tr>
</thead>
<tbody>
<tr>
<td>set_global_assignment -name AUTO_RESOURCE_SHARING &lt;value&gt;</td>
</tr>
<tr>
<td>set_global_assignment -name AUTO_RESOURCE_SHARING -entity &lt;entity name&gt; &lt;value&gt;</td>
</tr>
<tr>
<td>set_instance_assignment -name AUTO_RESOURCE_SHARING -to &lt;to&gt; -entity &lt;entity name&gt; &lt;value&gt;</td>
</tr>
</tbody>
</table>

**Default Value**

Off
1.2.19. AUTO_ROM_RECOGNITION

Allows the Compiler to find logic that can be replaced with the altsyncram or the lpm_rom megafuntion. Turning on this option may change the power-up state of the design.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name AUTO_ROM_RECOGNITION <value>
set_global_assignment -name AUTO_ROM_RECOGNITION -entity <entity name> <value>
set_instance_assignment -name AUTO_ROM_RECOGNITION -to <to> -entity <entity name> <value>
```

**Default Value**

On

**Example**

```
set_global_assignment -name auto_rom_recognition off
set_instance_assignment -name auto_rom_recognition off -to foo
```
1.2.20. AUTO_SHIFT_REGISTER_RECOGNITION

Allows the Compiler to find a group of shift registers of the same length that can be replaced with the altshift_taps megafunction. The shift registers must all use the same clock and clock enable signals, must not have any other secondary signals, and must have equally spaced taps that are at least three registers apart.

**Type**

Enumeration

**Values**

- Always
- Auto
- Off

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```plaintext
set_global_assignment -name AUTO_SHIFT_REGISTER_RECOGNITION <value>
set_global_assignment -name AUTO_SHIFT_REGISTER_RECOGNITION -entity <entity name> <value>
set_instance_assignment -name AUTO_SHIFT_REGISTER_RECOGNITION -to <to> -entity <entity name> <value>
```

**Default Value**

Auto

**Example**

```plaintext
set_global_assignment -name auto_shift_register_recognition off
set_instance_assignment -name auto_shift_register_recognition off -to foo
```
1.2.21. BARRELSHIFTER_CARRY_CHAIN_PACKING

Allows the Compiler to reduce the number of logic elements required by implementing barrelshifters in carry chains. This option repacks barrelshifters more efficiently for area, but may negatively affect timing. With the 'Auto' setting synthesis will make the trade-off between area and speed. Setting to 'Off' will disable this optimization, and setting to 'On' will enable it for all barrelshifters.

**Type**

Enumeration

**Values**

- Auto
- Off
- On

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```plaintext
set_global_assignment -name BARRELSHIFTER_CARRY_CHAIN_PACKING <value>
set_global_assignment -name BARRELSHIFTER_CARRY_CHAIN_PACKING -entity <entity name> <value>
set_instance_assignment -name BARRELSHIFTER_CARRY_CHAIN_PACKING -to <to> -entity <entity name> <value>
```

**Default Value**

Auto

**Example**

```plaintext
set_global_assignment -name barrelshifter_carry_chain_packing off
set_instance_assignment -name barrelshifter_carry_chain_packing on -to accel
```
1.2.22. BLOCK_DESIGN_NAMING

Specify the naming scheme used for the block design. This option is ignored if it is assigned to anything other than a design entity.

**Type**

Enumeration

**Values**

- Auto
- MaxPlusII
- QuartusII

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name BLOCK_DESIGN_NAMING -entity <entity name> <value>
set_instance_assignment -name BLOCK_DESIGN_NAMING -to <to> -entity <entity name> <value>
set_global_assignment -name BLOCK_DESIGN_NAMING <value>
```

**Default Value**

Auto

**Example**

```
set_global_assignment -name block_design_naming MaxPlusII
set_instance_assignment -name block_design_naming MaxPlusII -to top
```
1.2.23. BOARD

Specifies the board or development kit to use.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name BOARD <value>
```
1.2.24. DEVICE_FILTER_PACKAGE

Package filter for available devices.

Type
String

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
None

Syntax

```
set_global_assignment -name DEVICE_FILTER_PACKAGE <value>
```

Default Value

Any
1.2.25. DEVICE_FILTER_PIN_COUNT

Pin count filter for available devices.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
None

**Syntax**

```
set_global_assignment -name DEVICE_FILTER_PIN_COUNT <value>
```

**Default Value**
Any
1.2.26. DEVICE_FILTER_SPEED_GRADE

Speed grade filter for available devices.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name DEVICE_FILTER_SPEED_GRADE <value>
```

**Default Value**

Any
1.2.27. DEVICE_FILTER_VOLTAGE

Voltage filter for available devices.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```plaintext
set_global_assignment -name DEVICE_FILTER_VOLTAGE <value>
```
1.2.28. DISABLE_DSP_NEGATE_INFERENCING

Allow you to specify whether to use the negate port on an inferred DSP block.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```plaintext
set_global_assignment -name DISABLE_DSP_NEGATE_INFERENCING -entity <entity name> <value>
set_instance_assignment -name DISABLE_DSP_NEGATE_INFERENCING -to <to> -entity <entity name> <value>
set_global_assignment -name DISABLE_DSP_NEGATE_INFERENCING <value>
```

**Default Value**

Off

**Example**

```plaintext
set_global_assignment -name DISABLE_DSP_NEGATE_INFERENCING ON
set_instance_assignment -name DISABLE_DSP_NEGATE_INFERENCING OFF -to dps1
```
1.2.29. DISABLE_REGISTER_MERGING_ACROSS_HIERARCHIES

Specifies whether registers that are in different hierarchies are allowed to be merged if their inputs are the same.

**Type**

Enumeration

**Values**

- Auto
- Off
- On

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name DISABLE/Register_MERGING_ACROSS_HIERARCHIES <value>
```

**Default Value**

Auto
1.2.30. DISABLE_REGISTER_POWER_UP_INITIALIZATION

Specifies whether the Assembler generates a bit stream with register power-up initialization.

**Old Name**
DISABLE_REGISTER_POWERUP_INITIALIZATION

**Type**
Boolean

**Device Support**
- Intel Agilex
- Intel Stratix 10

**Notes**
This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name DISABLE_REGISTER_POWER_UP_INITIALIZATION <value>
```

**Default Value**
Off
1.2.31. DONT_MERGE_REGISTER

When set to On, this option prevents the specified register from merging with other registers, and prevents other registers from merging with the specified register.

Type

Boolean

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Notes

This assignment supports Fitter wildcards.
This assignment supports synthesis wildcards.

Syntax

```
set_global_assignment -name DONT_MERGE_REGISTER -entity <entity name> <value>
set_instance_assignment -name DONT_MERGE_REGISTER -to <to> -entity <entity name> <value>
```

Example

```
set_instance_assignment -name dont_merge_register on -to foo
```
1.2.32. DSE_SYNTH_EXTRA_EFFORT_MODE

Specifies the Design Space Explorer synthesis extra effort mode.

**Type**

Enumeration

**Values**

- MODE_1
- MODE_2
- MODE_3
- MODE_4
- MODE_5
- MODE_DEFAULT

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```shell
set_global_assignment -name DSE_SYNTH_EXTRA_EFFORT_MODE <value>
```
1.2.33. DSP_BLOCK_BALANCING

Allows you to control the conversion of certain DSP block slices during DSP block balancing.

**Type**

Enumeration

**Values**

- Auto
- DSP blocks
- Logic Elements
- Off
- Simple 18-bit Multipliers
- Simple Multipliers
- Width 18-bit Multipliers

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name DSP_BLOCK_BALANCING -entity <entity name> <value>
set_instance_assignment -name DSP_BLOCK_BALANCING -to <to> -entity <entity name> <value>
set_global_assignment -name DSP_BLOCK_BALANCING <value>
```

**Default Value**

Auto

**Example**

```
set_global_assignment -name dsp_block_balancing "dsp blocks"
set_instance_assignment -name dsp_block_balancing "logic elements" -to mult0
```
1.2.34. DUPLICATE_HIERARCHY_DEPTH

Pushes the last register and some number of registers that precede it in a chain of simple registers down the hierarchy tree of the modules it fans out to, creating a tree with duplicates for each instance at every level of the hierarchy. The registers in the chain must already be present in the design, with no logic in between them and no other fanins/fanouts between them. Value 0 to disable auto-duplication.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment supports Fitter wildcards.

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_instance_assignment -name DUPLICATE_HIERARCHY_DEPTH -to <to> -entity <entity name> <value>
```

**Example**

```
set_instance_assignment -name duplicate_hierarchy_depth -to last_reg_in_chain 2
```
1.2.35. EDA_DESIGN_ENTRY_SYNTHESIS_TOOL

Specifies the third-party EDA tool used for design entry/synthesis

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name EDA_DESIGN_ENTRY_SYNTHESIS_TOOL <value>
set_global_assignment -name EDA_DESIGN_ENTRY_SYNTHESIS_TOOL -entity <entity name> <value>
```

**Default Value**

<None>
1.2.36. EDA_INPUT_DATA_FORMAT

Specifies the format of the input data read from other EDA design entry/synthesis tools.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EDA_INPUT_DATA_FORMAT -section_id <section identifier> <value>
set_global_assignment -name EDA_INPUT_DATA_FORMAT -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

NONE, requires section identifier
1.2.37. EDA_INPUT_GND_NAME

Specifies the global high signal used in the files generated by the EDA synthesis tool, which is GND.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EDA_INPUT_GND_NAME -section_id <section identifier> <value>
set_global_assignment -name EDA_INPUT_GND_NAME -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

GND, requires section identifier
1.2.38. **EDA_INPUT_VCC_NAME**

Specifies the global power-down signal.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```plaintext
set_global_assignment -name EDA_INPUT_VCC_NAME -section_id <section identifier> <value>
set_global_assignment -name EDA_INPUT_VCC_NAME -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

VCC, requires section identifier
1.2.39. EDA_LMF_FILE

Specifies the default Library Mapping File (.lmf) for the current compilation.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_global_assignment -name EDA_LMF_FILE -section_id <section identifier> <value>
set_global_assignment -name EDA_LMF_FILE -entity <entity name> -section_id <section identifier> <value>
```
1.2.40. **EDA_RUN_TOOL_AUTOMATICALLY**

Runs the third-party EDA tool automatically from Quartus Prime when a design is compiled.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EDA_RUN_TOOL_AUTOMATICALLY -section_id <section identifier> <value>
set_global_assignment -name EDA_RUN_TOOL_AUTOMATICALLY -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

Off, requires section identifier
1.2.41. EDA_SHOW_LMF_MAPPING_MESSAGES

Determines whether to display messages describing the mappings used in the Library Mapping File.

Type

Boolean

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```
set_global_assignment -name EDA_SHOW_LMF_MAPPING_MESSAGES -section_id <section identifier> <value>
set_global_assignment -name EDA_SHOW_LMF_MAPPING_MESSAGES -entity <entity name> -section_id <section identifier> <value>
```

Default Value

Off, requires section identifier
1.2.42. EDA_VHDL_LIBRARY

Specifies the logical name of a user-defined VHDL design library: physical name.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```text
set_instance_assignment -name EDA_VHDL_LIBRARY -to <to> -section_id <section identifier> <value>
set_instance_assignment -name EDA_VHDL_LIBRARY -to <to> -entity <entity name> -section_id <section identifier> <value>
```
1.2.43. ENABLE_FORMAL_VERIFICATION

Allows the Compiler to write scripts that can be used to run OneSpin formal
verification tool. These are the only supported scripts used for formal verification.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```plaintext
set_global_assignment -name ENABLE_FORMAL_VERIFICATION <value>
```

**Default Value**

Off

**Example**

```plaintext
set_global_assignment -name enable_formal_verification on
```
1.2.44. ENABLE_FPGA_TAMPER_DETECTION

Enable FPGA tamper detection.

Type
Boolean

Device Support
- Intel Stratix 10

Notes
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name ENABLE_FPGA_TAMPER_DETECTION <value>
```

Default Value
Off

Example

```
set_global_assignment -name ENABLE_FPGA_TAMPER_DETECTION ON
```
1.2.45. ENABLE_STATE_MACHINE_INFERENCE

Allows the Compiler to infer state machines from Verilog/Vhdl Design Files. The Compiler optimizes state machines using special techniques to reduce area and/or improve performance. If set to Off, the Compiler extracts and optimizes state machines in Verilog/VHDL Design Files as regular logic.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name ENABLE_STATE_MACHINE_INFERENCE <value>
```

**Default Value**

On

**Example**

```
set_global_assignment -name enable_state_machine_inference on
```
1.2.46. ENABLE_SV_STATIC_ASSERTIONS

Evaluate SystemVerilog assertions using parameters and constants during synthesis.

Type
Boolean

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
This assignment is included in the Analysis & Synthesis report.

Syntax

set_global_assignment -name ENABLE_SV_STATIC_ASSERTIONS <value>

Default Value
Off

Example

set_global_assignment -name ENABLE_SV_STATIC_ASSERTIONS ON
1.2.47. ENABLE_VHDL_STATIC_ASSERTIONS

Evaluate VHDL assertions using generics and constants during synthesis.

Type
Boolean

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
This assignment is included in the Analysis & Synthesis report.

Syntax

```
set_global_assignment -name ENABLE_VHDL_STATIC_ASSERTIONS <value>
```

Default Value
Off

Example

```
set_global_assignment -name ENABLE_VHDL_STATIC_ASSERTIONS ON
```
1.2.48. FAMILY

Specifies the device family to use for compilation.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name FAMILY <value>
```

Default Value
Cyclone 10 GX
1.2.49. FORCE_CLOCK_ENABLE_INFERENCE

Directs the Compiler to aggressively infer clock enables on the specified registers. Turning on this option helps to infer clock enables on registers even the compiler would not have otherwise done so. It might negatively impact the fitting since the number of clock enable signals available in a LAB is limited.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment supports synthesis wildcards.

**Syntax**

```plaintext
set_global_assignment -name FORCE_CLOCK_ENABLE_INFERENCE -entity <entity name> <value>
set_instance_assignment -name FORCE_CLOCK_ENABLE_INFERENCE -to <to> -entity <entity name> <value>
```

**Example**

```plaintext
set_instance_assignment -name force_clock_enable_inference on -to foo
```

**See Also**

Allow Synchronous Control Signals
1.2.50. FORCE_SYNCH_CLEAR

Forces the Compiler to utilize synchronous clear signals in normal mode logic cells. Turning on this option helps to reduce the total number of logic cells used in the design, but might negatively impact the fitting since synchronous control signals are shared by all the logic cells in a LAB.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report. This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name FORCE_SYNCH_CLEAR <value>
set_global_assignment -name FORCE_SYNCH_CLEAR -entity <entity name> <value>
set_instance_assignment -name FORCE_SYNCH_CLEAR -to <to> -entity <entity name> <value>
```

**Default Value**

Off

**Example**

```
set_global_assignment -name force_synch_clear on
set_instance_assignment -name force_synch_clear on -to foo
```

**See Also**

Allow Synchronous Control Signals
1.2.5.1. FRACTAL_SYNTHESIS

Allows the Compiler to apply dense packing to arithmetic blocks, minimizing the area of the design.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```plaintext
set_global_assignment -name FRACTAL_SYNTHESIS <value>
set_global_assignment -name FRACTAL_SYNTHESIS -entity <entity name> <value>
set_instance_assignment -name FRACTAL_SYNTHESIS -to <to> -entity <entity name> <value>
```

**Default Value**

Off

**Example**

```plaintext
set_instance_assignment -name fractal_synthesis on -entity multiplier
```
1.2.52. HDLInicialFanoutLimit

Directs Integrated Synthesis to check the initial fan-out of each net in the netlist immediately after elaboration but prior to any netlist optimizations. If the fan-out for a net exceeds the specified limit, then Integrated Synthesis will issue a warning.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment supports synthesis wildcards.

**Syntax**

```plaintext
set_global_assignment -name HDLInicialFanoutLimit -entity <entity name> <value>
set_instance_assignment -name HDLInicialFanoutLimit -to <to> -entity <entity name> <value>
```

**Example**

```plaintext
set_instance_assignment -name hdl_initial_fanout_limit 100 -to foo
```
1.2.53. HDL_MESSAGE_LEVEL

Specifies the type of HDL messages you want to view, including messages that display processing errors in the HDL source code. 'Level1' allows you to view only the most important HDL messages. 'Level2' allows you to view most HDL messages, including warning and information based messages. 'Level3' allows you to view all HDL messages, including warning and information based messages and alerts about potential design problems or lint errors.

**Type**

Enumeration

**Values**

- Level1
- Level2
- Level3

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name HDL_MESSAGE_LEVEL <value>
```

**Default Value**

Level2
1.2.54. HDL_MESSAGE_OFF

Specifies the list of HDL message ids you want to turn off for this project.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**INTEGER_RANGE**

10000, 11000

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name HDL_MESSAGE_OFF <value>
```
1.2.55. HDL_MESSAGE_ON

Specifies the list of HDL message ids you want to turn on for this project.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**INTEGER_RANGE**

10000, 11000

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```bash
set_global_assignment -name HDL_MESSAGE_ON <value>
```
1.2.56. HPS_PARTITION

Specifies whether an entity or instance is a special-purpose partition that models the internals of the Hard Processor System (HPS).

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name HPS_PARTITION -entity <entity name> <value>
set_instance_assignment -name HPS_PARTITION -to <to> -entity <entity name> <value>
```

**Example**

```
set_instance_assignment -name hps_partition on -entity hps
```
1.2.57. IGNORE_GLOBAL_BUFFERS

Ignores GLOBAL buffers that are instantiated in the design. This option is ignored if it is applied to anything other than an individual GLOBAL buffer or a design entity containing GLOBAL buffers.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name IGNORE_GLOBAL_BUFFERS <value>
set_global_assignment -name IGNORE_GLOBAL_BUFFERS -entity <entity name> <value>
set_instance_assignment -name IGNORE_GLOBAL_BUFFERS -to <to> -entity <entity name> <value>
```

**Default Value**

Off
1.2.58. **IGNORE_LCELL_BUFFERS**

Ignores LCELL buffers that are instantiated in the design. This option is ignored if it is applied to anything other than an individual LCELL buffer or a design entity containing LCELL buffers.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name IGNORE_LCELL_BUFFERS <value>
set_global_assignment -name IGNORE_LCELL_BUFFERS -entity <entity name> <value>
set_instance_assignment -name IGNORE_LCELL_BUFFERS -to <to> -entity <entity name> <value>
```

**Default Value**

Off

**Example**

```
set_global_assignment -name ignore_lcell_buffers on
set_instance_assignment -name ignore_lcell_buffers on -to foo
```
1.2.59. IGNORE_MAX_FANOUT_ASSIGNMENTS

Directs the Compiler to ignore the Maximum Fan-Out Assignments on a node, an entity, or the whole design. One can remove the Maximum Fan-Out Assignments from the project but it is inconvenient/impossible as some assignments are embedded in the HDL sources.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name IGNORE_MAX_FANOUT_ASSIGNMENTS <value>
set_global_assignment -name IGNORE_MAX_FANOUT_ASSIGNMENTS -entity <entity name> <value>
set_instance_assignment -name IGNORE_MAX_FANOUT_ASSIGNMENTS -to <to> -entity <entity name> <value>
```

**Default Value**

Off
1.2.60. IGNORE_REGISTER_POWER_UP_INITIALIZATION

This allows the compiler to ignore the power-up condition of this register from what was specified in the RTL. Doing so gives more freedom to the tool to optimize this register, in particular for retiming.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name IGNORE_REGISTER_POWER_UP_INITIALIZATION -entity <entity name> <value>
set_instance_assignment -name IGNORE_REGISTER_POWER_UP_INITIALIZATION -to <to> -entity <entity name> <value>
```

**Example**

```
set_instance_assignment -name ignore_register_power_up_initialization on -to r
```
1.2.61. IGNORE_SOFT_BUFFERS

Ignores SOFT buffers that are instantiated in the design. This option is ignored if it is applied to anything other than an individual SOFT buffer or a design entity containing SOFT buffers.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```plaintext
set_global_assignment -name IGNORE_SOFT_BUFFERS <value>
set_global_assignment -name IGNORE_SOFT_BUFFERS -entity <entity name> <value>
set_instance_assignment -name IGNORE_SOFT_BUFFERS -to <to> -entity <entity name> <value>
```

**Default Value**

On

**Example**

```plaintext
set_global_assignment -name ignore_softBuffers off
set_instance_assignment -name ignore_softBuffers off -to foo
```
1.2.62. **IGNORE_TRANSLATE_OFF_AND_SYNTHESIS_OFF**

Instructs Analysis & Synthesis to ignore all translate_off/synthesis_off synthesis directives in your Verilog and VHDL design files. You can use this option to disable these synthesis directives and include previously ignored code during elaboration.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name IGNORE_TRANSLATE_OFF_AND_SYNTHESIS_OFF <value>
```

**Default Value**

Off

**Example**

```
set_global_assignment -name ignore_translate_off_and_synthesis_off on
```
1.2.63. IMPLEMENT_AS_CLOCK_ENABLE

Specifies that this node should function as a clock enable signal for one or more registers.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_instance_assignment -name IMPLEMENT_AS_CLOCK_ENABLE -to <to> -entity <entity name> <value>
```
1.2.64. IMPLEMENT_AS_OUTPUT_OF_LOGIC_CELL

Implements the output of a primitive in a logic cell. You can apply this option to a logic function that would not ordinarily be implemented in a logic cell, typically a combinatorial function such as an AND2 gate. Implementing the output of a primitive a logic cell makes it possible to observe its output in simulation and timing analysis. However, because an additional logic cell is used, overall device utilization will increase. This option does not insert an additional logic cell on a function that is already implemented in a logic cell, such as a flipflop. This option is ignored if it is applied to anything other than a primitive.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_instance_assignment -name IMPLEMENT_AS_OUTPUT_OF_LOGIC_CELL -to <to> -entity <entity name> <value>
```

**Example**

```
set_instance_assignment -name implement_as_output_of_logic_cell on -to foo
```
1.2.65. INFER_RAMS_FROM_RAW_LOGIC

Instructs the Compiler to infer RAM from registers and multiplexers. Some HDL patterns that differ from Intel FPGA RAM templates are initially converted into logic. However, these structures function as RAM and, because of that, the Compiler may create an altsyncram megafunction instance for them at a later stage when this assignment is on. With this assignment is turned on, the Compiler may use more device RAM resources and less LABs.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name INFER_RAMS_FROM_RAW_LOGIC <value>
set_global_assignment -name INFER_RAMS_FROM_RAW_LOGIC -entity <entity name> <value>
set_instance_assignment -name INFER_RAMS_FROM_RAW_LOGIC -to <to> -entity <entity name> <value>
```

**Default Value**

On

**Example**

```
set_global_assignment -name infer_rams_from_raw_logic off
set_instance_assignment -name infer_rams_from_raw_logic off -to foo
```
1.2.66. IP_SEARCH_PATHS

Specifies the IP search paths specific to the project.

Type

String

Device Support

• This setting can be used in projects targeting any Intel FPGA device family.

Notes

The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name IP_SEARCH_PATHS <value>
```
1.2.67. MAX_BALANCING_DSP_BLOCKS

Allows you to specify the maximum number of DSP blocks that the DSP block balancer will assume exist in the current device for each partition. This option overrides the usual method of using the maximum number of DSP blocks the current device supports.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name MAX_BALANCING_DSP_BLOCKS <value>
set_instance_assignment -name MAX_BALANCING_DSP_BLOCKS -to <to> -entity <entity name> <value>
```

**Default Value**

-1 (Unlimited)

**Example**

```
set_global_assignment -name max_balancing_dsp_blocks 4
set_instance_assignment -name max_balancing_dsp -to "my_partition_root_entity:my_partition_root_entity_inst"
```
1.2.68. **MAX_FANOUT**

Directs the Compiler to control the number of destinations the specified node feeds so the fan-out count does not exceed the value specified as the maximum number of fan-out allowed from the node.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name MAX_FANOUT -entity <entity name> <value>
set_instance_assignment -name MAX_FANOUT -to <to> -entity <entity name> <value>
```

**Example**

```
set_instance_assignment -name max_fanout 10 -to foo
```
1.2.69. MAX_FANOUT_FOR_SYNCH_CTRL

Directs the Compiler to limit the fanout of logic cells that feed clock enable or synchronous clear signal on the specified register. The logic cell will be duplicated if the fanout is higher than the number specified.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name MAX_FANOUT_FOR_SYNCH_CTRL -entity <entity name> <value>
set_instance_assignment -name MAX_FANOUT_FOR_SYNCH_CTRL -to <to> -entity <entity name> <value>
```

**Example**

```
set_instance_assignment -name max_fanout_for_synch_ctrl 10 -to foo
```
1.2.70. MAX_LABS

Allows you to specify the maximum number of LABs that Analysis & Synthesis should try to utilize for a device. This option overrides the usual method of using the maximum number of LABs the current device supports, when the value is non-negative and is less than the maximum number of LABs available on the current device.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```bash
set_global_assignment -name MAX_LABS <value>
set_instance_assignment -name MAX_LABS -to <to> -entity <entity name> <value>
```

**Default Value**

-1 (Unlimited)

**Example**

```bash
set_global_assignment -name max_labs 100
```
1.2.71. MAX_NUMBER_OF_REGISTERS_FROM_UNINFERRED_RAMS

Allows you to specify the maximum number of registers that Analysis & Synthesis can use for conversion of uninferred RAMs. You can use this option as a project-wide option or on a specific partition by setting the assignment on the instance name of the partition root. The assignment on a partition overrides the global assignment (if any) for that particular partition. This option prevents synthesis from causing long compilations and running out of memory when many registers are used for uninferred RAMs. Instead of continuing the compilation, the Quartus Prime software issues an error and exits.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name MAX_NUMBER_OF_REGISTERS_FROM_UNINFERRED_RAMS <value>
set_instance_assignment -name MAX_NUMBER_OF_REGISTERS_FROM_UNINFERRED_RAMS -to <to> -entity <entity name> <value>
```

**Default Value**

-1 (Unlimited)

**Example**

```
set_global_assignment -name max_number_of_registers_from_uninferred_rams 2048
```
1.2.72. MAX_RAM_BLOCKS_M4K

Allows you to specify the maximum number of M4K, M9K, M20K, or M10K memory blocks that the Compiler may use for a device. This option overrides the usual method of using the maximum number of M4K, M9K, M20K, or M10K memory blocks the current device supports, when the value is non-negative and is less than the maximum number of M4K, M9K, M20K, or M10K memory blocks available on the current device.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name MAX_RAM_BLOCKS_M4K <value>
set_instance_assignment -name MAX_RAM_BLOCKS_M4K -to <to> -entity <entity name> <value>
```

**Default Value**

-1 (Unlimited)

**Example**

```
set_global_assignment -name max_ram_blocks_m4k 4
```

**See Also**

- Maximum Number of M512 Memory Blocks
- Maximum Number of M-RAM Memory Blocks
1.2.73. MLAB_ADD_TIMING_CONSTRAINTS_FOR_MIXED_PORT_FEED_THROUGH_MODE_SETTING_DONT_CARE

Allows you to specify whether you want the Timing Analyzer to evaluate timing constraints between the write and the read operation of the MLAB memory block. Performing a write and read operation simultaneously at the same address might result in metastability because no timing constraints between those operations exist by default. Turning on this option introduces timing constraints between the write and read operation on the MLAB memory block and thereby avoids metastability issues; however, turning on this option degrades the performance of the MLAB memory blocks. If your design does not perform write and read operations simultaneously at the same address you do not need to set this option.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

This assignment supports synthesis wildcards.

**Syntax**

```plaintext
set_global_assignment -name MLAB_ADD_TIMING_CONSTRAINTS_FOR_MIXED_PORT_FEED_THROUGH_MODE_SETTING_DONT_CARE -entity <entity name> <value>
set_instance_assignment -name MLAB_ADD_TIMING_CONSTRAINTS_FOR_MIXED_PORT_FEED_THROUGH_MODE_SETTING_DONT_CARE -to <to> -entity <entity name> <value>
set_global_assignment -name MLAB_ADD_TIMING_CONSTRAINTS_FOR_MIXED_PORT_FEED_THROUGH_MODE_SETTING_DONT_CARE <value>
```

**Default Value**

Off
1.2.74. MUX_RESTRUCTURE

Allows the Compiler to reduce the number of logic elements required to implement multiplexers in a design. This option is useful if your design contains buses of fragmented multiplexers. This option repacks multiplexers more efficiently for area, allowing the design to implement multiplexers with a reduced number of logic elements. You can select the 'On' setting to minimize your design area; it will decrease logic element usage but may negatively affect design clock speed (fMAX). You can select the 'Off' to disable multiplexer restructuring; it does not decrease logic element usage and does not affect design clock speed (fMAX). You may select 'Auto' setting to allow the Quartus Prime software to determine whether multiplexer restructuring should be enabled. The Quartus Prime software uses other synthesis settings, for example, the Optimization Technique option, to determine if multiplexer restructuring should be applied to the design; the 'Auto' setting will decrease logic element usage but may negatively affect design clock speed (fMAX).

**Type**

Enumeration

**Values**

- Auto
- Off
- On

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name MUX_RESTRUCTURE <value>
set_global_assignment -name MUX_RESTRUCTURE -entity <entity name> <value>
set_instance_assignment -name MUX_RESTRUCTURE -to <to> -entity <entity name> <value>
```

**Default Value**

Auto

**Example**

```
set_global_assignment -name mux_restructure off
set_instance_assignment -name mux_restructure on -to accel
```
1.2.75. NOT_GATE_PUSH_BACK

Allows the Compiler to push an inversion (that is, a NOT gate) back through a register and implement it on that register's data input if it is necessary to implement the design. If this option is turned on, a register may power up to an active-high state, so it may need to be explicitly cleared during initial operation of the device. This option is ignored if it is applied to anything other than an individual register or a design entity containing registers. If it is applied to an output pin that is directly fed by a register, it is automatically transferred to that register.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```plaintext
set_global_assignment -name NOT_GATE_PUSH_BACK -entity <entity name> <value>
set_instance_assignment -name NOT_GATE_PUSH_BACK -to <to> -entity <entity name> <value>
set_global_assignment -name NOT_GATE_PUSH_BACK <value>
```

**Default Value**

On

**Example**

```plaintext
set_global_assignment -name not_gate_push_back off
set_instance_assignment -name not_gate_push_back off -to reg
```
1.2.76. NUMBER_OF_INVERTED_REGISTERS_REPORTED

Allows you to specify the maximum number of inverted registers that the Synthesis Report should display.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name NUMBER_OF_INVERTED_REGISTERS_REPORTED <value>
```

**Default Value**

100

**Example**

```
set_global_assignment -name NUMBER_OF_INVERTED_REGISTERS_REPORTED 200
```
1.2.77. NUMBER_OF_PROTECTED_REGISTERS_REPORTED

Allows you to specify the maximum number of protected registers that the Synthesis Report should display.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```plaintext
set_global_assignment -name NUMBER_OF_PROTECTED_REGISTERS_REPORTED <value>
```

**Default Value**

100

**Example**

```plaintext
set_global_assignment -name NUMBER_OF_PROTECTED_REGISTERS_REPORTED 200
```
1.2.78. NUMBER_OF_REMOVED_REGISTERS_REPORTED

Allows you to specify the maximum number of removed registers that the Synthesis Report should display.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```plaintext
set_global_assignment -name NUMBER_OF_REMOVED_REGISTERS_REPORTED <value>
```

**Default Value**

5000

**Example**

```plaintext
set_global_assignment -name NUMBER_OF_REMOVED_REGISTERS_REPORTED 200
```
1.2.79. NUMBER_OF_SWEPT_NODES_REPORTED

Allows you to specify the maximum number of swept nodes that the Synthesis Report displays. A swept node is any node which was eliminated from your design because the Quartus Prime software found the node to be unnecessary.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```bash
set_global_assignment -name NUMBER_OF_SWEPT_NODES_REPORTED <value>
```

**Default Value**

5000

**Example**

```bash
set_global_assignment -name NUMBER_OF_SWEPT_NODES_REPORTED 200
```
1.2.80. OCP_HW_EVAL

Enables or disables Intel FPGA IP Evaluation Mode feature.

**Type**
Enumeration

**Values**
- Disable
- Enable

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name OCP_HW_EVAL <value>
```

**Default Value**
Enable
1.2.81. OPTIMIZATION_TECHNIQUE

Specifies the overall optimization goal for Analysis & Synthesis: attempt to maximize performance, minimize logic usage, or balance high performance with minimal logic usage.

**Old Name**
Optimization Technique -- Stratix IV

**Type**
Enumeration

**Values**
- Area
- Balanced
- Speed

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**
This assignment is included in the Analysis & Synthesis report.
This assignment supports synthesis wildcards.

**Syntax**

```plaintext
set_global_assignment -name OPTIMIZATION_TECHNIQUE <value>
set_global_assignment -name OPTIMIZATION_TECHNIQUE -entity <entity name> <value>
set_instance_assignment -name OPTIMIZATION_TECHNIQUE -to <to> -entity <entity name> <value>
```

**Default Value**
Balanced

**Example**

```plaintext
set_global_assignment -name optimization_technique speed
```
1.2.82. OPTIMIZE_POWER_DURING_SYNTHESIS

Controls the power-driven compilation setting of Analysis & Synthesis. This option determines how aggressively Analysis & Synthesis optimizes the design for power. If this option is set to 'Off', Analysis & Synthesis does not perform any power optimizations. If this option is set to 'Normal compilation', Analysis & Synthesis performs power optimizations as long as they are not expected to reduce design performance. When this option is set to 'Extra effort', Analysis & Synthesis will perform additional power optimizations which may reduce design performance.

Type

Enumeration

Values

- Extra effort
- Normal compilation
- Off

Device Support

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes

This assignment is included in the Fitter report.

This assignment supports synthesis wildcards.

Syntax

```
set_global_assignment -name OPTIMIZE_POWER_DURING_SYNTHESIS <value>
set_global_assignment -name OPTIMIZE_POWER_DURING_SYNTHESIS -entity <entity name> <value>
set_instance_assignment -name OPTIMIZE_POWER_DURING_SYNTHESIS -to <to> -entity <entity name> <value>
```

Default Value

Normal compilation

Example

```
set_global_assignment -name optimize_power_during_synthesis off
```
1.2.83. PARAMETER

Assigns an attribute that determines the logic created or used to implement the function, for example, the width of a bus. Parameters are characteristics that determine the size, behavior, or silicon implementation of a function. Parameter values are inherited from project defaults or higher hierarchical levels unless you make explicit assignments to individual nodes. Parameters are also overridden by explicit logic synthesis and fitting options.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_parameter <value>
set_parameter -entity <entity name> <value>
```
1.2.84. PHYSICAL_SHIFT_REGISTER_INFERENCE

Allows the Compiler perform placement-driven shift register inference it in Fitter instead of performing shift register inference in Synthesis.

Type
Boolean

Device Support
- Intel Agilex
- Intel Stratix 10

Notes
This assignment is included in the Analysis & Synthesis report.

Syntax

set_global_assignment -name PHYSICAL_SHIFT_REGISTER_INFERENCE <value>

Example

set_global_assignment -name physical_shift_register_inference off
1.2.85. POWER_UP_LEVEL

Causes a register to power up with the specified logic level, either High (1) or Low (0). If this option is specified for an input pin, it is automatically transferred to the register that is driven by the pin if the following conditions are present: (1) there is no intervening logic, other than inversion, between the pin and the register; (2) the input pin drives the data input of the register; and (3) the input pin does not fan-out to any other logic. If this option is specified for an output or bidirectional pin, it is automatically transferred to the register that feeds the pin if: (1) there is no intervening logic, other than inversion, between the register and the pin; and (2) the register does not fan-out to any other logic. You can assign this option to any register, or to a pin with any logic configuration other than those described above. You can also assign this option to a design entity containing registers if you want to set the power level for all registers in the design entity. In order for the register to power up with the specified logic level, the Compiler may perform NOT Gate Push-Back on the register.

Type

Enumeration

Values

• High
• Low

Device Support

• This setting can be used in projects targeting any Intel FPGA device family.

Notes

This assignment supports synthesis wildcards.

Syntax

```
set_global_assignment -name POWER_UP_LEVEL -entity <entity name> <value>
set_instance_assignment -name POWER_UP_LEVEL -to <to> -entity <entity name> <value>
```

Example

```
set_instance_assignment -name power_up_level low -to foo
```

See Also

Power-Up Don't Care
1.2.86. PRESERVE_FANOUT_FREE_NODE

Prevents a register that has no fan-out from being removed during synthesis.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_instance_assignment -name PRESERVE_FANOUT_FREE_NODE -to <to> -entity <entity name> <value>
```

**Example**

```
set_instance_assignment -name preserve_fanout_free_node on -to reg
```
1.2.87. PRESERVE_FANOUT_FREE_WYSIWYG

Prevents a user-instantiated wysiwyg or primitive from being removed when it has no fanout.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```plaintext
set_global_assignment -name PRESERVE_FANOUT_FREE_WYSIWYG -entity <entity name> <value>
set_instance_assignment -name PRESERVE_FANOUT_FREE_WYSIWYG -to <to> -entity <entity name> <value>
```

**Example**

```plaintext
set_instance_assignment -name preserve_fanout_free_wysiwyg on -to wys
```
1.2.88. PRESERVE_REGISTER

Prevents a register from minimizing away during synthesis and prevents sequential netlist optimizations. Sequential netlist optimizations can eliminate redundant registers and registers with constant drivers.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment supports Fitter wildcards.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name PRESERVE_REGISTER -entity <entity name> <value>
set_instance_assignment -name PRESERVE_REGISTER -to <to> -entity <entity name> <value>
```

**Example**

```
set_instance_assignment -name preserve_register on -to foo
```
1.2.89. PRESERVE_REGISTER_SYN_ONLY

Prevents a register from minimizing away during synthesis. This does not affect retiming or other optimizations in the fitter.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment supports Fitter wildcards.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name PRESERVE_REGISTER_SYN_ONLY -entity <entity name> <value>
set_instance_assignment -name PRESERVE_REGISTER_SYN_ONLY -to <to> -entity <entity name> <value>
```

**Example**

```
set_instance_assignment -name preserve_register_syn_only on -to foo
```
### 1.2.90. PRPOF_ID

Specifies whether a register is a unique partial reconfiguration bitstream identifier. The same identifier value will be used to generate the partial reconfiguration bitstream.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

This assignment supports synthesis wildcards.

**Syntax**

- `set_global_assignment -name PRPOF_ID -entity <entity name> <value>`
- `set_instance_assignment -name PRPOF_ID -to <to> -entity <entity name> <value>`
- `set_global_assignment -name PRPOF_ID <value>`

**Default Value**

Off

**Example**

- `set_instance_assignment -name prpof_id on -to reg`
1.2.91. QUICK_ELAB_TILE_IP

Specifies that an entity is to be reported as a tile IP by the quick elaboration flow. The string value represents the tile type.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name QUICK_ELAB_TILE_IP -entity <entity name> <value>
set_instance_assignment -name QUICK_ELAB_TILE_IP -to <to> -entity <entity name> <value>
```
1.2.92. RAMSTYLE_ATTRIBUTE

Sets the ramstyle attribute of a shift register, RAM, or ROM.

**Type**

Enumeration

**Values**

- M10K
- M144K
- M20K
- M4K
- M512
- M9K
- MEGARAM
- MLAB
- auto
- logic

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name RAMSTYLE_ATTRIBUTE -entity <entity name> <value>
set_instance_assignment -name RAMSTYLE_ATTRIBUTE -to <to> -entity <entity name> <value>
```

**Example**

```
set_instance_assignment -name ramstyle_attribute M512 -to foo
```
1.2.93. RBCGEN_CRITICAL_WARNING_TO_ERROR

To convert Quartus Prime critical warning to error.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

None

**Syntax**

```
set_global_assignment -name RBCGEN_CRITICAL_WARNING_TO_ERROR <value>
```

**Default Value**

On
1.2.94. REMOVE_DUPLICATE_REGISTERS

Removes a register if it is identical to another register. If two registers generate the same logic, the second one will be deleted and the first one will be made to fan out to the second one’s destinations. Also, if the deleted register has different logic option assignments, they will be ignored. This option is useful if you wish to prevent the Compiler from removing duplicate registers that you have used deliberately. You can do this by setting the option to Off. This option is ignored if it is applied to anything other than an individual register or a design entity containing registers.

Old Name

DUPLICATE_REGISTER_EXTRACTION

Type

Boolean

Device Support

• This setting can be used in projects targeting any Intel FPGA device family.

Notes

This assignment supports Fitter wildcards.

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

Syntax

```
set_global_assignment -name REMOVE_DUPLICATE_REGISTERS <value>
set_global_assignment -name REMOVE_DUPLICATE_REGISTERS -entity <entity name> <value>
set_instance_assignment -name REMOVE_DUPLICATE_REGISTERS -to <to> -entity <entity name> <value>
```

Default Value

On

Example

```
set_global_assignment -name remove_duplicate_registers off
set_instance_assignment -name remove_duplicate_registers off -to foo
```
1.2.95. REMOVE_REDUNDANT_LOGIC_CELLS

Removes redundant LCELL primitives or WYSIWYG primitives. Turning this option on optimizes a circuit for area and speed. This option is ignored if it is applied to anything other than a design entity.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name REMOVE_REDUNDANT_LOGIC_CELLS -entity <entity name> <value>
set_instance_assignment -name REMOVE_REDUNDANT_LOGIC_CELLS -to <to> -entity <entity name> <value>
set_global_assignment -name REMOVE_REDUNDANT_LOGIC_CELLS <value>
```

**Default Value**

Off

**Example**

```
set_global_assignment -name remove_redundant_logic_cells on
set_instance_assignment -name remove_redundant_logic_cells on -to node
```
1.2.96. REPORT_ENTITY_UTILIZATION_TO_ASCII_PRO

Specifies whether panels of Resource Utilization by Entity for each partition should be printed to the ascii version of the synthesis report.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name REPORT_ENTITY_UTILIZATION_TO_ASCII_PRO <value>
```

**Default Value**

On
1.2.97. REPORT_PARAMETER_SETTINGS_PRO

Specifies whether the synthesis report should include the panels in the Parameter Settings by Entity Instance folder

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
This assignment is included in the Analysis & Synthesis report.

**Syntax**
```
set_global_assignment -name REPORT_PARAMETER_SETTINGS_PRO <value>
```

**Default Value**
On
1.2.98. REPORT_PARAMETER_SETTINGS_TO_ASCII_PRO

Specifies whether the Parameter Settings by Entity Instance folder should be printed to the ascii version of the synthesis report.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name REPORT_PARAMETER_SETTINGS_TO_ASCII_PRO <value>
```

**Default Value**

On
1.2.99. REPORT_PR_INITIAL_VALUES_AS_ERROR

Allows you to flag explicitly defined initial values found in PR partitions as Errors instead of Warnings.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name REPORT_PR_INITIAL_VALUES_AS_ERROR <value>
```

**Default Value**
Off

**Example**

```
set_global_assignment -name REPORT_PR_INITIAL_VALUES_AS_ERROR ON
```
1.2.100. REPORT_SOURCE_ASSIGNMENTS_PRO

Specifies whether the synthesis report should include the panels in the Source Assignments folder

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name REPORT_SOURCE_ASSIGNMENTS_PRO <value>
```

**Default Value**

On
1.2.101. REPORT_SOURCE_ASSIGNMENTS_TO_ASCII_PRO

Specifies whether the Source Assignments folder should be printed to the ascii version of the synthesis report.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name REPORT_SOURCE_ASSIGNMENTS_TO_ASCII_PRO <value>
```

**Default Value**

On
1.2.102. RESYNTHESIS_OPTIMIZATION_EFFORT

Specifies whether the resynthesis tool should focus on fmax or area during resynthesis.

Type
Enumeration

Values
- Low
- Normal

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name RESYNTHESIS_OPTIMIZATION_EFFORT -section_id <section identifier> <value>
set_global_assignment -name RESYNTHESIS_OPTIMIZATION_EFFORT -entity <entity name> -section_id <section identifier> <value>
```

Default Value
Normal, requires section identifier
1.2.103. RESYNTHESIS_PHYSICAL_SYNTHESIS

Specifies the physical synthesis level for resynthesis.

**Type**

Enumeration

**Values**

- ADVANCED
- Normal

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name RESYNTHESIS_PHYSICAL_SYNTHESIS -section_id <section identifier> <value>
set_global_assignment -name RESYNTHESIS_PHYSICAL_SYNTHESIS -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

Normal, requires section identifier
1.2.104. RESYNTHESIS_RETIMING

Specifies the paths on which retiming will be performed: all paths, register-to-register paths only, or none.

**Type**

Enumeration

**Values**

- CORE
- Full
- Off

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name RESYNTHESIS_RETIMING -section_id <section identifier> <value>
set_global_assignment -name RESYNTHESIS_RETIMING -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

FULL, requires section identifier
1.2.105. SAFE_STATE_MACHINE

Tells the compiler to implement state machines that can recover gracefully from an illegal state.

**Type**

Enumeration

**Values**

- Auto
- Never
- On

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name SAFE_STATEemachine -entity <entity name> <value>
set_instance_assignment -name SAFE_STATEemachine -to <to> -entity <entity name> <value>
set_global_assignment -name SAFE_STATEemachine <value>
```

**Default Value**

Auto

**Example**

```
set_global_assignment -name safe_state_machine on
set_instance_assignment -name safe_state_machine on -to foo
```

**See Also**

State Machine Processing Extract Verilog State Machines Extract VHDL State Machines
1.2.106. SAVE_DISK_SPACE

Saves disk space by reducing the number of node names available for entering assignments, simulation, timing analysis, reporting, etc.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name SAVE_DISK_SPACE <value>
```

**Default Value**

On
1.2.107. SEARCH_PATH

Specifies the path name of a user-defined library.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name SEARCH_PATH <value>
```
1.2.108. SECONDARY_TOP_LEVEL_ENTITY

Specifies the name of an entity that needs to be considered as top-level entity for analysis and elaboration but is not the main top-level entity.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive. This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name SECONDARY_TOP_LEVEL_ENTITY <value>
```
1.2.109. SHIFT_REGISTER_RECOGNITION_ACLR_SIGNAL

Allows the Compiler to find a group of shift registers of the same length that can be replaced with the altshift_taps megafunction. The shift registers must all use the same aclr signals, must not have any other secondary signals, and must have equally spaced taps that are at least three registers apart. To use this option, you must turn on the Auto Shift Register Replacement logic option.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name SHIFT_REGISTER_RECOGNITION_ACLR_SIGNAL <value>
set_global_assignment -name SHIFT_REGISTER_RECOGNITION_ACLR_SIGNAL -entity <entity name> <value>
set_instance_assignment -name SHIFT_REGISTER_RECOGNITION_ACLR_SIGNAL -to <to> -entity <entity name> <value>
```

**Default Value**

On

**Example**

```
set_global_assignment -name shift_register_recognition_aclr_signal off
set_instance_assignment -name shift_register_recognition_aclr_signal off -to foo
```
1.2.110. SIZE_OF_IGNORED_POWER_UP_REPORT

Allows you to specify the maximum number of registers with ignored power-up settings reported in synthesis report.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name SIZE_OF_IGNORED_POWER_UP_REPORT <value>
```

**Default Value**

500

**Example**

```
set_global_assignment -name SIZE_OF_IGNORED_POWER_UP_REPORT 200
```
1.2.111. SIZE_OF_LATCH_REPORT

Allows you to specify the maximum number of latches that the Synthesis Report should display.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name SIZE_OF_LATCH_REPORT <value>
```

**Default Value**

100

**Example**

```
set_global_assignment -name SIZE_OF_LATCH_REPORT 200
```
1.2.112. SIZE_OF_PRInicial CONDITIONS_REPORT

Allows you to specify the maximum number of registers that the PR Initial Conditions Report should display.

**Type**
Integer

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name SIZE_OF_PR_INITIAL_CONDITIONS_REPORT <value>
```

**Default Value**
100

**Example**

```
set_global_assignment -name SIZE_OF_PR_INITIAL_CONDITIONS_REPORT 200
```
1.2.113. SMART_COMPILE_IGNORES_TDC_FOR_STRATIX_PLL_CHANGES

Allows the Compiler to skip the fitting stage during smart recompilation when design changes may affect timing requirements. This option is available only for changes to Cyclone, Stratix, and Stratix GX PLL parameters, and Stratix GX gigabit transceiver block (GXB) parameters.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name SMART_COMPILE_IGNORES_TDC_FOR_STRATIX_PLL_CHANGES <value>
```

**Default Value**

Off
1.2.114. STATE_MACHINE_PROCESSING

Specifies the processing style used to compile a state machine. You can use your own 'User-Encoded' style, or select 'One-Hot', 'Minimal Bits', 'Gray', 'Johnson', 'Sequential' or 'Auto' (Compiler-selected) encoding.

**Type**

Enumeration

**Values**

- Auto
- Gray
- Johnson
- Minimal Bits
- One-Hot
- Sequential
- User-Encoded

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name STATE_MACHINE_PROCESSING -entity <entity name> <value>
set_instance_assignment -name STATE_MACHINE_PROCESSING -to <to> -entity <entity name> <value>
set_global_assignment -name STATE_MACHINE_PROCESSING <value>
```

**Default Value**

Auto

**Example**

```
set_global_assignment -name state_machine_processing "one-hot"
set_instance_assignment -name state_machine_processing "one-hot" -to foo
```

**See Also**

Extract Verilog State Machines Extract VHDL State Machines
1.2.115. STRICT_RAM_RECOGNITION

When this option is ON, the Compiler is only allowed to replace RAM if the hardware matches the design exactly.

Type
Boolean

Device Support
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes
This assignment is included in the Analysis & Synthesis report.
This assignment supports synthesis wildcards.

Syntax

```
set_global_assignment -name STRICT_RAM_RECOGNITION <value>
set_global_assignment -name STRICT_RAM_RECOGNITION -entity <entity name> <value>
set_instance_assignment -name STRICT_RAM_RECOGNITION -to <to> -entity <entity name> <value>
```

Default Value
Off

Example

```
set_global_assignment -name strict_ram_recognition on
set_global_assignment -name strict_ram_recognition on -to foo
```
1.2.116. SYNCHRONIZATION_REGISTER_CHAIN_LENGTH

This setting specifies the maximum number of registers in a row to be considered as a synchronization chain. Synchronization chains are sequences of registers with the same clock, no fanout in between, such that the first register is fed by a pin, or by logic in another clock domain. These registers will be considered for metastability analysis (available for some families), and are also protected from optimizations such as retiming. When gate-level retiming is turned on, these registers will not be moved. The default length is device-specific.

Old Name
ADV_NETLIST_OPT_METASTABLE_REGS

Type
Integer

Device Support
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes
This assignment is included in the Analysis & Synthesis report.
This assignment supports synthesis wildcards.

Syntax

```
set_global_assignment -name SYNCHRONIZATION_REGISTER_CHAIN_LENGTH <value>
set_global_assignment -name SYNCHRONIZATION_REGISTER_CHAIN_LENGTH -entity <entity name> <value>
set_instance_assignment -name SYNCHRONIZATION_REGISTER_CHAIN_LENGTH -to <to> -entity <entity name> <value>
```
1.2.117. SYNTHESIS_AVAILABLE_RESOURCE_MULTIPLIER

Specify a global resource multiplier for synthesis. Applies to RAM, DSP, and LUT resources.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name SYNTHESIS_AVAILABLE_RESOURCE_MULTIPLIER <value>
```

**Default Value**

1

**Example**

```
set_global_assignment -name synthesis_available_resource_multiplier 2
```
1.2.118. SYNTHESIS_EFFORT

Controls the synthesis trade-off between compilation speed and performance and area. The default is 'Auto'. You can select 'Fast' for faster compilation speed at the cost of performance and area.

**Type**

Enumeration

**Values**

- Auto
- Fast

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name SYNTHESIS_EFFORT <value>
```

**Default Value**

Auto

**Example**

```
set_global_assignment -name synthesis_effort fast
```
1.2.119. SYNTHESIS_KEEP_SYNCH_CLEAR_PRESET_BEHAVIOR_IN_UNMAPPER

When this option is set to On, synthesis will keep the synchronous clear/preset behavior when remap I/O wysiwyg primitives (from other device families) using DDIO INPUT feature to the targeted device family.

Type

Boolean

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Notes

This assignment supports synthesis wildcards.

Syntax

```text
set_global_assignment -name SYNTHESIS_KEEP_SYNCH_CLEAR_PRESET_BEHAVIOR_IN_UNMAPPER -entity <entity name> <value>
set_instance_assignment -name SYNTHESIS_KEEP_SYNCH_CLEAR_PRESET_BEHAVIOR_IN_UNMAPPER -to <to> -entity <entity name> <value>
set_global_assignment -name SYNTHESIS_KEEP_SYNCH_CLEAR_PRESET_BEHAVIOR_IN_UNMAPPER <value>
```

Example

```text
set_global_assignment -name synthesis_keep_synch_clear_preset_behavior_in_unmapper on
set_instance_assignment -name synthesis_keep_synch_clear_preset_behavior_in_unmapper on -to foo
```
1.2.120. SYNTHESIS_S10_MIGRATION_CHECKS

Option to enable/disable Arria 10 to Stratix 10 Synthesis Migration Checks.

**Type**

Boolean

**Device Support**

- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```plaintext
set_global_assignment -name SYNTHESIS_S10_MIGRATION_CHECKS <value>
```

**Default Value**

Off

**Example**

```plaintext
set_global_assignment -name SYNTHESIS_S10_MIGRATION_CHECKS on
```
1.2.121. SYNTH_CLOCK_MUX_PROTECTION

Causes the multiplexers in the clock network to be decomposed to 2to1 multiplexer trees, and protected from being merged with, or transferred to, other logic. This option helps the Timing Analyzer to understand clock behavior.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```plaintext
set_global_assignment -name SYNTH_CLOCK_MUX_PROTECTION <value>
```

**Default Value**

On

**Example**

```plaintext
set_global_assignment -name synth_clock_mux_protection off
```
1.2.122. SYNTH_GATED_CLOCK_CONVERSION

Automatically converts gated clocks in the design to use clock enable pins if clock enable pins are not used in the original design. Clock gating logic can contain AND, OR, MUX, and NOT gates. Turning on this option may increase memory use and overall run time. You must use the Timing Analyzer for timing analysis, and you must define all base clocks in Synopsys Design Constraints (SDC) format.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name SYNTH_GATED_CLOCK_CONVERSION -entity <entity name> <value>
set_instance_assignment -name SYNTH_GATED_CLOCK_CONVERSION -to <to> -entity <entity name> <value>
set_global_assignment -name SYNTH_GATED_CLOCK_CONVERSION <value>
```

**Default Value**

Off

**Example**

```
set_global_assignment -name synth_gated_clock_conversion on
set_instance_assignment -name synth_gated_clock_conversion on -to foo
```
1.2.123. SYNTH_GATED_CLOCK_CONVERSION_BASE_CLOCK

Identifies the signal as a base clock during gated clock conversion. Only has an impact if SYNTH_GATED_CLOCK_CONVERSION is also enabled.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
- This assignment is included in the Analysis & Synthesis report.
- This assignment supports synthesis wildcards.

**Syntax**

```plaintext
set_global_assignment -name SYNTH_GATED_CLOCK_CONVERSION_BASE_CLOCK -entity <entity name> <value>
set_instance_assignment -name SYNTH_GATED_CLOCK_CONVERSION_BASE_CLOCK -to <to> -entity <entity name> <value>
```

**Example**

```plaintext
set_instance_assignment -name synth_gated_clock_conversion_base_clock on -to foo
```

**See Also**
Auto Gated Clock Conversion
1.2.124. SYNTH_MESSAGE_LEVEL

Specifies the type of Analysis & Synthesis messages you want to view. Setting this option to 'Low' allows you to view only the most important Analysis & Synthesis messages. Setting this option to 'Medium' allows you to view most Analysis & Synthesis messages, but hides the detailed messages in Analysis & Synthesis report. Setting this option to 'High' allows you to view all Analysis & Synthesis messages.

**Type**

Enumeration

**Values**

- High
- Low
- Medium

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name SYNTH_MESSAGE_LEVEL <value>
```

**Default Value**

Medium
1.2.125. SYNTH_PROTECT_SDC_CONSTRAINT

Causes SDC constraint checking in register merging. It helps to maintain the validity of SDC constraints through compilation.

**Type**
Boolean

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**
This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name SYNTH_PROTECT_SDC_CONSTRAINT <value>
```

**Default Value**
Off

**Example**

```
set_global_assignment -name synth_protect_sdc_constraint on
```
1.2.126. SYNTH_RESOURCE_AWARE_INFERENCE_FOR_BLOCK_RAM

Specifies whether RAM, ROM, and shift-register inference should take the design and device resources into account.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name SYNTH_RESOURCE_AWARE_INFERENCE_FOR_BLOCK_RAM <value>
```

**Example**

```
set_global_assignment -name synth_resource_aware_inference_for_block_ram on
```
1.2.127. SYNTH_TIMING_DRIVEN_SYNTHESIS

Allows synthesis to use timing information during synthesis to better optimize the design.

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```plaintext
set_global_assignment -name SYNTH_TIMING_DRIVEN_SYNTHESIS <value>
set_global_assignment -name SYNTH_TIMING_DRIVEN_SYNTHESIS -entity <entity name> <value>
set_instance_assignment -name SYNTH_TIMING_DRIVEN_SYNTHESIS -to <to> -entity <entity name> <value>
```

**Example**

```plaintext
set_global_assignment -name synth_timing_driven_synthesis on
```
### 1.2.128. TOP_LEVEL_ENTITY

Specifies the full hierarchical path of the entity that is the focus of the current compilation or simulation.

**Old Name**

FOCUS_ENTITY_NAME

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name TOP_LEVEL_ENTITY <value>
```
1.2.129. UNCONNECTED_OUTPUT_PORT_MESSAGE_LEVEL

Tells the compiler whether to show a warning, and error or no message at all when an output port in a module does not have a driver.

**Type**

Enumeration

**Values**

- Error
- Error No Usage Check
- Off
- Warning
- Warning No Usage Check

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name UNCONNECTED_OUTPUT_PORT_MESSAGE_LEVEL <value>
set_global_assignment -name UNCONNECTED_OUTPUT_PORT_MESSAGE_LEVEL -entity <entity name> <value>
set_instance_assignment -name UNCONNECTED_OUTPUT_PORT_MESSAGE_LEVEL -to <to> -entity <entity name> <value>
```

**Default Value**

Warning

**Example**

```
set_global_assignment -name unconnected_output_port_message_level warning
set_instance_assignment -name unconnected_output_port_message_level error -to accel
```
1.2.130. USER_LIBRARIES

Specifies the pathnames of user-defined libraries.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name USER_LIBRARIES <value>
```
1.2.131. **USE_GENERATED_PHYSICAL_CONSTRAINTS**

Specifies the physical constraints file generated by the resynthesis tool to be used by the Quartus Prime software

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name USE_GENERATED_PHYSICAL_CONSTRAINTS -section_id <section identifier> <value>
set_global_assignment -name USE_GENERATED_PHYSICAL_CONSTRAINTS -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

On, requires section identifier
1.2.132. VERILOG_CONSTANT_LOOP_LIMIT

Defines the iteration limit for Verilog loops with loop conditions that evaluate to compile-time constants on each loop iteration. This limit exists primarily to identify potential infinite loops before they exhaust memory or trap the software in an actual infinite loop.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name VERILOG_CONSTANT_LOOP_LIMIT <value>
set_global_assignment -name VERILOG_CONSTANT_LOOP_LIMIT -entity <entity name> <value>
set_instance_assignment -name VERILOG_CONSTANT_LOOP_LIMIT -to <to> -entity <entity name> <value>
```

**Default Value**

5000

**Example**

```
set_global_assignment -name verilog_constant_loop_limit 3000
```
1.2.133. VERILOG_INPUT_VERSION


Type

Enumeration

Values

- SystemVerilog_2005
- SystemVerilog_2009
- SystemVerilog_2012
- Verilog_1995
- Verilog_2001

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Notes

This assignment is included in the Analysis & Synthesis report.

Syntax

```
set_global_assignment -name VERILOG_INPUT_VERSION <value>
```

Default Value

Verilog_2001
1.2.134. VERILOG_LMF_FILE

Specifies the default Library Mapping File (.lmf) for the current compilation.

Type
File name

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Analysis & Synthesis report.

Syntax

set_global_assignment -name VERILOG_LMF_FILE <value>
1.2.135. VERILOG_MACRO

Defines Verilog HDL macro - same as `define directive

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_global_assignment -name VERILOG_MACRO <value>
```
1.2.136. VERILOG_NON_CONSTANT_LOOP_LIMIT

Defines the iteration limit for Verilog loops with loop conditions that do not evaluate to compile-time constants on each loop iteration. This limit exists primarily to identify potential infinite loops before they exhaust memory or trap the software in an actual infinite loop.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name VERILOG_NON_CONSTANT_LOOP_LIMIT <value>
set_global_assignment -name VERILOG_NON_CONSTANT_LOOP_LIMIT -entity <entity name> <value>
set_instance_assignment -name VERILOG_NON_CONSTANT_LOOP_LIMIT -to <to> -entity <entity name> <value>
```

**Default Value**

250

**Example**

```
set_global_assignment -name verilog_non_constant_loop_limit 3000
```
1.2.137. VERILOG_SHOW_LMF_MAPPING_MESSAGES

Determines whether to display messages describing the mappings used in the Library Mapping File.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```plaintext
set_global_assignment -name VERILOG_SHOW_LMF_MAPPING_MESSAGES <value>
```
1.2.138. VHDL_INPUT_LIBRARY

Specifies the logical name of a user-defined VHDL design library : physical name.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_instance_assignment -name VHDL_INPUT_LIBRARY -to <to> <value>
```
1.2.139. VHDL_INPUT_VERSION


Type

Enumeration

Values

- VHDL_1987
- VHDL_1993
- VHDL_2008

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Notes

This assignment is included in the Analysis & Synthesis report.

Syntax

```bash
set_global_assignment -name VHDL_INPUT_VERSION <value>
```

Default Value

VHDL_1993
1.2.140. VHDL_LMF_FILE

Specifies the default Library Mapping File (.lmf) for the current compilation.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name VHDL_LMF_FILE <value>
```
1.2.141. **VHDL_SHOW_LMF_MAPPING_MESSAGES**

Determines whether to display messages describing the mappings used in the Library Mapping File.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name VHDL_SHOW_LMF_MAPPING_MESSAGES <value>
```
1.3. Assembler Assignments

1.3.1. ANTI_TAMPER_RESPONSE

Device Cleaning clears configuration information from the FPGA, HPS caches, and on-chip RAM. Device Cleaning and Zeroization also clears the AES key stored in BBRAM and zeros out memory. Device Cleaning, Zeroization, BBRAM key cleaning disables all security features and Clears BBRAM registers and the BBRAM key. Disabled does not respond to tampering events. Kill eFuse permanently disables the FPGA. Refer to the Stratix 10 Device Security User Guide for more detailed information about these choices.

**Type**

Enumeration

**Values**

- DISABLED
- Notification Device Wipe Device Lock Zeroization and BBRAM Key Zeroization
- Notification Device Wipe Device Lock and Zeroization
- Notification Device Wipe and Device Lock
- Notification only

**Device Support**

- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ANTI_TAMPER_RESPONSE <value>
```

**Default Value**

DISABLED
1.3.2. ATTESTATION_ALT_NAME_MANUFACTURER

The field for alternative name of manufacturer.

**Type**

String

**Device Support**

- Programmer Dummy Family

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ATTESTATION_ALT_NAME_MANUFACTURER <value>
```
1.3.3. ATTESTATION_ALT_NAME_PRODUCT

The field for alternative name of product.

**Type**

String

**Device Support**

- Programmer Dummy Family

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ATTESTATION_ALT_NAME_PRODUCT <value>
```
1.3.4. ATTESTATION_CRL_DISTRIBUTION_POINT

The field for Certificate Revocation List (CRL) distribution point.

Type
String

Device Support
- Programmer Dummy Family

Notes
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name ATTESTATION_CRL_DISTRIBUTION_POINT <value>
```
1.3.5. ATTESTATION_MODEL_INFO

The field for model information.

**Type**

String

**Device Support**

- Programmer Dummy Family

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ATTESTATION_MODEL_INFO <value>
```
1.3.6. ATTESTATION_RIM_URI_PREFIX

The field for Reference Integrity Manifests (RIM) uri prefix.

**Type**

String

**Device Support**

- Programmer Dummy Family

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ATTESTATION_RIM_URI_PREFIX <value>
```
1.3.7. ATTESTATION_RIM_URI_SUFFIX

The field for Reference Integrity Manifests (RIM) uri suffix.

**Type**
String

**Device Support**
- Programmer Dummy Family

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ATTESTATION_RIM_URI_SUFFIX <value>
```
1.3.8. ATTESTATION_VENDOR_INFO

The field for vendor information.

**Type**

String

**Device Support**

- Programmer Dummy Family

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name ATTESTATION_VENDOR_INFO <value>
```
1.3.9. AUTO_RESTART_CONFIGURATION

Directs the device to restart the configuration process automatically if a data error is encountered. If this option is turned off, you must externally direct the device to restart the configuration process if an error occurs.

Old Name
Auto restart on configuration error

Type
Boolean

Device Support
- Intel Arria 10
- Intel Cyclone 10 GX

Notes
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name AUTO_RESTART_CONFIGURATION <value>
```

Default Value
On
1.3.10. CLOCK_SOURCE

Specifies whether the configuration device generates an internal clock or applies an external clock.

**Type**

Enumeration

**Values**

- External
- Internal

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```text
set_global_assignment -name CLOCK_SOURCE <value>
```

**Default Value**

Internal
1.3.11. COMPRESSION_MODE

Allows you to compress SRAM Object Files (.sof) stored in a Programmer Object File (.pof) for a configuration device.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name COMPRESSION_MODE <value>
```

**Default Value**

Off
1.3.12. CONFIGURATION_CLOCK_DIVISOR

Specifies the clock frequency divisor, which is used to determine the period of the system clock.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name CONFIGURATION_CLOCK_DIVISOR <value>
```

**Default Value**

1
1.3.13. CONFIGURATION_CLOCK_FREQUENCY

Specifies the clock frequency of the configuration device.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
None

**Syntax**

```
set_global_assignment -name CONFIGURATION_CLOCK_FREQUENCY <value>
```

**Default Value**
10 MHz
1.3.14. ENABLE_ADV_SEU_DETECTION

Allows you to enable the Advanced SEU Detection compiler to generate design SEU sensitivity map file. If this option is turned on, the SMH file will be generated.

**Type**
Boolean

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**
None

**Syntax**

```
set_global_assignment -name ENABLE_ADV_SEU_DETECTION <value>
```

**Default Value**
Off

**Example**

```
set_global_assignment -name ENABLE_ADV_SEU_DETECTION ON
```

**See Also**

PARTITION_ASD_REGION_ID
1.3.15. ENABLE_AUTONOMOUS_PCIE_HIP

Directs the device to release the PCIe HIP after the periphery is configured and before core configuration is completed. This option doesn't take effect in CvP Init mode since the periphery automatically comes up first, all other modes bring the PCIe HIP up first when this option is selected.

**Old Name**

Auto restart on configuration error

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ENABLE_AUTONOMOUS_PCIE_HIP <value>
```

**Default Value**

Off
1.3.16. ENABLE_FPGA_TAMPERDEVICE_SELF_KILL

Enable the device self-kill on FPGA tamper events.

Type

Boolean

Device Support

• Intel Stratix 10

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name ENABLE_FPGA_TAMPERDEVICE_SELF_KILL <value>
```

Default Value

Off
1.3.17. ENABLE_FREQUENCY_TAMPER_DETECTION

Enable frequency tamper detection

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ENABLE_FREQUENCY_TAMPER_DETECTION <value>
```

**Default Value**

Off
1.3.18. ENABLE_FREQUENCY_TAMPER_DEVICE_SELF_KILL

Enable the device self-kill on frequency tamper events.

**Type**

Boolean

**Device Support**

- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```set_global_assignment -name ENABLE_FREQUENCY_TAMPERDEVICE_SELF_KILL <value>```

**Default Value**

Off
1.3.19. ENABLE_MULTI_AUTHORITY

Enable multiple owner authentication authorities.

**Type**
Boolean

**Device Support**
- Intel Agilex

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ENABLE_MULTI_AUTHORITY <value>
```

**Default Value**
Off
1.3.20. ENABLE_OCT_DONE

This option controls whether the INIT_DONE signal will be gated by OCT_DONE signal which indicates the Power-Up OCT calibration is completed. If this option is turned off, the INIT_DONE signal is not gated by the OCT_DONE signal.

**Type**  
Boolean

**Device Support**  
- Intel Arria 10  
- Intel Cyclone 10 GX

**Notes**  
This assignment is included in the Fitter report.

**Syntax**

```bash
set_global_assignment -name ENABLE_OCT_DONE <value>
```

**Default Value**  
Off
1.3.21. ENABLE_PARTIAL_RECONFIGURATION_BITSTREAM_ENCRYPTION

Enable partial reconfiguration bitstream encryption.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name ENABLE_PARTIAL_RECONFIGURATION_BITSTREAM_ENCRYPTION <value>
set_instance_assignment -name ENABLE_PARTIAL_RECONFIGURATION_BITSTREAM_ENCRYPTION -to <to> <value>
```

**Default Value**

Off
1.3.22. ENABLE_PR_POF_ID

Enable PR POF ID for bitstream compatibility check.

**Type**

Boolean

**Device Support**

- Intel Stratix 10

**Notes**

**Syntax**

```
set_global_assignment -name ENABLE_PR_POF_ID <value>
set_instance_assignment -name ENABLE_PR_POF_ID -to <to> <value>
```

**Default Value**

On
1.3.23. ENABLE_S10_ATTESTATION_COMMANDS

Enable the use of Stratix 10 attestation commands

**Type**

Boolean

**Device Support**

- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name ENABLE_S10_ATTESTATION_COMMANDS <value>
```

**Default Value**

Off
1.3.24. ENABLE_TEMPERATURE_TAMPER_DETECTION

Enable temperature tamper detection

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ENABLE_TEMPERATURE_TAMPER_DETECTION <value>
```

**Default Value**

Off
1.3.25. ENABLE_TEMPERATURE_TAMPERDEVICE_SELF_KILL

Enable the device self-kill on temperature tamper events.

**Type**
Boolean

**Device Support**
- Intel Stratix 10

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ENABLE_TEMPERATURE_TAMPERDEVICE_SELF_KILL <value>
```

**Default Value**
Off
1.3.26. ENABLE_VCCL_SDM_VOLTAGE_TAMPER_DETECTION

When enabled, triggers an anti-tamper response when the VCCL_SDM voltage differs by more than the Voltage tamper detection trigger percentage you specify.

**Type**

Boolean

**Device Support**

- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ENABLE_VCCL_SDM_VOLTAGE_TAMPER_DETECTION <value>
```

**Default Value**

Off
1.3.27. ENABLE_VCCL_VOLTAGE_TAMPER_DETECTION

When enabled, triggers an anti-tamper response when the VCCL voltage differs by more than the Voltage tamper detection trigger percentage you specify.

**Type**

Boolean

**Device Support**

- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ENABLE_VCCL_VOLTAGE_TAMPER_DETECTION <value>
```

**Default Value**

Off
1.3.28. ENABLE_VOLTAGE_TAMPER_DETECTION

Enable voltage tamper detection

Type

Boolean

Device Support

• Intel Agilex
• Intel Stratix 10

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name ENABLE_VOLTAGE_TAMPER_DETECTION <value>
```

Default Value

Off
1.3.29. ENABLE_VOLTAGE_TAMPER_DEVICE_SELF_KILL

Enable the device self-kill on voltage tamper events.

Type

Boolean

Device Support

• Intel Stratix 10

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name ENABLE_VOLTAGE_TAMPER_DEVICE_SELF_KILL <value>
```

Default Value

Off
1.3.30. ENCRYPT_PROGRAMMING_BITSTREAM

Enable configuration bitstream encryption.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ENCRYPT_PROGRAMMING_BITSTREAM <value>
set_instance_assignment -name ENCRYPT_PROGRAMMING_BITSTREAM -to <to> <value>
```

**Default Value**

Off
1.3.31. EPROM_USE_CHECKSUM_AS_USERCODE

Uses the checksum value from the Programmer Object File (.pof) as the JTAG user code.

**Type**

Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```bash
set_global_assignment -name EPROM_USE_CHECKSUM_AS_USERCODE <value>
```

**Default Value**

Off
1.3.32. FREQUENCY_TAMPER_DETECTION_RANGE

Specifies the maximum percentage frequency difference allowed between the OSC_CLK_1 input clock and the internal oscillator. Percentage differences larger than the value you specify trigger an anti-tamper response when you have enabled a response.

**Type**

Integer

**Device Support**

- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name FREQUENCY_TAMPER_DETECTION_RANGE <value>
```

**Default Value**

0
1.3.33. GENERATE_COMPRESSED_SOFTWARE

Allows you to enable the SOF compression and generate compressed SOF file

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name GENERATE_COMPRESSED_SOFTWARE <value>
```

**Default Value**

Off

**Example**

```plaintext
set_global_assignment -name GENERATE_COMPRESSED_SOFTWARE ON
```
1.3.34. GENERATE_HEX_FILE

Generates a Hexadecimal (Intel-format) Output File (.hexout) containing configuration data that can be programmed into a parallel data source, such as an EPROM or a mass storage device, which then in turn configures the target device.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
None

**Syntax**

```
set_global_assignment -name GENERATE_HEX_FILE <value>
```

**Default Value**

Off
1.3.35. GENERATE_PMSF_FILES

Generates a Partial-Masked SOF file (.pmsf) containing both configuration data and region definitions that can be used to re-configure a device region. If this option is turned on, the Partial-Masked SOF files (.pmsf) will be generated instead of Mask Settings files (.msf).

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Syntax**

```
set_global_assignment -name GENERATE_PMSF_FILES <value>
```

**Default Value**

On

**Example**

```
set_global_assignment -name GENERATE_PMSF_FILES ON
```

**See Also**

GENERATE_PMSF_FILES
1.3.36. GENERATE_PR_RBF_FILE

Generates a Partial Reconfiguration Raw Binary File (.rbf) containing configuration data that an intelligent external controller can use to reconfigure the portion of target device.

Type
Boolean

Device Support
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name GENERATE_PR_RBF_FILE <value>
```
1.3.37. GENERATE_RBF_FILE

Generates a Raw Binary File (.rbf) containing configuration data that an intelligent external controller can use to configure the target device.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

set_global_assignment -name GENERATE_RBF_FILE <value>

**Default Value**

Off
1.3.38. GENERATE_TTF_FILE

Generates a Tabular Text File (.ttf) containing configuration data that an intelligent external controller can use to configure the target device.

Type

Boolean

Device Support

• This setting can be used in projects targeting any Intel FPGA device family.

Notes

None

Syntax

```plaintext
set_global_assignment -name GENERATE_TTF_FILE <value>
```

Default Value

Off
1.3.39. HEXOUT_FILE_COUNT_DIRECTION

Specifies the count direction for the data in a Hexadecimal (Intel-Format) Output File (.hexout) as up or down.

Old Name
HEX_FILE_COUNT_UP_DOWN

Type
Enumeration

Values
- Down
- Up

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
None

Syntax

```
set_global_assignment -name HEXOUT_FILE_COUNT_DIRECTION <value>
```

Default Value

Up
1.3.40. HEXOUT_FILE_START_ADDRESS

Specifies the starting memory address for a Hexadecimal (Intel-Format) Output File (.hexout).

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name HEXOUT_FILE_START_ADDRESS <value>
```

**Default Value**

0
1.3.41. HPS_DAP_NO_CERTIFICATE

Allow HPS debug without certificate.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name HPS_DAP_NO_CERTIFICATE <value>
set_instance_assignment -name HPS_DAP_NO_CERTIFICATE -to <to> <value>
```

**Default Value**

Off
1.3.42. HPS_DAP_SPLIT_MODE

Enables the HPS debug access port (DAP) pins. When HPS JTAG pins are selected, these HPS JTAG pins are shared with other HPS uses and with user logic.

**Type**

Enumeration

**Values**

- Disabled
- HPS Pins
- SDM Pins

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name HPS_DAP_SPLIT_MODE <value>
```

**Default Value**

Disabled
1.3.43. HPS_INITIALIZATION

Selects the order in which the Hard Processor System (HPS) and the FPGA are configured.

**Type**

Enumeration

**Values**

- After INIT_DONE
- HPS First

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name HPS_INITIALIZATION <value>
```
1.3.44. HPS_RETAIN_DDR_CONTENT

Determine the condition for the DDR content be retained.

**Type**

Boolean

**Device Support**

- eASIC N5X

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name HPS_RETAIN_DDR_CONTENT <value>
```

**Default Value**

Off
1.3.45. ON_CHIP_BITSTREAM_DECOMPRESSION

Allows the device to accept and decompress bitstreams during configuration. Produces compressed bitstreams and enables bitstream decompression.

Type
Boolean

Device Support
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes
This assignment is included in the Fitter report.

Syntax

set_global_assignment -name ON_CHIP_BITSTREAM_DECOMPRESSION <value>

Default Value
On
1.3.46. PROGRAMMING_BITSTREAM_ENCRYPTION_CNOC_SCRAMBLING

Limits potential side-channel exposure when you store the AES key in eFuses.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name PROGRAMMING_BITSTREAM_ENCRYPTION_CNOC_SCRAMBLING <value>
set_instance_assignment -name PROGRAMMING_BITSTREAM_ENCRYPTION_CNOC_SCRAMBLING -to <to> <value>
```

**Default Value**

Off
1.3.47. PROGRAMMING_BITSTREAM_ENCRYPTION_KEY_SELECT

Configuration bitstream encryption key storage location.

**Type**

Enumeration

**Values**

- Battery Backup RAM
- Quad SPI Intrinsic ID PUF-wrapped
- eFuses

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**

The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name PROGRAMMING_BITSTREAM_ENCRYPTION_KEY_SELECT <value>
set_instance_assignment -name PROGRAMMING_BITSTREAM_ENCRYPTION_KEY_SELECT -to <value>
```
1.3.48. PROGRAMMING_BITSTREAM_ENCRYPTION_UPDATE_RATIO

Configuration bitstream encryption update ratio. Inserts new keys to limit the amount of data encrypted by a given key to the specified ratio.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name PROGRAMMING_BITSTREAM_ENCRYPTION_UPDATE_RATIO <value>
set_instance_assignment -name PROGRAMMING_BITSTREAM_ENCRYPTION_UPDATE_RATIO -to <to> <value>
```

**Default Value**

0
1.3.49. PR_BASE_MSF

Specify block name and path of base revision MSF file for mask comparison in a PR project.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name PR_BASE_MSF <value>
```
1.3.50. PR_BASE_SOF

Specify path of base revision SOF file for bit settings comparison in a PR project.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```bash
set_global_assignment -name PR_BASE_SOF <value>
```
1.3.51. PR_SKIP_BASE_CHECK

Disable mask comparison and logic verification for a reconfigurable partition in a PR project.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

set_global_assignment -name PR_SKIP_BASE_CHECK <value>
1.3.52. PWRMGT_ADV_CLOCK_DATA_FALL_TIME

Specify fall time of clock and data signals in nanoseconds. Integer value between 0 and 65535. The relevant SMBus requirement is tf as detailed in the SMBus AC Specifications. This is for PMBus Master mode.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name PWRMGT_ADV_CLOCK_DATA_FALL_TIME <value>
```

**Default Value**

0
1.3.53. PWRMGT_ADV_CLOCK_DATA_RISE_TIME

Specify rise time of clock and data signals in nanoseconds. Integer value between 0 and 65535. The relevant SMBus requirement is tf as detailed in the SMBus AC Specifications. This is for PMBus Master mode.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name PWRMGT_ADV_CLOCK_DATA_RISE_TIME <value>
```

**Default Value**

0
1.3.54. PWRMGT_ADV_DATA_HOLD_TIME

Specify data hold time in nanoseconds. Integer value between 0 and 65535. This parameter is used to control the hold time of SDA during transmit in both PMBus Master and PMBus Slave mode. The relevant SMBus requirement is tHD:DAT as detailed in the SMBus AC Specifications.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name PWRMGT_ADV_DATA_HOLD_TIME <value>
```

**Default Value**

0
1.3.55. **PWRMGT_ADV_DATA_SETUP_TIME**

Specify data setup time in nanoseconds. Integer value between 0 and 65535. The amount of time delay introduced in the rising edge of SCL relative to SDA changing when a read-request is serviced. The relevant SMBus requirement is tSU:DAT as detailed in the SMBus AC Specifications. This is for PMBus slave mode.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name PWRMGT_ADV_DATA_SETUP_TIME <value>
```

**Default Value**

0
1.3.56. PWRMGT_ADV_FPGA_RELEASE_DELAY

When operation mode is PMBus Slave mode, specify value in unassigned decimal value between 0 and 255 for delay duration in milliseconds before starting FPGA after first successful VOUT_COMMAND is responded.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name PWRMGT_ADV_FPGA_RELEASE_DELAY <value>
```

**Default Value**

10
### 1.3.57. PWRMGT_ADV_INITIAL_DELAY

When operation mode is PMBus Master mode, specify value in unassigned decimal value between 0 and 255 for delay duration in milliseconds before first command is used.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name PWRMGT_ADV_INITIAL_DELAY <value>
```

**Default Value**

0
1.3.58. PWRMGT_ADV_VOLTAGE_STABLE_DELAY

When operation mode is PMBus Master mode, specify value in unassigned decimal value between 0 and 255 for delay duration in milliseconds for voltage to stabilize after each voltage update.

Type
Integer

Device Support
- Intel Agilex
- Intel Stratix 10

Notes
This assignment is included in the Fitter report.

Syntax

```bash
set_global_assignment -name PWRMGT_ADV_VOLTAGE_STABLE_DELAY <value>
```

Default Value

10
1.3.59. PWRMGT_ADV_VOUT_READING_ERR_MARGIN

Specify power level feedback reading error margin index at 0.25% granularity, used by the controller to determine if target VID is achieved. 0: +/-1.00%, 1: +/-1.25%, ... 8: +/-3.00%

Type
Integer

Device Support
• Intel Agilex
• Intel Stratix 10

Notes
This assignment is included in the Fitter report.

Syntax

| set_global_assignment -name PWRMGT_ADV_VOUT_READING_ERR_MARGIN <value> |

Default Value
8
1.3.60. PWRMGT_BUS_SPEED_MODE

Specifies bus speed mode in PMBus Master mode

Type

Enumeration

Values

- 100 KHz
- 400 KHz

Device Support

- Intel Agilex
- Intel Stratix 10

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name PWRMGT_BUS_SPEED_MODE <value>
```

Default Value

100 KHz
1.3.61. PWRMGT_DEVICE_ADDRESS_IN_PMBUS_SLAVE_MODE

Specifies 7 bit Hexadecimal value without leading prefix 0x for address, for instance 7F, for device address assignment when in PMBus Slave mode. It must be non-zero address.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name PWRMGT_DEVICE_ADDRESS_IN_PMBUS_SLAVE_MODE <value>
```

**Default Value**

00
1.3.62. PWRMGT_DIRECT_FORMAT_COEFFICIENT_B

Specifies direct format coefficient b when in PMBus Master mode. Signed integer between -32768 and 32767. Coefficient b is the offset. This value is supplied by the PMBus devices manufacturer in the product literature. User must set this parameter when output voltage format of PMBus device is Direct formator or auto discovery format.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name PWRMGT_DIRECT_FORMAT_COEFFICIENT_B <value>
```

**Default Value**

0
1.3.63. PWRMGT_DIRECT_FORMAT_COEFFICIENT_M

Specifies direct format coefficient m when in PMBus Master mode. Signed integer between -32768 and 32767. Coefficient m is the slope coefficient. This value is supplied by the PMBus devices manufacturer in the product literature. User must set this parameter when output voltage format of PMBus device is Direct format or auto discovery format. It must be a non-zero value when output voltage format of PMBus device is Direct format.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name PWRMGT_DIRECT_FORMAT_COEFFICIENT_M <value>
```

**Default Value**

0
1.3.64. PWRMGT_DIRECT_FORMAT_COEFFICIENT_R

Specify direct format coefficient R when in PMBus Master mode. Signed integer between -128 and 127. Coefficient R is the exponent. This value is supplied by the PMBus devices manufacturer in the product literature. User must set this parameter when output voltage format of PMBus device is Direct format or auto discovery format.

Type

String

Device Support

- Intel Agilex
- Intel Stratix 10

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name PWRMGT_DIRECT_FORMAT_COEFFICIENT_R <value>
```

Default Value

0
1.3.65. PWRMGT_LINEAR_FORMAT_N

Specify linear format N when in PMBus Master mode. Signed integer between -16 and 15. This is exponent for the mantissa for output voltage related command when VOUT format is set to Linear format. This value is supplied by the PMBus devices manufacturer in the product literature. A nonzero value must be specified when linear voltage output format is chosen.

Type

String

Device Support

- Intel Agilex
- Intel Stratix 10

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name PWRMGT_LINEAR_FORMAT_N <value>
```

Default Value

0
1.3.66. PWRMGT_PAGE_COMMAND_ENABLE

By enabling PAGE command, the FPGA PMBus master will use PAGE command to set all output channels on registered regulator modules to respond to VOUT_COMMAND.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name PWRMGT_PAGE_COMMAND_ENABLE <value>
```

**Default Value**

Off
1.3.67. PWRMGT_PAGE_COMMAND_PAYLOAD

The Page Command Payload value is used to control the payload-value of the page command. The default payload is 0xFF which selects all pages inside of the Voltage Regulator. If the Voltage Regulator needs to limit interaction to a specific page, use this dialog to select the page. When enabled, the page command is emitted prior to any voltage adjustment commands.

Type

Integer

Device Support

- Intel Agilex
- Intel Stratix 10

Notes

This assignment is included in the Fitter report.

Syntax

```plaintext
set_global_assignment -name PWRMGT_PAGE_COMMAND_PAYLOAD <value>
```

Default Value

255
1.3.68. PWRMGT_SLAVE_DEVICE0_ADDRESS

Specifies 7 bit Hexadecimal value without leading prefix 0x, for instance 7F, for slave address of the voltage regulator when in PMBus Master mode. It must be non-zero address.

Type
String

Device Support
• Intel Agilex
• Intel Stratix 10

Notes
This assignment is included in the Fitter report.

Syntax

```python
set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS <value>
```

Default Value

00
1.3.69. PWRMGT_SLAVE_DEVICE1_ADDRESS

 Specifies 7 bit Hexadecimal value without leading prefix 0x, for instance 7F, for slave address of the voltage regulator when in PMBus Master mode.

 Type
 String

 Device Support
 • Intel Agilex
 • Intel Stratix 10

 Notes
 This assignment is included in the Fitter report.

 Syntax

 set_global_assignment -name PWRMGT_SLAVEDEVICE1_ADDRESS <value>

 Default Value
 00
1.3.70. PWRMGT_SLAVE_DEVICE2_ADDRESS

Specifies 7 bit Hexadecimal value without leading prefix 0x, for instance 7F, for slave address of the voltage regulator when in PMBus Master mode.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name PWRMGT_SLAVE_DEVICE2_ADDRESS <value>
```

**Default Value**

00
1.3.71. PWRMGT_SLAVE_DEVICE3_ADDRESS

Specifies 7 bit Hexadecimal value without leading prefix 0x, for instance 7F, for slave address of the voltage regulator when in PMBus Master mode.

Type
String

Device Support
- Intel Agilex
- Intel Stratix 10

Notes
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name PWRMGT_SLAVE_DEVICE3_ADDRESS <value>
```

Default Value
00
1.3.72. PWRMGT_SLAVE_DEVICE4_ADDRESS

Specifies 7 bit Hexadecimal value without leading prefix 0x, for instance 7F, for slave address of the voltage regulator when in PMBus Master mode.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name PWRMGT_SLAVE_DEVICE4_ADDRESS <value>
```

**Default Value**

00
1.3.73. PWRMGT_SLAVE_DEVICE5_ADDRESS

Specifies 7 bit Hexadecimal value without leading prefix 0x, for instance 7F, for slave address of the voltage regulator when in PMBus Master mode.

Type
String

Device Support
• Intel Agilex
• Intel Stratix 10

Notes
This assignment is included in the Fitter report.

Syntax

set_global_assignment -name PWRMGT_SLAVE_DEVICE5_ADDRESS <value>

Default Value
00
1.3.74. PWRMGT_SLAVE_DEVICE6_ADDRESS

Specifies 7 bit Hexadecimal value without leading prefix 0x, for instance 7F, for slave address of the voltage regulator when in PMBus Master mode.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name PWRMGT_SLAVEDEVICE6_ADDRESS <value>
```

**Default Value**

00
1.3.75. PWRMGT_SLAVE_DEVICE7_ADDRESS

Specifies 7 bit Hexadecimal value without leading prefix 0x, for instance 7F, for slave address of the voltage regulator when in PMBus Master mode.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name PWRMGT_SLAVE_DEVICE7_ADDRESS <value>
```

**Default Value**

00
1.3.76. PWRMGT_SLAVEDEVICE_TYPE

Specifies the slave device type when the target FPGA device is in PMBus master mode.

**Type**

Enumeration

**Values**

- ED8401
- EM21XX
- EM22XX
- ISL82XX
- LTM4677
- Other

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name PWRMGT_SLAVEDEVICE_TYPE <value>
```

**Default Value**

LTM4677
1.3.77. PWRMGT_TABLE_VERSION

Power table version. 0 is a reserved value to indicate the power table is invalid. 1 is used for Nadder and FM until Quartus version 20.x. 2 indicates the version after addition of PAGE command payload field.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name PWRMGT_TABLE_VERSION <value>
```

**Default Value**

1
1.3.78. PWRMGT_TRANSLATED_VOLTAGE_VALUE_UNIT

Specifies the output voltage format when in PMBus Master mode.

**Type**

Enumeration

**Values**

- Millivolts
- Volts

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name PWRMGT_TRANSLATED_VOLTAGE_VALUE_UNIT <value>
```

**Default Value**

Volts
1.3.79. PWRMGT_VOLTAGE_OUTPUT_FORMAT

Specifies the output voltage format when in PMBus Master mode.

Type

Enumeration

Values

• Auto discovery
• Direct format
• Linear format

Device Support

• This setting can be used in projects targeting any Intel FPGA device family.

Notes

This assignment is included in the Fitter report.

Syntax

set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT <value>

Default Value

Auto discovery
1.3.80. QKY_FILE

Specify a Quartus key file.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_global_assignment -name QKY_FILE <value>
set_instance_assignment -name QKY_FILE -to <to> <value>
```
1.3.81. RBF_FILE_GENERATION_FOR_SUPR

PR RBF generation for specified SUPR partition.

Type

Boolean

Device Support

• This setting can be used in projects targeting any Intel FPGA device family.

Notes

The value of this assignment is case sensitive.

Syntax

set_global_assignment -name RBF_FILE_GENERATION_FOR_SUPR <value>
set_instance_assignment -name RBF_FILE_GENERATION_FOR_SUPR -to <to> <value>

Default Value

On
1.3.82. RELEASE_CLEARS_BEFORE_TRI_STATES

Directs the device to release the clear signal on registered logic cells and I/O cells before releasing the output enable override on tri-state buffers. If this option is turned off, the output enable signals are released before the clear overrides are released.

**Old Name**

Release clears before tri-states

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name RELEASE_CLEARS_BEFORE_TRI_STATES <value>
```

**Default Value**

Off
1.3.83. RSU_MAX_RETRY_COUNT

Specify the maximum number of times that the current image will be retried in Remote System Update before giving up and starting failover flow. The valid values are 1, 2 and 3.

Type
Integer

Device Support
- Intel Agilex
- Intel Stratix 10
- eASIC N5X

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name RSU_MAX_RETRY_COUNT <value>
set_instance_assignment -name RSU_MAX_RETRY_COUNT -to <to> <value>
```

Default Value

1
1.3.84. RUN_CONFIG_CPU_FROM_INT_OSC

When set, the configuration CPU is run from the internal oscillator.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name RUN_CONFIG_CPU_FROM_INT_OSC <value>
```

**Default Value**

Off
1.3.85. SECU_OPTION_DISABLE_ENCRYPTION_KEY_IN_BBRAM

When set, the device does not use an AES key stored in BBRAM. Disabling the storage locations that you are not using may prevent an attack that uses a different storage location for the encryption key.

**Type**

Enumeration

**Values**

- OFF
- ON
- On check
- On sticky

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name SECU_OPTION_DISABLE_ENCRYPTION_KEY_IN_BBRAM <value>
```

**Default Value**

OFF
1.3.86. SECU_OPTION_DISABLE_ENCRYPTION_KEY_IN_EFUSES

When set, the device does not use an AES key stored in eFuses. Disabling the storage locations that you are not using may prevent an attack that uses a different storage location for the encryption key.

**Type**

Enumeration

**Values**

- OFF
- ON
- On check
- On sticky

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name SECU_OPTION_DISABLE_ENCRYPTION_KEY_IN_EFUSES <value>
```

**Default Value**

OFF
1.3.87. **SECU_OPTION_DISABLE_HPS_DEBUG**

When set, permanently disables debugging using JTAG to access the HPS.

**Type**

Enumeration

**Values**

- OFF
- ON
- On check
- On sticky

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC NSX

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name SECU_OPTION_DISABLE_HPS_DEBUG <value>
```

**Default Value**

OFF
1.3.88. **SECU_OPTION_DISABLE_JTAG**

When set, disables JTAG command and configuration. Setting this eFuse eliminates JTAG as mode of attack, but also eliminates boundary scan.

**Type**

Enumeration

**Values**

- OFF
- ON
- On check
- On sticky

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name SECU_OPTION_DISABLE_JTAG <value>
```

**Default Value**

OFF
1.3.89. SECU_OPTION_DISABLE_PUF_WRAPPED_ENCRYPTION_KEY

When set, the device does not use a PUF-wrapped AES key stored in Quad SPI. Disabling the storage locations that you are not using may prevent an attack that uses a different storage location for the encryption key.

**Type**

Enumeration

**Values**

- OFF
- ON
- On check
- On sticky

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name SECU_OPTION_DISABLE_PUF_WRAPPED_ENCRYPTION_KEY <value>
```

**Default Value**

OFF
1.3.90. SECU_OPTION_DISABLE_VIRTUAL_EFUSES

Security option to disable virtual eFuses.

**Type**

Enumeration

**Values**

- OFF
- ON
- On check
- On sticky

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name SECU_OPTION_DISABLE_VIRTUAL_EFUSES <value>
```

**Default Value**

OFF
1.3.91. SECU_OPTION_FORCE_ENCRYPTION_KEY_UPDATE

When set, all encrypted bitstreams must specify the Encryption Update Ratio.

**Type**

Enumeration

**Values**

- OFF
- ON
- On check
- On sticky

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC NSX

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name SECU_OPTION_FORCE_ENCRYPTION_KEY_UPDATE <value>
```

**Default Value**

OFF
1.3.92. SECU_OPTION_FORCE_SDM_CLOCK_TO_INT_OSC

When set, disables an external clock source for the SDM for bitstream configuration. Forcing the SDM to use an internal oscillator helps to limit potential interruptions or attacks by modifying an external clock during configuration.

**Type**

Enumeration

**Values**

- OFF
- ON
- On check
- On sticky

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name SECU_OPTION_FORCE_SDM_CLOCK_TO_INT_OSC <value>
```

**Default Value**

OFF
1.3.93. SECU_OPTION_LOCK_SECURITY_EFUSES

Programming this fuse prevents the future programming of any owner-accessible security policy fuses, not including key cancellation ID fuses.

**Type**

Enumeration

**Values**

- OFF
- ON
- On check
- On sticky

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name SECU_OPTION_LOCK_SECURITY_EFUSES <value>
```

**Default Value**

OFF
1.3.94. STRATIXII_CONFIGURATION_DEVICE

Specifies the configuration device that you want to use as the means of configuring the target device.

Old Name

STRATIX_II_CONFIGURATION_DEVICE

Type

String

Device Support

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name STRATIXII_CONFIGURATION_DEVICE <value>
```

Default Value

Auto
1.3.95. STRATIX_JTAG_USER_CODE

Specifies user-defined information about the target device. The JTAG user code is an extension of the option register. This data can be read with the JTAG USERCODE instruction.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10
- eASIC N5X

**Notes**

None

**Syntax**

```
set_global_assignment -name STRATIX_JTAG_USER_CODE <value>
```

**Default Value**

FFFFFFFF
1.3.96. TEMPERATURE_TAMPER_LOWER_BOUND

Specifies a signed fixed-point decimal value for the lower bound of the device temperature. Temperatures that exceed the lower bound you specify trigger an anti-tamper response when you have enabled a response.

**Type**

Integer

**Device Support**

- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name TEMPERATURE_TAMPER_LOWER_BOUND <value>
```

**Default Value**

-40
1.3.97. TEMPERATURE_TAMPER_UPPER_BOUND

Specifies a signed fixed-point decimal value for the upper bound of the device temperature. Temperatures that exceed the upper bound you specify trigger an anti-tamper response when you have enabled a response.

**Type**

Integer

**Device Support**

- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name TEMPERATURE_TAMPER_UPPER_BOUND <value>
```

**Default Value**

110
1.3.98. UNINITIALIZED_RAM_CONTENT_PATTERN

Set specified pattern for uninitialized RAM content pattern on specified instance

**Type**

Enumeration

**Values**

- 0000
- 0101
- 1010
- 1111
- OFF
- ON
- RANDOM

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_instance_assignment -name UNINITIALIZED_RAMCONTENT_PATTERN -to <to> <value>
```

**Example**

```
set_instance_assignment -name UNINITIALIZED_RAMCONTENT_PATTERN on -to ram_inst
```
1.3.99. USE_ALIAS_L1

Enable the use of AliasL1 feature.

Type

Boolean

Device Support

• Intel Agilex

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name USE_ALIAS_L1 <value>
```

Default Value

Off
1.3.100. USE_CHECKSUM_AS_USERCODE

Sets the JTAG user code to match the checksum value of the device programming file. The programming file is a Programmer Object File (.pof) for non-volatile devices, such as MAX II devices, or an SRAM Object File (.sof) for SRAM-based devices. If you turn this option on, the JTAG user code option is not available.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10
- eASIC N5X

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name USE_CHECKSUM_AS_USERCODE <value>
```

**Default Value**

On
1.3.101. USE_CONFIGURATION_DEVICE

Specifies that you intend to use a configuration device(s) such as the EPC2 as the means of configuring the target device. This option directs the Compiler to create a Programmer Output File (.pof) for programming the configuration device. If multiple configuration devices are needed, one POF is created for each device, with names of the following format: name.pof, name_1.pof, name_2.pof, etc.

**Type**

Boolean

**Device Support**

- EPC1
- EPC2
- Enhanced Configuration Devices
- Flash Memory
- Virtual JTAG TAP

**Notes**

None

**Syntax**

```plaintext
set_global_assignment -name USE_CONFIGURATION_DEVICE <value>
```
1.3.102. VCCL_SDM_VOLTAGE_DIFFERENCE_TRIGGER

Specify voltage difference trigger value on VCCL_SDM for tamper detection. It must be a valid 16-bit non-negative integer

**Type**

Integer

**Device Support**

- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCL_SDM_VOLTAGE_DIFFERENCE_TRIGGER <value>
```

**Default Value**

0
1.3.103. VCCL_VOLTAGE_DIFFERENCE_TRIGGER

Specify voltage difference trigger value on VCCL for tamper detection. It must be a valid 16-bit non-negative integer

**Type**

Integer

**Device Support**

- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```bash
set_global_assignment -name VCCL_VOLTAGE_DIFFERENCE_TRIGGER <value>
```

**Default Value**

0
1.3.104. VOLTAGE_TAMPER_DETECTION_TRIGGER

Specifies a voltage difference trigger value in percentage on all tamper detection power rails you enable. The percentage must be a valid 8-bit non-negative integer.

**Type**

Integer

**Device Support**

- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VOLTAGE_TAMPER_DETECTION_TRIGGER <value>
```

**Default Value**

15
1.4. Classic Timing Assignments

1.4.1. ANALYZE_LATCHES_AS_SYNCHRONOUS_ELEMENTS

Directs the Timing Analyzer to analyze latches as synchronous elements, rather than as combinational elements. Although latches continue to be implemented as a LUT feeding back onto itself, turning on this option directs the Timing Analyzer to analyze all latches as synchronous elements. Specifically, the clock enable is analyzed as an inverted clock. The Timing Analyzer reports the results of setup and hold analysis on these latches.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name ANALYZE_LATCHES_AS_SYNCHRONOUS_ELEMENTS <value>
```

**Default Value**

On
1.4.2. CUT_OFF_IO_PIN_FEEDBACK

Cuts off feedback from I/O pins during timing analysis. Cutting off I/O pin feedback is especially useful when a bidirectional pin is connected directly or indirectly to both the input and the output of a latch. This type of feedback path is continuous because it is not interrupted by any clocked logic primitives.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name CUT_OFF_IO_PIN_FEEDBACK <value>
```

**Default Value**

On
1.4.3. CUT_OFF_PATHS_BETWEEN_CLOCK_DOMAINS

Cuts the paths between registers clocked by unrelated clocks. This option makes the timing analysis reporting similar to MAX+PLUS II timing analysis reporting.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name CUT_OFF_PATHS_BETWEEN_CLOCK_DOMAINS <value>
```

**Default Value**

On
1.4.4. CUT_OFF_READ_DURING_WRITE_PATHS

Cuts the path from the write enable register through the ESB to a destination register.

Type
Boolean

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
None

Syntax

set_global_assignment -name CUT_OFF_READ_DURING_WRITE_PATHS <value>

Default Value
On
1.4.5. DEFAULT_HOLD_MULTICYCLE

Determines the default hold multicycle. The 'Same as Multicycle' setting ensures that the signal is latched on the final edge only. The 'One' setting assumes that the design can latch on any edge, up to and including the final edge. The 'Same as Multicycle' setting will give fewer hold time violation warnings. The 'One' setting is more restrictive, but it is the default setting for the Timing Analyzer and other third-party timing analyzers. This setting can be overridden on specific nodes with the Hold Multicycle option.

Type

Enumeration

Values

- One
- Same as Multicycle

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Notes

None

Syntax

```
set_global_assignment -name DEFAULT_HOLD_MULTICYCLE <value>
```

Default Value

Same as Multicycle

Example

```
set_global_assignment -name default_hold_multicycle "Same as Multicycle"
set_global_assignment -name default_hold_multicycle "One"
```

See Also

MULTICYCLE, SRC_MULTICYCLE, HOLD_MULTICYCLE, SRC_HOLD_MULTICYCLE, SETUP_RELATIONSHIP, HOLD_RELATIONSHIP
1.4.6. EMIF_SOC_PHYCLK_ADVANCE_MODELING

Instrucst routing annotation to adjust the AV-SoC Phyclk delays.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```plaintext
set_global_assignment -name EMIF_SOC_PHYCLK_ADVANCE_MODELING <value>
```

**Default Value**
Off
1.4.7. ENABLE_HPS_INTERNAL_TIMING

Enable HPS Internal Timing Characteristics

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name ENABLE_HPS_INTERNAL_TIMING <value>
```

**Default Value**

Off
1.4.8. FLOW_ENABLE_TIMING_ANALYZER_AFTER_PLAN_STAGE

Allows you to turn on or turn off running the Timing Analyzer after Plan stage during compilation.

**Old Name**
FLOW_ENABLE_TIMEQUEST_AFTER_PLAN_STAGE

**Type**
Boolean

**Device Support**
- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**
None

**Syntax**

```
set_global_assignment -name FLOW_ENABLE_TIMING_ANALYZER_AFTER_PLAN_STAGE <value>
```

**Default Value**
Off
1.4.9. IMPLEMENTS_FREE_RUNNING_CLOCK

Specifies if timing analysis should consider if a node implements a free-running clock versus assuming the node implement a clock that could be arbitrarily gated. The setting has implications on how end-of-life effects are applied.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment supports wildcards.
This assignment is copied to any duplicated nodes.
This assignment supports Fitter wildcards.
This assignment is included in the Fitter report.
The value of this assignment must be a node name.

**Syntax**

```
set_instance_assignment -name IMPLEMENTS_FREE_RUNNING_CLOCK -to <to> -entity <entity name> <value>
```
1.4.10. **INPUT_TRANSITION_TIME**

Specifies the input transition time. This assignment is used in Quartus to adjust the timing of the I/O buffers for all families that support AIOT. It is also used when generating the PrimeTime script that it is used by the HardCopy back end. This assignment gets converted as a set_input_transition SDC command. If the assignment does not exist, Quartus will generate a set_input_transition using 80% of VCCN * 1V/ns where VCCN depends on the I/O Standard used.

**Type**

Time

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports wildcards.

This assignment is copied to any duplicated nodes.

**Syntax**

```
set_instance_assignment -name INPUT_TRANSITION_TIME -to <to> -entity <entity name> <value>
```
1.4.11. MAX_CORE_JUNCTION_TEMP

This is the maximum core junction temperature that will be encountered during operation. Specified in degrees Celsius

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name MAX_CORE_JUNCTION_TEMP <value>
```
1.4.12. MIN_CORE_JUNCTION_TEMP

This is the minimum core junction temperature that will be encountered during operation. Specified in degrees Celsius

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name MIN_CORE_JUNCTION_TEMP <value>
```
1.4.13. MIN_MTBF_REQUIREMENT

Specifies the minimum acceptable Mean Time Between Failures (MTBF), either globally for the design or for a specific synchronizer chain (if applied to the head register of a synchronizer chain). The MTBF value used will be 10 to the power of this setting value, in years. If the MTBF of a synchronizer chain is less than this value, it will be marked as a dangerous, asynchronous transfer that is in need of additional synchronization registers to help avoid metastability.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**INTEGER_RANGE**

-8, 9

**Notes**

This assignment supports wildcards.

**Syntax**

```plaintext
set_global_assignment -name MIN_MTBF_REQUIREMENT <value>
set_instance_assignment -name MIN_MTBF_REQUIREMENT -to <to> -entity <entity name> <value>
```

**Default Value**

9
1.4.14. NOMINAL_CORE_SUPPLY_VOLTAGE

Specifies the voltage for the core power supply. For Stratix III devices, the core supply voltage applies only to the VCCL power rail. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name NOMINAL_CORE_SUPPLY_VOLTAGE <value>
```
1.4.15. PACKAGE_SKEW_COMPENSATION

Indicates that the package skew for the signal has been compensated by the board trace delays.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment supports Fitter wildcards.

**Syntax**

```
set_instance_assignment -name PACKAGE_SKEW_COMPENSATION -to <to> -entity <entity name> <value>
```
1.4.16. PLL_EXTERNAL_FEEDBACK_BOARD_DELAY

Specifies an external board delay between a feedback output pin and a feedback input pin (fbin) for a PLL in external feedback mode. This option is ignored if it is assigned to anything other than the fbin pin of a PLL.

Type
Time

Device Support
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes
None

Syntax

```plaintext
set_instance_assignment -name PLL_EXTERNAL_FEEDBACK_BOARD_DELAY -to <to> -entity <entity name> <value>
set_global_assignment -name PLL_EXTERNAL_FEEDBACK_BOARD_DELAY <value>
```
1.4.17. SDC_STATEMENT

Specifies the SDC statement to be evaluated by the Timing Analyzer.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name SDC_STATEMENT -entity <entity name> <value>
```

**Example**

```
set_global_assignment -name sdc_statement "set_multicycle_path -setup 2 -from *|mod_one -to *|mod_two" -entity "top|chip"
```
1.4.18. STA_AUTO_REPORT_SETUP_SUMMARY

Directs the Timing Analyzer to automatically generate Setup Summary report whenever this project is opened in an interactive Timing Analyzer session.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name STA_AUTO_REPORT_SETUP_SUMMARY <value>
```

**Default Value**

On
1.4.19. STA_AUTO_UPDATE_TIMING_NETLIST

Directs the Timing Analyzer to automatically create the timing netlist, read SDC constraints, and update the timing netlist whenever this project is opened in an interactive Timing Analyzer session.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name STA_AUTO_UPDATE_TIMING_NETLIST <value>
```

**Default Value**

On
1.4.20. TDC_AGGRESSIVE_HOLD_CLOSURE_EFFORT

Instructs the Fitter to aggressively optimize for hold timing closure.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name TDC_AGGRESSIVE_HOLD_CLOSURE_EFFORT <value>
```

**Default Value**
Off
1.4.21. TIMING_ANALYZER_DO_CCPP_REMOVAL

Directs the Timing Analyzer to remove common clock path pessimism (CCPP) during slack computation.

**Old Name**
TIMEQUEST_DO_CCPP_REMOVAL

**Type**
Boolean

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- EPC1
- EPC2
- Enhanced Configuration Devices
- Flash Memory
- Intel Stratix 10
- Virtual JTAG TAP

**Notes**
None

**Syntax**

```
set_global_assignment -name TIMING_ANALYZER_DO_CCPP_REMOVAL <value>
```
1.4.22. TIMING_ANALYZER_DO_REPORT_CDC_VIEWER

Directs the Timing Analyzer to report a table of all clock domain transfers for each analysis.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```python
set_global_assignment -name TIMING_ANALYZER_DO_REPORT_CDC_VIEWER <value>
```

**Default Value**

Off
1.4.23. TIMING_ANALYZER_DO_REPORT_TIMING

Directs the Timing Analyzer to report the worst-case path per clock domain and analysis.

**Old Name**
TIMEQUEST_DO_REPORT_TIMING

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
None

**Syntax**

```
set_global_assignment -name TIMING_ANALYZER_DO_REPORT_TIMING <value>
```

**Default Value**

Off
1.4.24. TIMING_ANALYZER_MULTICORNER_ANALYSIS

Directs the Timing Analyzer to perform multicorner timing analysis, which analyzes the design against best-case and worst-case operating conditions. Turning on this option does not enable multicorner analysis in the Fitter.

**Old Name**
TIMEQUEST_MULTICORNER_ANALYSIS

**Type**
Boolean

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- EPC1
- EPC2
- Enhanced Configuration Devices
- Flash Memory
- Intel Stratix 10
- Virtual JTAG TAP

**Notes**
None

**Syntax**

```
set_global_assignment -name TIMING_ANALYZER_MULTICORNER_ANALYSIS <value>
```
1.4.25. TIMING_ANALYZER_REPORT_NUM_WORST_CASE_TIMING_PATHS

Specifies the maximum number of worst-case timing paths for the Timing Analyzer to report per clock domain and analysis.

**Old Name**
TIMEQUEST_REPORT_NUM_WORST_CASE_TIMING_PATHS

**Type**
Integer

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**INTEGER_RANGE**
1, 100000

**Notes**
None

**Syntax**

```plaintext
set_global_assignment -name TIMING_ANALYZER_REPORT_NUM_WORST_CASE_TIMING_PATHS <value>
```

**Default Value**
10
1.4.26. TIMING_ANALYZER_REPORT_SCRIPT

Specifies the name of the tcl script that will be used to overwrite the default Timing Analyzer report panels created during a normal compile.

**Old Name**

TIMEQUEST_REPORT_SCRIPT

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name TIMING_ANALYZER_REPORT_SCRIPT <value>
```
1.4.27. TIMING_ANALYZER_REPORT_SCRIPT_INCLUDE_DEFAULT_ANALYSIS

Directs the Timing Analyzer to perform default timing analysis prior to running the user-specified report script specified by TIMING_ANALYZER_REPORT_SCRIPT.

Old Name
TIMEQUEST_REPORT_SCRIPT_INCLUDE_DEFAULT_ANALYSIS

Type
Boolean

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Syntax

set_global_assignment -name TIMING_ANALYZER_REPORT_SCRIPT_INCLUDE_DEFAULT_ANALYSIS <value>

Default Value
On
1.4.28. TIMING_ANALYZER_REPORT_WORST_CASE_TIMING_PATHS

Directs the Timing Analyzer to report worst-case timing paths per clock domain and analysis.

**Old Name**

TIMEQUEST_REPORT_WORST_CASE_TIMING_PATHS

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- EPC1
- EPC2
- Enhanced Configuration Devices
- Flash Memory
- Intel Stratix 10
- Virtual JTAG TAP

**Notes**

None

**Syntax**

```set_global_assignment -name TIMING_ANALYZER_REPORT_WORST_CASE_TIMING_PATHS <value>```

**Default Value**

On
1.4.29. TIMING_ANALYZER_SIMULTANEOUS_MULTICORNER_ANALYSIS

When multicorner timing analysis is enabled, directs the Timing Analyzer to analyze all corners at once, rather than only analyzing corners that are explicitly asked for. This can save time when it is known that analysis of multiple corners will be needed at some point. If analysis is only needed for a single corner, turning off this setting will save memory.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name TIMING_ANALYZER_SIMULTANEOUS_MULTICORNER_ANALYSIS <value>
```

**Default Value**

On
1.4.30. TIMING_ANALYZER_REPORT_WORST_CASE_TIMING_PATHS_SHOW_ROUTING

Toggles detailed routing information for each timing path.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
None

**Syntax**

```
set_global_assignment -name TIMING_ANALYZER_REPORT_WORST_CASE_TIMING_PATHS_SHOW_ROUTING <value>
```

**Default Value**
Off
1.4.31. USE_DLL_FREQUENCY_FOR_DQS_DELAY_CHAIN

Instructs STA to take DLL frequency into account while calculating phase shift of DQS delay chain

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name USE_DLL_FREQUENCY_FOR_DQS_DELAY_CHAIN <value>
```

**Default Value**

Off
1.5. Compiler Assignments

1.5.1. ALLOW_REGISTER_DUPLICATION

Controls whether the Compiler is allowed to duplicate registers to improve design performance. When register duplication is allowed, the Compiler may perform optimizations that create a second copy of a register and move a portion of its fan-out to this new node, in order to improve routability and/or reduce the total routing wire required to route a net with many fan-outs. If register duplication is disabled, optimizations that retime registers will also be disabled. This setting affects Analysis & Synthesis and the Fitter.

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

This assignment is included in the Fitter report.
This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name ALLOW_REGISTER_DUPLICATION <value>
```

**Default Value**

On

**Example**

```
set_global_assignment -name allow_register_duplication on
```
1.5.2. ALLOW_REGISTER_MERGING

Controls whether the Compiler is allowed to remove registers that are identical to other registers in the design. When register merging is allowed, in cases where two registers generate the same logic, one may be deleted and the remaining one will be made to also fan-out to the deleted register’s destinations. This option is useful if you wish to prevent the Compiler from removing duplicate registers that you have used deliberately.

If register merging is disabled, optimizations that retime registers will also be disabled. This setting affects Analysis & Synthesis and the Fitter.

Type
Boolean

Device Support
- Intel Arria 10
- Intel Cyclone 10 GX

Notes
This assignment is included in the Fitter report.
This assignment is included in the Analysis & Synthesis report.

Syntax

```
set_global_assignment -name ALLOW_REGISTER_MERGING <value>
```

Default Value
On

Example

```
set_global_assignment -name allow_register_merging off
```
1.5.3. ALLOW_REGISTER_RETIMING

Controls whether the Compiler is allowed to retime registers to improve design performance. When register retiming is allowed, the Compiler may perform optimizations that move combinational logic across register boundaries, maintaining the overall logic of the design component but also balancing the data path delays between each register. This setting affects the Fitter.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
This assignment supports wildcards.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ALLOW_REGISTER_RETIMING <value>
set_instance_assignment -name ALLOW_REGISTER_RETIMING -to <to> -entity <entity name> <value>
```

**Default Value**
On

**Example**

```
set_global_assignment -name allow_register_retiming on
```
1.5.4. OPTIMIZATION_MODE

Controls the Compiler's high-level optimization strategy. By default, the Quartus Prime Compiler optimizes in a balanced mode, targeting the design's timing constraints. The alternate modes cause the Compiler to prioritize a particular optimization metric. High effort modes primarily enable additional optimizations that increase compilation time. Superior and Aggressive modes may increase compilation time and also make trade-offs that may harm the other optimization metrics (performance, area, etc.).

'High Performance Effort' mode will cause the compiler to target increased positive timing margin, increase the timing optimization effort applied during placement and routing, and enable timing-related Physical Synthesis optimizations (as allowed by the register optimization settings below). Each of these additional optimizations can increase compilation time. 'Superior Performance' mode enables the same optimizations as 'High Performance Effort' mode, and additionally enables options during Analysis & Synthesis to maximize design performance at a potential increase to logic area. If design utilization is already very high, this option may lead to difficulty in fitting which could also negatively affect overall optimization quality. Modes with Maximum Placement Effort increase placement optimization effort by an additional amount.

'High Routability Effort' modes guide Placement or Packing to spend additional compilation time reducing routing utilization, which can improve routability and also saves dynamic power. 'Optimize Netlist for Routability' mode makes netlist modifications to increase routability at the possible expense of performance. In 'Aggressive Power' mode, the Compiler will further target reducing the routing usage of signals with the highest specified (via Signal Activity File) or estimated toggle rates, saving additional dynamic power but potentially affecting performance.

'Aggressive Area' mode instructs the Compiler to target an area minimal solution, even if this reduces overall timing performance.

'Aggressive Compile Time' mode instructs the Compiler to reduce performance optimization effort and perform minimal reporting in order to save compile time.

This setting affects Analysis & Synthesis and the Fitter.

Type

Enumeration

Values

- Aggressive Area
- Aggressive Compile Time
- Aggressive Power
- Balanced
- High Packing Routability Effort
- High Performance Effort
- High Performance Effort with Maximum Placement Effort
- High Placement Routability Effort
- High Power Effort
- High Routability Effort
- Optimize Netlist for Routability
- Superior Performance
- Superior Performance with Maximum Placement Effort


**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

This assignment is included in the Analysis & Synthesis report.

**Syntax**

```
set_global_assignment -name OPTIMIZATION_MODE <value>
```

**Default Value**

Balanced
1.6. Design Assistant Assignments

1.6.1. CLK_RULE_CLKNET_CLKSPINES_THRESHOLD

Specifies the threshold value for clock net not mapped to clock spines rule.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name CLK_RULE_CLKNET_CLKSPINES_THRESHOLD <value>
```

**Default Value**

25
1.6.2. DA_CUSTOM_RULE_FILE

Used to set the path for DA custom rule file

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name DA_CUSTOM_RULE_FILE <value>
```
1.6.3. DESIGN_ASSISTANT_EXCLUDE

Specify that a Design Assistant rule should ignore the target of the assignment. If set on an instance, the exclusion applies to the whole contents of that instance, regardless of any DESIGN_ASSISTANT_INCLUDE assignments targeting any sub-instance. If the assignment is global, or if it's set on the design root, it can be overridden by DESIGN_ASSISTANT_INCLUDE assignments to instances.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment supports wildcards.

This assignment is copied to any duplicated nodes.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name DESIGN_ASSISTANT_EXCLUDE <value>
set_instance_assignment -name DESIGN_ASSISTANT_EXCLUDE -to <to> -entity <entity name> <value>
```
1.6.4. DESIGN_ASSISTANT_INCLUDE

Specify that a Design Assistant rule should not ignore the target of the assignment. It can only be used to override a DESIGN_ASSISTANT_EXCLUDE assignment set globally or on the design root.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment supports wildcards.
This assignment is copied to any duplicated nodes.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name DESIGN_ASSISTANT_INCLUDE <value>
set_instance_assignment -name DESIGN_ASSISTANT_INCLUDE -to <to> -entity <entity name> <value>
```
1.6.5. DRC_DEADLOCK_STATE_LIMIT

Specifies the maximum number of states that you want the Design Assistant to detect as a deadlock condition. A larger number will result in longer processing time.

**Type**
Integer

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name DRC_DEADLOCK_STATE_LIMIT <value>
```

**Default Value**

2
1.6.6. DRC_DETAIL_MESSAGE_LIMIT

Specifies the maximum number of detail messages that you want the Design Assistant to report.

**Type**
Integer

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**
```
set_global_assignment -name DRC_DETAIL_MESSAGE_LIMIT <value>
```

**Default Value**
10
1.6.7. DRC_FANOUT_EXCEEDING

Specifies the minimum amount of fan-out that a node must have to be reported by the Design Assistant.

Type

Integer

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```
set_global_assignment -name DRC_FANOUT_EXCEEDING <value>
```

Default Value

30
1.6.8. DRC_GATED_CLOCK_FEED

Specifies the minimum amount of clock port a gated clock must feed so that it’s an acceptable gated clock.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name DRC_GATED_CLOCK_FEED <value>
```

**Default Value**

30
1.6.9. DRC_REPORT_FANOUT_EXCEEDING

Directs the Design Assistant to report all nodes with more than the specified amount of fan-out.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name DRC_REPORT_FANOUT_EXCEEDING <value>
```
1.6.10. DRC_REPORT_TOP_FANOUT

Directs the Design Assistant to report the specified number of nodes with the highest fan-out.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name DRC_REPORT_TOP_FANOUT <value>
```
1.6.11. DRC_TOP_FANOUT

Specifies the number of nodes with the highest fan-out that you want the Design Assistant to report.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name DRC_TOP_FANOUT <value>
```

**Default Value**

50
1.6.12. DRC_VIOLATION_MESSAGE_LIMIT

Specifies the maximum number of violation messages that you want the Design Assistant to report.

**Type**
Integer

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name DRC_VIOLATION_MESSAGE_LIMIT <value>
```

**Default Value**
30
1.6.13. HARDCOPY_FLOW_AUTOMATION

Specifies which HardCopy flow will be run in HardCopy timing wizard

**Type**

Enumeration

**Values**

- COMPILE_NEW_PROJECT
- FULL_COMPILATION
- MIGRATION_ONLY

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name HARDCOPY_FLOW_AUTOMATION <value>
```

**Default Value**

MIGRATION_ONLY
1.6.14. HARDCOPY_NEW_PROJECT_PATH

Specifies the directory path for the new/migrated HardCopy project.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name HARDCOPY_NEW_PROJECT_PATH <value>
```
1.6.15. HCPY_CAT

Direct Design Assistant to detect HardCopy rules on the design. All HardCopy rules apply to HardCopy devices only.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name HCPY_CAT <value>
```
1.6.16. HCPY_PLL_MULTIPLE_CLK_NETWORK_TYPES

Direct Design Assistant to detect PLL that feeds multiple clock network types.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name HCPY_PLL_MULTIPLE_CLK_NETWORK_TYPES <value>
```
1.6.17. HCPY_VREF_PINS

Direct Design Assistant to detect VREF pins on the design. This rule applies to HardCopy devices only.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name HCPY_VREF_PINS <value>
```
1.7. Design Partition Assignments

1.7.1. ABSORB_PATHS_FROM_OUTPUTS_TO_INPUTS

Allows the Compiler to optimize connections from a partition's outputs to its inputs by making the path internal to the partition. You must also enable the cross-boundary optimizations feature for this partition using the CROSS_BOUNDARY_OPTIMIZATIONS assignment.

_Type

Boolean

_Device Support_

• This setting can be used in projects targeting any Intel FPGA device family.

_Notes_

None

_Syntax_

```
set_global_assignment -name ABSORB_PATHS_FROM_OUTPUTS_TO_INPUTS -entity <entity name> -section_id <section identifier> <value>
set_instance_assignment -name ABSORB_PATHS_FROM_OUTPUTS_TO_INPUTS -to <to> -entity <entity name> -section_id <section identifier> <value>
```  

_Default Value_

On, requires section identifier and entity name
1.7.2. AUTOMATIC_DANGLING_PORT_TIEOFF

Disable automatic tie-off of dangling boundary ports in the partition rooted at the specified instance.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_instance_assignment -name AUTOMATIC_DANGLING_PORT_TIEOFF -to <to> <value>
```
1.7.3. CROSS_BOUNDARY_OPTIMIZATIONS

This setting specifies whether the Compiler should optimize across the partition’s boundary. If enabled, the Compiler may be able to optimize the logic inside the partition by applying various cross-boundary optimizations, such as constant propagation and dangling logic removal. Specific cross-boundary optimizations are enabled by individual assignments.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```plaintext
set_global_assignment -name CROSS_BOUNDARY_OPTIMIZATIONS -entity <entity name> -section_id <section identifier> <value>
set_instance_assignment -name CROSS_BOUNDARY_OPTIMIZATIONS -to <to> -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

Off, requires section identifier and entity name
1.7.4. EMPTY

Directs the compiler to empty a partition.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

**Syntax**

```
set_instance_assignment -name EMPTY -to <to> -entity <entity name> <value>
```
1.7.5. ENABLE_LAB_SHARING_WITH_PARENT_PARTITION

Allows logic from the target partition to share LAB resources with the immediate
parent partition.

Type
Boolean

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes

Syntax

set_instance_assignment -name ENABLE_LAB_SHARING_WITH_PARENT_PARTITION -to <to>
-entity <entity name> -section_id <section identifier> <value>
1.7.6. ENTITY_REBINDING

Entity Re-binding binds the Partial Reconfiguration/Reserved Core partition instance to its corresponding entity.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_instance_assignment -name ENTITY_REBINDING -to <to> -entity <entity name> <value>
```
1.7.7. EXPORT_BLOCK_NAME_OBFUSCATION

Obfuscate all names under this hierarchy during export.

Type
Boolean

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```
set_instance_assignment -name EXPORT_BLOCK_NAME_OBFUSCATION -to <to> <value>
```
1.7.8. IGNORE_PARTITIONS

Specifies whether the compiler should ignore partition assignments in the project.

Type

Boolean

Device Support

• This setting can be used in projects targeting any Intel FPGA device family.

Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

Syntax

```set_global_assignment -name IGNORE_PARTITIONS <value>```

Default Value

Off
1.7.9. INCREMENTAL_COMPILATION_EXPORT_FLATTEN

Specifies whether the netlist exported to the QXP file should flatten sub-partitions

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is not copied when you create a companion revision for HardCopy II devices.

**Syntax**

```
set_global_assignment -name INCREMENTAL_COMPILATION_EXPORT_FLATTEN <value>
```
1.7.10. INCREMENTAL_COMPILATION_EXPORT_POST_FIT

Specifies whether the exported QXP file contains the post-fit netlist

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is not copied when you create a companion revision for HardCopy II devices.

**Syntax**

```plaintext```
set_global_assignment -name INCREMENTAL_COMPILATION_EXPORT_POST_FIT <value>
```plaintext```
1.7.11. INCREMENTAL_COMPILATION_EXPORT_POST_SYNTH

Specifies whether the exported QXP file contains the post-synthesis netlist

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
This assignment is not copied when you create a companion revision for HardCopy II devices.

**Syntax**

```
set_global_assignment -name INCREMENTAL_COMPILATION_EXPORT_POST_SYNTH <value>
```
1.7.12. INSERT_BOUNDARY_WIRE_LUTS

Enables wire lut insertion for boundary ports in the given partition (the partition is named by hierarchy path). This ensures that the inputs and outputs can have their locations preserved, which is useful for partial reconfiguration and compiling a design containing a blackbox.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

**Syntax**

```
set_instance_assignment -name INSERT_BOUNDARY_WIRE_LUTS -to <to> -entity <entity name> <value>
```
1.7.13. MERGE_EQUIVALENT_BIDIRS

Allows the Compiler to merge electrically equivalent bidirectional inputs. You must also enable the cross-boundary optimizations feature for this partition using the CROSS_BOUNDARY_OPTIMIZATIONS assignment.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```plaintext
set_global_assignment -name MERGE_EQUIVALENT_BIDIRS -entity <entity name> -section_id <section identifier> <value>
set_instance_assignment -name MERGE_EQUIVALENT_BIDIRS -to <to> -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

On, requires section identifier and entity name
1.7.14. MERGE_EQUIVALENT_INPUTS

Allows the Compiler to merge inputs connected to the same source. You must also enable the cross-boundary optimizations feature for this partition using the CROSS_BOUNDARY_OPTIMIZATIONS assignment.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name MERGE_EQUIVALENT_INPUTS -entity <entity name> -section_id <section identifier> <value>
set_instance_assignment -name MERGE_EQUIVALENT_INPUTS -to <to> -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

On, requires section identifier and entity name
1.7.15. PARTIAL_RECONFIGURATION_PARTITION

Specifies if this partition in the design is partially reconfigurable.

**Old Name**

PR_PARTITION

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

**Syntax**

```
set_instance_assignment -name PARTIAL_RECONFIGURATION_PARTITION -to <to> -
entity <entity name> <value>
```
1.7.16. PARTITION

Creates a partition rooted at the specified instance. When an instance is defined as a partition, its hierarchical boundaries are fixed, allowing it to be independently exported or imported in many cases. The value of this assignment is the name of the design block that contains the implementation for the partition. The partition name must be unique in the complete design across all hierarchies.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_instance_assignment -name PARTITION -to <to> -entity <entity name> <value>
```
### 1.7.17. PARTITION_ALWAYS_USE_QXP_NETLIST

Specifies whether to always use the netlist in the QXP file associated with the partition, either because the QXP file is imported into the partition, or is specified as a source file for the partition. Setting defaults to off.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is not copied when you create a companion revision for HardCopy II devices.

**Syntax**

```plaintext
set_global_assignment -name PARTITION_ALWAYS_USE_QXP_NETLIST -entity <entity name> -section_id <section identifier> <value>
set_instance_assignment -name PARTITION_ALWAYS_USE_QXP_NETLIST -to <to> -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

Off, requires section identifier and entity name
1.7.18. PARTITION_ASD_REGION

Specifies the advanced SEU detection region assignment for this partition.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

**Syntax**

```plaintext
set_instance_assignment -name PARTITION_ASD_REGION -to <to> -entity <entity name> <value>
```
1.7.19. PARTITION_ASD_REGION_ID

Indicates the advanced sensitivity detection region assignment for this partition.

**Type**
Integer

**Device Support**
- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**
This assignment is not copied when you create a companion revision for HardCopy II devices.

**Syntax**

```
set_global_assignment -name PARTITION_ASD_REGION_ID -entity <entity name> -section_id <section identifier> <value>
set_instance_assignment -name PARTITION_ASD_REGION_ID -to <to> -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**
1, requires section identifier and entity name
1.7.20. PARTITION_IGNORE_SOURCE_FILE_CHANGES

Specifies whether to use the requested post-synthesis or post-fit netlist when it is available, even when source file changes are present. Setting defaults to off.

Type

Boolean

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

Syntax

```
set_global_assignment -name PARTITION_IGNORE_SOURCE_FILE_CHANGES -entity <entity name> -section_id <section identifier> <value>
set_instance_assignment -name PARTITION_IGNORE_SOURCE_FILE_CHANGES -to <to> -entity <entity name> -section_id <section identifier> <value>
```

Default Value

Off, requires section identifier and entity name
1.7.21. PARTITION_PRESERVE_HIGH_SPEED_TILES

Specifies whether to preserve the high-speed tiles in the post-fit netlist, if applicable.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is not copied when you create a companion revision for HardCopy II devices.

**Syntax**

```
set_global_assignment -name PARTITION_PRESERVE_HIGH_SPEED_TILES -entity <entity name> -section_id <section identifier> <value>
set_instance_assignment -name PARTITION_PRESERVE_HIGH_SPEED_TILES -to <to> -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

On, requires section identifier and entity name
1.7.22. PRESERVE

Directs the compiler to preserve the existing results of a partition. The value of this assignment is the snapshot to preserve, such as \"final\" or \"placed\". If the specified snapshot does not exist, the compiler will exit with an error message. By default, the partition’s results will not be preserved unless the only results available for the partition are later than the stage currently being compiled. For example, if the only snapshot for a partition is the \"placed\" snapshot, the Fitter will preserve the partition until the end of placement, and will not attempt to preserve it during routing.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_instance_assignment -name PRESERVE -to <to> -entity <entity name> <value>
```
1.7.23. PROPAGATE_CONSTANTS_ON_INPUTS

Allows the Compiler to use constants on a partition input to optimize the logic in the partition. You must also enable the cross-boundary optimizations feature for the partition using the CROSS_BOUNDARY_OPTIMIZATIONS assignment.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```plaintext
set_global_assignment -name PROPAGATE_CONSTANTS_ON_INPUTS -entity <entity name> -section_id <section identifier> <value>
set_instance_assignment -name PROPAGATE_CONSTANTS_ON_INPUTS -to <to> -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

On, requires section identifier and entity name
1.7.24. PROPAGATE_INVERSIONS_ON_INPUTS

Specifies that the Compiler should push inversions into partition inputs when possible. This cross-boundary optimization is especially important when inverted clock or asynchronous signals are connected to a partition input. Without this optimization, the Compiler may need to implement the inversion with a logic cell, introducing skew on the clock or reset path. The partition must also have enabled cross-boundary optimizations with the CROSS_BOUNDARY_OPTIMIZATIONS assignment.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name PROPAGATE_INVERSIONS_ON_INPUTS -entity <entity name> -section_id <section identifier> <value>
set_instance_assignment -name PROPAGATE_INVERSIONS_ON_INPUTS -to <to> -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

On, requires section identifier and entity name
1.7.25. QDB_FILE_PARTITION

Similar to the PARTITION assignment, this assignment creates a partition rooted at the specified instance. When an instance is defined as a partition, its hierarchical boundaries are fixed, allowing it to be independently exported or imported in many cases. The value of the assignment is the QDB partition archive that will be imported into the partition during Synthesis.

If a PARTITION and QDB_FILE_PARTITION assignment target the same instance then the PARTITION assignment determines the partition’s name. If no PARTITION assignment exists then the partition name will be automatically created.

**Type**

File name

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_instance_assignment -name QDB_FILE_PARTITION -to <to> -entity <entity name> <value>
```
1.7.26. QDB_PATH

Specify path to read and write compiler generated database to a directory other than project directory.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name QDB_PATH <value>
```

1.7.27. REMOVE_LOGIC_ON_UNCONNECTED_OUTPUTS

Allows the Compiler to remove logic connected to dangling partitions outputs. You must also enable the cross-boundary optimizations feature for this partition using the CROSS_BOUNDARY_OPTIMIZATIONS assignment.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name REMOVE_LOGIC_ON_UNCONNECTED_OUTPUTS -entity <entity name> -section_id <section identifier> <value>
set_instance_assignment -name REMOVE_LOGIC_ON_UNCONNECTED_OUTPUTS -to <to> -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

On, requires section identifier and entity name
1.7.28. RESERVED_CORE

Specifies that a core design partition can be compiled with preserved periphery from a Partition Database File (.qdb).

Old Name
PERIPHERY_REUSE_CORE

Type
Boolean

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes

Syntax

```
set_instance_assignment -name RESERVED_CORE -to <to> -entity <entity name> <value>
```
**1.7.29. RTL_PARAMETER**

Assignment can be used to override RTL parameters on verilog/vhdl modules that are instantiated from a pre-compiled partition.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_instance_assignment -name RTL_PARAMETER -to <to> -entity <entity name> <value>
```
1.8. EDA Netlist Writer Assignments

1.8.1. EDA_BOARD_BOUNDARY_SCAN_OPERATION

Specify the BSDL file operation either for pre-configuration or post-configuration

**Type**

Enumeration

**Values**

- POST_CONFIG
- PRE_CONFIG

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```plaintext
set_global_assignment -name EDA_BOARD_BOUNDARY_SCAN_OPERATION -section_id <section identifier> <value>
```

**Default Value**

PRE_CONFIG, requires section identifier
1.8.2. EDA_BOARD_DESIGN_BOUNDARY_SCAN_TOOL

Specifies the boundary scan format used for board level boundary scan testing.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name EDA_BOARD_DESIGN_BOUNDARY_SCAN_TOOL <value>
set_global_assignment -name EDA_BOARD_DESIGN_BOUNDARY_SCAN_TOOL -entity <entity name> <value>
```

**Default Value**

<None>
1.8.3. EDA_BOARD_DESIGN_SIGNAL_INTEGRITY_TOOL

Specifies the EDA third-party tool used for board level signal integrity analysis.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name EDA_BOARD_DESIGN_SIGNAL_INTEGRITY_TOOL <value>
set_global_assignment -name EDA_BOARD_DESIGN_SIGNAL_INTEGRITY_TOOL -entity <entity name> <value>
```

**Default Value**

<None>
1.8.4. EDA_BOARD_DESIGN_SYMBOL_TOOL

Specifies the EDA third-party tool used for board level schematic design.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name EDA_BOARD_DESIGN_SYMBOL_TOOL <value>
set_global_assignment -name EDA_BOARD_DESIGN_SYMBOL_TOOL -entity <entity name> <value>
```

Default Value

<None>
1.8.5. EDA_BOARD_DESIGN_TIMING_TOOL

Specifies the EDA third-party tool used for board level timing analysis.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```text
set_global_assignment -name EDA_BOARD_DESIGN_TIMING_TOOL <value>
set_global_assignment -name EDA_BOARD_DESIGN_TIMING_TOOL -entity <entity name> <value>
```

**Default Value**

<None>
1.8.6. EDA_BOARD_DESIGN_TOOL

Specifies the EDA third-party tool used for board level design and analysis.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name EDA_BOARD_DESIGN_TOOL <value>
set_global_assignment -name EDA_BOARD_DESIGN_TOOL -entity <entity name> <value>
```

**Default Value**

<None>
1.8.7. EDA_DESIGN EXTRA ALTERA SIM_LIB

Specify additional ALTERA simulation model libraries required is used by the design files

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name EDA_DESIGN_EXTRA_ALTERA_SIM_LIB -section_id <section_identifier> <value>
```
1.8.8. EDA_DESIGN_INSTANCE_NAME

Specify the instance name of the design in the test bench

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name EDA_DESIGN_INSTANCE_NAME -section_id <section_identifier> <value>
```
1.8.9. EDA_ENABLE_GLITCH_FILTERING

Write logic to filter glitches in the simulation netlist.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```plaintext
set_global_assignment -name EDA_ENABLE_GLITCH_FILTERING -section_id <section identifier> <value>
set_global_assignment -name EDA_ENABLE_GLITCH_FILTERING -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

Off, requires section identifier
1.8.10. EDA_ENABLE_IPUTF_MODE

Allows you to simulate designs containing hw.tcl based IP cores. This may require adding .sip files to your Quartus Prime project. This variable may be removed in future releases.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name EDA_ENABLE_IPUTF_MODE -section_id <section identifier> <value>
set_global_assignment -name EDA_ENABLE_IPUTF_MODE -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

On, requires section identifier
1.8.11. EDA_EXTRA_ELAB_OPTION

Additional custom simulation elaboration options for one or more simulators.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```bash
set_global_assignment -name EDA_EXTRA_ELAB_OPTION -section_id <section_identifier> <value>
set_global_assignment -name EDA_EXTRA_ELAB_OPTION -entity <entity name> -section_id <section_identifier> <value>
```

**Default Value**

"", requires section identifier
1.8.12. EDA_FLATTEN_BUSES

Flattens all buses when creating the VHDL Output File (.vho). You should turn on this option if your third-party EDA environment does not support buses.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name EDA_FLATTEN_BUSES -section_id <section identifier> <value>
set_global_assignment -name EDA_FLATTEN_BUSES -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

Off, requires section identifier
1.8.13. EDA_FORCE_GATE_LEVEL_REG_INIT_X

Modifies output gate level simulation netlist to force all registers to initialize to X (don't care) and propagate X

Type
Boolean

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name EDA_FORCE_GATE_LEVEL_REG_INIT_X -section_id <section identifier> <value>
set_global_assignment -name EDA_FORCE_GATE_LEVEL_REG_INIT_X -entity <entity name> -section_id <section identifier> <value>
```

Default Value
Off, requires section identifier
1.8.14. EDA_FORMAL_VERIFICATION_ALLOW_RETIMING

Allow register retiming to be turned on for formal verification

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EDA_FORMAL_VERIFICATION_ALLOW_RETIMING -section_id <section_identifier> <value>
set_global_assignment -name EDA_FORMAL_VERIFICATION_ALLOW_RETIMING -entity <entity_name> -section_id <section_identifier> <value>
```

**Default Value**

Off, requires section identifier
1.8.15. EDA_FORMAL_VERIFICATION_TOOL

Specifies the EDA third-party tool used for formal verification.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name EDA_FORMAL_VERIFICATION_TOOL <value>
set_global_assignment -name EDA_FORMAL_VERIFICATION_TOOL -entity <entity name> <value>
```

Default Value

<None>
1.8.16. EDA_FV_HIERARCHY

Determines how the hierarchy of design entities is to be processed during compilation. 'BLACKBOX' setting causes the entity to be handled as a black-box in the EDA flow. 'NONE' setting is the default and means no special handling to be done. The option applies only to the design entity to which it is assigned; lower-level entities do not inherit their parent entity's setting for this option.

**Type**

Enumeration

**Values**

- BLACKBOX
- Off

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```plaintext
set_global_assignment -name EDA_FV_HIERARCHY -entity <entity name> <value>
set_instance_assignment -name EDA_FV_HIERARCHY -to <to> -entity <entity name> <value>
```
1.8.17. EDA_GENERATE_POWER_INPUT_FILE

Generates a Power Input File (.pwf) to perform power analysis in the Quartus Prime software when using third-party simulation tools.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name EDA_GENERATE_POWER_INPUT_FILE -section_id <section identifier> <value>
set_global_assignment -name EDA_GENERATE_POWER_INPUT_FILE -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

Off, requires section identifier
1.8.18. EDA_GENERATE_SDF_FOR_POWER

Enable generation of SDO file containing delay estimates back-annotated on design netlist for improved accuracy of power estimates. This is only supported for Verilog Output simulation in ModelSim

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name EDA_GENERATE_SDF_FOR_POWER -section_id <section identifier> <value>
set_global_assignment -name EDA_GENERATE_SDF_FOR_POWER -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

Off, requires section identifier
1.8.19. EDA_GENERATE_TIMING_CLOSURE_DATA

Generates back-annotation data for performing in-place optimization with the LeonardoSpectrum software.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name EDA_GENERATE_TIMING_CLOSURE_DATA -section_id <section identifier> <value>
set_global_assignment -name EDA_GENERATE_TIMING_CLOSURE_DATA -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

Off, requires section identifier
1.8.20. EDA_IBIS_EXTENDED_MODEL_SELECTOR

Enable or disable information about related IO Standards in the model selector section of IBIS files. Will turn on EDA_IBIS_MODEL_SELECTOR when set to true.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EDA_IBIS_EXTENDED_MODEL_SELECTOR -section_id <section_identifier> <value>
set_global_assignment -name EDA_IBIS_EXTENDED_MODEL_SELECTOR -entity <entity name> -section_id <section_identifier> <value>
```

**Default Value**

Off, requires section identifier
1.8.21. EDA_IBIS_MODEL_SELECTOR

Enable or disable model selector feature for IBIS Writer

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EDA_IBIS_MODEL_SELECTOR -section_id <section identifier> <value>
set_global_assignment -name EDA_IBIS_MODEL_SELECTOR -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

Off, requires section identifier
1.8.22. EDA_IBIS_MUTUAL_COUPLING

Allows you to print the per pin RLC package model with mutual coupling when
generating IBIS Output Files (.ibs) with the EDA Netlist Writer. The lumped RLC
package model information appears in the IBIS Output File.

Type

Boolean

Device Support

• This setting can be used in projects targeting any Intel FPGA device family.

Syntax

set_global_assignment -name EDA_IBIS_MUTUAL_COUPLING -section_id <section identifier> <value>
set_global_assignment -name EDA_IBIS_MUTUAL_COUPLING -entity <entity name> -section_id <section identifier> <value>

Default Value

Off, requires section identifier
1.8.23. EDA_IBIS_SPECIFICATION_VERSION

Specifies the IBIS Specification version.

**Type**

Enumeration

**Values**

- 4p2
- 5p0

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Syntax**

```bash
set_global_assignment -name EDA_IBIS_SPECIFICATION_VERSION -section_id <section_identifier> <value>
```

**Default Value**

4p2, requires section identifier
1.8.24. EDA_IPFS_FILE

Specifies the library to which IPFS file should be compiled

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```bash
set_global_assignment -name EDA_IPFS_FILE -section_id <section identifier> <value>
```
1.8.25. EDA_LAUNCH_CMD_LINE_TOOL

Allows you to launch third-party EDA tools in the command-line mode rather than opening the graphical user interface.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name EDA_LAUNCH_CMD_LINE TOOL -section_id <section identifier> <value>
set_global_assignment -name EDA_LAUNCH_CMD_LINE TOOL -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**
Off, requires section identifier
1.8.26. EDA_MAP_ILLEGAL_CHARACTERS

Maps the vertical bar (|), tilde (~), and colon (:) characters in Quartus Prime hierarchical node names to the legal Verilog HDL characters z, x, and underscore (_), respectively, in Verilog Output Files. Turning on this option also maps other illegal non-alphanumeric characters, including brackets [], parentheses (), angle brackets <>, and braces {} to underscores (_).

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name EDA_MAP_ILLEGAL_CHARACTERS -section_id <section identifier> <value>
set_global_assignment -name EDA_MAP_ILLEGAL_CHARACTERS -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

Off, requires section identifier
1.8.27. EDA_NATIVELINK_GENERATE_SCRIPT_ONLY

Allows you to generate the script for a third-party EDA tool without running the EDA tool.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name EDA_NATIVELINK_GENERATE_SCRIPT_ONLY -section_id <section identifier> <value>
```

**Default Value**

Off, requires section identifier
1.8.28. EDA_NATIVELINK_PORTABLE_FILE_PATHS

Specifies that the file paths in the generated third-party EDA tool command scripts should be written out using relative paths for design and testbench files, and by using a variable to refer to Quartus Prime simulation library path.

Type

Boolean

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name EDA_NATIVELINK_PORTABLE_FILE_PATHS -section_id <section identifier> <value>
set_global_assignment -name EDA_NATIVELINK_PORTABLE_FILE_PATHS -entity <entity name> -section_id <section identifier> <value>
```

Default Value

Off, requires section identifier
1.8.29. **EDA_NATIVELINK_SIMULATION_SETUP_SCRIPT**

Specify the script for EDA Tool. After compiling models, design files and test bench files, Native Link uses this script to set up the simulation.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```bash
set_global_assignment -name EDA_NATIVELINK_SIMULATION_SETUP_SCRIPT -section_id <section identifier> <value>
```
1.8.30. EDA_NATIVELINK_SIMULATION_TEST_BENCH

Specify the active logical name of the test bench, that will be used to perform NativeLink Simulation

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name EDA_NATIVELINK_SIMULATION_TEST_BENCH -section_id <section identifier> <value>
```
1.8.31. EDA_NETLIST_WRITER_OUTPUT_DIR

Specify the output directory for EDA Netlist Writer

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name EDA_NETLIST_WRITER_OUTPUT_DIR -section_id <section identifier> <value>
```
1.8.32. EDA_RESYNTHESIS_TOOL

Specifies the EDA tool used for resynthesis.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name EDA_RESYNTHESIS_TOOL <value>
set_global_assignment -name EDA_RESYNTHESIS_TOOL -entity <entity name> <value>
```

**Default Value**

<None>
1.8.33. EDA_RTL_SIMULATION_RUN_SCRIPT

Specifies the script file for performing RTL simulation using third-party simulation software.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name EDA_RTL_SIMULATION_RUN_SCRIPT -section_id <section_identifier> <value>
set_global_assignment -name EDA_RTL_SIMULATION_RUN_SCRIPT -entity <entity name> -section_id <section_identifier> <value>
```
1.8.34. EDA_RTL_SIM_MODE

Enables the Advanced Options - VHDL or Verilog Simulation options for Test Bench mode or Command/macro mode.

**Type**

Enumeration

**Values**

- COMMAND_MACRO_MODE
- NOT_USED
- TEST_BENCH_MODE

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EDA_RTL_SIM_MODE -section_id <section identifier> <value>
set_global_assignment -name EDA_RTL_SIM_MODE -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

NOT_USED, requires section identifier
1.8.35. EDA_RTL_TEST_BENCH_FILE_NAME

Specifies the RTL simulation test bench file name for Test Bench Mode. File type can be a VHDL Test Bench File (.vht), VHDL File (.vhd), Verilog HDL Test Bench File (.vt), or Verilog HDL file (.v).

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name EDA_RTL_TEST_BENCH_FILE_NAME -section_id <section_identifier> <value>
set_global_assignment -name EDA_RTL_TEST_BENCH_FILE_NAME -entity <entity name> -section_id <section_identifier> <value>
```
1.8.36. EDA_RTL_TEST_BENCH_NAME

Specifies the name of top-level test bench in RTL simulation test bench file.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```bash
set_global_assignment -name EDA_RTL_TEST_BENCH_NAME -section_id <section identifier> <value>
set_global_assignment -name EDA_RTL_TEST_BENCH_NAME -entity <entity name> -section_id <section identifier> <value>
```
1.8.37. EDA_RTL_TEST_BENCH_RUN_FOR

Specifies the time duration for RTL simulation using third-party simulation.

**Type**
Time

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EDA_RTL_TEST_BENCH_RUN_FOR -section_id <section identifier> <value>
set_global_assignment -name EDA_RTL_TEST_BENCH_RUN_FOR -entity <entity name> -section_id <section identifier> <value>
```
1.8.38. EDA_SDC_FILE_NAME

Name of Design Constraints file to be sourced in scripts generated for third party tools

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name EDA_SDC_FILE_NAME -section_id <section identifier> <value>
set_global_assignment -name EDA_SDC_FILE_NAME -entity <entity name> -section_id <section identifier> <value>
```
1.8.39. EDA_SIMULATION_RUN_SCRIPT

 Specifies the script file for running a third-party simulation in Command/macro mode.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name EDA_SIMULATION_RUN_SCRIPT -section_id <section identifier> <value>
set_global_assignment -name EDA_SIMULATION_RUN_SCRIPT -entity <entity name> -section_id <section identifier> <value>
```
1.8.40. EDA_SIMULATION_TOOL

Specifies the third-party EDA tool used for simulation.

Type

String

Device Support

• This setting can be used in projects targeting any Intel FPGA device family.

Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

Syntax

set_global_assignment -name EDA_SIMULATION_TOOL <value>
set_global_assignment -name EDA_SIMULATION_TOOL -entity <entity name> <value>

Default Value

<None>
1.8.41. EDA_TEST_BENCH_DESIGN_INSTANCE_NAME

Specifies the instance name of the design entity in the test bench file.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name EDA_TEST_BENCH_DESIGN_INSTANCE_NAME -section_id <section identifier> <value>
set_global_assignment -name EDA_TEST_BENCH_DESIGN_INSTANCE_NAME -entity <entity name> -section_id <section identifier> <value>
```
1.8.42. EDA_TEST_BENCH_ENABLE_STATUS

Enables the Advanced Options - VHDL or Verilog Simulation options for Test Bench mode or Command/macro mode.

Type
Enumeration

Values
- COMMAND_MACRO_MODE
- NOT_USED
- TEST_BENCH_MODE

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```
set_global_assignment -name EDA_TEST_BENCH_ENABLE_STATUS -section_id <section identifier> <value>
set_global_assignment -name EDA_TEST_BENCH_ENABLE_STATUS -entity <entity name> -section_id <section identifier> <value>
```

Default Value

NOT_USED, requires section identifier
1.8.43. **EDA_TEST_BENCH_ENTITY_MODULE_NAME**

Specifies the top-level design entity in the test bench file.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_global_assignment -name EDA_TEST_BENCH_ENTITY_MODULE_NAME -section_id <section identifier> <value>
set_global_assignment -name EDA_TEST_BENCH_ENTITY_MODULE_NAME -entity <entity name> -section_id <section identifier> <value>
```
1.8.44. EDA_TEST_BENCH_EXTRA_ALTERA_SIM_LIB

Tells NativeLink to add extra simulation libraries to the specified module. This is required by the memory controllers (both new and legacy).

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name EDA_TEST_BENCH_EXTRA_ALTERA_SIM_LIB -section_id <section identifier> <value>
```
1.8.45. EDA_TEST_BENCH_FILE

Associates a test bench file with the logical test bench name

Type
File name

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name EDA_TEST_BENCH_FILE -section_id <section identifier> <value>
```
## 1.8.46. EDA_TEST_BENCH_FILE_NAME

Specifies the test bench file name for Test Bench Mode. File type can be a VHDL Test Bench File (.vht), Verilog HDL Test Bench File (.vt), or another design file type.

### Type

File name

### Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

### Notes

The value of this assignment is case sensitive.

### Syntax

```
set_global_assignment -name EDA_TEST_BENCH_FILE_NAME -section_id <section identifier> <value>
set_global_assignment -name EDA_TEST_BENCH_FILE_NAME -entity <entity name> -section_id <section identifier> <value>
```
1.8.47. EDA_TEST_BENCH_GATE_LEVEL_NETLIST_LIBRARY

Specify the simulation library to which Gate Level Netlist will be compiled

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_global_assignment -name EDA_TEST_BENCH_GATE_LEVEL_NETLIST_LIBRARY -
section_id <section identifier> <value>
```
1.8.48. EDA_TEST_BENCH_MODULE_NAME

Associates a test bench file with the logical test bench name

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name EDA_TEST_BENCH_MODULE_NAME -section_id <section_identifier> <value>
```
1.8.49. EDA_TEST_BENCH_NAME

Define a logical name for test bench. Each test bench logical name has associated section, containing test bench information, and section_id being the logical test bench name.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name EDA_TEST_BENCH_NAME -section_id <section identifier> <value>
```
1.8.50. EDA_TEST_BENCH_RUN_FOR

Specifies the simulation run time for a third-party simulation in Test Bench Mode.

**Type**

Time

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EDA_TEST_BENCH_RUN_FOR -section_id <section identifier> <value>
set_global_assignment -name EDA_TEST_BENCH_RUN_FOR -entity <entity name> -section_id <section identifier> <value>
```
1.8.51. EDA_TEST_BENCH_RUN_SIM_FOR

Specify the time interval for running EDA Simulation

**Type**

Time

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EDA_TEST_BENCH_RUN_SIM_FOR -section_id <section_identifier> <value>
```
1.8.52. EDA_TIME_SCALE

Specifies the time unit used to represent timing delays in each Verilog Output File. The value for the Time Scale option may be between 0.001 ns and 10ns, and should be a multiple of 10.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name EDA_TIME_SCALE -section_id <section identifier> <value>
set_global_assignment -name EDA_TIME_SCALE -entity <entity name> -section_id <section identifier> <value>
```
1.8.53. EDA_TIMING_ANALYSIS_TOOL

Specifies the EDA third-party tool used for timing analysis.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name EDA_TIMING_ANALYSIS_TOOL <value>
set_global_assignment -name EDA_TIMING_ANALYSIS_TOOL -entity <entity name> <value>
```

**Default Value**

<None>
1.8.54. EDA_TRUNCATE_LONG_HIERARCHY_PATHS

Truncate hierarchical node names to 80 characters.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name EDA_TRUNCATE_LONG_HIERARCHY_PATHS -section_id <section identifier> <value>
set_global_assignment -name EDA_TRUNCATE_LONG_HIERARCHY_PATHS -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

Off, requires section identifier
1.8.55. EDA_USER_COMPILED_SIMULATION_LIBRARY_DIRECTORY

Specify the directory where you store the library generated with the EDA Simulation Library Compiler tool. Note: Do not use this option to specify the directory for ModelSim - Intel FPGA precompiled libraries or Active-HDL precompiled libraries.

Type

File name

Device Support

• This setting can be used in projects targeting any Intel FPGA device family.

Notes

The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name EDA_USER_COMPILED_SIMULATION_LIBRARY_DIRECTORY - section_id <section_identifier> <value>
```

Default Value

<None>, requires section identifier
1.8.56. **EDA_VHDL_ARCH_NAME**

Specify the name of Architecture in the generated VHDL simulation netlist.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name EDA_VHDL_ARCH_NAME -section_id <section identifier> <value>
```

**Default Value**

structure, requires section identifier
1.8.57. EDA_WAIT_FOR_GUI_TOOL_COMPLETION

Specifies that NativeLink should wait for the EDA tool GUI launched by it to finish.

Type

Boolean

Device Support

• This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```plaintext
set_global_assignment -name EDA_WAIT_FOR_GUI_TOOL_COMPLETION -section_id <section identifier> <value>
```

Default Value

Off, requires section identifier
1.8.58. EDA_WRITER_DONT_WRITE_TOP_ENTITY

Do not write top-level entity in VHDL Output File (.vho).

Type
Boolean

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
This assignment is included in the Fitter report.

Syntax

```plaintext
set_global_assignment -name EDA_WRITER_DONT_WRITE_TOP_ENTITY -section_id
<section identifier> <value>
```

Default Value
Off, requires section identifier
1.8.59. EDA_WRITE_DEVICE_CONTROL_PORTS

Add the devpor, devclrn, and devoe signals in the design as input ports in the top-level design hierarchy in the Verilog or VHDL simulation netlist for the project.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name EDA_WRITE_DEVICE_CONTROL_PORTS -section_id <section identifier> <value>
set_global_assignment -name EDA_WRITEDEVICECONTROLPORTS -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

Off, requires section identifier
1.8.60. EDA_WRITE_NODES_FOR_POWER_ESTIMATION

Write script for Simulation tool to generate VCD file for outputs for power estimation.

**Type**

Enumeration

**Values**

- ALL_NODES
- NO_COMBINATIONAL_OUTPUT
- Off

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name EDA_WRITE_NODES_FOR_POWER_ESTIMATION -section_id <section identifier> <value>
set_global_assignment -name EDA_WRITE_NODES_FOR_POWER_ESTIMATION -entity <entity name> -section_id <section identifier> <value>
```

**Default Value**

OFF, requires section identifier
1.9. Equivalence Checker Assignments

1.9.1. EQC_AUTO_BREAK_CONE

Enable EQC for auto cone break when compare is abort.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EQC_AUTO_BREAK_CONE <value>
```

**Default Value**
On
1.9.2. EQC_AUTO_COMP_LOOP_CUT

Enable EQC for auto cut comp loop.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EQC_AUTO_COMP_LOOP_CUT <value>
```

**Default Value**

On
1.9.3. EQC_AUTO_INVERSION

Enable EQC for auto check inversion level.

Type
Boolean

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```
set_global_assignment -name EQC_AUTO_INVERSION <value>
```

Default Value
On
1.9.4. EQC_AUTO_PORTSWAP

Enable EQC auto swap the port.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EQC_AUTO_PORTSWAP <value>
```

**Default Value**

On
1.9.5. EQC_AUTO_TERMINATE

Enable auto terminates when conclusion (not equivalent or undecided) is met.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EQC_AUTO_TERMINATE <value>
```

**Default Value**

On
1.9.6. EQC_BBOX_MERGE

Enable EQC automatic merge black box.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EQC_BBOX_MERGE <value>
```

**Default Value**

On
1.9.7. EQC_CONSTANT_DFF_DETECTION

Enable EQC automatic constant DFF detection

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EQC_CONSTANT_DFF_DETECTION <value>
```

**Default Value**

On
1.9.8. EQC_DETECT_DONT_CARES

Enable EQC detect don't cares.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EQC_DETECT_DONT_CARES <value>
```

**Default Value**

On
1.9.9. EQC_DFF_SS_EMULATION

Enable EQC DFF secondary signal emulation.

Type
Boolean

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Syntax

set_global_assignment -name EQC_DFF_SS_EMULATION <value>

Default Value
On
1.9.10. EQC_DUPLICATE_DFF_DETECTION

Enable EQC automatic duplicate DFF detection

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```bash
set_global_assignment -name EQC_DUPLICATE_DFF_DETECTION <value>
```

**Default Value**

On
1.9.11. EQC_LVDS_MERGE

Enable EQC automatic merge LVDS.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EQC_LVDS_MERGE <value>
```

**Default Value**
On
1.9.12. EQC_MAC_REGISTER_UNPACK

Enable EQC for auto unpack MAC register.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EQC_MAC_REGISTER_UNPACK <value>
```

**Default Value**

On
1.9.13. EQC_PARAMETER_CHECK

Enable EQC check parameter.

Type

Boolean

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```bash
set_global_assignment -name EQC_PARAMETER_CHECK <value>
```

Default Value

On
1.9.14. EQC_POWER_UP_COMPARE

Enable EQC for comparing on the power-up level.

Type
Boolean

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```
set_global_assignment -name EQC_POWER_UP_COMPARE <value>
```

Default Value
Off
1.9.15. EQC_RAM_REGISTER_UNPACK

Enable EQC for auto unpack RAM register.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```shell
set_global_assignment -name EQC_RAM_REGISTER_UNPACK <value>
```

**Default Value**

On
1.9.16. EQC_RAM_UNMERGING

Enable EQC automatic unmerge RAM.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```plaintext
set_global_assignment -name EQC_RAM_UNMERGING <value>
```

**Default Value**

On
1.9.17. EQC_RENAMINGRULES

Enable EQC use renaming rules.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EQC_RENAMINGRULES <value>
```

**Default Value**

On
1.9.18. EQC_RENAMINGRULES_LIST

Store eqc renaming rules

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

set_global_assignment -name EQC_RENAMINGRULES_LIST <value>
1.9.19. EQC_SET_PARTITION_BB_TO_VCC_GND

Enable EQC for set partition Black-box unconnected input to VCC or GND.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EQC_SET_PARTITION_BB_TO_VCC_GND <value>
```

**Default Value**
On
1.9.20. EQC_SHOW_ALL_MAPPED_POINTS

Enable EQC show all mapped points.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EQC_SHOW_ALL_MAPPED_POINTS <value>
```

**Default Value**
Off
1.9.21. EQC_STRUCTURE_MATCHING

Enable EQC for map using structure matching.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EQC_STRUCTURE_MATCHING <value>
```

**Default Value**

On
1.9.22. EQC_SUB_CONE_REPORT

Enable EQC show sub cone report.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name EQC_SUB_CONE_REPORT <value>
```

**Default Value**

Off
## 1.10. Fitter Assignments

### 1.10.1. ACTIVE_SERIAL_CLOCK

Specifies the clock source for Fast Active Serial programming.

**Type**

Enumeration

**Values**

- AS_FREQ_100MHZ
- AS_FREQ_108MHZ
- AS_FREQ_115MHZ_IOSC
- AS_FREQ_125MHZ
- AS_FREQ_133MHZ
- AS_FREQ_166MHZ
- AS_FREQ_166_6MHZ
- AS_FREQ_25MHZ
- AS_FREQ_25MHZ_IOSC
- AS_FREQ_38MHZ_IOSC
- AS_FREQ_50MHZ
- AS_FREQ_58MHZ_IOSC
- AS_FREQ_71_5MHZ
- AS_FREQ_77MHZ_IOSC
- AS_FREQ_80MHZ
- CLKUSR
- FREQ_100MHz
- FREQ_12_5MHz
- FREQ_20MHz
- FREQ_25MHz
- FREQ_40MHz
- FREQ_50MHz

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10
- eASIC N5X
**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ACTIVE_SERIAL_CLOCK <value>
```

**Example**

```
set_global_assignment -name active_serial_clock "CLKUSR"
```

**See Also**

USER_START_UP_CLOCK
1.10.2. ALLOW_ROUTING_TO_PERIPHERY_THROUGH_GLOBAL_NETWORK

Specifies that a signal can be routed from an IO pin to periphery destinations using global routing paths. This allows the router to consider global and non-global routing paths and does not guarantee that a signal will be routed using global routing paths. Additionally, this will not route the signal to its destinations in a skew balanced manner. Only supported for Stratix 10 devices.

Type
Boolean

Device Support
- Intel Agilex
- Intel Stratix 10

Notes
This assignment supports wildcards.
This assignment supports Fitter wildcards.

Syntax

- set_instance_assignment -name ALLOW_ROUTING_TO_PERIPHERY_THROUGH_GLOBAL_NETWORK -to <to> <value>
- set_instance_assignment -name ALLOW_ROUTING_TO_PERIPHERY_THROUGH_GLOBAL_NETWORK -from <from> -to <to> <value>

Example

- set_instance_assignment -name ALLOW_ROUTING_TO_PERIPHERY_THROUGH_GLOBAL_NETWORK -to clk
1.10.3. ALLOW_SEU_FAULT_INJECTION

Allow SEU fault injection.

Type

Boolean

Device Support

- Intel Agilex
- Intel Stratix 10

Notes

None

Syntax

set_global_assignment -name ALLOW_SEU_FAULT_INJECTION <value>

Example

set_global_assignment -name ALLOW_SEU_FAULT_INJECTION ON
1.10.4. ALLOW_VCCR_VCCT_PER_BANK

Allow VCCR VCCT power supply to be set per-six-bank instead of per-Crete

**Type**

Boolean

**Device Support**

- Intel Stratix 10

**Notes**

None

**Syntax**

```
set_global_assignment -name ALLOW_VCCR_VCCT_PER_BANK <value>
```

**Default Value**

Off

**Example**

```
set_global_assignment -name ALLOW_VCCR_VCCT_PER_BANK ON
```
1.10.5. ALM_REGISTER_PACKING_EFFORT

This guides how aggressively the Fitter will pack ALMs when trying to place registers into desired LAB locations. Specifically, this option can be used to increase the usage of secondary register locations during placement. Increasing ALM packing density may lower the number of ALMs needed to fit the design but it may also reduce routing flexibility and timing performance. It should also be noted that this setting is used as a hint for the Fitter only. Low - The Fitter will avoid ALM packing configurations that combine LUTs and registers which have no direct connectivity. Avoiding these configurations may improve timing performance but will increase the number of ALMs used to implement the design. Medium - The Fitter allows some configurations that combine unconnected LUTs and registers to be implemented in ALM locations. The Fitter will make more usage of secondary register locations within the ALM. High - The Fitter enables all legal and desired ALM packing configurations. In dense designs, the Fitter will automatically increase the ALM register packing effort as required to enable the design to fit.

**Type**

Enumeration

**Values**

- High
- Low
- Medium

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name ALM_REGISTER_PACKING_EFFORT <value>
```

**Default Value**

Medium
1.10.6. ANTI_TAMPER_RESPONSE_FAILED

Output to indicate an anti-tampering response failed.

**Type**
String

**Device Support**
- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ANTI_TAMPER_RESPONSE_FAILED <value>
```

**Default Value**
Off
1.10.7. AUTO_ANALYZE_METASTABILITY

Specifies whether synchronization register chains detected with the 'Auto' setting of the Synchronizer Identification option are analyzed for metastability. When this option is disabled, only 'Forced' or 'Forced if Asynchronous' chains are analyzed for metastability. When a synchronization register chain is analyzed for metastability, then its registers are optimized for improved Mean Time Between Failure (MTBF) as long as the Optimize Design for Metastability option is turned on, and the Timing Analyzer reports the metastability MTBF for the chain if it meets the design timing requirements.

**Type**
Boolean

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**
This assignment supports wildcards.
This assignment supports Fitter wildcards.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name AUTO_ANALYZE_METASTABILITY <value>
set_global_assignment -name AUTO_ANALYZE_METASTABILITY -entity <entity name> <value>
set_instance_assignment -name AUTO_ANALYZE_METASTABILITY -to <to> -entity <entity name> <value>
```

**Default Value**
Off
1.10.8. AUTO_DELAY_CHAINS

Allows the Fitter to choose the optimal delay chain to meet tsu and tco timing requirements for all I/O elements. Turning on this option may reduce the number of tsu violations while introducing a minimal number of th violations. Turning on this option does not override delay chain settings on individual nodes.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name AUTO_DELAY_CHAINS <value>
```
1.10.9. AUTO_DELAY_CHAINS_FOR_HIGH_FANOUT_INPUT_PINS

Allows the Fitter to choose how to optimize the delay chains for high fanout input pins. You must enable the Auto Delay Chains option for this option to work. Enabling this option may reduce the number of tsu violation, but the compile time increases significantly, as the Fitter tries to optimize the settings for all fanouts.

**Type**

Enumeration

**Values**

- Off
- On

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name AUTO_DELAY_CHAINS_FOR_HIGH_FANOUT_INPUT_PINS <value>
```

**Default Value**

OFF
1.10.10. AUTO_GLOBAL_CLOCK

Allows the Compiler to choose the signal that feeds the most clock inputs to flipflops as a global clock signal that is made available throughout the device on the global routing paths. If you want to prevent the Compiler from automatically selecting a particular signal as global clock, set the Global Signal option to 'Off' on that signal.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- EPC1
- EPC2
- Enhanced Configuration Devices
- Flash Memory
- Intel Stratix 10
- Virtual JTAG TAP

**Notes**

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name AUTO_GLOBAL_CLOCK <value>
set_global_assignment -name AUTO_GLOBAL_CLOCK -entity <entity name> <value>
set_instance_assignment -name AUTO_GLOBAL_CLOCK -to <to> -entity <entity name> <value>
```

**Default Value**

On
1.10.11. AUTO_GLOBAL_REGISTER_CONTROLS

Allows the Compiler to choose the signals that feed the most control signal inputs to flipflops (excluding clock signals) as global signals that are made available throughout the device on the global routing paths. Depending on the target device family, these control signals can include asynchronous clear and load, synchronous clear and load, clock enable, and preset signals. If you want to prevent the Compiler from automatically selecting a particular signal as global register control signal, set the Global Signal option to 'Off' on that signal.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- EPC1
- EPC2
- Enhanced Configuration Devices
- Flash Memory
- Intel Stratix 10
- Virtual JTAG TAP

**Notes**

This assignment supports Fitter wildcards.
This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name AUTO_GLOBAL_REGISTER_CONTROLS <value>
set_global_assignment -name AUTO_GLOBAL_REGISTER_CONTROLS -entity <entity name> <value>
set_instance_assignment -name AUTO_GLOBAL_REGISTER_CONTROLS -to <to> -entity <entity name> <value>
```

**Default Value**

On
1.10.12. **AUTO_RESERVE_CLKUSR_FOR_CALIBRATION**

Automatically reserve CLKUSR pin for calibration purposes

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name AUTO_RESERVE_CLKUSR_FOR_CALIBRATION <value>
```

**Default Value**

On

**Example**

```
set_global_assignment -name AUTO_RESERVE_CLKUSR_FOR_CALIBRATION OFF
```
1.10.13. **BASE_PIN_OUT_FILE_ONSAMEFRAME_DEVICE**

Directs the Compiler to base the Pin-Out File (.pin) and floorplan package views on the largest selected SameFrame device.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```plaintext
set_global_assignment -name BASE_PIN_OUT_FILE_ONSAMEFRAME_DEVICE <value>
```

**Default Value**

Off
1.10.14. **BLOCK_RAM_AND_MLAB_EQUIVALENT_PAUSED_READ_CAPABILITIES**

Controls whether RAMs implemented in MLAB cells must have equivalent pause read capabilities as RAMs implemented in block RAM. Pausing a read is the ability to keep around the last read value when reading is disabled. Allowing differences in paused read capabilities will provide the fitter more flexibility in implementing RAMs using MLAB cells. If this option is set to 'Don't Care', the Fitter may convert RAMs to MLAB cells even if they won't have equivalent paused read capabilities to a block RAM implementation. The Fitter will also output an information message notifying the user of RAMs with different paused read capabilities. If this option is set to 'Care', the Fitter will not convert RAMs to MLAB cells unless they have the equivalent paused read capabilities to a block RAM implementation. To allow the fitter the most flexibility in deciding which RAMs are implemented using MLAB cells, set this option to 'Don't Care'.

**Type**

Enumeration

**Values**

- Care
- Dont Care

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name BLOCK_RAM_AND_MLAB_EQUIVALENT_PAUSED_READ_CAPABILITIES <value>
set_global_assignment -name BLOCK_RAM_AND_MLAB_EQUIVALENT_PAUSED_READ_CAPABILITIES -entity <entity name> <value>
set_instance_assignment -name BLOCK_RAM_AND_MLAB_EQUIVALENT_PAUSED_READ_CAPABILITIES -to <to> -entity <entity name> <value>
```

**Default Value**

Care
1.10.15. BLOCK_RAM_AND_MLAB_EQUIVALENT_POWER_UP_CONDITIONS

Controls whether RAMs implemented in MLAB cells must have equivalent power up conditions as RAMs implemented in block RAM. Power up conditions occur when the device is powered up or globally reset. Allowing non-equivalent power up conditions will provide the fitter more flexibility in implementing RAMs using MLAB cells. If this option is set to 'Auto', the Fitter may convert RAMs to MLAB cells even if they won't have equivalent power up conditions to a block RAM implementation. The Fitter will also output a warning message notifying the user of RAMs with non-equivalent power up conditions. If this option is set to 'Don't Care', the same behavior as 'Auto' applies, but the warning message will instead be an information message. If this option is set to 'Care', the Fitter will not convert RAMs to MLAB cells unless they have equivalent power up conditions to a block RAM implementation. To allow the fitter the most flexibility in deciding which RAMs are implemented using MLAB cells, set this option to 'Auto' or 'Don't Care'.

Type

Enumeration

Values

- Auto
- Care
- Don't Care

Device Support

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name BLOCK_RAM_AND_MLAB_EQUIVALENT_POWER_UP_CONDITIONS <value>
set_global_assignment -name BLOCK_RAM_AND_MLAB_EQUIVALENT_POWER_UP_CONDITIONS -entity <entity name> <value>
set_instance_assignment -name BLOCK_RAM_AND_MLAB_EQUIVALENT_POWER_UP_CONDITIONS -to <to> -entity <entity name> <value>
```

Default Value

Auto
1.10.16. BLOCK_RAM_TO_MLAB_CELL_CONVERSION

Controls whether the fitter is able to convert RAMs to use LAB locations when those RAMs use 'Auto' as the selected block type. If this option is changed to 'Off' then only MLAB cells in the design or RAM cells with a block type setting of 'MLAB' will use LAB locations to implement memory.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name BLOCK_RAM_TO_MLAB_CELL_CONVERSION <value>
set_global_assignment -name BLOCK_RAM_TO_MLAB_CELL_CONVERSION -entity <entity name> <value>
set_instance_assignment -name BLOCK_RAM_TO_MLAB_CELL_CONVERSION -to <to> -entity <entity name> <value>
```

**Default Value**

On
1.10.17. CDR_BANDWIDTH_PRESET

Specifies the CDR (clock data recovery) bandwidth preset setting.

**Type**

Enumeration

**Values**

- Auto
- High
- Low
- Medium

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

**Syntax**

```
set_instance_assignment -name CDR_BANDWIDTH_PRESET -to <to> -entity <entity name> <value>
```
1.10.18. CKN_CK_PAIR

Specifies the pairing of a CKn pin to a CK pin. The I/O pin of a CK CKn pair must be placed on a differential pin pair. This option is ignored if is assigned to anything other than an I/O pad, input buffer, or output buffer.

Type

Boolean

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Notes

This assignment supports Fitter wildcards.

Syntax

```set_instance_assignment -name CKN_CK_PAIR -from <from> -to <to> -entity <entity name> <value>```
1.10.19. CLOCK_REGION

Specifies the placement of the clock region of a global signal for floorplanning reasons. For example, a Clock Region assignment can be used to ensure that a certain area of the device has access to a global signal, throughout all future design iterations. A Clock Region assignment can also be used in cases of congestion involving global signal resources. By specifying a smaller clock region size, the assignment prevents a signal using spine clock and other clock routing resources in the excluded sectors that may be encountering clock-related congestion.

For devices up to and including Arria 10, this assignment takes as its value the names of those Global, Regional, Periphery or Spine Clock regions. These region names are visible in Chip Planner by enabling the appropriate Clock Region layer in the Layers Settings dialog box. Examples of valid values include "Regional Clock Region 1" or "Peripheral Clock Region 1". When constraining a global signal to a smaller than normal region, for example, to avoid clock congestion, you may specify a clock region of a different type than the global resources being used. For example, a signal with a Global Signal assignment of "Global Clock", but a Clock Region assignment of "Regional Clock Region 0", constrains the clock to use global network routing resources, but only to the region covered by Regional Clock Region 0. To provide a finer level of control, you can also list multiple smaller clock regions, separated by commas. For example: "Peripheral Clock Region 0, Peripheral Clock Region 1" constrains a signal to only the area reachable by those two periphery clock networks.

For Stratix 10 devices, clock regions can be constrained to a rectangle whose dimensions are defined by the sector grid, as seen in the Clock Sector Region layer of the Chip Planner. This assignment specifies the bottom left and top right coordinates of the rectangle in the format "SX# SY# SX# SY#". For example, "SX0 SY0 SX1 SY1" constrains the clock to a 2x2 region, from the bottom left of sector (0,0) to the top right of sector (1,1). For a constraint spanning only one sector, it is sufficient to specify the location of that sector, for example "SX1 SY1". The bounding rectangle can also be specified by the bottom left and top right corners in chip coordinates, for example, "X37 Y181 X273 Y324". However, such a constraint should be sector aligned (using sector coordinates guarantees this) or the Fitter automatically snaps to the smallest sector aligned rectangle that still encompasses the original assignment. The "SX# SY# SX# SY#"| "X# Y# X# Y#" strings are case-insensitive.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports wildcards.

This assignment supports Fitter wildcards.
Syntax

set_instance_assignment -name CLOCK_REGION -to <to> -entity <entity name> <value>
set_instance_assignment -name CLOCK_REGION -from <from> -to <to> -entity <entity name> <value>
1.10.20. CLOCK_SPINE

Specifies the Spine Clock (SCLK) wire index to use for the targeted global signal. Each clock sector contains 32 SCLK resources, and an allocated global clock tree will use the same SCLK index in each driven clock sector. This is an advanced assignment that can potentially be useful to control global signal routing decisions in cases of global resource congestion. When used, this assignment should typically be paired with a Clock Region assignment to ensure the driven clock sectors are also constrained.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Stratix 10

**INTEGER_RANGE**

0, 31

**Notes**

This assignment supports wildcards.

This assignment supports Fitter wildcards.

**Syntax**

```
set_instance_assignment -name CLOCK_SPINE -to <to> -entity <entity name> <value>
set_instance_assignment -name CLOCK_SPINE -from <from> -to <to> -entity <entity name> <value>
```
1.10.21. CONFIGURATION_VCCIO_LEVEL

Specifies the VCCIO voltage of the configuration pins for the current configuration scheme on the target device.

**Type**
String

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**
None

**Syntax**

```
set_global_assignment -name CONFIGURATION_VCCIO_LEVEL <value>
```

**Default Value**
Auto

**Example**

```
set_global_assignment -name CONFIGURATION_VCCIO_LEVEL 1.8V
```

**See Also**

FORCE.Configuration_VCCIO
1.10.22. CONVERT_PR_WARNINGS_TO_ERRORS

Turns PR warnings into errors when enabled.

Type
Boolean

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes

Syntax

```
set_global_assignment -name CONVERT_PR_WARNINGS_TO_ERRORS <value>
```

Default Value
Off

Example

```
set_global_assignment -name CONVERT_PR_WARNINGS_TO_ERRORS ON
```
1.10.23. CRC_ERROR_OPEN_DRAIN

Specify open drain on the CRC Error pin should be enabled or not

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

None

**Syntax**

```
set_global_assignment -name CRC_ERROR_OPEN_DRAIN <value>
```

**Example**

```
set_global_assignment -name crc_error_open_drain on
set_global_assignment -name crc_error_open_drain off
```

**See Also**

CRC_ERROR_CHECKINGERROR_CHECK_FREQUENCY_DIVISOR
1.10.24. CURRENT_STRENGTH_NEW

Sets the drive strength of a pin. Specify a number (in mA), MIN, or MAX for output or bidirectional pins that support programmable drive strength. Please refer to the family data sheet for which drive strengths are allowed for each I/O standard. This option is ignored if it is applied to anything other than an output or bidirectional pin.

**Old Name**

CURRENT_STRENGTH

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10
- eASIC N5X

**Notes**

This assignment supports Fitter wildcards.

**Syntax**

```
set_instance_assignment -name CURRENT_STRENGTH_NEW -to <to> -entity <entity name> <value>
```

**Example**

```
set_instance_assignment -name CURRENT_STRENGTH_NEW 12MA -to output_pin
```

**See Also**

IO_STANDARD
OUTPUT_TERMINATION
1.10.25. CVP_CONF_DONE_OPEN_DRAIN

Specify open drain on the CVP_CONF_DONE pin should be enabled or not

Old Name
CV_PCIE_CONF_DONE_OPEN_DRAIN

Type
Boolean

Device Support
- Intel Arria 10
- Intel Cyclone 10 GX

Notes
None

Syntax

```plaintext
set_global_assignment -name CVP_CONF_DONE_OPEN_DRAIN <value>
```

Default Value
On

Example

```plaintext
set_global_assignment -name CVP_CONF_DONE_OPEN_DRAIN on
set_global_assignment -name CVP_CONF_DONE_OPEN_DRAIN off
```

See Also
ENABLE_CVP_CONF_DONE
1.10.26. CVP_MODE

Specifies the configuration mode for Configuration via Protocol (CvP). In Core initialization mode, the periphery image is stored in an external configuration device and is loaded into the FPGA through the conventional configuration scheme. The core image is stored in a host memory and is loaded into the FPGA through the PCIe link. In core update mode, the FPGA device is initialized after initial system power up by loading the full configuration image from the external local configuration device to the FPGA. User can use the PCIe link to perform one or more FPGA core image update through this mode. In the Off mode, CvP is turned off.

Old Name
CVPCIE_MODE

Type
 Enumeration

Values
• Core initialization
• Core initialization and update
• Core update
• Off

Device Support
• Intel Agilex
• Intel Arria 10
• Intel Cyclone 10 GX
• Intel Stratix 10

Notes
None

Syntax
set_global_assignment -name CVP_MODE <value>

Default Value
Off

Example
set_global_assignment -name CVP_MODE "Power up and subsequent core configuration"
1.10.27. DEVICE

Specifies the device to use.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name DEVICE <value>
```
1.10.28. DEVICE_INITIALIZATION_CLOCK

In 20nm device families, this specifies the clock source for device initialization (the duration between CONF_DONE signal went high and before INIT_DONE signal goes high). In 14nm or later device families, this specifies the clock source used to run the PLL which produces the clock used by the device configuration and monitoring system.

Type
Enumeration

Values
- INIT_CLKUSR
- INIT_DCLK
- INIT_INTOSC
- OSC_CLK_1_100MHZ
- OSC_CLK_1_125MHZ
- OSC_CLK_1_25MHZ

Device Support
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10
- eASIC N5X

Notes
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name DEVICE_INITIALIZATION_CLOCK <value>
```

Default Value
INIT_INTOSC

Example

```
set_global_assignment -name DEVICE_INITIALIZATION_CLOCK "CLKUSR"
```

See Also
USER_START_UP_CLOCK
1.10.29. DEVICE_IO_STANDARD_ALL

Specifies the default I/O standard to be used for pins on the target device.

**Old Name**

STRATIX_DEVICE_IO_STANDARD, YEAGER_DEVICE_IO_STANDARD

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name DEVICE_IO_STANDARD_ALL <value>
```

**Example**

```
set_global_assignment -name DEVICE_IO_STANDARD_ALL "1.2 V"
```

**See Also**

IO_STANDARD
1.10.30. DEVICE_MIGRATION_LIST

Shows the selected migration devices for the current device.

Type
String

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```bash
set_global_assignment -name DEVICE_MIGRATION_LIST <value>
```
1.10.31. DEVICE_TECHNOLOGY_MIGRATION_LIST

Shows the selected technology migration devices for the current device.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

set_global_assignment -name DEVICE_TECHNOLOGY_MIGRATION_LIST <value>
1.10.32. DQ_GROUP

Specifies the grouping from a DQS pin to its associated DQ pins and the width (4, 9, 18, or 36) of the group. Setting this option allows the Fitter to view the pins as a DQS/DQ pin group. I/O pins of a DQ pin group must be placed in the DQ pin locations of a single DQS group. This option is ignored if is assigned to anything other than an I/O pad, input buffer, or output buffer.

Type

Integer

Device Support

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes

This assignment supports Fitter wildcards.

Syntax

```
set_instance_assignment -name DQ_GROUP -from <from> -to <to> -entity <entity name> <value>
```

Example

```
set_instance_assignment -name DQ_GROUP 9 -from mem_dqs[0] -to mem_dq[0..7]
```

See Also

DQSB_DQS_PAIRMEMORY_INTERFACE_DATA_PIN_GROUP
1.10.33. DSP_REGISTER_PACKING

Controls how aggressively the fitter optimizes DSP performance by automatically packing registers into the internal registers of the specified DSP blocks. When the 'Balanced' option is enabled, the Fitter will pack registers into the specified DSP blocks that should improve timing. When 'Always' is enabled, the fitter will aggressively try to pack registers into the specified DSP blocks unless prevented by user constraints or other legality restrictions. When 'Disable' is selected, registers will not be packed into the specified DSP blocks.

**Type**

Enumeration

**Values**

- Always
- Balanced
- Disable

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

**Syntax**

```plaintext
set_instance_assignment -name DSP_REGISTER_PACKING -to <to> -entity <entity name> <value>
```
1.10.34. DSP_REGISTER_PACKING_LEVEL

Controls how many levels of registers to be packed in the specified DSP instance, if registers are available. Setting the packing level to 0 is equivalent to disabling DSP register packing operation of the DSP. If the packing level is set to 1, the Fitter tries to pack one layer of registers from the DSP's input side. When set to 2, an additional layer of registers will get packed from DSP's output side. 3 or 4 will add one or two layers of the pipeline registers from the input side.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**INTEGER_RANGE**

0, 4

**Notes**

This assignment supports Fitter wildcards.

**Syntax**

```
set_instance_assignment -name DSP_REGISTER_PACKING_LEVEL -to <to> -entity <entity name> <value>
```
1.10.35. DUPLICATE_ATOM

Directs the Compiler to duplicate the source node, and uses the new duplicate node to fan out to the destination node; the original source node no longer fans out to the destination node. Use the 'Value' field to specify the name of the duplicate node.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

The value of this assignment is case sensitive.

This assignment supports Fitter wildcards.

The value of this assignment must be a node name.

**Syntax**

```
set_instance_assignment -name DUPLICATE_ATOM -from <from> -to <to> -entity <entity name> <value>
```
1.10.36. DUPLICATE_REGISTER

Directs the Compiler to create a number of duplicates of a register, including the original, and redistribute the fanouts of the original register among the duplicates.

Type
Integer

Device Support
- Intel Agilex
- Intel Stratix 10

INTEGER_RANGE
1, 1000000

Notes
The value of this assignment is case sensitive.
This assignment is copied to any duplicated nodes.
This assignment supports Fitter wildcards.
The value of this assignment must be a node name.

Syntax

```
set_instance_assignment -name DUPLICATE_REGISTER -to <to> -entity <entity name> <value>
```
1.10.37. ENABLE_BUS_HOLD_CIRCUITRY

Enables bus-hold circuitry during device operation. If this option is turned on, a pin will retain its last logic level when it is not driven, and will not go to a high impedance logic level. The 'Enable Bus-Hold Circuitry' option should not be used at the same time as the 'Weak Pull-Up Resistor' option. This option is ignored if it is applied to anything other than a pin.

**Type**
Boolean

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**
This assignment supports Fitter wildcards.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ENABLE_BUS_HOLD_CIRCUITRY <value>
set_global_assignment -name ENABLE_BUS_HOLD_CIRCUITRY -entity <entity name> <value>
set_instance_assignment -name ENABLE_BUS_HOLD_CIRCUITRY -to <to> -entity <entity name> <value>
```

**Default Value**
Off

**Example**

```
set_instance_assignment -name ENABLE_BUS_HOLD_CIRCUITRY ON -to pin
```
1.10.38. ENABLE_CRC_ERROR_PIN

Specifies error detection CRC and CRC_ERROR pin usage for the selected device. If error detection CRC is turned on, the device checks the validity of the programming data in the device. Any changes in the data while the device is in operation generates an error.

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

None

**Syntax**

```plaintext
cset_global_assignment -name ENABLE_CRC_ERROR_PIN <value>
```

**Default Value**

Off

**Example**

```plaintext
cset_global_assignment -name ENABLE_CRC_ERROR_PIN ON
```

**See Also**

ERROR_CHECK_FREQUENCY_DIVISORCRC_ERROR_OPEN_DRAIN
1.10.39. ENABLE_CVP_CONFDONE

Enable the CvP_CONFDONE pin, which indicates that the device finished core programming in Configuration via Protocol mode. If this option is turned off, the CvP_CONFDONE pin is disabled when the device operates in user mode and is available as a user I/O pin.

Old Name

ENABLE_CVPCIE_CONFDONE

Type

Boolean

Device Support

- Intel Arria 10
- Intel Cyclone 10 GX

Notes

None

Syntax

```markdown
set_global_assignment -name ENABLE_CVP_CONFDONE <value>
```

Default Value

Off

Example

```markdown
set_global_assignment -name ENABLE_CVP_CONFDONE ON
```

See Also

CVP_CONFDONE_OPEN_DRAIN
1.10.40. ENABLE_DEVICE_WIDE_OE

Enables the DEV_OE pin when the device is in user mode. If this option is turned on, all outputs on the chip operate normally. When the pin is disabled, all outputs are tri-stated. If this option is turned off, the DEV_OE pin is disabled when the device operates in user mode and is available as a user I/O pin.

**Old Name**

ENABLE_CHIP_WIDE_OE

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

None

**Syntax**

```
set_global_assignment -name ENABLE_DEVICE_WIDE_OE <value>
```

**Default Value**

Off

**Example**

```
set_global_assignment -name ENABLE_DEVICE_WIDE_OE ON
```
1.10.41. ENABLE_DEVICE_WIDE_RESET

Enables the DEV_CLRn pin, which allows all registers of the device to be reset by an external source. If this option is turned off, the DEV_CLRn pin is disabled when the device operates in user mode and is available as a user I/O pin.

**Old Name**

ENABLE_CHIP_WIDE_RESET

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

None

**Syntax**

```plaintext
set_global_assignment -name ENABLE_DEVICE_WIDE_RESET <value>
```

**Default Value**

Off

**Example**

```plaintext
set_global_assignment -name ENABLE_DEVICE_WIDE_RESET ON
```
1.10.42. ENABLE_DSP_REGISTER_UNPACKING

Controls whether registers can be unpacked from DSPs after packing to improve timing.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

**Syntax**

- `set_global_assignment -name ENABLE_DSP_REGISTER_UNPACKING <value>`
- `set_global_assignment -name ENABLE_DSP_REGISTER_UNPACKING -entity <entity name> <value>`
- `set_instance_assignment -name ENABLE_DSP_REGISTER_UNPACKING -to <to> -entity <entity name> <value>`

**Default Value**

On

**Example**

- `set_global_assignment -name ENABLE_DSP_REGISTER_UNPACKING OFF`
- `set_instance_assignment -name ENABLE_DSP_REGISTER_UNPACKING OFF -to <to> -entity <entity name> <value>`

**See Also**

DSP_REGISTER_PACKING
1.10.43. ENABLE_ED_CRC_CHECK

Enable the error detection check. The status is SEU_ERROR output SDM_IO. If error detection CRC is turned on, the device checks the validity of the programming data in the device. Any changes in the data while the device is in operation generates an error.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

None

**Syntax**

```
set_global_assignment -name ENABLE_ED_CRC_CHECK <value>
```

**Example**

```
set_global_assignment -name ENABLE_ED_CRC_CHECK ON
```
1.10.44. ENABLE_INFERRED_SHIFT_REG_COUNTER_DUPLICATION

Controls if the address counters of RAM-implementation shift registers can be duplicated.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

**Syntax**

```
set_global_assignment -name ENABLE_INFERRED_SHIFT_REG_COUNTER_DUPLICATION <value>
set_global_assignment -name ENABLE_INFERRED_SHIFT_REG_COUNTER_DUPLICATION -entity <entity name> <value>
set_instance_assignment -name ENABLE_INFERRED_SHIFT_REG_COUNTER_DUPLICATION -to <to> -entity <entity name> <value>
```

**Default Value**

On

**Example**

```
set_global_assignment -name ENABLE_INFERRED_SHIFT_REG_COUNTER_DUPLICATION OFF
set_instance_assignment -name ENABLE_INFERRED_SHIFT_REG_COUNTER_DUPLICATION OFF -to inferred_shift_reg_to_ram_dout0
```
1.10.45. ENABLE_INIT_DONE_OUTPUT

Enables the INIT_DONE pin, which allows you to externally monitor when initialization is completed and the device is in user mode. If this option is turned off, the INIT_DONE pin is disabled when the device operates in user mode and is available as a user I/O pin.

Old Name
Enable INIT_DONE Output

Type
Boolean

Device Support
- Intel Arria 10
- Intel Cyclone 10 GX

Notes
None

Syntax

```
set_global_assignment -name ENABLE_INIT_DONE_OUTPUT <value>
```

Default Value
Off

Example

```
set_global_assignment -name ENABLE_INIT_DONE_OUTPUT OFF
```

See Also

INIT_DONE_OPEN_DRAIN
1.10.46. **ENABLE_INTERMEDIATE_SNAPSHOTS**

Turning on this option will generate all intermediate fitter snapshots (planned, placed, routed, retimed) during compilation for design analysis. The option is off by default. If 'Run Fast Forward Timing Closure Recommendations during compilation' is on, then the option is forced on.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name ENABLE_INTERMEDIATE_SNAPSHOTS <value>
```

**Default Value**

Off

**Example**

```plaintext
set_global_assignment -name ENABLE_INTERMEDIATE_SNAPSHOTS on
```
1.10.47. ENABLE_NCEO_OUTPUT

Enables the nCEO pin. This pin should be connected to the nCE of the succeeding device when multiple devices are being programmed. If this option is turned off, the nCEO pin is disabled when the device operates in user mode and is available as a user I/O pin.

**Type**
Boolean

**Device Support**
- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**
None

**Syntax**

```
set_global_assignment -name ENABLE_NCEO_OUTPUT <value>
```

**Default Value**
Off

**Example**

```
set_global_assignment -name ENABLE_NCEO_OUTPUT OFF
```
1.10.48. ENABLE_PR_PINS

Allows you to enable the PR_REQUEST, PR_READY, PR_ERROR, PR_DONE, DCLK, and DATA[31..0] pins. These pins are needed to support partial reconfiguration (PR) with an external host. An external host uses the PR_REQUEST pin to request partial reconfiguration, the PR_READY pin to determine if the device is ready to receive programming data, the PR_ERROR pin to externally monitor programming errors, and the PR_DONE pin to indicate the device finished programming. If this option is turned off, these pins are not available as PR pins when the device operates in user mode and the dual-purpose programming pins are available as user I/O pins.

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

None

**Syntax**

```
set_global_assignment -name ENABLE_PR_PINS <value>
```

**Default Value**

Off

**Example**

```
set_global_assignment -name ENABLE_PR_PINS ON
```

**See Also**

PR_PINS_OPEN_DRAIN
1.10.49. ENABLE_TIME_BORROWING_OPTIMIZATION

Enables optimal time borrowing algorithm. Turned on automatically for performance optimization mode.

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ENABLE_TIME_BORROWING_OPTIMIZATION <value>
```

**Default Value**

Off
1.10.50. ENABLE_UNUSED_RX_CLOCK_WORKAROUND

Enable workaround for unused RX clock to preserve its performance over time

Type
Boolean

Device Support
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name ENABLE_UNUSED_RX_CLOCK_WORKAROUND <value>
set_instance_assignment -name ENABLE_UNUSED_RX_CLOCK_WORKAROUND -to <to> -entity <entity name> <value>
```

Default Value
Off

Example
```
set_global_assignment -name ENABLE_UNUSED_RX_CLOCK_WORKAROUND ON
set_instance_assignment -name ENABLE_UNUSED_RX_CLOCK_WORKAROUND ON -to AW34
```
1.10.51. ERROR_CHECK_FREQUENCY_DIVISOR

Specifies the divide value of the internal clock, which determines the frequency of the CRC. The divide value must be a power of two. Refer to the device handbook to find the frequency of the internal clock for the selected device.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

None

**Syntax**

```plaintext
set_global_assignment -name ERROR_CHECK_FREQUENCY_DIVISOR <value>
```

**Example**

```plaintext
set_global_assignment -name ERROR_CHECK_FREQUENCY_DIVISOR 16
```

**See Also**

CRC_ERROR_CHECKING
1.10.52. EXCLUSIVE_IO_GROUP

Assigns an exclusive group number for the specified I/O. I/Os with the different exclusive group number cannot share the same bank.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

**Syntax**

```plaintext
set_instance_assignment -name EXCLUSIVE_IO_GROUP -to <to> -entity <entity name> <value>
```

**Example**

```plaintext
set_instance_assignment -name "EXCLUSIVE_IO_GROUP" -to pin
```
1.10.53. FINAL_PLACEMENT_OPTIMIZATION

Specifies whether the Fitter performs final placement optimizations. Performing final placement optimizations may improve timing and routability, but may also require longer compilation time. The default setting of Automatically can be used with the Auto Fit Fitter Effort Level (also the default) to let the fitter decide whether these optimizations should run based on the routability and timing requirements of the design.

Type

Enumeration

Values

- Always
- Automatically
- Never

Device Support

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name FINAL_PLACEMENT_OPTIMIZATION <value>
```

Default Value

Automatically
1.10.54. FITTER_AGGRESSIVE_ROUTABILITY_OPTIMIZATION

Specifies whether the Fitter aggressively optimizes for routability. Performing aggressive routability optimizations may decrease design speed, but may also reduce routing wire usage and routing time. The default setting of Automatically lets the fitter decide whether to perform these optimizations based on the routability and timing requirements of the design.

**Type**

Enumeration

**Values**

- Always
- Automatically
- Never

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name FITTER_AGGRESSIVE_ROUTABILITY_OPTIMIZATION <value>
```

**Default Value**

Automatically
1.10.55. FITTER_AUTO_EFFORT_DESIRED_SLACK_MARGIN

Specifies the amount of worst-case slack margin the fitter should try to maintain when the Fitter Effort option is set to 'Auto Fit'. If the design is likely to have at least this much slack on every path, the fitter will reduce optimization effort to reduce compilation time. Otherwise, its behavior will be the same as it is with the 'Standard Fit' Fitter Effort setting.

**Type**

Time

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

None

**Syntax**

```
set_global_assignment -name FITTER_AUTO_EFFORT_DESIRED_SLACK_MARGIN <value>
```

**Default Value**

0ns
1.10.56. FITTER_DENSITY_PACKING_EFFORT

Specifies the level of effort Fitter uses to optimize for area when packing. By default, this option is set to 'Normal'. A setting of 'High' can help high utilization designs to successfully fit into the target device. A setting of 'Aggressive' will provide additional area optimization but may impact the timing performance of the design.

**Type**

Enumeration

**Values**

- Aggressive
- High
- Normal

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name FITTER_DENSITY_PACKING_EFFORT <value>
```

**Default Value**

Normal

**Example**

```
set_global_assignment -name FITTER_DENSITY_PACKING_EFFORT high
```
1.10.57. FITTER_EARLY_RETIMING

Allows the Compiler to run global retiming early in the fitter.

Type

Boolean

Device Support

- Intel Agilex
- Intel Stratix 10

Notes

None

Syntax

set_global_assignment -name FITTER_EARLY_RETIMING <value>

Example

set_global_assignment -name FITTER_EARLY_RETIMING on
1.10.58. FITTER_EFFORT

Controls the fitter's trade-off between performance and compilation speed. Auto Fit adjusts the fitter optimization effort to minimize compilation time, while still achieving the design timing requirements. The Auto Fit Effort Desired Slack Margin option can be used to request that Auto Fit apply sufficient optimization effort to achieve additional timing margin. Standard Fit will use maximum effort regardless of the design's requirements, leading to higher compilation time and more margin on easier designs. For difficult designs, Auto Fit and Standard Fit will both use maximum effort. Fast Fit will decrease optimization effort to reduce compilation time, which may degrade design performance.

Type

Enumeration

Values

• Auto Fit
• Fast Fit
• Standard Fit

Device Support

• Intel Arria 10
• Intel Cyclone 10 GX

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name FITTER_EFFORT <value>
```

Default Value

Auto Fit
1.10.59. **FLEX10K_MAX_PERIPHERAL_OE**

Sets the limit on the number of peripheral OE buses that can be used.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```plaintext
set_global_assignment -name FLEX10K_MAX_PERIPHERAL_OE <value>
```
1.10.60. FORCE_CONFIGURATION_VCCIO

Forces the VCCIO voltage of the configuration pins to be the same as the configuration device I/O voltage.

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

None

**Syntax**

```
set_global_assignment -name FORCE_CONFIGURATION_VCCIO <value>
```

**Default Value**

Off

**Example**

```
set_global_assignment -name FORCE_CONFIGURATION_VCCIO ON
```

**See Also**

CONFIGURATION_VCCIO_LEVEL
1.10.61. GLOBAL_PLACEMENT_EFFORT

Controls how much effort the fitter spends during advanced physical placement optimization. High, Optimized and Maximum effort settings spend additional compile time to further optimize the placement solution. The setting Optimize for High Utilization will perform targeted optimization to reduce core logic utilization, which may help address placement or routing issues in high utilization designs.

**Type**

Enumeration

**Values**

- High Effort
- Maximum Effort
- Normal
- Optimized Effort

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name GLOBAL_PLACEMENT_EFFORT <value>
```

**Default Value**

Normal
1.10.62. GLOBAL_SIGNAL

Specifies whether the signal should be routed using global routing paths. Global signals can be both pin- and logic-driven, and can be any signal in the design. In Arria 10 and Cyclone 10 GX devices, setting this option for a pin or a single-output logic function signal is equivalent to feeding the signal through a GLOBAL buffer of the specified type. In all other families, the buffer type is not specified. Rather, a setting of "On" specifies that the signal must use global routing to route to all destinations (or specified subset). Alternatively, a setting of "On - Auto Promote Fanout" on the source specifies that global routing must be used for all destinations, except those that the fitter would normally not consider automatically. In all families, turning this option off for a particular signal will prevent any of the Auto Global options from using the signal as an automatic global signal.

Type

Enumeration

Values

- Dual-Fast Regional Clock
- Dual-Regional Clock
- Fast Regional Clock
- Global Clock
- Large Periphery Clock
- Off
- On
- On - Auto Promote Fanout
- Periphery Clock
- Regional Clock

Device Support

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- EPC1
- EPC2
- Enhanced Configuration Devices
- Flash Memory
- Intel Stratix 10
- Virtual JTAG TAP

Notes

This assignment supports wildcards.

This assignment supports Fitter wildcards.
Syntax

set_instance_assignment -name GLOBAL_SIGNAL -to <to> -entity <entity name> <value>
set_instance_assignment -name GLOBAL_SIGNAL -from <from> -to <to> -entity <entity name> <value>
1.10.63. GNDIO_CURRENT_1PT8V

For user to override GNDIO current of 1.8-V io standard. Original current is 2mA

Type
Integer

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
None

Syntax

```
set_global_assignment -name GNDIO_CURRENT_1PT8V <value>
```
1.10.64. GNDIO_CURRENT_2PT5V

For user to override GNDIO current of 2.5-V io standard. Original current is 2mA

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name GNDIO_CURRENT_2PT5V <value>
```
1.10.65. GNDIO_CURRENT_GTL

For user to override GNDIO current of GTL. Not yet supported in MAX7000.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```text
set_global_assignment -name GNDIO_CURRENT_GTL <value>
```
1.10.66. GNDIO_CURRENT_GTL_PLUS

For user to override GNDIO current of GTL+. Original current is 50mA

Type
Integer

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
None

Syntax

```
set_global_assignment -name GNDIO_CURRENT_GTL_PLUS <value>
```
1.10.67. GNDIO_CURRENT_LVCMOS

For user to override GNDIO current of LVCMOS. Original current is 2mA

**Type**
Integer

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
None

**Syntax**

```plaintext
set_global_assignment -name GNDIO_CURRENT_LVCMOS <value>
```
1.10.68. GNDIO_CURRENT_LVTTL

For user to override GNDIO current of LVTTL. Original current is 4mA

**Type**
Integer

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
None

**Syntax**

```
set_global_assignment -name GNDIO_CURRENT_LVTTL <value>
```
1.10.69. GNDIO_CURRENT_PCI

For user to override GNDIO current of PCI. Original current is 4mA

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```set_global_assignment -name GNDIO_CURRENT_PCI <value>```
1.10.70. GNDIO_CURRENT_SSTL2_CLASS1

For user to override GNDIO current of SSTL2_CLASS1. Original current is 14mA

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name GNDIO_CURRENT_SSTL2_CLASS1 <value>
```
1.10.71. GNDIO_CURRENT_SSTL2_CLASS2

For user to override GNDIO current of SSTL2_CLASS2. Original current is 21mA

Type

Integer

Device Support

• This setting can be used in projects targeting any Intel FPGA device family.

Notes

None

Syntax

set_global_assignment -name GNDIO_CURRENT_SSTL2_CLASS2 <value>
1.10.72. **GNDIO_CURRENT_SSTL3_CLASS1**

For user to override GNDIO current of SSTL3_CLASS1. Original current is 18mA

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name GNDIO_CURRENT_SSTL3_CLASS1 <value>
```
1.10.73. GNDIO_CURRENT_SSTL3_CLASS2

For user to override GNDIO current of SSTL3_CLASS2. Original current is 25mA

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name GNDIO_CURRENT_SSTL3_CLASS2 <value>
```
1.10.74. GXB_0PPM_CORECLK

Specifies core clocks that have zero PPM difference. Follow the Intel High Speed I/O Applications Technical Support recommendations when using this assignment.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

**Syntax**

```
set_instance_assignment -name GXB_0PPM_CORECLK -to <to> -entity <entity name> <value>
```
1.10.75. HPS_COLD_RESET_PIN_MODE

Use the reset pin as input-only or open-drain bidirectional.

Type

Enumeration

Device Support

- Intel Agilex
- Intel Stratix 10

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name HPS_COLD_RESET_PIN_MODE <value>
```

Default Value

BIDIRECTIONAL
1.10.76. HPS_WARM_RESET_PIN_MODE

Use the reset pin as input-only or open-drain bidirectional.

**Type**

Enumeration

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name HPS_WARM_RESET_PIN_MODE <value>
```

**Default Value**

BIDIRECTIONAL
1.10.77. HSSI_PARAMETER

A logic option that allows you to set the parameter settings of the transmitter/receiver channel.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_instance_assignment -name HSSI_PARAMETER -to <to> -entity <entity name> <value>
```
1.10.78. **IGNORE_HSSI_COLUMN_POWER_WHEN_PRESERVING_UNUSED_XCVR_CHANNELS**

Ignore the power supply of HSSI column when preserving unused RX/TX channels. By default, any unused RX/TX channels in each HSSI column will be preserved.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name IGNORE_HSSI_COLUMN_POWER_WHEN_PRESERVING_UNUSED_XCVR_CHANNELS <value>
```

**Default Value**

On

**Example**

```
set_global_assignment -name IGNORE_HSSI_COLUMN_POWER_WHEN_PRESERVING_UNUSED_XCVR_CHANNELS OFF
```
1.10.79. INIT_DONE_OPEN_DRAIN

Specify open drain on the INIT_DONE pin should be enabled or not

Type

Boolean

Device Support

- Intel Arria 10
- Intel Cyclone 10 GX

Notes

None

Syntax

```
set_global_assignment -name INIT_DONE_OPEN_DRAIN <value>
```

Default Value

On

Example

```
set_global_assignment -name init_done_open_drain on
set_global_assignment -name init_done_open_drain off
```

See Also

ENABLE_INIT_DONE_OUTPUT
1.10.80. INPUT_DELAY_CHAIN

Specifies the propagation delay for Input Delay Chain. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

**Old Name**

INPUT_DELAY

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**INTEGER_RANGE**

0, 63

**Notes**

This assignment supports Fitter wildcards.

**Syntax**

```
set_instance_assignment -name INPUT_DELAY_CHAIN -to <to> -entity <entity name> <value>
set_instance_assignment -name INPUT_DELAY_CHAIN -from <from> -to <to> -entity <entity name> <value>
```
1.10.81. INPUT_TERMINATION

Allows the Compiler to configure the on-chip termination (OCT) and impedance matching for an I/O pin. OCT helps to prevent signal reflections and maintain signal integrity. This option is ignored if it is applied to anything other than an I/O pad, input buffer, or output buffer.

Type
String

Device Support
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes
This assignment supports Fitter wildcards.

Syntax

```plaintext
set_instance_assignment -name INPUT_TERMINATION -to <to> -entity <entity name> <value>
```

Example

```plaintext
set_instance_assignment -name INPUT_TERMINATION "PARALLEL 50 OHM WITH CALIBRATION" -to pin_name
```

See Also

IO_STANDARD_OCT_CONTROL_BLOCK_OUTPUT_OCT_VALUE
1.10.82. INTERNAL_SCRUBBING

Specifies internal scrubbing usage for the selected device. If internal scrubbing is turned on, the device corrects single error or double adjacent error within the core configuration memory while the device is still running.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

None

**Syntax**

```
set_global_assignment -name INTERNAL_SCRUBBING <value>
```

**Default Value**

Off

**Example**

```
set_global_assignment -name INTERNAL_SCRUBBING ON
```
1.10.83. **IO_12_LANE_INPUT_DATA_DELAY_CHAIN**

Specifies the propagation delay for IO_12_LANE Input Data Delay Chain. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

**Old Name**

IO_12_LANE_INPUT_DATA_DELAY

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

**Syntax**

```plaintext
set_instance_assignment -name IO_12_LANE_INPUT_DATA_DELAY_CHAIN -to <to> -entity <entity name> <value>
set_instance_assignment -name IO_12_LANE_INPUT_DATA_DELAY_CHAIN -from <from> -to <to> -entity <entity name> <value>
```
1.10.84. IO_12_LANE_INPUT_STROBEDELAY_CHAIN

Specifies the propagation delay for IO_12_LANE Input Strobe Delay Chain. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an input or bidirectional pin.

**Old Name**

IO_12_LANE_INPUT_STROBE_DELAY

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

**Syntax**

```
set_instance_assignment -name IO_12_LANE_INPUT_STROBE_DELAY_CHAIN -to <to> -
entity <entity name> <value>
set_instance_assignment -name IO_12_LANE_INPUT_STROBE_DELAY_CHAIN -from <from> -
to <to> -entity <entity name> <value>
```
1.10.85. IO_MAXIMUM_TOGGLE_RATE

Specifies the toggle rate of this node. You can specify the desired frequency setting. This option is ignored if it is applied to anything other than pins. This option can be used to direct the Fitter in its toggle-rate checking while allowing a single-ended pin to be placed closer to a differential pin. This assignment is used to analyze signal integrity under worst case conditions (highest possible toggle rate). A different assignment, Power Toggle Rate, is used to specify the expected time-averaged toggle rate rather than worst-case toggle rate, and is used by the Power Analyzer to estimate time-averaged power consumption. Use the Synchronizer Toggle Rate if you want to configure the data rates used for Metastability Reporting in the Timing Analyzer.

Old Name

TOGGLE RATE, TOGGLE_RATE

Type

Frequency

Device Support

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes

This assignment supports Fitter wildcards.

Syntax

```
set_instance_assignment -name IO_MAXIMUM_TOGGLE_RATE -to <to> -entity <entity name> <value>
```
1.10.86. IO_PARTITION_PLACEMENT

Specifies whether the I/O should be put in a preserved partition to preserve I/O settings, or if it should be put in the root. Typically I/Os should be placed in the root to maximize the flexibility for the design. However, for some IPs it is desirable to preserve I/O settings such as I/O Standards, in which case it would need to go in the partition.

Type

Enumeration

Values

- PARTITION
- ROOT

Device Support

- Intel Agilex
- Intel Arria 10
- Intel Stratix 10

Notes

None

Syntax

```
set_instance_assignment -name IO_PARTITION_PLACEMENT -to <to> -entity <entity name> <value>
```

Example

```
set_instance_assignment -name IO_PARTITION_PLACEMENT PARTITION -to pin
```
1.10.87. IO_STANDARD

Specifies the I/O standard of a pin. Different device families support different I/O standards, and restrictions apply to placing pins with different I/O standards together. For detailed information, refer to the device family data sheet and to Application Note 117 (Using Selectable I/O Standards in Intel FPGA Devices). This option is ignored if it is applied to anything other than a pin or a top-level design entity.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

This assignment supports synthesis wildcards.

**Syntax**

```
set_instance_assignment -name IO_STANDARD -to <to> -entity <entity name> <value>
```

**Example**

```
set_instance_assignment -name IO_STANDARD LVDS -to pin
```

**See Also**

DEVICE_IO_STANDARD_ALLCURRENT_STRENGTH_NWSLEW_RATEOUTPUT_TERMINATIONINPUT_TERMINATIONPROGRAMMABLE_PREEMPHASISPROGRAMMABLE_VOD
1.10.88. IP_BB_LOCATION

Assign an IP Building Block to a location within a tile

**Type**

String

**Device Support**

- Intel Agilex

**Notes**

None

**Syntax**

```
set_instance_assignment -name IP_BB_LOCATION -to <to> <value>
```
1.10.89. IP_COLOCATE

Assign the IPs implied by the path on or near the specified Tile type

**Type**
Enumeration

**Values**
F_TILE

**Device Support**
- Intel Agilex

**Notes**
None

**Syntax**

```
set_instance_assignment -name IP_COLOCATE -from <from> -to <to> <value>
```
1.10.90. IP_RECONFIG_GROUP_MASTER_CLOCK_CHANNEL

Set AIB that will supply the master clock for the specified reconfiguration group.

**Type**

String

**Device Support**

- Intel Agilex

**Notes**

None

**Syntax**

```plaintext
set_instance_assignment -name IP_RECONFIG_GROUP_MASTER_CLOCK_CHANNEL -to <to> <value>
```
1.10.91. IP_RECONFIG_GROUP_PARENT

Create group hierarchy, should be cumulative like VERILOG_FILE <parent-reconfig-group-id-string>:<child-reconfig-group-id-string>

**Type**

String

**Device Support**

- Intel Agilex

**Notes**

None

**Syntax**

```plaintext
set_global_assignment -name IP_RECONFIG_GROUP_PARENT <value>
```
1.10.92. IP_RECONFIG_GROUP_SHARED_SIP

The SIP of this IP will serve all the profiles of its shared_sip group.

**Type**

Boolean

**Device Support**

- Intel Agilex

**Notes**

None

**Syntax**

```bash
set_instance_assignment -name IP_RECONFIG_GROUP_SHARED_SIP -to <to> <value>
```
### 1.10.93. IP_RECONFIG_ID

Assign a TileIP compliant IP an identifier ID <IP-id>

**Type**

String

**Device Support**

- Intel Agilex

**Notes**

None

**Syntax**

- `set_global_assignment -name IP_RECONFIG_ID <value>`
- `set_instance_assignment -name IP_RECONFIG_ID -to <to> <value>`
1.10.94. IP_TILE_ASSIGNMENT

Assign an IP to a Tile

**Old Name**
IP_TILE_PLACEMENT

**Type**
String

**Device Support**
- Intel Agilex

**Notes**
None

**Syntax**

```
set_instance_assignment -name IP_TILE_ASSIGNMENT -to <to> <value>
```
1.10.95. IP_TILE_SETTING

Specify the topology for the selected tile. Format of the value is: tile id:name:value

Type
String

Device Support
• Intel Agilex

Notes
None

Syntax

set_global_assignment -name IP_TILE_SETTING <value>
1.10.96. LVDS_DIRECT_LOOPBACK_MODE

Enable the LVDS Direct Loop Mode on a True Differential output pin. This assignment should only apply from an input pin to an output pin and both of them should have True Differential I/O standard. When this feature is enabled, data coming in from the adjacent RX pair gets looped back to the TX pair. This feature can be used to verify the Tx and Rx buffer by checking the data transmit and received. This option is ignored if it is applied to anything other than a pin or a top-level design entity.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

**Syntax**

```
set_instance_assignment -name LVDS_DIRECT_LOOPBACK_MODE -from <from> -to <to> -entity <entity name> <value>
```

**Example**

```
set_instance_assignment -name LVDS_DIRECT_LOOPBACK_MODE ON -from true_diff_in_pin_p -to true_diff_out_pin_p
```

**See Also**

IO_STANDARD
1.10.97. MACRO_HEAD

Specifies the head block of a macro.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_instance_assignment -name MACRO_HEAD -to <to> -entity <entity name> <value>
```
1.10.98. MACRO_MEMBER

Specifies a block to be placed with respect to its macro head.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```plaintext
set_global_assignment -name MACRO_MEMBER -entity <entity name> <value>
set_instance_assignment -name MACRO_MEMBER -to <to> -entity <entity name> <value>
set_instance_assignment -name MACRO_MEMBER -from <from> -to <to> -entity <entity name> <value>
```
1.10.99. MATCH_PLL_COMPENSATION_CLOCK

Allows you to specify a PLL output clock feeding a clock network as a compensation target for a PLL in NORMAL or SOURCE_SYNCHRONOUS mode. This configures the PLL to match its feedback path to the target's clock network. This option is ignored if it is applied to anything other than a PLL output clock.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

**Syntax**

```
set_instance_assignment -name MATCH_PLL_COMPENSATION_CLOCK -to <to> -entity <entity name> <value>
```
1.10.100. MIGRATION_DEVICES

Shows the selected migration devices for the target device.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is not copied when you create a companion revision for HardCopy II devices.

**Syntax**

```
set_global_assignment -name MIGRATION_DEVICES <value>
```
1.10.101. MINIMUM_SEU_INTERVAL

Specifies the minimum time between two checks of the same bit. Setting to 0 millisecond means check as frequently as possible. Setting to a large value saves power. The unit of interval is millisecond. The maximum allowed interval time is 10000 milliseconds. The actual minimum interval may exceed the value set here and will be reported in Quartus system messages window when you select the generated .sof file as the input to Quartus Programming File Generator or Quartus Programmer.

Type

Integer

Device Support

• Intel Agilex
• Intel Stratix 10

Notes

None

Syntax

set_global_assignment -name MINIMUM_SEU_INTERVAL <value>
set_instance_assignment -name MINIMUM_SEU_INTERVAL -to <to> <value>

Default Value

10000

Example

set_global_assignment -name MINIMUM_SEU_INTERVAL 300

See Also

CRC_ERROR_CHECKING
1.10.102. MODULE_BLOATING_FACTOR

Allows the Compiler to set a placement bloating factor on a specified entity in the Fitter.

Type

String

Device Support

• This setting can be used in projects targeting any Intel FPGA device family.

Notes

This assignment supports Fitter wildcards.

Syntax

```plaintext
set_global_assignment -name MODULE_BLOATING_FACTOR <value>
set_global_assignment -name MODULE_BLOATING_FACTOR -entity <entity name> <value>
set_instance_assignment -name MODULE_BLOATING_FACTOR -to <to> -entity <entity name> <value>
```

Default Value

0.0

Example

```plaintext
set_instance_assignment -name MODULE_BLOATING_FACTOR 1 -entity ddr
```
1.10.103. NCEO_OPEN_DRAIN

Specify open drain on the nCEO pin should be enabled or not

Type
Boolean

Device Support
• Intel Arria 10
• Intel Cyclone 10 GX

Notes
None

Syntax

```
set_global_assignment -name NCEO_OPEN_DRAIN <value>
```

Default Value
On

Example

```
set_global_assignment -name nceo_open_drain on
set_global_assignment -name nceo_open_drain off
```

See Also
ENABLE_NCEO_OUTPUT
1.10.104. NUMBER_OF_EXAMPLE_NODES_REPORTED

Allows you to specify the maximum number of example nodes fitter messages should display.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name NUMBER_OF_EXAMPLE_NODES_REPORTED <value>
```

**Default Value**

50

**Example**

```
set_global_assignment -name NUMBER_OF_EXAMPLE_NODES_REPORTED 200
```
1.10.105. OE_DELAY_CHAIN

Specifies the propagation delay for Output Enable Delay Chain. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an output or bidirectional pin.

**Old Name**
OE_DELAY

**Type**
Integer

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**INTEGER_RANGE**
0, 15

**Notes**
This assignment supports Fitter wildcards.

**Syntax**

```bash
set_instance_assignment -name OE_DELAY_CHAIN -to <to> -entity <entity name> <value>
```
1.10.106. OPTIMIZE_FOR_METASTABILITY

This setting improves the reliability of the design by increasing its Mean Time Between Failures (MTBF). When this setting is enabled, the Fitter will aim to increase the output setup slacks of synchronizer registers in the design, which can exponentially increase the design MTBF. This option takes effect only if the Timing Analyzer is being used for timing-driven compilation. Use the Timing Analyzer’s report_metastability command to review the synchronizers detected in your design and to produce MTBF estimates.

**Type**

Enumeration

**Values**

- Off
- On

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name OPTIMIZE_FOR_METASTABILITY <value>
```

**Default Value**

On
1.10.107. OPTIMIZE_HOLD_TIMING

Allows the Fitter to optimize hold time by adding delay to the appropriate paths. The Optimize Timing option must be turned on in order for this option to work. If you are using the Timing Analyzer, and specify the I/O paths and Minimum tpd Paths setting, all assignments involving I/O pins are optimized. Specifying the All Paths setting directs the Fitter to optimize the hold time of all paths. Turning off this option directs the Fitter not to optimize the hold time of any paths.

**Type**

Enumeration

**Values**

- All Paths
- IO Paths and Minimum TPD Paths
- Off

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name OPTIMIZE_HOLD_TIMING <value>
```
1.10.108. OPTIMIZE_IOC_REGISTER_PLACEMENT_FOR_TIMING

Controls whether the fitter optimizes I/O pin timing by automatically packing registers into I/Os to minimize I/O -> register and register -> I/O delays. When the 'Normal' option is enabled, the Fitter will opportunistically pack registers into I/Os that should improve I/O timing. When 'Pack All I/O Registers' is enabled, the fitter will aggressively try to pack any registers connected to input, output or output enable pins into I/Os unless prevented by user constraints or other legality restrictions. By default, this option is set to 'Normal'. This option requires the Optimize Timing option to be enabled for it to work.

Type

Enumeration

Values

- Normal
- Off
- Pack All IO Registers

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Notes

This assignment is included in the Fitter report.

Syntax

```set_global_assignment -name OPTIMIZE_IOC_REGISTER_PLACEMENT_FOR_TIMING <value>```

Default Value

Normal
1.10.109. OPTIMIZE_MULTI_CORNER_TIMING

Controls whether the Fitter optimizes a design to meet timing requirements at all process corners and operating conditions. The Optimize Timing logic option must be enabled for this option to work. When this setting is turned off, designs are optimized to meet timing only at the slow timing process corner and operating condition. When this option is turned on, designs are optimized to meet timing at all corners and operating conditions; as a result, turning on this option helps create a design implementation that is more robust across process, temperature, and voltage variations.

Turning on this option does not enable multicorner support for the Timing Analyzer and EDA Netlist Writer. To enable multicorner support for the Timing Analyzer and EDA Netlist Writer, see the Compilation Process Settings page of the Settings dialog box.

Old Name

OPTIMIZE_FAST_CORNER_TIMING, Optimize Fast-Corner Timing

Type

Boolean

Device Support

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- EPC1
- EPC2
- Enhanced Configuration Devices
- Flash Memory
- Intel Stratix 10
- Virtual JTAG TAP

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name OPTIMIZE_MULTI_CORNER_TIMING <value>
```
1.10.110. OPTIMIZE_PERSONA_ROUTABILITY

Allows users to avoid PR aggregate compilation by applying optimization techniques in the router during PR implementation compiles.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name OPTIMIZE_PERSONA_ROUTABILITY <value>
```

**Default Value**

Off
1.10.111. OPTIMIZE_POWER_DURING_FITTING

Controls the power-driven compilation setting of the Fitter. This option determines how aggressively the Fitter optimizes the design for power. If this option is set to 'Off', the Fitter does not perform any power optimizations. If this option is set to 'Normal compilation', the Fitter performs power optimizations which should not impact design performance or increase compile time. When this option is set to 'Extra effort', the Fitter will perform additional power optimizations which may affect design performance and/or increase compile time. For the best results with Extra Effort power optimization during fitting, you should specify a Signal Activity File (SAF file) that lists the toggle rate of each signal in the design. To generate the most accurate Signal Activity File (SAF file) use a gate-level simulation, with glitch filtering, of the compiled design. Specify this SAF file as an input to the Power Analyzer in the Power Analysis Settings, and recompile the design with Extra Effort Power Optimization during fitting. The signal activities (toggle rates) in the SAF file help guide the fitter to reduce power.

**Type**

Enumeration

**Values**

- Extra effort
- Normal compilation
- Off

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

- `set_global_assignment -name OPTIMIZE_POWER_DURING_FITTING <value>`
- `set_global_assignment -name OPTIMIZE_POWER_DURING_FITTING -entity <entity name> <value>`
- `set_instance_assignment -name OPTIMIZE_POWER_DURING_FITTING -to <to> -entity <entity name> <value>`

**Default Value**

Normal compilation
1.10.112. OPTIMIZE_TIMING

Controls whether the Fitter optimizes to meet the maximum delay timing requirements (for example, clock cycle time). By default, this option is set to Normal compilation. Turning it off can help fit designs that have extremely high interconnect requirements and can also reduce compilation time, although at the expense of significant timing performance (since the fitter will be ignoring the design’s timing requirements). If this option is off, other fitter timing optimization options have no effect (such as Optimize Hold Timing).

Old Name

OPTIMIZE_INTERNAL_TIMING, USE_TIMING_DRIVEN_COMPILATION

Type

Enumeration

Values

- Normal compilation
- Off

Device Support

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name OPTIMIZE_TIMING <value>
```

Default Value

Normal compilation
1.10.113. OUTPUT_DELAY_CHAIN

Specifies the propagation delay for Output Delay Chain. This is an advanced option that should be used only after you have compiled a project, checked the I/O timing, and determined that the timing is unsatisfactory. For detailed information on how to use this option, refer to the data sheet for the device family. This option is ignored if it is applied to anything other than an output or bidirectional pin.

**Old Name**
OUTPUT_DELAY

**Type**
Integer

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**INTEGER_RANGE**
0, 15

**Notes**
This assignment supports Fitter wildcards.

**Syntax**

```
set_instance_assignment -name OUTPUT_DELAY_CHAIN -to <to> -entity <entity name> <value>
```
1.10.114. OUTPUT_PIN_LOAD

Specifies the capacitive load, in picofarads (pF), on output pins for each I/O standard. Note: These settings affect FPGA pins only. To specify board trace, termination, and capacitive load parameters for use with Advanced I/O Timing, use the Board Trace Model tab. Capacitive loading is ignored if applied to anything other than an output or bidirectional pin, or if Advanced I/O Timing is enabled.

**Type**

Integer

**Device Support**

- Intel Agilex

**INTEGER_RANGE**

0, 10000

**Notes**

This assignment is copied to any duplicated nodes.

**Syntax**

```
set_instance_assignment -name OUTPUT_PIN_LOAD -to <to> -entity <entity name> <value>
set_global_assignment -name OUTPUT_PIN_LOAD -section_id <section identifier> <value>
```
1.10.115. OUTPUT_TERMINATION

Allows the Compiler to configure the on-chip termination (OCT) and impedance matching for an I/O pin. OCT helps to prevent signal reflections and maintain signal integrity. This option is ignored if it is applied to anything other than an I/O pad, input buffer, or output buffer.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

**Syntax**

```
set_instance_assignment -name OUTPUT_TERMINATION -to <to> -entity <entity name> <value>
```

**Example**

```
set_instance_assignment -name OUTPUT_TERMINATION "SERIES 50 OHM WITH CALIBRATION" -to pin_name
```

**See Also**

INPUT_OCT_VALUEIO_STANDARDOCT_CONTROL_BLOCK
1.10.116. PERIPHERY_TO_CORE_PLACEMENT_AND_ROUTING_OPTIMIZATION

Specifies whether the Fitter should perform targeted placement and routing optimization on direct connections between periphery logic and registers in the FPGA core. If this option is set to 'Auto', the Fitter will automatically identify transfers with tight timing windows, place the core registers, and route all connections to or from the periphery. These placement and routing decisions are performed before the rest of core placement and routing, ensuring these timing-critical connections can meet timing, and also avoid routing congestion. If this option is set to 'On', all transfers between the periphery and core registers will be optimized, regardless of timing requirements. Setting this option to 'On' globally is not recommended -- instead it is intended for use in the Assignment Editor to force optimization to a targeted set of nodes or entities.

**Type**

Enumeration

**Values**

- Auto
- Off
- On

**Device Support**

- Intel Arria 10

**Notes**

This assignment supports wildcards.

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

The value of this assignment must be a node name.

**Syntax**

```plaintext
set_global_assignment -name PERIPHERY_TO_CORE_PLACEMENT_AND_ROUTING_OPTIMIZATION <value>
set_global_assignment -name PERIPHERY_TO_CORE_PLACEMENT_AND_ROUTING_OPTIMIZATION -entity <entity name> <value>
set_instance_assignment -name PERIPHERY_TO_CORE_PLACEMENT_AND_ROUTING_OPTIMIZATION -to <to> -entity <entity name> <value>
```

**Default Value**

OFF
1.10.117. **PERIPH_FITTER_SCRIPT**

Specifies the name of the tcl script that will be used to overwrite the default periphery fitter placement script used during a normal compile.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name PERIPH_FITTER_SCRIPT <value>
```
1.10.118. PERIPH_REPORT_SCRIPT

Specifies the name of the tcl script that will be used to overwrite the default periphery fitter report panels created during a normal compile.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name PERIPH_REPORT_SCRIPT <value>
```
1.10.119. PHYSICAL_RAM_RPT_MAX_ROW

Allows you to specify the maximum number of physical M20Ks reported in the physical RAM report.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name PHYSICAL_RAM_RPT_MAX_ROW <value>
```

**Default Value**

500

**Example**

```
set_global_assignment -name PHYSICAL_RAM_RPT_MAX_ROW 1000
```
1.10.120. PHYSICAL_SYNTHESIS

Enables the Physical Synthesis engine that includes combinational and sequential optimization during fitting to improve circuit performance.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name PHYSICAL_SYNTHESIS <value>
```
1.10.121. PLACEMENT_EFFORT_MULTIPLIER

Controls how much time the fitter spends in placement. The default value is 1.0 and legal values must be greater than 0. Specifying a floating-point number allows you to control the placement effort. A higher value increases CPU time but may improve placement quality. For example, a value of ‘4’ will increase fitting time by approximately 2 to 4 times but may increase quality.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- EPC1
- EPC2
- Enhanced Configuration Devices
- Flash Memory
- Intel Stratix 10
- Virtual JTAG TAP

**Notes**

This assignment is not copied when you create a companion revision for HardCopy II devices.

This assignment is included in the Fitter report.

**Syntax**

```display
set_global_assignment -name PLACEMENT_EFFORT_MULTIPLIER <value>
```

**Default Value**

1.0
1.10.122. PLL_AUTO_RESET

Causes the PLL to self-reset automatically on loss of lock.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_instance_assignment -name PLL_AUTO_RESET -to <to> -entity <entity name> <value>
```
1.10.123. PLL_BANDWIDTH_PRESET

Specifies the PLL bandwidth preset setting.

**Type**

Enumeration

**Values**

- Auto
- High
- Low
- Medium

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

This assignment supports synthesis wildcards.

**Syntax**

```
set_instance_assignment -name PLL_BANDWIDTH_PRESET -to <to> -entity <entity name> <value>
```
1.10.124. PLL_COMPENSATION_MODE

Specifies the routing path of the PLL feedback clock and adjusts the delay chains in the PLL.

Type

Enumeration

Values

- Direct
- External Feedback
- LVDS
- Normal
- Source Synchronous
- Zero Delay Buffer

Device Support

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes

This assignment supports Fitter wildcards.
This assignment is included in the Fitter report.
This assignment supports synthesis wildcards.

Syntax

```
set_instance_assignment -name PLL_COMPENSATION_MODE -to <to> -entity <entity name> <value>
```
1.10.125. PLL_OPTIMIZE_PHASE_SHIFT_FOR_TIMING

Allows the Fitter to set the phase shift of a PLL output counter, and hence the phase shift of its generated clock, to improve timing for all edges affected by this clock. Apply multicycle timing exceptions to paths between the generated clock and other clocks in the design to avoid timing violations.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_instance_assignment -name PLL_OPTIMIZE_PHASE_SHIFT_FOR_TIMING -to <to> -entity <entity name> <value>
```
1.10.126. PRESERVE_UNUSED_XCVR_CHANNEL

Preserve the performance of unused RX/TX channels over time, if they are intended to be used in future

Type
Boolean

Device Support
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes
This assignment is included in the Fitter report.

Syntax

set_global_assignment -name PRESERVE_UNUSED_XCVR_CHANNEL <value>
set_instance_assignment -name PRESERVE_UNUSED_XCVR_CHANNEL -to <to> -entity <entity name> <value>

Default Value
Off

Example

set_global_assignment -name PRESERVE_UNUSED_XCVR_CHANNEL ON
set_instance_assignment -name PRESERVE_UNUSED_XCVR_CHANNEL ON -to AW34
1.10.127. PRIORITY_SEU_AREA

Priority SEU checks on the specified area as fast as possible

**Type**
Boolean

**Device Support**
- Intel Agilex
- Intel Stratix 10

**Notes**
None

**Syntax**

```
set_global_assignment -name PRIORITY_SEU_AREA <value>
set_instance_assignment -name PRIORITY_SEU_AREA -to <to> <value>
```

**Default Value**
Off
1.10.128. PROGRAMMABLE_DEEMPHASIS

Specifies Programmable De-emphasis of a pin.

**Type**

Enumeration

**Values**

- HIGH_CZ
- HIGH_LP
- LOW_CZ
- LOW_LP
- MEDIUM_CZ
- MEDIUM_LP
- OFF

**Device Support**

- Intel Agilex

**Notes**

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name PROGRAMMABLE_DEEMPHASIS <value>
set_global_assignment -name PROGRAMMABLE_DEEMPHASIS -entity <entity name> <value>
set_instance_assignment -name PROGRAMMABLE_DEEMPHASIS -to <to> -entity <entity name> <value>
```

**Example**

```plaintext
set_instance_assignment -name PROGRAMMABLE_DEEMPHASIS HIGH_LP -to pin
```

**See Also**

IO_STANDARD
1.10.129. PROGRAMMABLE_POWER_MAXIMUM_HIGH_SPEED_FRACTION_OF_USED_LAB_TILES

Sets an upper limit on the fraction of the LAB tiles used by your design that can be high-speed. Legal values must be between 0.0 and 1.0. The default value is 1.0. A value of 1.0 means that there is no restriction on the number of high-speed tiles, and the fitter will use the minimum number needed to meet the timing requirements of your design. Specifying a value lower than 1.0 might degrade timing quality, because some timing critical resources might be forced into low-power mode.

**Type**

String

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name PROGRAMMABLE_POWER_MAXIMUM_HIGH_SPEED_FRACTION_OF_USED_LAB_TILES <value>
```

**Default Value**

1.0
1.10.130. PROGRAMMABLE_POWER_TECHNOLOGY_SETTING

Controls how the fitter configures tiles to operate in high-speed mode or low-power mode. Automatic specifies that the fitter should try to minimize power without sacrificing timing performance. Minimize Power Only specifies that the fitter should set the maximum number of tiles to operate in low-power mode. Force All Used Tiles to High Speed specifies that the fitter should set all used tiles to operate in high-speed mode. Force All Tiles with Failing Timing Paths to High Speed specifies that the fitter should ensure that all paths that are failing timing are set to high-speed mode. For designs that meet timing, the behavior of this setting should be similar to the Automatic setting. For designs that fail timing, all paths with negative slack will be put in high-speed mode. Note that this will likely not increase the speed of the design, and it may increase static power consumption, but it may assist in determining which logic paths need to be re-designed in order to close timing.

**Type**

Enumeration

**Values**

- Automatic
- Force All Tiles with Failing Timing Paths to High Speed
- Force All Used Tiles to High Speed
- Minimize Power Only

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name PROGRAMMABLE_POWER_TECHNOLOGY_SETTING <value>
```
1.10.131. PROGRAMMABLE_PREEMPHASIS

Implements control of programmable pre-emphasis, which helps compensate for high frequency losses. This option is ignored if it is applied to anything other than an output or bidirectional pin, or a top-level design entity containing output or bidirectional pins.

Type

Integer

Device Support

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

INTEGER_RANGE

0, 3

Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name PROGRAMMABLE_PREEMPHASIS -entity <entity name> <value>
set_instance_assignment -name PROGRAMMABLE_PREEMPHASIS -to <to> -entity <entity name> <value>
set_global_assignment -name PROGRAMMABLE_PREEMPHASIS <value>
```

Example

```
set_instance_assignment -name PROGRAMMABLE_PREEMPHASIS 0 -to pin
```

See Also

IO_STANDARD
1.10.132. PROGRAMMABLE_VOD

Implements control of programmable VOD. This option is ignored if it is applied to anything other than an output or bidirectional pin, or a top-level design entity containing output or bidirectional pins.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**INTEGER_RANGE**

0, 3

**Notes**

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name PROGRAMMABLE_VOD -entity <entity name> <value>
set_instance_assignment -name PROGRAMMABLE_VOD -to <to> -entity <entity name> <value>
set_global_assignment -name PROGRAMMABLE_VOD <value>
```

**Example**

```
set_instance_assignment -name PROGRAMMABLE_PREEMPHASIS 0 -to pin
```

**See Also**

IO_STANDARD
1.10.133. **PR_DONE_OPEN_DRAIN**

Specify open drain on the PR_DONE pin should be enabled or not

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

None

**Syntax**

```plaintext
set_global_assignment -name PR_DONE_OPEN_DRAIN <value>
```

**Default Value**

On

**Example**

```plaintext
set_global_assignment -name pr_done_open_drain on
set_global_assignment -name pr_done_open_drain off
```

**See Also**

ENABLE_PR_PINS
1.10.134. PR_ERROR_OPEN_DRAIN

Specify open drain on the PR_ERROR pin should be enabled or not

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

None

**Syntax**

```
set_global_assignment -name PR_ERROR_OPEN_DRAIN <value>
```

**Default Value**

On

**Example**

```
set_global_assignment -name pr_error_open_drain on
set_global_assignment -name pr_error_open_drain off
```

**See Also**

ENABLE_PR_PINS
1.10.135. PR_PINS_OPEN_DRAIN

Specifies open drain on the Partial Reconfiguration pins (PR_READY, PR_ERROR, and PR_DONE) should be enabled or not

**Type**
Boolean

**Device Support**
- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**
None

**Syntax**

```plaintext
set_global_assignment -name PR_PINS_OPEN_DRAIN <value>
```

**Default Value**

Off

**Example**

```plaintext
set_global_assignment -name pr_pins_open_drain on
set_global_assignment -name pr_pins_open_drain off
```

**See Also**

ENABLE_PR_PINS
### 1.10.136. PR_READY.OPEN_DRAIN

Specify open drain on the PR READY pin should be enabled or not

**Type**
Boolean

**Device Support**
- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**
None

**Syntax**

```shell
set_global_assignment -name PR_READY_OPEN_DRAIN <value>
```

**Default Value**
On

**Example**

```shell
set_global_assignment -name pr_ready_open_drain on
set_global_assignment -name pr_ready_open_drain off
```

**See Also**
ENABLE_PR_PINS
### 1.10.137. PR_SECURITY_VALIDATION

Generates a Partial Reconfiguration Security Masked Settings files (.smsf) containing data that an external controller can use to verify integrity of a new configuration of the target device region.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```shell
set_global_assignment -name PR_SECURITY_VALIDATION <value>
```

**Default Value**

Off

**Example**

```shell
set_global_assignment -name pr_security_validation on
```
1.10.138. PUD_CTRL

Pull up/down for resistor. This ACF variable only applies to Diamond Mesa.

Type
String

Device Support
- eASIC N5X

Notes
This assignment supports Fitter wildcards.

Syntax

set_instance_assignment -name PUD_CTRL -to <to> -entity <entity name> <value>

Example

set_instance_assignment -name PUD_CTRL 6 -to output_pin
1.10.139. QII_AUTO_PACKED_REGISTERS

Allows the Compiler to combine a register and a combinational function, or to implement registers using I/O cells, RAM blocks, or DSP blocks instead of logic cells. This option controls how aggressively the Fitter combines registers with other function blocks to reduce the area of the design. Generally, the 'Auto' or 'Sparse Auto' settings should be used for this option. The other options limit the flexibility of the Fitter to combine registers with other function blocks and can result in no fits. When 'Auto', the default setting is selected, the Fitter attempts to achieve the best performance with good area. If necessary, additional logic is combined to reduce the area of the design so that it can fit within the selected device. When this setting is 'Sparse Auto', the Fitter attempts to achieve the highest performance with possibly increased area, but without exceeding the logic capacity of the device. If this option is set to 'Off', the Fitter does not combine registers with other functions. The 'Off' setting severely increases the area of the design and may cause a no fit. If this option is set to 'Sparse', the Fitter combines functions in a way which improves performance for many designs. If this option is set to 'Normal', the Fitter combines functions that are expected to maximize design performance and reduce area. When this option is set to 'Minimize Area', the Fitter aggressively combines unrelated functions to reduce the area required for placing the design, at the expense of performance. When this option is set to 'Minimize Area with Chains', the Fitter even more aggressively combines functions that are part of register cascade chains or can be converted to register cascade chains. If this option is set to any value but 'Off', registers are combined with I/O cells to improve I/O timing (as long as the Optimize IOC Register Placement For Timing option allows it), and with DSP blocks and RAM blocks to reduce the area required for placing the design or to improve timing when possible.

Old Name
AUTO_PACKED_REGISTERS_ARMSTRONG, AUTO_PACKED_REGISTERS_STRATIXII,
Auto Packed Registers -- Stratix II/II GX/III Cyclone II/III Arria GX

Type
Enumeration

Values
- Auto
- Minimize Area
- Minimize Area with Chains
- Normal
- Off
- Sparse
- Sparse Auto

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
This assignment supports Fitter wildcards.
This assignment is included in the Fitter report.
Syntax

set_global_assignment -name QII_AUTO_PACKED_REGISTERS <value>
set_global_assignment -name QII_AUTO_PACKED_REGISTERS -entity <entity name> <value>
set_instance_assignment -name QII_AUTO_PACKED_REGISTERS -to <to> -entity <entity name> <value>

Default Value

Auto
1.10.140. RELATIVE_NEUTRON_FLUX

is the neutron flux rate used by the seu calculator

Type
Double

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```
set_global_assignment -name RELATIVE_NEUTRON_FLUX <value>
```

Default Value

1.0
1.10.141. RESERVE_ALL_UNUSED_PINS_WEAK_PULLUP

Reserves all unused pins on the target device in one of 5 states: as inputs that are tri-stated, as outputs that drive ground, as outputs that drive an unspecified signal, as input tri-stated with bus-hold, or as input tri-stated with weak pull-up.

**Type**

Enumeration

**Values**

- As input tri-stated
- As input tri-stated with bus-hold
- As input tri-stated with weak pull-up
- As output driving an unspecified signal
- As output driving ground

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name RESERVE_ALL_UNUSED_PINS_WEAK_PULLUP <value>
```

**Default Value**

As input tri-stated with weak pull-up
1.10.142. RESERVE_AVST_CLK_AFTER_CONFIGURATION

Specifies how the AVST clock pin should be used when the device is operating in user mode after configuration via AVST x16 or AVST x32 is complete.

**Type**

Enumeration

**Values**

- As input tri-stated
- Use as regular IO

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

None

**Syntax**

```
set_global_assignment -name RESERVE_AVST_CLK_AFTER_CONFIGURATION <value>
```

**Default Value**

Use as regular IO

**Example**

```
set_global_assignment -name RESERVE_AVST_CLK_AFTER_CONFIGURATION "USE AS REGULAR IO"
```
1.10.143. RESERVE_AVST_DATA15_THROUGH_DATA0_AFTER_CONFIGURATION

Specifies how the AVST data[15:0] pin should be used when the device is operating in user mode after configuration via AVST x16 or AVST x32 is complete.

**Type**

Enumeration

**Values**

- As input tri-stated
- Use as regular IO

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

None

**Syntax**

```
set_global_assignment -name RESERVE_AVST_DATA15_THROUGH_DATA0_AFTER_CONFIGURATION <value>
```

**Default Value**

Use as regular IO

**Example**

```
set_global_assignment -name RESERVE_AVST_DATA15_THROUGH_DATA0_AFTER_CONFIGURATION "USE AS REGULAR IO"
```
### 1.10.144. RESERVE_AVST_DATA31_THROUGH_DATA16_AFTER_CONFIGURATION

Specifies how the AVST data[31:16] pin should be used when the device is operating in user mode after configuration via AVST x32 is complete.

**Type**

Enumeration

**Values**

- As input tri-stated
- Use as regular IO

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

None

**Syntax**

```bash
set_global_assignment -name RESERVE_AVST_DATA31_THROUGH_DATA16_AFTER_CONFIGURATION <value>
```

**Default Value**

Use as regular IO

**Example**

```bash
set_global_assignment -name RESERVE_AVST_DATA31_THROUGH_DATA16_AFTER_CONFIGURATION "USE AS REGULAR IO"
```
1.10.145. RESERVE_AVST_VALID_AFTER_CONFIGURATION

Specifies how the AVST valid pin should be used when the device is operating in user mode after configuration via AVST x16 or AVST x32 is complete.

**Type**

Enumeration

**Values**

- As input tri-stated
- Use as regular IO

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

None

**Syntax**

```plaintext
set_global_assignment -name RESERVE_AVST_VALID_AFTER_CONFIGURATION <value>
```

**Default Value**

Use as regular IO

**Example**

```plaintext
set_global_assignment -name RESERVE_AVST_VALID_AFTER_CONFIGURATION "USE AS REGULAR IO"
```
1.10.146. RESERVE_DATA0_AFTER_CONFIGURATION

Specifies how the Data[0] pin should be used when the device is operating in user mode after configuration is complete. Depending on the current device and configuration scheme, the Data[0] pin can be reserved as a regular I/O pin, as an input that is tri-stated, as an output that drives ground, as an output that drives an unspecified signal, or compiler configured. If the Data[0] pin is reserved as a regular I/O pin, the Data[0] pin can be used as an ordinary I/O pin after configuration. If the Data[0] pin is only used to interface with external memory for configuration, the Data[0] pin should be reserved as compiler configured.

**Type**

Enumeration

**Values**

- As input tri-stated
- As output driving an unspecified signal
- As output driving ground
- Compiler configured
- Use as regular IO

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

None

**Syntax**

```
set_global_assignment -name RESERVE_DATA0_AFTER_CONFIGURATION <value>
```

**Default Value**

As input tri-stated

**Example**

```
set_global_assignment -name RESERVE_DATA0_AFTER_CONFIGURATION "USE AS REGULAR IO"
```
1.10.147. **RESERVE_DATA15_THROUGH_DATA8_AFTER_CONFIGURATION**

Specifies how the Data[15..8] pins should be used when the device is operating in user mode after configuration is complete.

**Type**

Enumeration

**Values**

- As input tri-stated
- As output driving an unspecified signal
- As output driving ground
- Use as regular IO

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

None

**Syntax**

```plaintext
set_global_assignment -name RESERVE_DATA15_THROUGH_DATA8_AFTER_CONFIGURATION <value>
```

**Default Value**

Use as regular IO

**Example**

```plaintext
set_global_assignment -name RESERVE_DATA15_THROUGH_DATA8_AFTER_CONFIGURATION "USE AS REGULAR IO"
```
1.10.148. RESERVE_DATA31_THROUGH_DATA16_AFTER_CONFIGURATION

Specifies how the Data[31..16] pins should be used when the device is operating in user mode after configuration is complete.

Type
Enumeration

Values
• As input tri-stated
• As output driving an unspecified signal
• As output driving ground
• Use as regular IO

Device Support
• Intel Arria 10
• Intel Cyclone 10 GX

Notes
None

Syntax

```
set_global_assignment -name RESERVE_DATA31_THROUGH_DATA16_AFTER_CONFIGURATION <value>
```

Default Value
Use as regular IO

Example

```
set_global_assignment -name RESERVE_DATA31_THROUGH_DATA16_AFTER_CONFIGURATION "USE AS REGULAR IO"
```
1.10.149. RESERVE_DATA7_THROUGH_DATA1_AFTER_CONFIGURATION

Specifies how the Data[7..1] pins should be used when the device is operating in user mode after configuration is complete. Depending on the current device and configuration scheme, these pins can be reserved as regular I/O pins, as inputs that are tri-stated, as outputs that drive ground, or as outputs that drive an unspecified signal. If this pin is reserved as a regular I/O pin, the Data[7..1] pins can be used as ordinary I/O pins after configuration.

**Type**

Enumeration

**Values**

- As input tri-stated
- As output driving an unspecified signal
- As output driving ground
- Use as regular IO

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

None

**Syntax**

```
set_global_assignment -name RESERVE_DATA7_THROUGH_DATA1_AFTER_CONFIGURATION <value>
```

**Default Value**

Use as regular IO

**Example**

```
set_global_assignment -name RESERVE_DATA7_THROUGH_DATA1_AFTER_CONFIGURATION
"USE AS REGULAR IO"
```
1.10.150. RESERVE_FLEXIBLE_CLOCK_NETWORK

Allows you to specify whether this clock should be routed using only flexible section clock network routing. This setting may improve routability for reconfigurable clocks, or clocks that will drive new logic in a later compile.

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

This assignment supports Fitter wildcards.

**Syntax**

```plaintext
set_instance_assignment -name RESERVE_FLEXIBLE_CLOCK_NETWORK -to <to> -entity <entity name> <value>
```
1.10.151. RESERVE_PR_PINS

Allows you to reserve the PR_REQUEST, PR_READY, PR_ERROR, PR_DONE, DCLK, and DATA[15..0] pins and prevent other pins from using them. Once these pins are reserved, they could not use to support partial reconfiguration (PR) with an external host as well when the device operates in user mode.

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

None

**Syntax**

```plaintext
set_global_assignment -name RESERVE_PR_PINS <value>
```

**Default Value**

Off

**Example**

```plaintext
set_global_assignment -name RESERVE_PR_PINS ON
```

**See Also**

ENABLE_PR_PINS
1.10.152. RESERVE_ROUTING_OUTPUT_FLEXIBILITY

Allows you to specify whether the router should reserve output flexibility in this compilation. This setting helps maintain certain routing flexibility for later compilation, but may affect routability in this compilation.

Type
Boolean

Device Support
- Intel Arria 10
- Intel Cyclone 10 GX

Notes
This assignment supports Fitter wildcards.

Syntax

```bash
set_global_assignment -name RESERVE_ROUTING_OUTPUT_FLEXIBILITY <value>
```

Default Value
Off
1.10.153. ROUTER_CLOCKING_TOPOLOGY_ANALYSIS

Directs the router to perform an analysis of the design's clocking topology and adjust the optimization approach on paths with significant clock skew. Enabling this option may improve hold timing at the cost of increased compile time.

Type

Boolean

Device Support

- Intel Arria 10
- Intel Cyclone 10 GX

Notes

This assignment is not copied when you create a companion revision for HardCopy II devices.

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name ROUTER_CLOCKING_TOPOLOGY_ANALYSIS <value>
```

Default Value

Off
1.10.154. ROUTER_EFFORT_MULTIPLIER

Controls how quickly the router tries to find a valid solution. The default value is 1.0 and legal values must be greater than or equal to 0.25. Values higher than 1.0 may improve routing quality at the expense of run-time on difficult-to-route circuits. Values lower than 1.0 can reduce router run-time, but usually reduces routing quality slightly.

**Type**

String

**Device Support**

- EPC1
- EPC2
- Enhanced Configuration Devices
- Flash Memory
- Virtual JTAG TAP

**Notes**

This assignment is not copied when you create a companion revision for HardCopy II devices.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ROUTER_EFFORT_MULTIPLIER <value>
```

**Default Value**

1.0
1.10.155. ROUTER_LCELL_INSERTION_AND_LOGIC_DUPLICATION

Allows the Fitter to automatically insert buffer logic cells between two nodes without altering the functionality of the design. Buffer logic cells are created from unused logic cells in the device. This option also allows the Fitter to duplicate a logic cell within a LAB when there are unused logic cells available in a LAB. Using this option can increase compilation time. The default setting of Auto will allow these operations to run when 1) the design requires them to fit the design or 2) the performance of the design can be improved by this optimization with a nominal compilation time increase.

**Type**

Enumeration

**Values**

- Auto
- Off
- On

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ROUTER_LCELL_INSERTION_AND_LOGIC_DUPLICATION <value>
```

**Default Value**

Auto
1.10.156. ROUTER_REGISTER_DUPLICATION

Allows the Fitter to automatically duplicate registers within a LAB containing empty logic cells. This option does not alter the functionality of the design. The Auto Register Duplication option is also ignored if you select OFF as the setting for the Logic Cell Insertion -- Logic Duplication logic option. Turning on this option can allow the Logic Cell Insertion -- Logic Duplication logic option to improve a design's routability, but can make formal verification of a design more difficult.

**Type**

Enumeration

**Values**

- Auto
- Off
- On

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ROUTER_REGISTER_DUPLICATION <value>
```

**Default Value**

Auto
1.10.157. ROUTER_TIMING_OPTIMIZATION_LEVEL

Controls how aggressively the router tries to meet timing requirements. Setting this option to Maximum can increase design speed slightly, at the cost of increased compile time. Setting this option to Minimum can reduce compile time, at the cost of slightly reduced design speed. The default value is Normal.

Type
Enumeration

Values
- MAXIMUM
- MINIMUM
- Normal

Device Support
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- EPC1
- EPC2
- Enhanced Configuration Devices
- Flash Memory
- Intel Stratix 10
- Virtual JTAG TAP

Notes
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name ROUTER_TIMING_OPTIMIZATION_LEVEL <value>
```

Default Value
Normal
1.10.158. RZQ_GROUP

Specifies an RZQ pin name and an OCT to terminate the given pin. Using the same RZQ pin name instructs the fitter to use the same OCT to terminate the group of pins.

Type

String

Device Support

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes

This assignment supports Fitter wildcards.

Syntax

```
set_instance_assignment -name RZQ_GROUP -to <to> -entity <entity name> <value>
```

Example

```
set_instance_assignment -name RZQ_GROUP oct_rzq_in -to output_pin
```

See Also

OUTPUT_TERMINATION
1.10.159. SCHMITT_TRIGGER

Turn on schmitt trigger.

Type
Boolean

Device Support
- Intel Agilex

Notes
This assignment supports Fitter wildcards.
This assignment is included in the Fitter report.

Syntax

- `set_global_assignment -name SCHMITT_TRIGGER -entity <entity name> <value>`
- `set_instance_assignment -name SCHMITT_TRIGGER -to <to> -entity <entity name> <value>`
- `set_global_assignment -name SCHMITT_TRIGGER <value>`

Default Value

On
1.10.160. **SDM_DIRECT_TO_FACTORY_IMAGE**

If this pin asserted then device loads the factory image as the first image after boot without attempting to load any application image.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```text
set_global_assignment -name SDM_DIRECT_TO_FACTORY_IMAGE <value>
```

**Default Value**

Off
1.10.161. SDM_PCIE_CALIB_START

Output to drive high when configuration has started PCIe Calibration.

Type
String

Device Support
• Intel Agilex
• Intel Stratix 10

Notes
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name SDM_PCIE_CALIB_START <value>
```

Default Value
Off
1.10.162. SEED

Specifies the starting value the Fitter uses when randomly determining the initial placement for the current design. The value can be any non-negative integer value. Changing the starting value may or may not produce better fitting. Specify a starting value only if the Fitter is not meeting timing requirements by a small amount. The Design Space Explorer tool lets you sweep many seed values easily to find the best value for a given project. Modifying the design or Quartus settings even slightly will usually change which seed is best for the design.

**Old Name**

INITIAL_PLACEMENT_CONFIGURATION

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is not copied when you create a companion revision for HardCopy II devices.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name SEED <value>
```

**Default Value**

1
1.10.163. SEU_FIT_REPORT

determines whether the SEU report is displayed or not

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name SEU_FIT_REPORT <value>
```

**Default Value**
Off
1.10.164. SLEW_RATE

Implements control of low-to-high/high-to-low transitions on output pins to help reduce switching noise. When a large number of output pins switch simultaneously, pins that use the lower Slew Rate option help reduce switching noise. This option is ignored if it is applied to anything other than an output or bidirectional pin, or a top-level design entity containing output or bidirectional pins. Note that using this option may increase the delay for output or bidir pins, which can affect slack on Tco paths for the pins this is applied to.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10
- eASIC N5X

**INTEGER_RANGE**

0, 3

**Notes**

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name SLEW_RATE -entity <entity name> <value>
set_instance_assignment -name SLEW_RATE -to <to> -entity <entity name> <value>
set_global_assignment -name SLEW_RATE <value>
```

**Example**

```
set_instance_assignment -name SLEW_RATE 0 -to pin
```

**See Also**

IO_STANDARDCURRENT_STRENGTH_NEWOUTPUT_TERMINATION
1.10.165. SLOW_SLEW_RATE

Implements slow low-to-high/high-to-low transitions on output pins to help reduce switching noise. When a large number of output pins switch simultaneously, pins that use the Slow Slew Rate option help reduce switching noise. This option is ignored if it is applied to anything other than an output or bidirectional pin, or a top-level design entity containing output or bidirectional pins. Note that using this option increases the delay for output or bidir pins, which can affect slack on Tco paths for the pins this is applied to.

Type
Boolean

Device Support
• EPC1
• EPC2
• Enhanced Configuration Devices

Notes
This assignment supports Fitter wildcards.
This assignment is included in the Fitter report.

Syntax

- `set_global_assignment -name SLOW_SLEW_RATE -entity <entity name> <value>`
- `set_instance_assignment -name SLOW_SLEW_RATE -to <to> -entity <entity name> <value>`
- `set_global_assignment -name SLOW_SLEW_RATE <value>`

Default Value
Off
1.10.166. STRATIXV_CONFIGURATION_SCHEME

The method used to configure a device with a design. Available configuration schemes depend on selected device family: Passive Serial (PS), Passive Parallel x8 (PPx8), Passive Parallel x16 (PPx16), Passive Parallel x32 (PPx32), Active Serial x1 (ASx1), Active Serial x4 (ASx4) and AVST x8, x16 and x32.

Type

Enumeration

Values

- AVST x16
- AVST x32
- AVST x8
- Active Serial
- Active Serial x1
- Active Serial x4
- Passive Parallel x16
- Passive Parallel x32
- Passive Parallel x8
- Passive Serial

Device Support

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10
- eASIC N5X

Notes

None

Syntax

```bash
set_global_assignment -name STRATIXV_CONFIGURATION_SCHEME <value>
```

Example

```bash
set_global_assignment -name STRATIXV_CONFIGURATION_SCHEME "Active Serial"
```
1.10.167. SYNCHRONIZER_IDENTIFICATION

Specifies how the Timing Analyzer identifies registers as being part of a synchronization register chain for metastability analysis. A synchronization register chain is a sequence of registers with the same clock with no fan-out in between, which is driven by a pin or logic from another clock domain. When this option is set to 'Off', the Timing Analyzer does not identify the specified registers, or the registers within the specified entity, as synchronization registers. When the option is set to 'Auto', the Timing Analyzer identifies valid synchronization registers that are part of a chain with more than one register that contains no combinational logic. When this option is set to 'Forced if Asynchronous', the Timing Analyzer identifies synchronization register chains if the software detects an asynchronous signal transfer, even if there is combinational logic or only one register in the chain. When this option is set to 'Forced', then the specified register, or all registers within the specified entity, are always identified as synchronizers, even if the software does not detect an asynchronous signal transfer. Note that the 'Forced' option should not be applied to the entire design (and cannot be applied from the Quartus GUI's Settings dialog), because doing so identifies all registers in the design as synchronizers. Also, it is not possible to set the global detection setting to 'Off'; attempting to do so will have it changed to 'Auto'. If a synchronization register chain is identified with the 'Forced' or 'Forced if Asynchronous' option, then its registers are optimized for improved Mean Time Between Failure (MTBF) as long as the Optimize Design for Metastability option is turned on, and the Timing Analyzer reports the metastability MTBF for the chain if it meets the design timing requirements. However, synchronization register chains identified with the 'Auto' option instead of the 'Forced' or 'Forced if Asynchronous' options will be excluded from metastability optimization and reporting unless the 'Analyze Auto-Detected Synchronizers for Metastability' setting is enabled. Otherwise, you can use the 'Auto' setting to generate a report of possible synchronization chains in your design.

Old Name
ANALYZE_METASTABILITY

Type
Enumeration

Values
• Auto
• Forced
• Forced If Asynchronous
• Off

Device Support
• Intel Agilex
• Intel Arria 10
• Intel Cyclone 10 GX
• Intel Stratix 10

Notes
This assignment supports wildcards.
This assignment supports Fitter wildcards.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name SYNCHRONIZER_IDENTIFICATION <value>
set_global_assignment -name SYNCHRONIZER_IDENTIFICATION -entity <entity name> <value>
set_instance_assignment -name SYNCHRONIZER_IDENTIFICATION -to <to> -entity <entity name> <value>
```

**Default Value**

Auto
1.10.168. SYNCHRONIZER_TOGGLE_RATE

Specifies the toggle rate of this register. The units for this value are in transitions per second, and must be positive. This is used when calculating the Mean Time Between Failures (MTBF) of a synchronizer chain in the Metastability Report. This only applies when the Timing Analyzer is used. You can specify the desired frequency setting on the first register of a synchronizer chain, and this will determine the data rate used in the MTBF estimation. There are two other assignments associated with toggle rates. The I/O Maximum Toggle Rate is only used for pins, and specifies the worst-case toggle rates used for signal integrity purposes. The Power Toggle Rate assignment is used to specify the expected time-averaged toggle rate, and is used by the Power Analyzer to estimate time-averaged power consumption.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment supports Fitter wildcards.

**Syntax**

```
set_instance_assignment -name SYNCHRONIZER_TOGGLE_RATE -to <to> -entity <entity name> <value>
```
1.10.169. TERMINATION_CONTROL_BLOCK

Specifies the control block used for calibrated on-chip termination (OCT) and impedance matching for an I/O pin. OCT helps to prevent signal reflections and maintain signal integrity. This option is ignored if it is applied to anything other than an I/O pad, input buffer, or output buffer. This option should only be used on I/O pins which have a calibrated termination assignment.

**Type**
String

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**
The value of this assignment is case sensitive.
This assignment is copied to any duplicated nodes.
This assignment supports Fitter wildcards.
The value of this assignment must be a node name.

**Syntax**

```
set_instance_assignment -name TERMINATION_CONTROL_BLOCK -to <to> -entity <entity name> <value>
```

**Example**

```
set_instance_assignment -name TERMINATION_CONTROL_BLOCK "my_oct:inst|my_oct_alt_oct_toq:my_oct_alt_oct_toq_component|sd1a_0" -to pin_name
```

**See Also**
INPUT_OCT_VALUE | IO_STANDARD | OUTPUT_OCT_VALUE
1.10.170. TREAT_BIDIR_AS_OUTPUT

Directs the bidirectional pin to be essentially treated as an output pin meaning that the input path is used for feedback from the output path.

Type

Boolean

Device Support

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

Syntax

```plaintext
set_global_assignment -name TREAT_BIDIR_AS_OUTPUT <value>
set_global_assignment -name TREAT_BIDIR_AS_OUTPUT -entity <entity name> <value>
set_instance_assignment -name TREAT_BIDIR_AS_OUTPUT -to <to> -entity <entity name> <value>
```

Default Value

Off

Example

```plaintext
set_instance_assignment -name TREAT_BIDIR_AS_OUTPUT ON -to bidir_pin
```

See Also

IO_STANDARD
1.10.171. TRI_STATE_SPI_PINS

This option controls Active Configuration Controller to tri-state the Active Configuration pins in user mode. This option would be ignored if the selected configuration scheme is not an Active Configuration scheme.

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name TRI_STATE_SPI_PINS <value>
```

**Default Value**

Off
1.10.172. UNFORCE_MERGE_PLL

Prevents the specified PLL to be merged with the master PLL. Use this option only for two compatible PLLs driven by the same clock source.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

**Syntax**

```
set_instance_assignment -name UNFORCE_MERGE_PLL -to <to> -entity <entity name> <value>
```
1.10.173. UNUSED_IO_BANK_VOLTAGE

Specifies the configuration for vccio for unused bank.

**Type**

Enumeration

**Values**

- 0V
- 1.2V
- 1.5V

**Device Support**

- Intel Agilex

**Notes**

None

**Syntax**

```
set_global_assignment -name UNUSED_IO_BANK_VOLTAGE <value>
```

**Example**

```
set_global_assignment -name UNUSED_IO_BANK_VOLTAGE 1.2V
```
1.10.174. UNUSED_TSD_PINS_GND

If this option is turned on, unused temperature sensing diode (TSD) pins, TEMPDIODEp/TEMPDIODEn, on the device are automatically set to GND in the Pin-Out File (.pin) file. By default, the TSD pins are available for connection to an external temperature sensing device; however, you must manually connect the pins to GND if they are not connected. Turning on this option only updates the information in the .pin file, it does not affect FPGA behavior.

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

None

**Syntax**

```
set_global_assignment -name UNUSED_TSD_PINS_GND <value>
```

**Default Value**

Off
1.10.175. **USE_ANTI_TAMPER**

Output to indicate anti-tampering activity.

**Type**
String

**Device Support**
- Intel Agilex
- Intel Stratix 10

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name USE_ANTI_TAMPER <value>
```

**Default Value**
Off
1.10.176. USE_AS_3V_GPIO

This assignment is required when attempting to place a GPIO using a non-3V IO standard in a location that supports 3V IOs. It allows the fitter to place this in a 3V IO location (not allowed by default). Applies to S10 only.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

This assignment supports synthesis wildcards.

**Syntax**

```bash
set_global_assignment -name USE_AS_3V_GPIO -entity <entity name> <value>
set_instance_assignment -name USE_AS_3V_GPIO -to <to> -entity <entity name> <value>
```

**Example**

```bash
set_instance_assignment -name USE_AS_3V_GPIO ON -to pin
```
1.10.177. USE_CONF_DONE

Implement CONF_DONE using appropriate configuration pin resource.

**Type**
String

**Device Support**
- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name USE_CONF_DONE <value>
```

**Default Value**
Off
1.10.178. USE_CVP_CONFDONE

Enable the CvP_CONFDONE pin, which indicates that the device finished core programming in Configuration via Protocol mode. If this option is turned off, the CvP_CONFDONE pin is disabled when the device operates in user mode and is available as a user I/O pin.

**Type**
String

**Device Support**
- Intel Agilex
- Intel Stratix 10

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name USE_CVP_CONFDONE <value>
```

**Default Value**
Off
1.10.179. USE_DATA_UNLOCK

Output to indicate Direct Interface Bus on both FPGA die in the same package is ready for data transfer. This is applicable to multiple FPGA die device only.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name USE_DATA_UNLOCK <value>
```

**Default Value**

Off
1.10.180. USE_HPS_COLD_RESET

Enable the HPS cold reset pin.

**Type**
String

**Device Support**
- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name USE_HPS_COLD_RESET <value>
```

**Default Value**
Off
1.10.181. USE_HPS_WARM_RESET

Enable the HPS warm reset pin.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitler report.

**Syntax**

```
set_global_assignment -name USE_HPS_WARM_RESET <value>
```

**Default Value**

Off
1.10.182. USE_INIT_DONE

Enables the INIT_DONE pin, which allows you to externally monitor when initialization is completed and the device is in user mode. If this option is turned off, the INIT_DONE pin is disabled when the device operates in user mode and is available as a user I/O pin.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name USE_INIT_DONE <value>
```

**Default Value**

Off
1.10.183. **USE_NCATTRIP**

Output to indicate an extreme over-temperature conditioning.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name USE_NCATTRIP <value>
```

**Default Value**

Off
1.10.184. USE_PWRMGT_ALERT

Implement PWRMGT_ALERT using appropriate configuration pin resource.

**Type**
String

**Device Support**
- Intel Agilex
- Intel Stratix 10

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name USE_PWRMGT_ALERT <value>
```

**Default Value**
Off
1.10.185. USE_PWRMGT_PWM0

An output signal generated from PMW master.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name USE_PWRMGT_PWM0 <value>
```

**Default Value**

Off
### 1.10.186. USE_PWRMGT_SCL

Implement PWRMGT_SCL using appropriate configuration pin resource.

**Type**
String

**Device Support**
- Intel Agilex
- Intel Stratix 10

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name USE_PWRMGT_SCL <value>
```

**Default Value**
Off
1.10.187. USE_PWRMGT_SDA

Implement PWRMGT_SDA using appropriate configuration pin resource.

**Type**
String

**Device Support**
- Intel Agilex
- Intel Stratix 10

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name USE_PWRMGT_SDA <value>
```

**Default Value**
Off
1.10.188. USE_SEU_ERROR

Enable the SEU_ERROR pin.

Type
String

Device Support
• Intel Agilex
• Intel Stratix 10

Notes
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name USE_SEU_ERROR <value>
```

Default Value
Off
1.10.189. USE_TAMPER_DETECT

Output to indicate a tampering detected.

**Type**
String

**Device Support**
- Intel Agilex
- Intel Stratix 10
- eASIC N5X

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name USE_TAMPER_DETECT <value>
```

**Default Value**
Off
1.10.190. USE_UIB_CATTRIP

Output to indicate an extreme over-temperature conditioning.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name USE_UIB_CATTRIP <value>
```

**Default Value**

Off
1.10.191. VCCIO_CURRENT_1PT8V

For user to override VCCIO current of 1.8-V io standard. Original current is 2mA

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name VCCIO_CURRENT_1PT8V <value>
```
1.10.192. VCCIO_CURRENT_2PT5V

For user to override VCCIO current of 2.5-V io standard. Original current is 2mA

Type
Integer

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
None

Syntax

set_global_assignment -name VCCIO_CURRENT_2PT5V <value>
1.10.193. VCCIO_CURRENT_GTL

For user to override VCCIO current of GTL. Not yet supported in MAX7000.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name VCCIO_CURRENT_GTL <value>
```
1.10.194. VCCIO_CURRENT_GTL_PLUS

For user to override VCCIO current of GTL+. Original current is 0mA

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```plaintext
set_global_assignment -name VCCIO_CURRENT_GTL_PLUS <value>
```
1.10.195. VCCIO_CURRENT_LVCMOS

For user to override VCCIO current of LVCMOS. Original current is 2mA

Type
Integer

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
None

Syntax

```plaintext
set_global_assignment -name VCCIO_CURRENT_LVCMOS <value>
```
1.10.196. VCCIO_CURRENT_LVTTL

For user to override VCCIO current of LVTTL. Original current is 4mA

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name VCCIO_CURRENT_LVTTL <value>
```
1.10.197. **VCCIO_CURRENT_PCI**

For user to override VCCIO current of PCI. Original current is 4mA

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```plaintext
set_global_assignment -name VCCIO_CURRENT_PCI <value>
```
1.10.198. VCCIO_CURRENT_SSTL2_CLASS1

For user to override VCCIO current of SSTL2_CLASS1. Original current is 14mA

**Type**
Integer

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
None

**Syntax**

```
set_global_assignment -name VCCIO_CURRENT_SSTL2_CLASS1 <value>
```
1.10.199. VCCIO_CURRENT_SSTL2_CLASS2

For user to override VCCIO current of SSTL2_CLASS2. Original current is 21mA

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name VCCIO_CURRENT_SSTL2_CLASS2 <value>
```
1.10.200. **VCCIO_CURRENT_SSTL3_CLASS1**

For user to override VCCIO current of SSTL3_CLASS1. Original current is 18mA

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name VCCIO_CURRENT_SSTL3_CLASS1 <value>
```
1.10.201. VCCIO_CURRENT_SSTL3_CLASS2

For user to override VCCIO current of SSTL3_CLASS2. Original current is 25mA

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name VCCIO_CURRENT_SSTL3_CLASS2 <value>
```
1.10.202. VID_OPERATION_MODE

Enable Voltage Identification Logic in the target device with selected operation mode.

**Type**

Enumeration

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VID_OPERATION_MODE <value>
```

**Default Value**

PMBus Master

**Example**

```
set_global_assignment -name VID_OPERATION_MODE "PMBus Master"
```
1.10.203. VREF_MODE

Specifies VREF mode of a pin.

**Type**

Enumeration

**Values**

- CALIBRATED
- CALIBRATED_SSTL
- DDR4_CAL
- DDR4_CAL_RANGE2
- DDR4_NOCAL
- EXTERNAL
- HALF_NOCAL
- VCCIO_45
- VCCIO_50
- VCCIO_55
- VCCIO_65
- VCCIO_70
- VCCIO_75

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

**Syntax**

```bash
set_global_assignment -name VREF_MODE <value>
set_global_assignment -name VREF_MODE -entity <entity name> <value>
set_instance_assignment -name VREF_MODE -to <to> -entity <entity name> <value>
```

**Example**

```bash
set_instance_assignment -name VREF_MODE EXTERNAL -to pin
```

**See Also**

VREF_MODE
1.10.204. WEAK_PULL_UP_DN_SEL

Weak pull up or pull down select for 3 flavors of pull up or pull down resistors, i.e. 20 KOhm, 50 KOhm and 80 KOhm. This option is intended to work for HPS dedicated IOs

**Type**

Enumeration

**Values**

- NO_PULL_UP_DN
- PULL_DN_20
- PULL_DN_50
- PULL_DN_80
- PULL_UP_20
- PULL_UP_50
- PULL_UP_80

**Device Support**

- Intel Agilex

**Notes**

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name WEAK_PULL_UP_DN_SEL -entity <entity name> <value>
set_instance_assignment -name WEAK_PULL_UP_DN_SEL -to <to> -entity <entity name> <value>
set_global_assignment -name WEAK_PULL_UP_DN_SEL <value>
```
1.10.205. WEAK_PULL_UP_RESISTOR

Enables the weak pull-up resistor when the device is operating in user mode. This option pulls a high-impedance bus signal to VCC. The Weak Pull-Up Resistor option should not be used at the same time as the Enable Bus-Hold Circuitry option. This option is ignored if it is applied to anything other than a pin.

Type

Boolean

Device Support

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

Syntax

```plaintext
set_global_assignment -name WEAK_PULL_UP_RESISTOR <value>
set_global_assignment -name WEAK_PULL_UP_RESISTOR -entity <entity name> <value>
set_instance_assignment -name WEAK_PULL_UP_RESISTOR -to <to> -entity <entity name> <value>
```

Default Value

Off

Example

```plaintext
set_instance_assignment -name WEAK_PULL_UP_RESISTOR ON -to pin
```
1.10.206. WIRELUT_REMOVAL_HOLD_GUARD_BAND

Hold guard band value used in wirelut removal stage.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name WIRELUT_REMOVAL_HOLD_GUARD_BAND <value>
```

**Default Value**

100
1.10.207. WIRELUT_REMOVAL_SETUP_GUARD_BAND

Setup guard band value used in wirelut removal stage.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name WIRELUT_REMOVAL_SETUP_GUARD_BAND <value>
```

**Default Value**

100
1.10.208. XCVR_A10_REFCLK_TERM_TRISTATE

A logic option that directs the Compiler to enable the internal termination of the dedicated reference clock pin.

**Type**

Enumeration

**Values**

- TRISTATE_OFF
- TRISTATE_ON

**Device Support**

- Intel Arria 10

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_REFCLK_TERM_TRISTATE -to <to> -entity <entity name> <value>
```
1.10.209. XCVR_A10_RX_ADPA2_CTLE_ACGAIN_4S

A logic option that allows you to control the amount of AC gain on the equalizer in high gain mode. The amount of AC gain is proportional to the setting where '0' gives the lowest AC gain and '31' gives the largest AC gain. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- `RADP_CTLE_ACGAIN_4S_0`
- `RADP_CTLE_ACGAIN_4S_1`
- `RADP_CTLE_ACGAIN_4S_10`
- `RADP_CTLE_ACGAIN_4S_11`
- `RADP_CTLE_ACGAIN_4S_12`
- `RADP_CTLE_ACGAIN_4S_13`
- `RADP_CTLE_ACGAIN_4S_14`
- `RADP_CTLE_ACGAIN_4S_15`
- `RADP_CTLE_ACGAIN_4S_16`
- `RADP_CTLE_ACGAIN_4S_17`
- `RADP_CTLE_ACGAIN_4S_18`
- `RADP_CTLE_ACGAIN_4S_19`
- `RADP_CTLE_ACGAIN_4S_2`
- `RADP_CTLE_ACGAIN_4S_20`
- `RADP_CTLE_ACGAIN_4S_21`
- `RADP_CTLE_ACGAIN_4S_22`
- `RADP_CTLE_ACGAIN_4S_23`
- `RADP_CTLE_ACGAIN_4S_24`
- `RADP_CTLE_ACGAIN_4S_25`
- `RADP_CTLE_ACGAIN_4S_26`
- `RADP_CTLE_ACGAIN_4S_27`
- `RADP_CTLE_ACGAIN_4S_28`
- `RADP_CTLE_ACGAIN_4S_3`
- `RADP_CTLE_ACGAIN_4S_4`
- `RADP_CTLE_ACGAIN_4S_5`
- `RADP_CTLE_ACGAIN_4S_6`
- `RADP_CTLE_ACGAIN_4S_7`
- `RADP_CTLE_ACGAIN_4S_8`
- `RADP_CTLE_ACGAIN_4S_9`
Device Support
- Intel Arria 10

Notes

Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_CTLE_ACGAIN_4S -to <to> -entity <entity name> <value>
```
1.10.210. XCVR_A10_RX_ADPA_DP_CTLE_EQZ_1S_SEL

A logic option that allows you to control the amount of AC gain on the one-stage equalizer. The amount of AC gain is proportional to the setting where '0' gives the lowest AC gain and '15' gives the largest AC gain. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_CTLE_EQZ_1S_SEL_0
- RADP_CTLE_EQZ_1S_SEL_1
- RADP_CTLE_EQZ_1S_SEL_10
- RADP_CTLE_EQZ_1S_SEL_11
- RADP_CTLE_EQZ_1S_SEL_12
- RADP_CTLE_EQZ_1S_SEL_13
- RADP_CTLE_EQZ_1S_SEL_14
- RADP_CTLE_EQZ_1S_SEL_15
- RADP_CTLE_EQZ_1S_SEL_2
- RADP_CTLE_EQZ_1S_SEL_3
- RADP_CTLE_EQZ_1S_SEL_4
- RADP_CTLE_EQZ_1S_SEL_5
- RADP_CTLE_EQZ_1S_SEL_6
- RADP_CTLE_EQZ_1S_SEL_7
- RADP_CTLE_EQZ_1S_SEL_8
- RADP_CTLE_EQZ_1S_SEL_9

**Device Support**

- Intel Arria 10

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_RX_ADPA_DP_CTLE_EQZ_1S_SEL -to <to> -entity <entity name> <value>
```
A logic option that allows you to specify the coefficient setting for fix tap one in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP1_0
- RADP_DFE_FXTAP1_1
- RADP_DFE_FXTAP1_10
- RADP_DFE_FXTAP1_100
- RADP_DFE_FXTAP1_101
- RADP_DFE_FXTAP1_102
- RADP_DFE_FXTAP1_103
- RADP_DFE_FXTAP1_104
- RADP_DFE_FXTAP1_105
- RADP_DFE_FXTAP1_106
- RADP_DFE_FXTAP1_107
- RADP_DFE_FXTAP1_108
- RADP_DFE_FXTAP1_109
- RADP_DFE_FXTAP1_11
- RADP_DFE_FXTAP1_110
- RADP_DFE_FXTAP1_111
- RADP_DFE_FXTAP1_112
- RADP_DFE_FXTAP1_113
- RADP_DFE_FXTAP1_114
- RADP_DFE_FXTAP1_115
- RADP_DFE_FXTAP1_116
- RADP_DFE_FXTAP1_117
- RADP_DFE_FXTAP1_118
- RADP_DFE_FXTAP1_119
- RADP_DFE_FXTAP1_12
- RADP_DFE_FXTAP1_120
- RADP_DFE_FXTAP1_121
- RADP_DFE_FXTAP1_122
- RADP_DFE_FXTAP1_123
- RADP_DFE_FXTAP1_124
• RADP_DFE_FXTAP1_45
• RADP_DFE_FXTAP1_46
• RADP_DFE_FXTAP1_47
• RADP_DFE_FXTAP1_48
• RADP_DFE_FXTAP1_49
• RADP_DFE_FXTAP1_5
• RADP_DFE_FXTAP1_50
• RADP_DFE_FXTAP1_51
• RADP_DFE_FXTAP1_52
• RADP_DFE_FXTAP1_53
• RADP_DFE_FXTAP1_54
• RADP_DFE_FXTAP1_55
• RADP_DFE_FXTAP1_56
• RADP_DFE_FXTAP1_57
• RADP_DFE_FXTAP1_58
• RADP_DFE_FXTAP1_59
• RADP_DFE_FXTAP1_6
• RADP_DFE_FXTAP1_60
• RADP_DFE_FXTAP1_61
• RADP_DFE_FXTAP1_62
• RADP_DFE_FXTAP1_63
• RADP_DFE_FXTAP1_64
• RADP_DFE_FXTAP1_65
• RADP_DFE_FXTAP1_66
• RADP_DFE_FXTAP1_67
• RADP_DFE_FXTAP1_68
• RADP_DFE_FXTAP1_69
• RADP_DFE_FXTAP1_7
• RADP_DFE_FXTAP1_70
• RADP_DFE_FXTAP1_71
• RADP_DFE_FXTAP1_72
• RADP_DFE_FXTAP1_73
• RADP_DFE_FXTAP1_74
• RADP_DFE_FXTAP1_75
• RADP_DFE_FXTAP1_76
• RADP_DFE_FXTAP1_77
• RADP_DFE_FXTAP1_78
• RADP_DFE_FXTAP1_79
- RADP_DFE_FXTAP1_8
- RADP_DFE_FXTAP1_80
- RADP_DFE_FXTAP1_81
- RADP_DFE_FXTAP1_82
- RADP_DFE_FXTAP1_83
- RADP_DFE_FXTAP1_84
- RADP_DFE_FXTAP1_85
- RADP_DFE_FXTAP1_86
- RADP_DFE_FXTAP1_87
- RADP_DFE_FXTAP1_88
- RADP_DFE_FXTAP1_89
- RADP_DFE_FXTAP1_9
- RADP_DFE_FXTAP1_90
- RADP_DFE_FXTAP1_91
- RADP_DFE_FXTAP1_92
- RADP_DFE_FXTAP1_93
- RADP_DFE_FXTAP1_94
- RADP_DFE_FXTAP1_95
- RADP_DFE_FXTAP1_96
- RADP_DFE_FXTAP1_97
- RADP_DFE_FXTAP1_98
- RADP_DFE_FXTAP1_99

**Device Support**
- Intel Arria 10

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_RX_ADPA_DFE_FXTAP1 -to <to> -entity <entity name> <value>
```
1.10.212. XCVR_A10_RX_ADJ_DFE_FXTAP10

A logic option that allows you to specify the coefficient setting for fix tap ten in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP10_0
- RADP_DFE_FXTAP10_1
- RADP_DFE_FXTAP10_10
- RADP_DFE_FXTAP10_11
- RADP_DFE_FXTAP10_12
- RADP_DFE_FXTAP10_13
- RADP_DFE_FXTAP10_14
- RADP_DFE_FXTAP10_15
- RADP_DFE_FXTAP10_16
- RADP_DFE_FXTAP10_17
- RADP_DFE_FXTAP10_18
- RADP_DFE_FXTAP10_19
- RADP_DFE_FXTAP10_2
- RADP_DFE_FXTAP10_20
- RADP_DFE_FXTAP10_21
- RADP_DFE_FXTAP10_22
- RADP_DFE_FXTAP10_23
- RADP_DFE_FXTAP10_24
- RADP_DFE_FXTAP10_25
- RADP_DFE_FXTAP10_26
- RADP_DFE_FXTAP10_27
- RADP_DFE_FXTAP10_28
- RADP_DFE_FXTAP10_29
- RADP_DFE_FXTAP10_3
- RADP_DFE_FXTAP10_30
- RADP_DFE_FXTAP10_31
- RADP_DFE_FXTAP10_32
- RADP_DFE_FXTAP10_33
- RADP_DFE_FXTAP10_34
- RADP_DFE_FXTAP10_35
Device Support

- Intel Arria 10
Notes

Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP10 -to <to> -entity <entity name> <value>
```
1.10.213. XCVR_A10_RX_ADJ_DFE_FXTAP10_SGN

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP10_SGN_0
- RADP_DFE_FXTAP10_SGN_1

**Device Support**

- Intel Arria 10

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_RX_ADJ_DFE_FXTAP10_SGN -to <to> -entity <entity name> <value>
```
1.10.214. XCVR_A10_RX_ADH_DFE_FXTAP11

A logic option that allows you to specify the coefficient setting for fix tap eleven in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP11_0
- RADP_DFE_FXTAP11_1
- RADP_DFE_FXTAP11_10
- RADP_DFE_FXTAP11_11
- RADP_DFE_FXTAP11_12
- RADP_DFE_FXTAP11_13
- RADP_DFE_FXTAP11_14
- RADP_DFE_FXTAP11_15
- RADP_DFE_FXTAP11_16
- RADP_DFE_FXTAP11_17
- RADP_DFE_FXTAP11_18
- RADP_DFE_FXTAP11_19
- RADP_DFE_FXTAP11_2
- RADP_DFE_FXTAP11_20
- RADP_DFE_FXTAP11_21
- RADP_DFE_FXTAP11_22
- RADP_DFE_FXTAP11_23
- RADP_DFE_FXTAP11_24
- RADP_DFE_FXTAP11_25
- RADP_DFE_FXTAP11_26
- RADP_DFE_FXTAP11_27
- RADP_DFE_FXTAP11_28
- RADP_DFE_FXTAP11_29
- RADP_DFE_FXTAP11_3
- RADP_DFE_FXTAP11_30
- RADP_DFE_FXTAP11_31
- RADP_DFE_FXTAP11_32
- RADP_DFE_FXTAP11_33
- RADP_DFE_FXTAP11_34
- RADP_DFE_FXTAP11_35
Device Support

- Intel Arria 10
Notes

Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP11 -to <to> -entity <entity name> <value>
```
1.10.215. XCVR_A10_RX_ADP_DFE_FXTAP11_SGN

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP11_SGN_0
- RADP_DFE_FXTAP11_SGN_1

**Device Support**

- Intel Arria 10

**Notes**

**Syntax**

```bash
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP11_SGN -to <to> -entity <entity name> <value>
```
1.10.216. XCVR_A10_RX_ADPIP DFE_FXTAP2

A logic option that allows you to specify the coefficient setting for fix tap two in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP2_0
- RADP_DFE_FXTAP2_1
- RADP_DFE_FXTAP2_10
- RADP_DFE_FXTAP2_100
- RADP_DFE_FXTAP2_101
- RADP_DFE_FXTAP2_102
- RADP_DFE_FXTAP2_103
- RADP_DFE_FXTAP2_104
- RADP_DFE_FXTAP2_105
- RADP_DFE_FXTAP2_106
- RADP_DFE_FXTAP2_107
- RADP_DFE_FXTAP2_108
- RADP_DFE_FXTAP2_109
- RADP_DFE_FXTAP2_11
- RADP_DFE_FXTAP2_110
- RADP_DFE_FXTAP2_111
- RADP_DFE_FXTAP2_112
- RADP_DFE_FXTAP2_113
- RADP_DFE_FXTAP2_114
- RADP_DFE_FXTAP2_115
- RADP_DFE_FXTAP2_116
- RADP_DFE_FXTAP2_117
- RADP_DFE_FXTAP2_118
- RADP_DFE_FXTAP2_119
- RADP_DFE_FXTAP2_12
- RADP_DFE_FXTAP2_120
- RADP_DFE_FXTAP2_121
- RADP_DFE_FXTAP2_122
- RADP_DFE_FXTAP2_123
- RADP_DFE_FXTAP2_124
• RADP_DFE_FXTAP2_125
• RADP_DFE_FXTAP2_126
• RADP_DFE_FXTAP2_127
• RADP_DFE_FXTAP2_13
• RADP_DFE_FXTAP2_14
• RADP_DFE_FXTAP2_15
• RADP_DFE_FXTAP2_16
• RADP_DFE_FXTAP2_17
• RADP_DFE_FXTAP2_18
• RADP_DFE_FXTAP2_19
• RADP_DFE_FXTAP2_2
• RADP_DFE_FXTAP2_20
• RADP_DFE_FXTAP2_21
• RADP_DFE_FXTAP2_22
• RADP_DFE_FXTAP2_23
• RADP_DFE_FXTAP2_24
• RADP_DFE_FXTAP2_25
• RADP_DFE_FXTAP2_26
• RADP_DFE_FXTAP2_27
• RADP_DFE_FXTAP2_28
• RADP_DFE_FXTAP2_29
• RADP_DFE_FXTAP2_3
• RADP_DFE_FXTAP2_30
• RADP_DFE_FXTAP2_31
• RADP_DFE_FXTAP2_32
• RADP_DFE_FXTAP2_33
• RADP_DFE_FXTAP2_34
• RADP_DFE_FXTAP2_35
• RADP_DFE_FXTAP2_36
• RADP_DFE_FXTAP2_37
• RADP_DFE_FXTAP2_38
• RADP_DFE_FXTAP2_39
• RADP_DFE_FXTAP2_4
• RADP_DFE_FXTAP2_40
• RADP_DFE_FXTAP2_41
• RADP_DFE_FXTAP2_42
• RADP_DFE_FXTAP2_43
• RADP_DFE_FXTAP2_44

MNL-1088 | 2021.06.21

- RADP_DFE_FXTAP2_45
- RADP_DFE_FXTAP2_46
- RADP_DFE_FXTAP2_47
- RADP_DFE_FXTAP2_48
- RADP_DFE_FXTAP2_49
- RADP_DFE_FXTAP2_5
- RADP_DFE_FXTAP2_50
- RADP_DFE_FXTAP2_51
- RADP_DFE_FXTAP2_52
- RADP_DFE_FXTAP2_53
- RADP_DFE_FXTAP2_54
- RADP_DFE_FXTAP2_55
- RADP_DFE_FXTAP2_56
- RADP_DFE_FXTAP2_57
- RADP_DFE_FXTAP2_58
- RADP_DFE_FXTAP2_59
- RADP_DFE_FXTAP2_6
- RADP_DFE_FXTAP2_60
- RADP_DFE_FXTAP2_61
- RADP_DFE_FXTAP2_62
- RADP_DFE_FXTAP2_63
- RADP_DFE_FXTAP2_64
- RADP_DFE_FXTAP2_65
- RADP_DFE_FXTAP2_66
- RADP_DFE_FXTAP2_67
- RADP_DFE_FXTAP2_68
- RADP_DFE_FXTAP2_69
- RADP_DFE_FXTAP2_7
- RADP_DFE_FXTAP2_70
- RADP_DFE_FXTAP2_71
- RADP_DFE_FXTAP2_72
- RADP_DFE_FXTAP2_73
- RADP_DFE_FXTAP2_74
- RADP_DFE_FXTAP2_75
- RADP_DFE_FXTAP2_76
- RADP_DFE_FXTAP2_77
- RADP_DFE_FXTAP2_78
- RADP_DFE_FXTAP2_79
Device Support

- Intel Arria 10

Notes

Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP2 -to <to> -entity <entity name> <value>
```
1.10.217. XCVR_A10_RX_AD_P_DFE_FXTAP2_SGN

Type
Enumeration

Values
- RADP_DFE_FXTAP2_SGN_0
- RADP_DFE_FXTAP2_SGN_1

Device Support
- Intel Arria 10

Notes

Syntax

```
set_instance_assignment -name XCVR_A10_RX_AD_P_DFE_FXTAP2_SGN -to <to> -entity <entity name> <value>
```
1.10.218. XCVR_A10_RX_ADG_DFE_FXTAP3

A logic option that allows you to specify the coefficient setting for fix tap three in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP3_0
- RADP_DFE_FXTAP3_1
- RADP_DFE_FXTAP3_10
- RADP_DFE_FXTAP3_100
- RADP_DFE_FXTAP3_101
- RADP_DFE_FXTAP3_102
- RADP_DFE_FXTAP3_103
- RADP_DFE_FXTAP3_104
- RADP_DFE_FXTAP3_105
- RADP_DFE_FXTAP3_106
- RADP_DFE_FXTAP3_107
- RADP_DFE_FXTAP3_108
- RADP_DFE_FXTAP3_109
- RADP_DFE_FXTAP3_11
- RADP_DFE_FXTAP3_110
- RADP_DFE_FXTAP3_111
- RADP_DFE_FXTAP3_112
- RADP_DFE_FXTAP3_113
- RADP_DFE_FXTAP3_114
- RADP_DFE_FXTAP3_115
- RADP_DFE_FXTAP3_116
- RADP_DFE_FXTAP3_117
- RADP_DFE_FXTAP3_118
- RADP_DFE_FXTAP3_119
- RADP_DFE_FXTAP3_12
- RADP_DFE_FXTAP3_120
- RADP_DFE_FXTAP3_121
- RADP_DFE_FXTAP3_122
- RADP_DFE_FXTAP3_123
- RADP_DFE_FXTAP3_124
• RADP_DFE_FXTAP3_125
• RADP_DFE_FXTAP3_126
• RADP_DFE_FXTAP3_127
• RADP_DFE_FXTAP3_13
• RADP_DFE_FXTAP3_14
• RADP_DFE_FXTAP3_15
• RADP_DFE_FXTAP3_16
• RADP_DFE_FXTAP3_17
• RADP_DFE_FXTAP3_18
• RADP_DFE_FXTAP3_19
• RADP_DFE_FXTAP3_2
• RADP_DFE_FXTAP3_20
• RADP_DFE_FXTAP3_21
• RADP_DFE_FXTAP3_22
• RADP_DFE_FXTAP3_23
• RADP_DFE_FXTAP3_24
• RADP_DFE_FXTAP3_25
• RADP_DFE_FXTAP3_26
• RADP_DFE_FXTAP3_27
• RADP_DFE_FXTAP3_28
• RADP_DFE_FXTAP3_29
• RADP_DFE_FXTAP3_3
• RADP_DFE_FXTAP3_30
• RADP_DFE_FXTAP3_31
• RADP_DFE_FXTAP3_32
• RADP_DFE_FXTAP3_33
• RADP_DFE_FXTAP3_34
• RADP_DFE_FXTAP3_35
• RADP_DFE_FXTAP3_36
• RADP_DFE_FXTAP3_37
• RADP_DFE_FXTAP3_38
• RADP_DFE_FXTAP3_39
• RADP_DFE_FXTAP3_4
• RADP_DFE_FXTAP3_40
• RADP_DFE_FXTAP3_41
• RADP_DFE_FXTAP3_42
• RADP_DFE_FXTAP3_43
• RADP_DFE_FXTAP3_44
• RADP_DFE_FXTAP3_45
• RADP_DFE_FXTAP3_46
• RADP_DFE_FXTAP3_47
• RADP_DFE_FXTAP3_48
• RADP_DFE_FXTAP3_49
• RADP_DFE_FXTAP3_5
• RADP_DFE_FXTAP3_50
• RADP_DFE_FXTAP3_51
• RADP_DFE_FXTAP3_52
• RADP_DFE_FXTAP3_53
• RADP_DFE_FXTAP3_54
• RADP_DFE_FXTAP3_55
• RADP_DFE_FXTAP3_56
• RADP_DFE_FXTAP3_57
• RADP_DFE_FXTAP3_58
• RADP_DFE_FXTAP3_59
• RADP_DFE_FXTAP3_6
• RADP_DFE_FXTAP3_60
• RADP_DFE_FXTAP3_61
• RADP_DFE_FXTAP3_62
• RADP_DFE_FXTAP3_63
• RADP_DFE_FXTAP3_64
• RADP_DFE_FXTAP3_65
• RADP_DFE_FXTAP3_66
• RADP_DFE_FXTAP3_67
• RADP_DFE_FXTAP3_68
• RADP_DFE_FXTAP3_69
• RADP_DFE_FXTAP3_7
• RADP_DFE_FXTAP3_70
• RADP_DFE_FXTAP3_71
• RADP_DFE_FXTAP3_72
• RADP_DFE_FXTAP3_73
• RADP_DFE_FXTAP3_74
• RADP_DFE_FXTAP3_75
• RADP_DFE_FXTAP3_76
• RADP_DFE_FXTAP3_77
• RADP_DFE_FXTAP3_78
• RADP_DFE_FXTAP3_79
- RADP_DFE_FXTAP3_8
- RADP_DFE_FXTAP3_80
- RADP_DFE_FXTAP3_81
- RADP_DFE_FXTAP3_82
- RADP_DFE_FXTAP3_83
- RADP_DFE_FXTAP3_84
- RADP_DFE_FXTAP3_85
- RADP_DFE_FXTAP3_86
- RADP_DFE_FXTAP3_87
- RADP_DFE_FXTAP3_88
- RADP_DFE_FXTAP3_89
- RADP_DFE_FXTAP3_9
- RADP_DFE_FXTAP3_90
- RADP_DFE_FXTAP3_91
- RADP_DFE_FXTAP3_92
- RADP_DFE_FXTAP3_93
- RADP_DFE_FXTAP3_94
- RADP_DFE_FXTAP3_95
- RADP_DFE_FXTAP3_96
- RADP_DFE_FXTAP3_97
- RADP_DFE_FXTAP3_98
- RADP_DFE_FXTAP3_99

**Device Support**
- Intel Arria 10

**Notes**

**Syntax**

```bash
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP3 -to <to> -entity <entity name> <value>
```
1.10.219. XCVR_A10_RX_AD_P_DFE_FXTAP3_SGN

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP3_SGN_0
- RADP_DFE_FXTAP3_SGN_1

**Device Support**

- Intel Arria 10

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_RX_AD_P_DFE_FXTAP3_SGN -to <to> -entity <entity name> <value>
```
1.10.220. XCVR_A10_RX_ADП_DFE_FXTAP4

A logic option that allows you to specify the coefficient setting for floating tap four in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP4_0
- RADP_DFE_FXTAP4_1
- RADP_DFE_FXTAP4_10
- RADP_DFE_FXTAP4_11
- RADP_DFE_FXTAP4_12
- RADP_DFE_FXTAP4_13
- RADP_DFE_FXTAP4_14
- RADP_DFE_FXTAP4_15
- RADP_DFE_FXTAP4_16
- RADP_DFE_FXTAP4_17
- RADP_DFE_FXTAP4_18
- RADP_DFE_FXTAP4_19
- RADP_DFE_FXTAP4_2
- RADP_DFE_FXTAP4_20
- RADP_DFE_FXTAP4_21
- RADP_DFE_FXTAP4_22
- RADP_DFE_FXTAP4_23
- RADP_DFE_FXTAP4_24
- RADP_DFE_FXTAP4_25
- RADP_DFE_FXTAP4_26
- RADP_DFE_FXTAP4_27
- RADP_DFE_FXTAP4_28
- RADP_DFE_FXTAP4_29
- RADP_DFE_FXTAP4_3
- RADP_DFE_FXTAP4_30
- RADP_DFE_FXTAP4_31
- RADP_DFE_FXTAP4_32
- RADP_DFE_FXTAP4_33
- RADP_DFE_FXTAP4_34
- RADP_DFE_FXTAP4_35
Device Support

- Intel Arria 10
Note

Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP4 -to <to> -entity <entity name> <value>
```
1.10.221. **XCVR_A10_RX_ADП_DFE_FXTAP4_SGN**

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP4_SGN_0
- RADP_DFE_FXTAP4_SGN_1

**Device Support**

- Intel Arria 10

**Notes**

**Syntax**

```bash
set_instance_assignment -name XCVR_A10_RX_ADП_DFE_FXTAP4_SGN -to <to> -entity <entity name> <value>
```
1.10.222. XCVR_A10_RX_ADP_DFE_FXTAP5

A logic option that allows you to specify the coefficient setting for fix tap five in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP5_0
- RADP_DFE_FXTAP5_1
- RADP_DFE_FXTAP5_10
- RADP_DFE_FXTAP5_11
- RADP_DFE_FXTAP5_12
- RADP_DFE_FXTAP5_13
- RADP_DFE_FXTAP5_14
- RADP_DFE_FXTAP5_15
- RADP_DFE_FXTAP5_16
- RADP_DFE_FXTAP5_17
- RADP_DFE_FXTAP5_18
- RADP_DFE_FXTAP5_19
- RADP_DFE_FXTAP5_2
- RADP_DFE_FXTAP5_20
- RADP_DFE_FXTAP5_21
- RADP_DFE_FXTAP5_22
- RADP_DFE_FXTAP5_23
- RADP_DFE_FXTAP5_24
- RADP_DFE_FXTAP5_25
- RADP_DFE_FXTAP5_26
- RADP_DFE_FXTAP5_27
- RADP_DFE_FXTAP5_28
- RADP_DFE_FXTAP5_29
- RADP_DFE_FXTAP5_3
- RADP_DFE_FXTAP5_30
- RADP_DFE_FXTAP5_31
- RADP_DFE_FXTAP5_32
- RADP_DFE_FXTAP5_33
- RADP_DFE_FXTAP5_34
- RADP_DFE_FXTAP5_35
Device Support

- Intel Arria 10
Syntax

```
set_instance_assignment -name XCVR_A10_RX_ADPA_DFE_FXTAP5 -to <to> -entity <entity name> <value>
```
1.10.223. XCVR_A10_RX_ADП_DFE_FXTAP5_SGN

Type
Enumeration

Values
- RADP_DFE_FXTAP5_SGN_0
- RADP_DFE_FXTAP5_SGN_1

Device Support
- Intel Arria 10

Notes

Syntax

set_instance_assignment -name XCVR_A10_RX_ADП_DFE_FXTAP5_SGN -to <to> -entity <entity name> <value>
1.10.224. `XCVR_A10_RX_ADП_DFE_FXTAP6`

A logic option that allows you to specify the coefficient setting for fix tap six in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- `RADP_DFE_FXTAP6_0`
- `RADP_DFE_FXTAP6_1`
- `RADP_DFE_FXTAP6_10`
- `RADP_DFE_FXTAP6_11`
- `RADP_DFE_FXTAP6_12`
- `RADP_DFE_FXTAP6_13`
- `RADP_DFE_FXTAP6_14`
- `RADP_DFE_FXTAP6_15`
- `RADP_DFE_FXTAP6_16`
- `RADP_DFE_FXTAP6_17`
- `RADP_DFE_FXTAP6_18`
- `RADP_DFE_FXTAP6_19`
- `RADP_DFE_FXTAP6_2`
- `RADP_DFE_FXTAP6_20`
- `RADP_DFE_FXTAP6_21`
- `RADP_DFE_FXTAP6_22`
- `RADP_DFE_FXTAP6_23`
- `RADP_DFE_FXTAP6_24`
- `RADP_DFE_FXTAP6_25`
- `RADP_DFE_FXTAP6_26`
- `RADP_DFE_FXTAP6_27`
- `RADP_DFE_FXTAP6_28`
- `RADP_DFE_FXTAP6_29`
- `RADP_DFE_FXTAP6_3`
- `RADP_DFE_FXTAP6_30`
- `RADP_DFE_FXTAP6_31`
- `RADP_DFE_FXTAP6_4`
- `RADP_DFE_FXTAP6_5`
- `RADP_DFE_FXTAP6_6`
• RADP_DFE_FXTAP6_7
• RADP_DFE_FXTAP6_8
• RADP_DFE_FXTAP6_9

**Device Support**

• Intel Arria 10

**Notes**

**Syntax**

```bash
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP6 -to <to> -entity <entity name> <value>
```
1.10.225. XCVR_A10_RX_ADP_DFE_FXTAP6_SGN

Type

Enumeration

Values

• RADP_DFE_FXTAP6_SGN_0
• RADP_DFE_FXTAP6_SGN_1

Device Support

• Intel Arria 10

Notes

Syntax

set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP6_SGN -to <to> -entity <entity name> <value>
1.10.226. XCVR_A10_RX_ADP_DFE_FXTAP7

A logic option that allows you to specify the coefficient setting for fix tap seven in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP7_0
- RADP_DFE_FXTAP7_1
- RADP_DFE_FXTAP7_10
- RADP_DFE_FXTAP7_11
- RADP_DFE_FXTAP7_12
- RADP_DFE_FXTAP7_13
- RADP_DFE_FXTAP7_14
- RADP_DFE_FXTAP7_15
- RADP_DFE_FXTAP7_16
- RADP_DFE_FXTAP7_17
- RADP_DFE_FXTAP7_18
- RADP_DFE_FXTAP7_19
- RADP_DFE_FXTAP7_2
- RADP_DFE_FXTAP7_20
- RADP_DFE_FXTAP7_21
- RADP_DFE_FXTAP7_22
- RADP_DFE_FXTAP7_23
- RADP_DFE_FXTAP7_24
- RADP_DFE_FXTAP7_25
- RADP_DFE_FXTAP7_26
- RADP_DFE_FXTAP7_27
- RADP_DFE_FXTAP7_28
- RADP_DFE_FXTAP7_29
- RADP_DFE_FXTAP7_3
- RADP_DFE_FXTAP7_30
- RADP_DFE_FXTAP7_31
- RADP_DFE_FXTAP7_4
- RADP_DFE_FXTAP7_5
- RADP_DFE_FXTAP7_6
• RADP_DFE_FXTAP7_7
• RADP_DFE_FXTAP7_8
• RADP_DFE_FXTAP7_9

**Device Support**

• Intel Arria 10

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP7 -to <to> -entity <entity name> <value>
```
1.10.227. XCVR_A10_RX_ADP_DFE_FXTAP7_SGN

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP7_SGN_0
- RADP_DFE_FXTAP7_SGN_1

**Device Support**

- Intel Arria 10

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP7_SGN -to <to> -entity <entity name> <value>
```
1.10.228. XCVR_A10_RX_ADPI_DP_FXTAP8

A logic option that allows you to specify the coefficient setting for fix tap eight in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP8_0
- RADP_DFE_FXTAP8_1
- RADP_DFE_FXTAP8_10
- RADP_DFE_FXTAP8_11
- RADP_DFE_FXTAP8_12
- RADP_DFE_FXTAP8_13
- RADP_DFE_FXTAP8_14
- RADP_DFE_FXTAP8_15
- RADP_DFE_FXTAP8_16
- RADP_DFE_FXTAP8_17
- RADP_DFE_FXTAP8_18
- RADP_DFE_FXTAP8_19
- RADP_DFE_FXTAP8_2
- RADP_DFE_FXTAP8_20
- RADP_DFE_FXTAP8_21
- RADP_DFE_FXTAP8_22
- RADP_DFE_FXTAP8_23
- RADP_DFE_FXTAP8_24
- RADP_DFE_FXTAP8_25
- RADP_DFE_FXTAP8_26
- RADP_DFE_FXTAP8_27
- RADP_DFE_FXTAP8_28
- RADP_DFE_FXTAP8_29
- RADP_DFE_FXTAP8_3
- RADP_DFE_FXTAP8_30
- RADP_DFE_FXTAP8_31
- RADP_DFE_FXTAP8_32
- RADP_DFE_FXTAP8_33
- RADP_DFE_FXTAP8_34
- RADP_DFE_FXTAP8_35
Device Support

- Intel Arria 10
Syntax

```shell
set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP8 -to <to> -entity <entity name> <value>
```
1.10.229. XCVR_A10_RX_ADП_DFE_FXTAP8_SGN

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP8_SGN_0
- RADP_DFE_FXTAP8_SGN_1

**Device Support**

- Intel Arria 10

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_RX_ADП_DFE_FXTAP8_SGN -to <to> -entity <entity name> <value>
```
1.10.230. XCVR_A10_RX_ADP_DFE_FXTAP9

A logic option that allows you to specify the coefficient setting for fix tap nine in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP9_0
- RADP_DFE_FXTAP9_1
- RADP_DFE_FXTAP9_10
- RADP_DFE_FXTAP9_11
- RADP_DFE_FXTAP9_12
- RADP_DFE_FXTAP9_13
- RADP_DFE_FXTAP9_14
- RADP_DFE_FXTAP9_15
- RADP_DFE_FXTAP9_16
- RADP_DFE_FXTAP9_17
- RADP_DFE_FXTAP9_18
- RADP_DFE_FXTAP9_19
- RADP_DFE_FXTAP9_2
- RADP_DFE_FXTAP9_20
- RADP_DFE_FXTAP9_21
- RADP_DFE_FXTAP9_22
- RADP_DFE_FXTAP9_23
- RADP_DFE_FXTAP9_24
- RADP_DFE_FXTAP9_25
- RADP_DFE_FXTAP9_26
- RADP_DFE_FXTAP9_27
- RADP_DFE_FXTAP9_28
- RADP_DFE_FXTAP9_29
- RADP_DFE_FXTAP9_3
- RADP_DFE_FXTAP9_30
- RADP_DFE_FXTAP9_31
- RADP_DFE_FXTAP9_32
- RADP_DFE_FXTAP9_33
- RADP_DFE_FXTAP9_34
- RADP_DFE_FXTAP9_35
Device Support

- Intel Arria 10
Notes

Syntax

set_instance_assignment -name XCVR_A10_RX_ADP_DFE_FXTAP9 -to <to> -entity <entity name> <value>
1.10.231. **XCVR_A10_RX_ADJ_DFE_FXTAP9_SGN**

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP9_SGN_0
- RADP_DFE_FXTAP9_SGN_1

**Device Support**

- Intel Arria 10

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_RX_ADJ_DFE_FXTAP9_SGN -to <to> -entity <entity name> <value>
```
1.10.232. **XCVR_A10_RX_ADPAVGALSEL**

A logic option that allows you to control the amount of output voltage swing on the variable gain amplifier. The amount of voltage swing is proportional to the setting where '0' gives the lowest swing and '7' gives the largest swing. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_VGA_SEL_0
- RADP_VGA_SEL_1
- RADP_VGA_SEL_2
- RADP_VGA_SEL_3
- RADP_VGA_SEL_4
- RADP_VGA_SEL_5
- RADP_VGA_SEL_6
- RADP_VGA_SEL_7

**Device Support**

- Intel Arria 10

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_RX_ADPAVGALSEL -to <to> -entity <entity name> <value>
```
1.10.233. XCVR_A10_RX_EQ_BW_SEL

Type

Enumeration

Values

- EQ_BW_1
- EQ_BW_2
- EQ_BW_3
- EQ_BW_4

Device Support

- Intel Arria 10

Notes

Syntax

```bash
set_instance_assignment -name XCVR_A10_RX_EQ_BW_SEL -to <to> -entity <entity name> <value>
```
1.10.234. XCVR_A10_RX_EQ_DC_GAIN_TRIM

A logic option that allows you to control the amount of DC gain on equalizer in high gain mode. The amount of DC gain is proportional to the setting where '0' gives the lowest DC gain and '28' gives the largest DC gain.

Type

Enumeration

Values

- NO_DC_GAIN
- STG1_GAIN7
- STG2_GAIN7
- STG3_GAIN7
- STG4_GAIN7

Device Support

- Intel Arria 10

Notes

Syntax

```
set_instance_assignment -name XCVR_A10_RX_EQ_DC_GAIN_TRIM -to <to> -entity <entity name> <value>
```
1.10.235. XCVR_A10_RX_LINK

A logic option that allows you to specify the type of communication for the receiver link. Quartus Prime will use this option to determine the legal data rate and power mode for the link.

**Type**

Enumeration

**Values**

- LR
- SR

**Device Support**

- Intel Arria 10

**Notes**

**Syntax**

```bash
set_instance_assignment -name XCVR_A10_RX_LINK -to <to> -entity <entity name> <value>
```
1.10.236. XCVR_A10_RX_ONE_STAGE_ENABLE

Type
Enumeration

Values
• NON_S1_MODE
• S1_MODE

Device Support
• Intel Arria 10

Notes

Syntax

set_instance_assignment -name XCVR_A10_RX_ONE_STAGE_ENABLE -to <to> -entity <entity name> <value>
### 1.10.237. XCVR_A10_RX_TERM_SEL

A logic option that allows you to specify the termination value of a transceiver Rx pin.

**Type**

Enumeration

**Values**

- R_EXT0
- R_R1
- R_R2

**Device Support**

- Intel Arria 10

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_RX_TERM_SEL -to <to> -entity <entity_name> <value>
```
1.10.238. **XCVR_A10_TX_COMPENSATION_EN**

A logic option that allows you to turn on the compensation for transmitter data rate above 9 Gbps. Turning on this option draws more power on the transmitter buffer.

**Type**

Enumeration

**Values**

- DISABLE
- ENABLE

**Device Support**

- Intel Arria 10

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_TX_COMPENSATION_EN -to <to> -entity <entity name> <value>
```
1.10.239. XCVR_A10_TX_LINK

A logic option that allows you to specify the type of communication for the transmitter link. Quartus Prime will use this option to determine the legal data rate and power mode for the link.

**Type**

Enumeration

**Values**

- LR
- SR

**Device Support**

- Intel Arria 10

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_TX_LINK -to <to> -entity <entity name> <value>
```
1.10.240. XCVR_A10_TX_PRE_EMP_SIGN_1ST_POST_TAP

A logic option that allows you to specify the output polarity of the transmitter pre-emphasis first post-tap.

Type
Enumeration

Values
- FIR_POST_1T_NEG
- FIR_POST_1T_POS

Device Support
- Intel Arria 10

Notes

Syntax

set_instance_assignment -name XCVR_A10_TX_PRE_EMP_SIGN_1ST_POST_TAP -to <to> -entity <entity name> <value>
1.10.241. XCVR_A10_TX_PRE_EMP_SIGN_2ND_POST_TAP

A logic option that allows you to specify the output polarity of the transmitter pre-emphasis second post-tap.

**Type**

Enumeration

**Values**

- FIR_POST_2T_NEG
- FIR_POST_2T_POS

**Device Support**

- Intel Arria 10

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_TX_PRE_EMP_SIGN_2ND_POST_TAP -to <to> -entity <entity name> <value>
```
1.10.242. XCVR_A10_TX_PRE_EMP_SIGN_PRE_TAP_1T

A logic option that allows you to specify the output polarity of the transmitter pre-emphasis first pre-tap.

**Type**

Enumeration

**Values**

- FIR_PRE_1T_NEG
- FIR_PRE_1T_POS

**Device Support**

- Intel Arria 10

**Notes**

**Syntax**

```sh
set_instance_assignment -name XCVR_A10_TX_PRE_EMP_SIGN_PRE_TAP_1T -to <to> -entity <entity name> <value>
```
1.10.243. XCVR_A10_TX_PRE_EMP_SIGN_PRE_TAP_2T

A logic option that allows you to specify the output polarity of the transmitter pre-emphasis second pre-tap.

**Type**

Enumeration

**Values**

- FIR_PRE_2T_NEG
- FIR_PRE_2T_POS

**Device Support**

- Intel Arria 10

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_TX_PRE_EMP_SIGN_PRE_TAP_2T -to <to> -entity <entity name> <value>
```
1.10.244. XCVR_A10_TX_PRE_EMP_SWITCHING_CTRL_1ST_POST_TAP

A logic option that allows you to control the magnitude of transmitter pre-emphasis first post-tap. Legal values are: 0 to 25.

**Type**

Integer

**Device Support**

- Intel Arria 10

**INTEGER RANGE**

0, 25

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_TX_PRE_EMP_SWITCHING_CTRL_1ST_POST_TAP -
to <to> -entity <entity name> <value>
```
1.10.245. XCVR_A10_TX_PRE_EMP_SWITCHING_CTRL_2ND_POST_TAP

A logic option that allows you to control the magnitude of transmitter pre-emphasis second post-tap. Legal values are: 0 to 12.

**Type**

Integer

**Device Support**

- Intel Arria 10

**INTEGER_RANGE**

0, 12

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_TX_PRE_EMP_SWITCHING_CTRL_2ND_POST_TAP -to <to> -entity <entity name> <value>
```
1.10.246. XCVR_A10_TX_PRE_EMP_SWITCHING_CTRL_PRE_TAP_1T

A logic option that allows you to control the magnitude of transmitter pre-emphasis first pre-tap. Legal values are: 0 to 16.

**Type**

Integer

**Device Support**

- Intel Arria 10

**INTEGER_RANGE**

0, 16

**Notes**

**Syntax**

```sh
set_instance_assignment -name XCVR_A10_TX_PRE_EMP_SWITCHING_CTRL_PRE_TAP_1T -to <to> -entity <entity name> <value>
```
1.10.247. XCVR_A10_TX_PRE_EMP_SWITCHING_CTRL_PRE_TAP_2T

A logic option that allows you to control the magnitude of transmitter pre-emphasis second pre-tap. Legal values are: 0 to 7.

**Type**

Integer

**Device Support**

- Intel Arria 10

**INTEGER_RANGE**

0, 7

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_TX_PRE_EMP_SWITCHING_CTRL_PRE_TAP_2T -to <to> -entity <entity name> <value>
```
1.10.248. XCVR_A10_TX_SLEW_RATE_CTRL

**Type**

Enumeration

**Values**

- SLEW_R0
- SLEW_R1
- SLEW_R2
- SLEW_R3
- SLEW_R4
- SLEW_R5
- SLEW_R6
- SLEW_R7

**Device Support**

- Intel Arria 10

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_TX_SLEW_RATE_CTRL -to <to> -entity <entity name> <value>
```
1.10.249. **XCVR_A10_TX_TERM_SEL**

A logic option that allows you to specify the termination value of a transceiver Tx pin.

**Type**

Enumeration

**Values**

- R_R1
- R_R2

**Device Support**

- Intel Arria 10

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_A10_TX_TERM_SEL -to <to> -entity <entity name> <value>
```
1.10.250. XCVR_A10_TX_VOD_OUTPUT_SWING_CTRL

A logic option that allows you to control the transmitter output swing level. Legal values are: 0 to 31.

**Type**

Integer

**Device Support**

- Intel Arria 10

**INTEGER_RANGE**

0, 31

**Notes**

**Syntax**

```plaintext
set_instance_assignment -name XCVR_A10_TX_VOD_OUTPUT_SWING_CTRL -to <to> -entity <entity name> <value>
```
1.10.251. XCVR_A10_TX_XTX_PATH_ANALOG_MODE

**Type**

**Enumeration**

**Values**

- CEI_11100_LR
- CEI_11100_SR
- CEI_4976_LR
- CEI_4976_SR
- CEI_6375_LR
- CEI_6375_SR
- CEI_9950_LR
- CEI_9950_SR
- CPRI_12500
- CPRI_E12LVII
- CPRI_E12LVIII
- CPRI_E24LVII
- CPRI_E24LVIII
- CPRI_E30LVII
- CPRI_E30LVIII
- CPRI_E48LVII
- CPRI_E48LVIII
- CPRI_E60LVII
- CPRI_E60LVIII
- CPRI_E6LVII
- CPRI_E6LVIII
- CPRI_E96LVIII
- CPRI_E99LVIII
- HIGIG_4062
- HIGIG_5000
- HIGIG_6250
- HIGIG_6562
- IEEE_10G_BASE_CR_10312
- IEEE_10G_KR_10312
- IEEE_40G_BASE_KR_10312
- INTERLAKEN_11100
- INTERLAKEN_12500
• INTERLAKEN_6375
• JESD204_A_B_12500
• JESD204_A_B_6375
• QSGMII_5000
• SERIAL_LITE_III_16400
• SERIAL_LITE_III_17400
• SFI_S_6250
• SRIO_5000_LR
• SRIO_5000_MR
• SRIO_5000_SR
• SRIO_6250_LR
• SRIO_6250_MR
• SRIO_6250_SR
• USER_CUSTOM

Device Support
• Intel Arria 10

Notes

Syntax

set_instance_assignment -name XCVR_A10_TX_XTX_PATH_ANALOG_MODE -to <to> -entity <entity name> <value>
1.10.252. XCVR_C10_REFCLK_TERM_TRISTATE

A logic option that directs the Compiler to enable the internal termination of the dedicated reference clock pin.

**Type**

Enumeration

**Values**

- TRISTATE_OFF
- TRISTATE_ON

**Device Support**

- Intel Cyclone 10 GX

**Notes**

**Syntax**

```bash
set_instance_assignment -name XCVR_C10_REFCLK_TERM_TRISTATE -to <to> -entity <entity name> <value>
```
1.10.253. **XCVR_C10_RX_ADJP_CTLE_ACGAIN_4S**

A logic option that allows you to control the amount of AC gain on the equalizer in high gain mode. The amount of AC gain is proportional to the setting where '0' gives the lowest AC gain and '31' gives the largest AC gain. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_CLTE_ACGAIN_4S_0
- RADP_CLTE_ACGAIN_4S_1
- RADP_CLTE_ACGAIN_4S_10
- RADP_CLTE_ACGAIN_4S_11
- RADP_CLTE_ACGAIN_4S_12
- RADP_CLTE_ACGAIN_4S_13
- RADP_CLTE_ACGAIN_4S_14
- RADP_CLTE_ACGAIN_4S_15
- RADP_CLTE_ACGAIN_4S_16
- RADP_CLTE_ACGAIN_4S_17
- RADP_CLTE_ACGAIN_4S_18
- RADP_CLTE_ACGAIN_4S_19
- RADP_CLTE_ACGAIN_4S_2
- RADP_CLTE_ACGAIN_4S_20
- RADP_CLTE_ACGAIN_4S_21
- RADP_CLTE_ACGAIN_4S_22
- RADP_CLTE_ACGAIN_4S_23
- RADP_CLTE_ACGAIN_4S_24
- RADP_CLTE_ACGAIN_4S_25
- RADP_CLTE_ACGAIN_4S_26
- RADP_CLTE_ACGAIN_4S_27
- RADP_CLTE_ACGAIN_4S_28
- RADP_CLTE_ACGAIN_4S_3
- RADP_CLTE_ACGAIN_4S_4
- RADP_CLTE_ACGAIN_4S_5
- RADP_CLTE_ACGAIN_4S_6
- RADP_CLTE_ACGAIN_4S_7
- RADP_CLTE_ACGAIN_4S_8
- RADP_CLTE_ACGAIN_4S_9
Device Support

- Intel Cyclone 10 GX

Notes

Syntax

```
set_instance_assignment -name XCVR_C10_RX_ADPT_CTE_ACGAIN_4S -to <to> -entity <entity name> <value>
```
1.10.254. **XCVR_C10_RX_AD_DP_CTLE_EQZ_1S_SEL**

A logic option that allows you to control the amount of AC gain on the one-stage equalizer. The amount of AC gain is proportional to the setting where '0' gives the lowest AC gain and '15' gives the largest AC gain. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_CTLE_EQZ_1S_SEL_0
- RADP_CTLE_EQZ_1S_SEL_1
- RADP_CTLE_EQZ_1S_SEL_10
- RADP_CTLE_EQZ_1S_SEL_11
- RADP_CTLE_EQZ_1S_SEL_12
- RADP_CTLE_EQZ_1S_SEL_13
- RADP_CTLE_EQZ_1S_SEL_14
- RADP_CTLE_EQZ_1S_SEL_15
- RADP_CTLE_EQZ_1S_SEL_2
- RADP_CTLE_EQZ_1S_SEL_3
- RADP_CTLE_EQZ_1S_SEL_4
- RADP_CTLE_EQZ_1S_SEL_5
- RADP_CTLE_EQZ_1S_SEL_6
- RADP_CTLE_EQZ_1S_SEL_7
- RADP_CTLE_EQZ_1S_SEL_8
- RADP_CTLE_EQZ_1S_SEL_9

**Device Support**

- Intel Cyclone 10 GX

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_RX_AD_DP_CTLE_EQZ_1S_SEL -to <to> -entity <entity name> <value>
```
1.10.255. XCVR_C10_RX_ADPD_FDE_FXTAP1

A logic option that allows you to specify the coefficient setting for fix tap one in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP1_0
- RADP_DFE_FXTAP1_1
- RADP_DFE_FXTAP1_10
- RADP_DFE_FXTAP1_100
- RADP_DFE_FXTAP1_101
- RADP_DFE_FXTAP1_102
- RADP_DFE_FXTAP1_103
- RADP_DFE_FXTAP1_104
- RADP_DFE_FXTAP1_105
- RADP_DFE_FXTAP1_106
- RADP_DFE_FXTAP1_107
- RADP_DFE_FXTAP1_108
- RADP_DFE_FXTAP1_109
- RADP_DFE_FXTAP1_11
- RADP_DFE_FXTAP1_110
- RADP_DFE_FXTAP1_111
- RADP_DFE_FXTAP1_112
- RADP_DFE_FXTAP1_113
- RADP_DFE_FXTAP1_114
- RADP_DFE_FXTAP1_115
- RADP_DFE_FXTAP1_116
- RADP_DFE_FXTAP1_117
- RADP_DFE_FXTAP1_118
- RADP_DFE_FXTAP1_119
- RADP_DFE_FXTAP1_12
- RADP_DFE_FXTAP1_120
- RADP_DFE_FXTAP1_121
- RADP_DFE_FXTAP1_122
- RADP_DFE_FXTAP1_123
- RADP_DFE_FXTAP1_124
- RADP_DFE_FXTAP1_125
- RADP_DFE_FXTAP1_126
- RADP_DFE_FXTAP1_127
- RADP_DFE_FXTAP1_13
- RADP_DFE_FXTAP1_14
- RADP_DFE_FXTAP1_15
- RADP_DFE_FXTAP1_16
- RADP_DFE_FXTAP1_17
- RADP_DFE_FXTAP1_18
- RADP_DFE_FXTAP1_19
- RADP_DFE_FXTAP1_2
- RADP_DFE_FXTAP1_20
- RADP_DFE_FXTAP1_21
- RADP_DFE_FXTAP1_22
- RADP_DFE_FXTAP1_23
- RADP_DFE_FXTAP1_24
- RADP_DFE_FXTAP1_25
- RADP_DFE_FXTAP1_26
- RADP_DFE_FXTAP1_27
- RADP_DFE_FXTAP1_28
- RADP_DFE_FXTAP1_29
- RADP_DFE_FXTAP1_3
- RADP_DFE_FXTAP1_30
- RADP_DFE_FXTAP1_31
- RADP_DFE_FXTAP1_32
- RADP_DFE_FXTAP1_33
- RADP_DFE_FXTAP1_34
- RADP_DFE_FXTAP1_35
- RADP_DFE_FXTAP1_36
- RADP_DFE_FXTAP1_37
- RADP_DFE_FXTAP1_38
- RADP_DFE_FXTAP1_39
- RADP_DFE_FXTAP1_4
- RADP_DFE_FXTAP1_40
- RADP_DFE_FXTAP1_41
- RADP_DFE_FXTAP1_42
- RADP_DFE_FXTAP1_43
- RADP_DFE_FXTAP1_44
• RADP_DFE_FXTAP1_45
• RADP_DFE_FXTAP1_46
• RADP_DFE_FXTAP1_47
• RADP_DFE_FXTAP1_48
• RADP_DFE_FXTAP1_49
• RADP_DFE_FXTAP1_5
• RADP_DFE_FXTAP1_50
• RADP_DFE_FXTAP1_51
• RADP_DFE_FXTAP1_52
• RADP_DFE_FXTAP1_53
• RADP_DFE_FXTAP1_54
• RADP_DFE_FXTAP1_55
• RADP_DFE_FXTAP1_56
• RADP_DFE_FXTAP1_57
• RADP_DFE_FXTAP1_58
• RADP_DFE_FXTAP1_59
• RADP_DFE_FXTAP1_6
• RADP_DFE_FXTAP1_60
• RADP_DFE_FXTAP1_61
• RADP_DFE_FXTAP1_62
• RADP_DFE_FXTAP1_63
• RADP_DFE_FXTAP1_64
• RADP_DFE_FXTAP1_65
• RADP_DFE_FXTAP1_66
• RADP_DFE_FXTAP1_67
• RADP_DFE_FXTAP1_68
• RADP_DFE_FXTAP1_69
• RADP_DFE_FXTAP1_7
• RADP_DFE_FXTAP1_70
• RADP_DFE_FXTAP1_71
• RADP_DFE_FXTAP1_72
• RADP_DFE_FXTAP1_73
• RADP_DFE_FXTAP1_74
• RADP_DFE_FXTAP1_75
• RADP_DFE_FXTAP1_76
• RADP_DFE_FXTAP1_77
• RADP_DFE_FXTAP1_78
• RADP_DFE_FXTAP1_79
Device Support

- Intel Cyclone 10 GX

Notes

Syntax

```
set_instance_assignment -name XCVR_C10_RX_ADP_DFE_FXTAP1 -to <to> -entity <entity name> <value>
```
1.10.256. **XCVR_C10_RX_AD_P_DFE_FXTAP10**

A logic option that allows you to specify the coefficient setting for fix tap ten in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP10_0
- RADP_DFE_FXTAP10_1
- RADP_DFE_FXTAP10_10
- RADP_DFE_FXTAP10_11
- RADP_DFE_FXTAP10_12
- RADP_DFE_FXTAP10_13
- RADP_DFE_FXTAP10_14
- RADP_DFE_FXTAP10_15
- RADP_DFE_FXTAP10_16
- RADP_DFE_FXTAP10_17
- RADP_DFE_FXTAP10_18
- RADP_DFE_FXTAP10_19
- RADP_DFE_FXTAP10_2
- RADP_DFE_FXTAP10_20
- RADP_DFE_FXTAP10_21
- RADP_DFE_FXTAP10_22
- RADP_DFE_FXTAP10_23
- RADP_DFE_FXTAP10_24
- RADP_DFE_FXTAP10_25
- RADP_DFE_FXTAP10_26
- RADP_DFE_FXTAP10_27
- RADP_DFE_FXTAP10_28
- RADP_DFE_FXTAP10_29
- RADP_DFE_FXTAP10_3
- RADP_DFE_FXTAP10_30
- RADP_DFE_FXTAP10_31
- RADP_DFE_FXTAP10_32
- RADP_DFE_FXTAP10_33
- RADP_DFE_FXTAP10_34
- RADP_DFE_FXTAP10_35
Device Support

- Intel Cyclone 10 GX
Notes

Syntax

```
set_instance_assignment -name XCVR_C10_RX_ADPI_DFE_FXTAP10 -to <to> -entity <entity name> <value>
```
### 1.10.257. XCVR_C10_RX_ADG_DFE_FXTAP10_SGN

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP10_SGN_0
- RADP_DFE_FXTAP10_SGN_1

**Device Support**

- Intel Cyclone 10 GX

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_RX_ADG_DFE_FXTAP10_SGN -to <to> -entity <entity name> <value>
```
1.10.258. XCVR_C10_RX_ADJ_DFE_FXTAP11

A logic option that allows you to specify the coefficient setting for fix tap eleven in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP11_0
- RADP_DFE_FXTAP11_1
- RADP_DFE_FXTAP11_10
- RADP_DFE_FXTAP11_11
- RADP_DFE_FXTAP11_12
- RADP_DFE_FXTAP11_13
- RADP_DFE_FXTAP11_14
- RADP_DFE_FXTAP11_15
- RADP_DFE_FXTAP11_16
- RADP_DFE_FXTAP11_17
- RADP_DFE_FXTAP11_18
- RADP_DFE_FXTAP11_19
- RADP_DFE_FXTAP11_2
- RADP_DFE_FXTAP11_10
- RADP_DFE_FXTAP11_21
- RADP_DFE_FXTAP11_22
- RADP_DFE_FXTAP11_23
- RADP_DFE_FXTAP11_24
- RADP_DFE_FXTAP11_25
- RADP_DFE_FXTAP11_26
- RADP_DFE_FXTAP11_27
- RADP_DFE_FXTAP11_28
- RADP_DFE_FXTAP11_29
- RADP_DFE_FXTAP11_3
- RADP_DFE_FXTAP11_30
- RADP_DFE_FXTAP11_31
- RADP_DFE_FXTAP11_32
- RADP_DFE_FXTAP11_33
- RADP_DFE_FXTAP11_34
- RADP_DFE_FXTAP11_35
Device Support

- Intel Cyclone 10 GX
Notes

Syntax

```
set_instance_assignment -name XCVR_C10_RX_ADP_DFE_FXTAP11 -to <to> -entity <entity name> <value>
```
1.10.259. XCVR_C10_RX_AD_P_DFE_FXTAP11_SGN

Type

Enumeration

Values

• RADP_DFE_FXTAP11_SGN_0
• RADP_DFE_FXTAP11_SGN_1

Device Support

• Intel Cyclone 10 GX

Notes

Syntax

```
set_instance_assignment -name XCVR_C10_RX_AD_P_DFE_FXTAP11_SGN -to <to> -entity <entity name> <value>
```
1.10.260. XCVR_C10_RX_ADPLAYER_C10_RX_ADPLAYER_C10

A logic option that allows you to specify the coefficient setting for fix tap two in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP2_0
- RADP_DFE_FXTAP2_1
- RADP_DFE_FXTAP2_10
- RADP_DFE_FXTAP2_100
- RADP_DFE_FXTAP2_101
- RADP_DFE_FXTAP2_102
- RADP_DFE_FXTAP2_103
- RADP_DFE_FXTAP2_104
- RADP_DFE_FXTAP2_105
- RADP_DFE_FXTAP2_106
- RADP_DFE_FXTAP2_107
- RADP_DFE_FXTAP2_108
- RADP_DFE_FXTAP2_109
- RADP_DFE_FXTAP2_11
- RADP_DFE_FXTAP2_110
- RADP_DFE_FXTAP2_111
- RADP_DFE_FXTAP2_112
- RADP_DFE_FXTAP2_113
- RADP_DFE_FXTAP2_114
- RADP_DFE_FXTAP2_115
- RADP_DFE_FXTAP2_116
- RADP_DFE_FXTAP2_117
- RADP_DFE_FXTAP2_118
- RADP_DFE_FXTAP2_119
- RADP_DFE_FXTAP2_12
- RADP_DFE_FXTAP2_120
- RADP_DFE_FXTAP2_121
- RADP_DFE_FXTAP2_122
- RADP_DFE_FXTAP2_123
- RADP_DFE_FXTAP2_124
• RADP_DFE_FXTAP2_125
• RADP_DFE_FXTAP2_126
• RADP_DFE_FXTAP2_127
• RADP_DFE_FXTAP2_13
• RADP_DFE_FXTAP2_14
• RADP_DFE_FXTAP2_15
• RADP_DFE_FXTAP2_16
• RADP_DFE_FXTAP2_17
• RADP_DFE_FXTAP2_18
• RADP_DFE_FXTAP2_19
• RADP_DFE_FXTAP2_2
• RADP_DFE_FXTAP2_20
• RADP_DFE_FXTAP2_21
• RADP_DFE_FXTAP2_22
• RADP_DFE_FXTAP2_23
• RADP_DFE_FXTAP2_24
• RADP_DFE_FXTAP2_25
• RADP_DFE_FXTAP2_26
• RADP_DFE_FXTAP2_27
• RADP_DFE_FXTAP2_28
• RADP_DFE_FXTAP2_29
• RADP_DFE_FXTAP2_3
• RADP_DFE_FXTAP2_30
• RADP_DFE_FXTAP2_31
• RADP_DFE_FXTAP2_32
• RADP_DFE_FXTAP2_33
• RADP_DFE_FXTAP2_34
• RADP_DFE_FXTAP2_35
• RADP_DFE_FXTAP2_36
• RADP_DFE_FXTAP2_37
• RADP_DFE_FXTAP2_38
• RADP_DFE_FXTAP2_39
• RADP_DFE_FXTAP2_4
• RADP_DFE_FXTAP2_40
• RADP_DFE_FXTAP2_41
• RADP_DFE_FXTAP2_42
• RADP_DFE_FXTAP2_43
• RADP_DFE_FXTAP2_44
Device Support

- Intel Cyclone 10 GX

Notes

Syntax

```
set_instance_assignment -name XCVR_C10_RX_ADP_DFE_FXTAP2 -to <to> -entity <entity name> <value>
```
1.10.261. XCVR_C10_RX_ADIP_DFE_FXTAP2_SGN

**Type**
Enumeration

**Values**
- RADP_DFE_FXTAP2_SGN_0
- RADP_DFE_FXTAP2_SGN_1

**Device Support**
- Intel Cyclone 10 GX

**Notes**

**Syntax**

```plaintext
set_instance_assignment -name XCVR_C10_RX_ADIP_DFE_FXTAP2_SGN -to <to> -entity <entity name> <value>
```
1.10.262. XCVR_C10_RX_ADAP_DFE_FXTAP3

A logic option that allows you to specify the coefficient setting for fix tap three in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP3_0
- RADP_DFE_FXTAP3_1
- RADP_DFE_FXTAP3_10
- RADP_DFE_FXTAP3_100
- RADP_DFE_FXTAP3_101
- RADP_DFE_FXTAP3_102
- RADP_DFE_FXTAP3_103
- RADP_DFE_FXTAP3_104
- RADP_DFE_FXTAP3_105
- RADP_DFE_FXTAP3_106
- RADP_DFE_FXTAP3_107
- RADP_DFE_FXTAP3_108
- RADP_DFE_FXTAP3_109
- RADP_DFE_FXTAP3_11
- RADP_DFE_FXTAP3_110
- RADP_DFE_FXTAP3_111
- RADP_DFE_FXTAP3_112
- RADP_DFE_FXTAP3_113
- RADP_DFE_FXTAP3_114
- RADP_DFE_FXTAP3_115
- RADP_DFE_FXTAP3_116
- RADP_DFE_FXTAP3_117
- RADP_DFE_FXTAP3_118
- RADP_DFE_FXTAP3_119
- RADP_DFE_FXTAP3_12
- RADP_DFE_FXTAP3_120
- RADP_DFE_FXTAP3_121
- RADP_DFE_FXTAP3_122
- RADP_DFE_FXTAP3_123
- RADP_DFE_FXTAP3_124
• RADP_DFE_FXTAP3_125
• RADP_DFE_FXTAP3_126
• RADP_DFE_FXTAP3_127
• RADP_DFE_FXTAP3_13
• RADP_DFE_FXTAP3_14
• RADP_DFE_FXTAP3_15
• RADP_DFE_FXTAP3_16
• RADP_DFE_FXTAP3_17
• RADP_DFE_FXTAP3_18
• RADP_DFE_FXTAP3_19
• RADP_DFE_FXTAP3_2
• RADP_DFE_FXTAP3_20
• RADP_DFE_FXTAP3_21
• RADP_DFE_FXTAP3_22
• RADP_DFE_FXTAP3_23
• RADP_DFE_FXTAP3_24
• RADP_DFE_FXTAP3_25
• RADP_DFE_FXTAP3_26
• RADP_DFE_FXTAP3_27
• RADP_DFE_FXTAP3_28
• RADP_DFE_FXTAP3_29
• RADP_DFE_FXTAP3_3
• RADP_DFE_FXTAP3_30
• RADP_DFE_FXTAP3_31
• RADP_DFE_FXTAP3_32
• RADP_DFE_FXTAP3_33
• RADP_DFE_FXTAP3_34
• RADP_DFE_FXTAP3_35
• RADP_DFE_FXTAP3_36
• RADP_DFE_FXTAP3_37
• RADP_DFE_FXTAP3_38
• RADP_DFE_FXTAP3_39
• RADP_DFE_FXTAP3_4
• RADP_DFE_FXTAP3_40
• RADP_DFE_FXTAP3_41
• RADP_DFE_FXTAP3_42
• RADP_DFE_FXTAP3_43
• RADP_DFE_FXTAP3_44
• RADP_DFE_FXTAP3_45
• RADP_DFE_FXTAP3_46
• RADP_DFE_FXTAP3_47
• RADP_DFE_FXTAP3_48
• RADP_DFE_FXTAP3_49
• RADP_DFE_FXTAP3_5
• RADP_DFE_FXTAP3_50
• RADP_DFE_FXTAP3_51
• RADP_DFE_FXTAP3_52
• RADP_DFE_FXTAP3_53
• RADP_DFE_FXTAP3_54
• RADP_DFE_FXTAP3_55
• RADP_DFE_FXTAP3_56
• RADP_DFE_FXTAP3_57
• RADP_DFE_FXTAP3_58
• RADP_DFE_FXTAP3_59
• RADP_DFE_FXTAP3_6
• RADP_DFE_FXTAP3_60
• RADP_DFE_FXTAP3_61
• RADP_DFE_FXTAP3_62
• RADP_DFE_FXTAP3_63
• RADP_DFE_FXTAP3_64
• RADP_DFE_FXTAP3_65
• RADP_DFE_FXTAP3_66
• RADP_DFE_FXTAP3_67
• RADP_DFE_FXTAP3_68
• RADP_DFE_FXTAP3_69
• RADP_DFE_FXTAP3_7
• RADP_DFE_FXTAP3_70
• RADP_DFE_FXTAP3_71
• RADP_DFE_FXTAP3_72
• RADP_DFE_FXTAP3_73
• RADP_DFE_FXTAP3_74
• RADP_DFE_FXTAP3_75
• RADP_DFE_FXTAP3_76
• RADP_DFE_FXTAP3_77
• RADP_DFE_FXTAP3_78
• RADP_DFE_FXTAP3_79
- RADP_DFE_FXTAP3_8
- RADP_DFE_FXTAP3_80
- RADP_DFE_FXTAP3_81
- RADP_DFE_FXTAP3_82
- RADP_DFE_FXTAP3_83
- RADP_DFE_FXTAP3_84
- RADP_DFE_FXTAP3_85
- RADP_DFE_FXTAP3_86
- RADP_DFE_FXTAP3_87
- RADP_DFE_FXTAP3_88
- RADP_DFE_FXTAP3_89
- RADP_DFE_FXTAP3_9
- RADP_DFE_FXTAP3_90
- RADP_DFE_FXTAP3_91
- RADP_DFE_FXTAP3_92
- RADP_DFE_FXTAP3_93
- RADP_DFE_FXTAP3_94
- RADP_DFE_FXTAP3_95
- RADP_DFE_FXTAP3_96
- RADP_DFE_FXTAP3_97
- RADP_DFE_FXTAP3_98
- RADP_DFE_FXTAP3_99

**Device Support**
- Intel Cyclone 10 GX

**Notes**

**Syntax**

```plaintext
set_instance_assignment -name XCVR_C10_RX_ADPIF_FXTAP3 -to <to> -entity <entity name> <value>
```
1.10.263. XCVR_C10_RX_AD cancelling DFE FXTAP3_SGN

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP3_SGN_0
- RADP_DFE_FXTAP3_SGN_1

**Device Support**

- Intel Cyclone 10 GX

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_RX_AD cancelling DFE_FXTAP3_SGN -to <to> -entity <entity name> <value>
```
1.10.264. XCVR_C10_RX_ADp_DFE_FXTAP4

A logic option that allows you to specify the coefficient setting for floating tap four in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP4_0
- RADP_DFE_FXTAP4_1
- RADP_DFE_FXTAP4_10
- RADP_DFE_FXTAP4_11
- RADP_DFE_FXTAP4_12
- RADP_DFE_FXTAP4_13
- RADP_DFE_FXTAP4_14
- RADP_DFE_FXTAP4_15
- RADP_DFE_FXTAP4_16
- RADP_DFE_FXTAP4_17
- RADP_DFE_FXTAP4_18
- RADP_DFE_FXTAP4_19
- RADP_DFE_FXTAP4_2
- RADP_DFE_FXTAP4_20
- RADP_DFE_FXTAP4_21
- RADP_DFE_FXTAP4_22
- RADP_DFE_FXTAP4_23
- RADP_DFE_FXTAP4_24
- RADP_DFE_FXTAP4_25
- RADP_DFE_FXTAP4_26
- RADP_DFE_FXTAP4_27
- RADP_DFE_FXTAP4_28
- RADP_DFE_FXTAP4_29
- RADP_DFE_FXTAP4_3
- RADP_DFE_FXTAP4_30
- RADP_DFE_FXTAP4_31
- RADP_DFE_FXTAP4_32
- RADP_DFE_FXTAP4_33
- RADP_DFE_FXTAP4_34
- RADP_DFE_FXTAP4_35
Device Support

- Intel Cyclone 10 GX
**Notes**

**Syntax**

```bash
set_instance_assignment -name XCVR_C10_RX_ADP_DFE_FXTAP4 -to <to> -entity <entity name> <value>
```
1.10.265. XCVR_C10_RX_ADPO_DFE_FXTAP4_SGN

Type

Enumeration

Values

- RADP_DFE_FXTAP4_SGN_0
- RADP_DFE_FXTAP4_SGN_1

Device Support

- Intel Cyclone 10 GX

Notes

Syntax

```
set_instance_assignment -name XCVR_C10_RX_ADPO_DFE_FXTAP4_SGN -to <to> -entity <entity name> <value>
```
1.10.266. XCVR_C10_RX_ADPA_DFE_FXTAP5

A logic option that allows you to specify the coefficient setting for fix tap five in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP5_0
- RADP_DFE_FXTAP5_1
- RADP_DFE_FXTAP5_10
- RADP_DFE_FXTAP5_11
- RADP_DFE_FXTAP5_12
- RADP_DFE_FXTAP5_13
- RADP_DFE_FXTAP5_14
- RADP_DFE_FXTAP5_15
- RADP_DFE_FXTAP5_16
- RADP_DFE_FXTAP5_17
- RADP_DFE_FXTAP5_18
- RADP_DFE_FXTAP5_19
- RADP_DFE_FXTAP5_2
- RADP_DFE_FXTAP5_20
- RADP_DFE_FXTAP5_21
- RADP_DFE_FXTAP5_22
- RADP_DFE_FXTAP5_23
- RADP_DFE_FXTAP5_24
- RADP_DFE_FXTAP5_25
- RADP_DFE_FXTAP5_26
- RADP_DFE_FXTAP5_27
- RADP_DFE_FXTAP5_28
- RADP_DFE_FXTAP5_29
- RADP_DFE_FXTAP5_3
- RADP_DFE_FXTAP5_30
- RADP_DFE_FXTAP5_31
- RADP_DFE_FXTAP5_32
- RADP_DFE_FXTAP5_33
- RADP_DFE_FXTAP5_34
- RADP_DFE_FXTAP5_35
Device Support

- Intel Cyclone 10 GX
Notes

Syntax

```
set_instance_assignment -name XCVR_C10_RX_ADP_DFE_FXTAP5 -to <to> -entity <entity name> <value>
```
1.10.267. XCVR_C10_RX_ADPSFE_FXTAP5_SGN

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP5_SGN_0
- RADP_DFE_FXTAP5_SGN_1

**Device Support**

- Intel Cyclone 10 GX

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_RX_ADPSFE_FXTAP5_SGN -to <to> -entity <entity name> <value>
```
1.10.268. XCVR_C10_RX_ADП_DFE_FXTAP6

A logic option that allows you to specify the coefficient setting for fix tap six in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP6_0
- RADP_DFE_FXTAP6_1
- RADP_DFE_FXTAP6_10
- RADP_DFE_FXTAP6_11
- RADP_DFE_FXTAP6_12
- RADP_DFE_FXTAP6_13
- RADP_DFE_FXTAP6_14
- RADP_DFE_FXTAP6_15
- RADP_DFE_FXTAP6_16
- RADP_DFE_FXTAP6_17
- RADP_DFE_FXTAP6_18
- RADP_DFE_FXTAP6_19
- RADP_DFE_FXTAP6_2
- RADP_DFE_FXTAP6_20
- RADP_DFE_FXTAP6_21
- RADP_DFE_FXTAP6_22
- RADP_DFE_FXTAP6_23
- RADP_DFE_FXTAP6_24
- RADP_DFE_FXTAP6_25
- RADP_DFE_FXTAP6_26
- RADP_DFE_FXTAP6_27
- RADP_DFE_FXTAP6_28
- RADP_DFE_FXTAP6_29
- RADP_DFE_FXTAP6_3
- RADP_DFE_FXTAP6_30
- RADP_DFE_FXTAP6_31
- RADP_DFE_FXTAP6_4
- RADP_DFE_FXTAP6_5
- RADP_DFE_FXTAP6_6
• RADP_DFE_FXTAP6_7
• RADP_DFE_FXTAP6_8
• RADP_DFE_FXTAP6_9

Device Support
• Intel Cyclone 10 GX

Notes

Syntax

```
set_instance_assignment -name XCVR_C10_RX_ADP_DFE_FXTAP6 -to <to> -entity <entity name> <value>
```
1.10.269. XCVR_C10_RX_ADP_DFE_FXTAP6_SGN

Type
Enumeration

Values
- RADP_DFE_FXTAP6_SGN_0
- RADP_DFE_FXTAP6_SGN_1

Device Support
- Intel Cyclone 10 GX

Notes

Syntax

```plaintext
set_instance_assignment -name XCVR_C10_RX_ADP_DFE_FXTAP6_SGN -to <to> -entity <entity name> <value>
```
A logic option that allows you to specify the coefficient setting for fix tap seven in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP7_0
- RADP_DFE_FXTAP7_1
- RADP_DFE_FXTAP7_10
- RADP_DFE_FXTAP7_11
- RADP_DFE_FXTAP7_12
- RADP_DFE_FXTAP7_13
- RADP_DFE_FXTAP7_14
- RADP_DFE_FXTAP7_15
- RADP_DFE_FXTAP7_16
- RADP_DFE_FXTAP7_17
- RADP_DFE_FXTAP7_18
- RADP_DFE_FXTAP7_19
- RADP_DFE_FXTAP7_2
- RADP_DFE_FXTAP7_20
- RADP_DFE_FXTAP7_21
- RADP_DFE_FXTAP7_22
- RADP_DFE_FXTAP7_23
- RADP_DFE_FXTAP7_24
- RADP_DFE_FXTAP7_25
- RADP_DFE_FXTAP7_26
- RADP_DFE_FXTAP7_27
- RADP_DFE_FXTAP7_28
- RADP_DFE_FXTAP7_29
- RADP_DFE_FXTAP7_3
- RADP_DFE_FXTAP7_30
- RADP_DFE_FXTAP7_31
- RADP_DFE_FXTAP7_4
- RADP_DFE_FXTAP7_5
- RADP_DFE_FXTAP7_6
- RADP_DFE_FXTAP7_7
- RADP_DFE_FXTAP7_8
- RADP_DFE_FXTAP7_9

**Device Support**
- Intel Cyclone 10 GX

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_RX_ADAP_DFE_FXTAP7 -to <to> -entity <entity name> <value>
```
1.10.271. XCVR_C10_RX_ADJP_DFE_FXTAP7_SGN

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP7_SGN_0
- RADP_DFE_FXTAP7_SGN_1

**Device Support**

- Intel Cyclone 10 GX

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_RX_ADJP_DFE_FXTAP7_SGN -to <to> -entity <entity name> <value>
```
1.10.272. XCVR_C10_RX_ADП_DFE_FXTAP8

A logic option that allows you to specify the coefficient setting for fix tap eight in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP8_0
- RADP_DFE_FXTAP8_1
- RADP_DFE_FXTAP8_10
- RADP_DFE_FXTAP8_11
- RADP_DFE_FXTAP8_12
- RADP_DFE_FXTAP8_13
- RADP_DFE_FXTAP8_14
- RADP_DFE_FXTAP8_15
- RADP_DFE_FXTAP8_16
- RADP_DFE_FXTAP8_17
- RADP_DFE_FXTAP8_18
- RADP_DFE_FXTAP8_19
- RADP_DFE_FXTAP8_2
- RADP_DFE_FXTAP8_20
- RADP_DFE_FXTAP8_21
- RADP_DFE_FXTAP8_22
- RADP_DFE_FXTAP8_23
- RADP_DFE_FXTAP8_24
- RADP_DFE_FXTAP8_25
- RADP_DFE_FXTAP8_26
- RADP_DFE_FXTAP8_27
- RADP_DFE_FXTAP8_28
- RADP_DFE_FXTAP8_29
- RADP_DFE_FXTAP8_3
- RADP_DFE_FXTAP8_30
- RADP_DFE_FXTAP8_31
- RADP_DFE_FXTAP8_32
- RADP_DFE_FXTAP8_33
- RADP_DFE_FXTAP8_34
- RADP_DFE_FXTAP8_35
Device Support

- Intel Cyclone 10 GX
Notes
Syntax

```
set_instance_assignment -name XCVR_C10_RX_ADP_DFE_FXTAP8 -to <to> -entity <entity name> <value>
```
1.10.273. XCVR_C10_RX_ADП_DFE_FXTAP8_SGN

Type
Enumeration

Values
- RADP_DFE_FXTAP8_SGN_0
- RADP_DFE_FXTAP8_SGN_1

Device Support
- Intel Cyclone 10 GX

Notes

Syntax

```bash
set_instance_assignment -name XCVR_C10_RX_ADП_DFE_FXTAP8_SGN -to <to> -entity <entity name> <value>
```
A logic option that allows you to specify the coefficient setting for fix tap nine in the receiver decision feedback equalizer. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP9_0
- RADP_DFE_FXTAP9_1
- RADP_DFE_FXTAP9_10
- RADP_DFE_FXTAP9_11
- RADP_DFE_FXTAP9_12
- RADP_DFE_FXTAP9_13
- RADP_DFE_FXTAP9_14
- RADP_DFE_FXTAP9_15
- RADP_DFE_FXTAP9_16
- RADP_DFE_FXTAP9_17
- RADP_DFE_FXTAP9_18
- RADP_DFE_FXTAP9_19
- RADP_DFE_FXTAP9_2
- RADP_DFE_FXTAP9_20
- RADP_DFE_FXTAP9_21
- RADP_DFE_FXTAP9_22
- RADP_DFE_FXTAP9_23
- RADP_DFE_FXTAP9_24
- RADP_DFE_FXTAP9_25
- RADP_DFE_FXTAP9_26
- RADP_DFE_FXTAP9_27
- RADP_DFE_FXTAP9_28
- RADP_DFE_FXTAP9_29
- RADP_DFE_FXTAP9_3
- RADP_DFE_FXTAP9_30
- RADP_DFE_FXTAP9_31
- RADP_DFE_FXTAP9_32
- RADP_DFE_FXTAP9_33
- RADP_DFE_FXTAP9_34
- RADP_DFE_FXTAP9_35
Device Support

- Intel Cyclone 10 GX
Notes

Syntax

```bash
set_instance_assignment -name XCVR_C10_RX_ADG_DFE_FXTAP9 -to <to> -entity <entity name> <value>
```
1.10.275. XCVR_C10_RX_ADPA_DP_FE_FXTAP9_SGN

**Type**

Enumeration

**Values**

- RADP_DFE_FXTAP9_SGN_0
- RADP_DFE_FXTAP9_SGN_1

**Device Support**

- Intel Cyclone 10 GX

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_RX_ADPA_DP_FE_FXTAP9_SGN -to <to> -entity <entity name> <value>
```
1.10.276. XCVR_C10_RX_ADG_VGA_SEL

A logic option that allows you to control the amount of output voltage swing on the variable gain amplifier. The amount of voltage swing is proportional to the setting where '0' gives the lowest swing and '4' gives the largest swing. This option is only valid when equalizer operates in manual mode.

**Type**

Enumeration

**Values**

- RADP_VGA_SEL_0
- RADP_VGA_SEL_1
- RADP_VGA_SEL_2
- RADP_VGA_SEL_3
- RADP_VGA_SEL_4

**Device Support**

- Intel Cyclone 10 GX

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_RX_ADG_VGA_SEL -to <to> -entity <entity name> <value>
```
1.10.277. **XCVR_C10_RX_EQ_BW_SEL**

**Type**
Enumeration

**Values**
- EQ_BW_1
- EQ_BW_2
- EQ_BW_3
- EQ_BW_4

**Device Support**
- Intel Cyclone 10 GX

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_RX_EQ_BW_SEL -to <to> -entity <entity name> <value>
```
1.10.278. **XCVR_C10_RX_EQ_DC_GAIN_TRIM**

A logic option that allows you to control the amount of DC gain on equalizer in high gain mode. The amount of DC gain is proportional to the setting where '0' gives the lowest DC gain and '28' gives the largest DC gain.

**Type**

Enumeration

**Values**
- NO_DC_GAIN
- STG1_GAIN7
- STG2_GAIN7
- STG3_GAIN7
- STG4_GAIN7

**Device Support**
- Intel Cyclone 10 GX

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_RX_EQ_DC_GAIN_TRIM -to <to> -entity <entity name> <value>
```
1.10.279. XCVR_C10_RX_LINK

A logic option that allows you to specify the type of communication for the receiver link. Quartus Prime will use this option to determine the legal data rate and power mode for the link.

**Type**
Enumeration

**Values**
- LR
- SR

**Device Support**
- Intel Cyclone 10 GX

**Notes**

**Syntax**

```plaintext
set_instance_assignment -name XCVR_C10_RX_LINK -to <to> -entity <entity name> <value>
```
1.10.280. XCVR_C10_RX_ONE_STAGE_ENABLE

**Type**

Enumeration

**Values**

- NON_S1_MODE
- S1_MODE

**Device Support**

- Intel Cyclone 10 GX

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_RX_ONE_STAGE_ENABLE -to <to> -entity <entity name> <value>
```
1.10.281. XCVR_C10_RX_TERM_SEL

A logic option that allows you to specify the termination value of a transceiver Rx pin.

**Type**

Enumeration

**Values**

- R_EXT0
- R_R1
- R_R2

**Device Support**

- Intel Cyclone 10 GX

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_RX_TERM_SEL -to <to> -entity <entity name> <value>
```
1.10.282. XCVR_C10_TX_COMPENSATION_EN

A logic option that allows you to turn on the compensation for transmitter data rate above 9 Gbps. Turning on this option draws more power on the transmitter buffer.

**Type**

Enumeration

**Values**

- DISABLE
- ENABLE

**Device Support**

- Intel Cyclone 10 GX

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_TX_COMPENSATION_EN -to <to> -entity <entity name> <value>
```
1.10.283. XCVR_C10_TX_LINK

A logic option that allows you to specify the type of communication for the transmitter link. Quartus Prime will use this option to determine the legal data rate and power mode for the link.

Type

Enumeration

Values

- LR
- SR

Device Support

- Intel Cyclone 10 GX

Notes

Syntax

```
set_instance_assignment -name XCVR_C10_TX_LINK -to <to> -entity <entity name> <value>
```
1.10.284. XCVR_C10_TX_PRE_EMP_SIGN_1ST_POST_TAP

A logic option that allows you to specify the output polarity of the transmitter pre-emphasis first post-tap.

Type

Enumeration

Values

- FIR_POST_1T_NEG
- FIR_POST_1T_POS

Device Support

- Intel Cyclone 10 GX

Notes

Syntax

```
set_instance_assignment -name XCVR_C10_TX_PRE_EMP_SIGN_1ST_POST_TAP -to <to> -
entity <entity name> <value>
```
1.10.285. **XCVR_C10_TX_PRE_EMP_SIGN_2ND_POST_TAP**

A logic option that allows you to specify the output polarity of the transmitter pre-emphasis second post-tap.

**Type**

Enumeration

**Values**

- FIR_POST_2T_NEG
- FIR_POST_2T_POS

**Device Support**

- Intel Cyclone 10 GX

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_TX_PRE_EMP_SIGN_2ND_POST_TAP -to <to> -entity <entity name> <value>
```
1.10.286. XCVR_C10_TX_PRE_EMP_SIGN_PRE_TAP_1T

A logic option that allows you to specify the output polarity of the transmitter pre-emphasis first pre-tap.

Type
Enumeration

Values
• FIR_PRE_1T_NEG
• FIR_PRE_1T_POS

Device Support
• Intel Cyclone 10 GX

Notes

Syntax

```plaintext
set_instance_assignment -name XCVR_C10_TX_PRE_EMP_SIGN_PRE_TAP_1T -to <to> -
entity <entity name> <value>
```
1.10.287. **XCVR_C10_TX_PRE_EMP_SIGN_PRE_TAP_2T**

A logic option that allows you to specify the output polarity of the transmitter preemphasis second pre-tap.

**Type**

Enumeration

**Values**

- FIR_PRE_2T_NEG
- FIR_PRE_2T_POS

**Device Support**

- Intel Cyclone 10 GX

**Notes**

**Syntax**

```plaintext
set_instance_assignment -name XCVR_C10_TX_PRE_EMP_SIGN_PRE_TAP_2T -to <to> -entity <entity name> <value>
```
1.10.288. XCVR_C10_TX_PRE_EMP_SWITCHING_CTRL_1ST_POST_TAP

A logic option that allows you to control the magnitude of transmitter pre-emphasis first post-tap. Legal values are: 0 to 25.

**Type**
Integer

**Device Support**
- Intel Cyclone 10 GX

**INTEGER_RANGE**
0, 25

**Notes**

**Syntax**

```sh
set_instance_assignment -name XCVR_C10_TX_PRE_EMP_SWITCHING_CTRL_1ST_POST_TAP -to <to> -entity <entity name> <value>
```
1.10.289. **XCVR_C10_TX_PRE_EMP_SWITCHING_CTRL_2ND_POST_TAP**

A logic option that allows you to control the magnitude of transmitter pre-emphasis second post-tap. Legal values are: 0 to 12.

**Type**
Integer

**Device Support**
- Intel Cyclone 10 GX

**INTEGER_RANGE**
0, 12

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_TX_PRE_EMP_SWITCHING_CTRL_2ND_POST_TAP -to <to> -entity <entity name> <value>
```
1.10.290. **XCVR_C10_TX_PRE_EMP_SWITCHING_CTRL_PRE_TAP_1T**

A logic option that allows you to control the magnitude of transmitter pre-emphasis first pre-tap. Legal values are: 0 to 16.

**Type**

Integer

**Device Support**

- Intel Cyclone 10 GX

**INTEGER_RANGE**

0, 16

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_TX_PRE_EMP_SWITCHING_CTRL_PRE_TAP_1T -to <to> -entity <entity name> <value>
```
1.10.291. XCVR_C10_TX_PRE_EMP_SWITCHING_CTRL_PRE_TAP_2T

A logic option that allows you to control the magnitude of transmitter pre-emphasis second pre-tap. Legal values are: 0 to 7.

**Type**

Integer

**Device Support**

- Intel Cyclone 10 GX

**INTEGER_RANGE**

0, 7

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_TX_PRE_EMP_SWITCHING_CTRL_PRE_TAP_2T -to <to> -entity <entity name> <value>
```
1.10.292. XCVR_C10_TX_SLEW_RATE_CTRL

**Type**

Enumeration

**Values**

- SLEW_R0
- SLEW_R1
- SLEW_R2
- SLEW_R3
- SLEW_R4
- SLEW_R5
- SLEW_R6
- SLEW_R7

**Device Support**

- Intel Cyclone 10 GX

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_TX_SLEW_RATE_CTRL -to <to> -entity <entity name> <value>
```
1.10.293. XCVR_C10_TX_TERM_SEL

A logic option that allows you to specify the termination value of a transceiver Tx pin.

**Type**
Enumeration

**Values**
- R_R1
- R_R2

**Device Support**
- Intel Cyclone 10 GX

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_TX_TERM_SEL -to <to> -entity <entity name> <value>
```
1.10.294. XCVR_C10_TX_VOD_OUTPUT_SWING_CTRL

A logic option that allows you to control the transmitter output swing level. Legal values are: 0 to 31.

Type
Integer

Device Support
- Intel Cyclone 10 GX

INTEGER_RANGE
0, 31

Notes

Syntax

```
set_instance_assignment -name XCVR_C10_TX_VOD_OUTPUT_SWING_CTRL -to <to> -
  entity <entity name> <value>
```
1.10.295. XCVR_C10_TX_XTX_PATH_ANALOG_MODE

**Type**

Enumeration

**Values**

- CEI_11100_LR
- CEI_11100_SR
- CEI_4976_LR
- CEI_4976_SR
- CEI_6375_LR
- CEI_6375_SR
- CEI_9950_LR
- CEI_9950_SR
- CPRI_12500
- CPRI_E12LVII
- CPRI_E12LVIII
- CPRI_E24LVII
- CPRI_E24LVIII
- CPRI_E30LVII
- CPRI_E30LVIII
- CPRI_E48LVII
- CPRI_E48LVIII
- CPRI_E60LVII
- CPRI_E60LVIII
- CPRI_E6LVII
- CPRI_E6LVIII
- CPRI_E96LVIII
- CPRI_E99LVIII
- HIGIG_4062
- HIGIG_5000
- HIGIG_6250
- HIGIG_6562
- IEEE_10G_BASE_CR_10312
- IEEE_10G_KR_10312
- IEEE_40G_BASE_KR_10312
- INTERLAKEN_11100
- INTERLAKEN_12500
- INTERLAKEN_6375
- JESD204_A_B_12500
- JESD204_A_B_6375
- QSGMII_5000
- SFI_S_6250
- SRIO_5000_LR
- SRIO_5000_MR
- SRIO_5000_SR
- SRIO_6250_LR
- SRIO_6250_MR
- SRIO_6250_SR
- USER_CUSTOM

**Device Support**

- Intel Cyclone 10 GX

**Notes**

**Syntax**

```
set_instance_assignment -name XCVR_C10_TX_TTX_PATH_ANALOG_MODE -to <to> -entity <entity name> <value>
```
1.10.296. XCVR_RECONFIG_GROUP

Assigns the node you specify to a transceiver Avalon Memory-Mapped interface group. The Avalon Memory-Mapped interfaces of an RX-only channel and a TX-only channel, or a CDR PLL and a TX-only channel, can be merged and placed into one transceiver channel. You can assign this option to the instance names of the transceiver Avalon Memory-Mapped interfaces you want the Fitter to merge. You can also assign this to options to a CDR PLL instance name and the transceiver TX (or RX) positive pin name of a TX-only (or RX-only) channel, instead of the corresponding transceiver Avalon Memory-Mapped interface instance name. Assigning this option to two nodes directs the Fitter to view the specified nodes as single group. The Fitter does not automatically merge the transceiver Avalon Memory-Mapped interfaces; by default a CDR PLL, RX-only channel, and a TX-only channel map to three different transceiver channels. If the Avalon Memory-Mapped interfaces of the transceiver channels can be merged into one Avalon Memory-Mapped interface, the Fitter merges and places them in the same transceiver channel. If the Fitter cannot merge the transceiver channels, your compilation will result in an error.

Type
String

Device Support
• Intel Agilex
• Intel Arria 10
• Intel Cyclone 10 GX
• Intel Stratix 10

Notes
This assignment supports wildcards.
This assignment supports Fitter wildcards.

Syntax

set_instance_assignment -name XCVR_RECONFIG_GROUP -to <to> -entity <entity name> <value>

Example

set_instance_assignment -name XCVR_RECONFIG_GROUP myChannel -to output_pin[0]
set_instance_assignment -name XCVR_RECONFIG_GROUP myChannel -to input_pin[1]
1.10.297. XCVR_S10_REFCLK_TERM_TRISTATE

A logic option that directs the Compiler to enable the internal termination of the dedicated reference clock pin.

**Type**

Enumeration

**Values**

- TRISTATE_OFF
- TRISTATE_ON

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

**Syntax**

```bash
set_instance_assignment -name XCVR_S10_REFCLK_TERM_TRISTATE -to <to> -entity <entity name> <value>
```
1.10.298. XCVR_USE_HQ_REFCLK

Instructs the Fitter to use high quality reference clock lines for the specified transceiver TX channel.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

**Syntax**

```bash
set_instance_assignment -name XCVR_USE_HQ_REFCLK -to <to> -entity <entity name> <value>
```

**Example**

```bash
set_instance_assignment -name XCVR_USE_HQ_REFCLK ON -to tx_pin
```
1.10.299. XCVR_USE_SKEW_BALANCED

Instructs the Fitter to use low skew balanced reference clock for the specified transceiver channel.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

This assignment is included in the Fitter report.

**Syntax**

```
set_instance_assignment -name XCVR_USE_SKEW_BALANCED -to <to> -entity <entity name> <value>
```

**Example**

```
set_instance_assignment -name XCVR_USE_SKEW_BALANCED ON -to tx_pin
```
1.10.300. XCVR_VCCR_VCCT_VOLTAGE

Configure the VCCR_GXB and VCCT_GXB voltage for an GXB I/O pin by specifying the intended supply voltages for a GXB I/O pin. If this is not set, the compiler automatically sets the correct VCCR_GXB and VCCT_GXB voltage.

**Old Name**
GXB_VCCR_VCCT_VOLTAGE

**Type**
Enumeration

**Values**
- 0.85V
- 0.9V
- 1.0V
- 1.15V
- 1.1V
- 1.2V

**Device Support**
- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**
This assignment supports Fitter wildcards.

**Syntax**

```bash
set_instance_assignment -name XCVR_VCCR_VCCT_VOLTAGE -to <to> -entity <entity name> <value>
```
1.11. Netlist Viewer Assignments

1.11.1. RTLV_GROUP_COMB_LOGIC_IN_CLOUD

Allow RTL Viewer to group combinational logic in logic cloud

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name RTLV_GROUP_COMB_LOGIC_IN_CLOUD <value>
```

**Default Value**

Off
1.11.2. RTLV_GROUP_COMB_LOGIC_IN_CLOUD_TMV

Allow Technology Map Viewer to group combinational logic in logic cloud

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name RTLV_GROUP_COMB_LOGIC_IN_CLOUD_TMV <value>
```

**Default Value**

Off
1.11.3. RTLV_GROUPRELATED_NODES

Allow RTL Viewer to group all related nodes into a single bus node

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name RTLV_GROUPRELATED_NODES <value>
```

**Default Value**

On
1.11.4. RTLV_GROUPRELATED_NODES_TMV

Allow Technology Map Viewer to group all related nodes into a single bus node

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name RTLV_GROUPRELATED_NODES_TMV <value>
```

**Default Value**

On
1.11.5. RTLV_REMOVE_FANOUT_FREE_REGSITERS

Allow RTL Viewer to remove fanout free registers

**Type**

Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name RTLV_REMOVE_FANOUT_FREE_REGSITERS <value>
```

**Default Value**

On
1.11.6. RTLV_SIMPLIFIED_LOGIC

Allow RTL Viewer to remove wire nodes and merge chain of equivalent combinatorial gates

Type
Boolean

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```plaintext
set_global_assignment -name RTLV_SIMPLIFIED_LOGIC <value>
```

Default Value

On
1.12. Pin & Location Assignments

1.12.1. FAST_INPUT_REGISTER

Implements an input register in a cell that has a fast, direct connection from an I/O pin. If such a fast, direct connection from the I/O pin is not available on the I/O cell hardware, this option instructs the Fitter to lock the input register in the LAB adjacent to the I/O cell feeding it. Turning on the Fast Input Register option can help maximize I/O timing performance, for example, by permitting fast setup times. Turning this option off for a particular signal prevents the Fitter from implementing the signal automatically in an I/O cell or locking down the input register in the LAB adjacent to the I/O cell. This option is ignored if it is applied to anything other than a register or an input or bidirectional pin that feeds a register.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

**Syntax**

```
set_instance_assignment -name FAST_INPUT_REGISTER -to <to> -entity <entity name> <value>
```
1.12.2. FAST_OUTPUT_ENABLE_REGISTER

Implements an output enable register in a cell that has a fast, direct connection to an I/O pin. If such a fast, direct connection to the I/O pin is not available in the I/O cell hardware, this option instructs the Fitter to lock the output enable register in the LAB adjacent to the I/O cell it is feeding. Turning on the Fast Output Enable Register option can help maximize I/O timing performance, for example, by permitting fast clock-to-output times. Turning this option off for a particular signal prevents the Fitter from implementing the signal automatically in an I/O cell or locking down the output enable register in the LAB adjacent to the I/O cell. This option is ignored if it is applied to anything other than a register or an output or bidirectional pin fed by a register.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

**Syntax**

```
set_instance_assignment -name FAST_OUTPUT_ENABLE_REGISTER -to <to> -entity <entity name> <value>
```
1.12.3. FAST_OUTPUT_REGISTER

Implements an output register in a cell that has a fast, direct connection to an I/O pin. If such a fast, direct connection to the I/O pin is not available in the I/O cell hardware, this option instructs the Fitter to lock the output register in the LAB adjacent to the I/O cell it is feeding. Turning on the Fast Output Register option can help maximize I/O timing performance, for example, by permitting fast clock-to-output times. Turning this option off for a particular signal prevents the Fitter from implementing the signal automatically in an I/O cell or locking down the output register in the LAB adjacent to the I/O cell. This option is ignored if it is applied to anything other than a register or an output or bidirectional pin fed by a register.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports Fitter wildcards.

**Syntax**

```
set_instance_assignment -name FAST_OUTPUT_REGISTER -to <to> -entity <entity name> <value>
```
1.12.4. IP_DEBUG_VISIBLE

When assigned to an Encrypted IP node this option directs Quartus Prime to display the node in the Node Finder.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_instance_assignment -name IP_DEBUG_VISIBLE -to <to> -entity <entity name> <value>
```
### 1.12.5. LOCATION

Assigns a location on the device for the current node(s) and/or pin(s).

**Type**

Location

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment supports Fitter wildcards.

**Syntax**

```
set_location_assignment -to <to> <value>
```
### 1.12.6. PIN_CONNECT_FROM_NODE

Directs the Compiler to generate a device pin with the specified name and connect the device pin to an internal signal.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_instance_assignment -name PIN_CONNECT_FROM_NODE -to <to> <value>
```
1.12.7. RESERVE_PIN

Reserves the pin in one of seven states: as an input that is tri-stated; as an output that drives ground; as an output that drives VCC; as an output that drives an unspecified signal; as Signal Probe output; as a voltage reference (VREF); or as bidirectional. Note: The 'As VREF' setting is not appropriate for all device families. Please refer to the device data sheet for information on VREF support.

Old Name
RESERVED_PIN

Type
Enumeration

Values
• As Signal Probe output
• As VREF
• As bidirectional
• As input tri-stated
• As output driving VCC
• As output driving an unspecified signal
• As output driving ground

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
None

Syntax

```
set_instance_assignment -name RESERVE_PIN -to <to> <value>
set_global_assignment -name RESERVE_PIN <value>
```
1.12.8. SUBCLIQUE_OF

Specifies that the current clique is a member of another clique.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_instance_assignment -name SUBCLIQUE_OF -to <to> -entity <entity name> -section_id <section identifier> <value>
```
1.12.9. VIRTUAL_PIN

Specifies whether an I/O element in a lower-level design entity can be temporarily mapped to a logic element and not to a pin during compilation. The virtual pin is then implemented as a LUT. This option should be specified only for I/O elements that become nodes when imported to the top-level design.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment supports synthesis wildcards.

**Syntax**

```text
set_instance_assignment -name VIRTUAL_PIN -to <to> -entity <entity name> <value>
```
1.13. Power Estimation Assignments

1.13.1. EARLY_POWER_ESTIMATOR_EXPORT_FILE

Tell QPA to export a summary of the design power estimate suitable for importing into the Early Power Estimator.

**Type**

File name

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name EARLY_POWER_ESTIMATOR_EXPORT_FILE <value>
```
1.13.2. ENABLE_SMART_VOLTAGE_ID

Specifies whether smart voltage ID feature is used.

**Type**
Boolean

**Device Support**
- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```bash
set_global_assignment -name ENABLE_SMART_VOLTAGE_ID <value>
```

**Default Value**
Off
1.13.3. POWER_AND_THERMAL_CALCULATOR_EXPORT_FILE

Tell QPA to export a summary of the design power estimate suitable for importing into the Power and Thermal Calculator.

**Type**

File name

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_AND_THERMAL_CALCULATOR_EXPORT_FILE <value>
```
1.13.4. POWER_APPLY_THERMAL_MARGIN

Specifies whether to apply recommended margins to power estimates for thermal analysis. These margins apply only to thermal analysis results.

**Type**

Enumeration

**Values**

- OFF
- RECOMMENDED

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_APPLY_THERMAL_MARGIN <value>
```

**Default Value**

OFF
1.13.5. POWER_AUTO_COMPUTE_TJ

Specifies whether the junction temperature is auto-computed during power estimation. If the junction temperature is not auto-computed, you must specify the junction temperature.

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_AUTO_COMPUTE_TJ <value>
```
1.13.6. POWER_BOARD_TEMPERATURE

Specifies the board temperature, in degrees Celsius, used during power estimation.

**Type**

Integer

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_BOARD_TEMPERATURE <value>
```

**Default Value**

25
1.13.7. POWER_BOARD_THERMAL_MODEL

Specifies the board thermal model used during power estimation.

Type

String

Device Support

- Intel Arria 10
- Intel Cyclone 10 GX

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name POWER_BOARD_THERMAL_MODEL <value>
```
1.13.8. POWER_COOLING_FOR_MAX_TJ

Specifies that the power estimator should find cooling solution required to not exceed specified maximum junction temperature limit. Junction temperatures used for power estimation of different parts of the chip will be actual temperatures resulting from using the found cooling solution and will typically vary across the chip.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_COOLING_FOR_MAX_TJ <value>
```

**Default Value**

Off
1.13.9. **POWER_DEFAULT_INPUT_IO_TOGGLE_RATE**

Specifies the default toggle rate to be used on input I/O pins during power estimation. This value is only used if a toggle rate has not been specified for a node either through a Signal Activity File, VCD file or user assignment.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_DEFAULT_INPUT_IO_TOGGLE_RATE <value>
```

**Default Value**

12.5%
1.13.10. POWER_DEFAULT_TOGGLE_RATE

Specifies the default toggle rate to be used on all nodes except input I/O pins during power estimation. This value is only used if a toggle rate has not been specified for a node either through a Signal Activity File, VCD file or user assignment.

Type
String

Device Support
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name POWER_DEFAULT_TOGGLE_RATE <value>
```

Default Value
12.5%
1.13.11. POWER_GLITCH_FACTOR

Specifies the multiplication factor to the toggle rates used for power estimation for part of design hierarchy. This is useful to adjust toggle rates of parts of the design with high number of glitches. The value must be positive.

**Type**

Double

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

**Syntax**

```plaintext
set_global_assignment -name POWER_GLITCH_FACTOR -entity <entity name> <value>
set_instance_assignment -name POWER_GLITCH_FACTOR -to <to> -entity <entity name> <value>
```
1.13.12. POWER_HPS_DYNAMIC_POWER_DUAL

Dynamic Power of dual processor core when HPS is active.

Type
String

Device Support
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name POWER_HPS_DYNAMIC_POWER_DUAL <value>
```
1.13.13. POWER_HPS_DYNAMIC_POWER_SINGLE

Dynamic power of single processor core when HPS is active.

Type
String

Device Support
• Intel Agilex
• Intel Arria 10
• Intel Cyclone 10 GX
• Intel Stratix 10

Notes
This assignment is included in the Fitter report.

Syntax

set_global_assignment -name POWER_HPS_DYNAMIC_POWER_SINGLE <value>
1.13.14. **POWER_HPS_ENABLE**

Specifies whether or not you must include the HPS processor subsystem for SoC power estimation.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_HPS_ENABLE <value>
```

**Default Value**

Off
1.13.15. POWER_HPS_JUNCTION_TEMPERATURE

Junction Temperature when HPS is active.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name POWER_HPS_JUNCTION_TEMPERATURE <value>
```
1.13.16. POWER_HPS_PROC_FREQ

 Specifies the processor frequency of the HPS assumed by power estimation. The units for this value are MHz and the value must be positive. The value provided should be within 0 to 1000.

 **Type**

 Double

 **Device Support**

 - Intel Agilex
 - Intel Arria 10
 - Intel Cyclone 10 GX
 - Intel Stratix 10

 **Notes**

 This assignment is included in the Fitter report.

 **Syntax**

 ```
 set_global_assignment -name POWER_HPS_PROC_FREQ <value>
 ```

 **Default Value**

 0.0
1.13.17. POWER_HPS_STATIC_POWER

Static Power when HPS is active.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name POWER_HPS_STATIC_POWER <value>
```
1.13.18. POWER_HPS_TOTAL_POWER

Total power when HPS is active.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_HPS_TOTAL_POWER <value>
```
1.13.19. POWER_HSSI

If the transceivers are unused, setting this option to "Opportunistically power off" directs the Quartus Prime software to consider the transceivers as powered down. Setting this option to "Power on" directs the Quartus Prime software to consider the transceivers powered regardless of their use. This setting affects the VCCA, VCCH_GXB, and VCCL_GXB power rails.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_HSSI <value>
```
1.13.20. POWER_HSSI_LEFT

If the transceivers on the left side of the device are unused, setting this option to "Opportunistically power off" directs the Quartus Prime software to consider the transceivers on the left side of the device powered down. Setting this option to "Power on" directs the Quartus Prime software to consider the transceivers on the left side powered regardless of their use. This setting affects the VCCA_L, VCCH_GXBL, VCCL_GXBL, VCCR_L, and VCCT_L power rails.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_HSSI_LEFT <value>
```
1.13.21. POWER_HSSI_RIGHT

If the transceivers on the right side of the device are unused, setting this option to "Opportunistically power off" directs the Quartus Prime software to consider the transceivers on the right side of the device powered down. Setting this option to "Power on" directs the Quartus Prime software to consider the transceivers on the right side powered regardless of their use. This setting affects the VCCA_R, VCCH_GXBR, VCCL_GXBR, VCCR_R, and VCCT_R power rails.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_HSSI_RIGHT <value>
```
1.13.22. POWER_HSSI_VCCHIP_LEFT

If the PCI Express hard IP blocks on the left side of the device are unused, setting this option to "Opportunistically power off" directs the Quartus Prime software to consider the PCI Express hard IP blocks on the left side of the device powered down. Setting this option to "Power on" directs the Quartus Prime software to consider the PCI Express hard IP blocks on the left side powered regardless of their use.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_HSSI_VCCHIP_LEFT <value>
```
1.13.23. POWER_HSSI_VCCHIP_RIGHT

If the PCI Express hard IP blocks on the right side of the device are unused, setting this option to "Opportunistically power off" directs the Quartus Prime software to consider the PCI Express hard IP blocks on the right side of the device powered down. Setting this option to "Power on" directs the Quartus Prime software to consider the PCI Express hard IP blocks on the right side powered regardless of their use.

Type
String

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

set_global_assignment -name POWER_HSSI_VCCHIP_RIGHT <value>
1.13.24. POWER_INPUT_FILE_NAME

Specifies the name of the VCD File or Signal Activity File which should be used to initialize the toggle rates and static probabilities that will be used during power estimation.

**Type**

File name

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name POWER_INPUT_FILE_NAME -entity <entity name> -section_id <section identifier> <value>
```
1.13.25. POWER_INPUT_FILE_TYPE

Specifies whether the input power file is a VCD file or SAF file.

Type

Enumeration

Values

• SAF
• VCD

Device Support

• Intel Agilex
• Intel Arria 10
• Intel Cyclone 10 GX
• Intel Stratix 10

Notes

Syntax

```
set_global_assignment -name POWER_INPUT_FILE_TYPE -entity <entity name> -section_id <section identifier> <value>
```
1.13.26. POWER_MAX_TJ_VALUE

Specifies the maximum junction temperature limit that no part of any die in the package should exceed.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_MAX_TJ_VALUE <value>
```

**Default Value**

100
1.13.27. **POWER_OCS_VALUE**

Specifies the case-to-heat sink thermal resistance, in degrees Celsius per watt, used during power estimation.

**Type**

String

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_OCS_VALUE <value>
```
1.13.28. POWER_OJB_VALUE

Specifies the junction-to-board thermal resistance, in degrees Celsius per watt, used during power estimation.

**Type**
String

**Device Support**
- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name POWER_OJB_VALUE <value>
```
1.13.29. POWER_OJC_VALUE

Specifies the junction-to-case-sink thermal resistance, in degrees Celsius per watt, used during power estimation.

Type
String

Device Support
- Intel Arria 10
- Intel Cyclone 10 GX

Notes
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name POWER_OJC_VALUE <value>
```
1.13.30. POWER_OSA_VALUE

Specifies the heat sink-to-ambient thermal resistance, in degrees Celsius per watt, used during power estimation.

**Type**
String

**Device Support**
- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_OSA_VALUE <value>
```
1.13.31. POWER_OUTPUT_SAF_NAME

Specifies the name the Signal Activity File should be written to containing the toggle rates and static probabilities used during power estimation.

**Type**

File name

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_OUTPUT_SAF_NAME <value>
```
1.13.32. **POWER_PRESET_COOLING_SOLUTION**

Specifies the preset cooling solution used during power estimation.

**Type**

String

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_PRESET_COOLING_SOLUTION <value>
```
1.13.33. POWER_PSI_CA_VALUE

Specifies the cooling solution case-to-ambient thermal resistance, in degrees Celsius per watt.

**Type**
String

**Device Support**
- Intel Agilex
- Intel Stratix 10

**Notes**
This assignment is included in the Fitter report.

**Syntax**
```
set_global_assignment -name POWER_PSI_CA_VALUE <value>
```

**Default Value**
0.5
1.13.34. POWER_READ_INPUT_FILE

Assigns user-defined power input file characteristics to an entity. To specify a power input file, you must define a named group of 'power input file settings' and assign them to an entity with this option. You can create these settings using the Power Analyzer Settings page.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_instance_assignment -name POWER_READ_INPUT_FILE -to <to> -entity <entity name> <value>
```
1.13.35. POWER_REPORT_POWER_DISSIPATION

Specifies whether the Power Analyzer should report the thermal power dissipation calculated during power analysis in the Thermal Power Dissipation By Block report panel.

Type

Boolean

Device Support

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name POWER_REPORT_POWER_DISSIPATION <value>
set_instance_assignment -name POWER_REPORT_POWER_DISSIPATION -to <to> -entity <entity name> <value>
```

Default Value

Off
1.13.36. POWER_REPORT_SIGNAL_ACTIVITY

Specifies whether the Power Analyzer should report the signal activities assumed for power analysis, and the sources for those activities. Signal activity consists of both the static probability and the toggle rate for the signals generated by the node or entity.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name POWER_REPORT_SIGNAL_ACTIVITY <value>
set_instance_assignment -name POWER_REPORT_SIGNAL_ACTIVITY -to <to> -entity <entity name> <value>
```

**Default Value**

Off
1.13.37. POWER_STATIC_PROBABILITY

Specifies the fraction of time the signals generated by the node or entity are expected to be at VCC. Allowable values range from and include 0.0 through 1.0.

**Type**
String

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

**Syntax**

```
set_instance_assignment -name POWER_STATIC_PROBABILITY -to <to> <value>
```
1.13.38. POWER_TEMPERATURE_MEASUREMENT_METHOD

Specifies the method to use for reporting temperature sensors for thermal analysis.

**Type**

Enumeration

**Values**

- DTS
- TSD

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_TEMPERATURE_MEASUREMENT_METHOD <value>
```

**Default Value**

DTS
1.13.39. POWER_THERMAL_SOLVER_MODE

Specifies the thermal solver mode to use.

Type

Enumeration

Values

- FIND_MAX_TJ
- FIND_PSI_CA
- FIND_TA
- OFF

Device Support

- Intel Agilex
- Intel Stratix 10

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name POWER_THERMAL_SOLVER_MODE <value>
```
1.13.40. POWER_TJ_VALUE

Specifies the junction temperature value, in degrees Celsius, used during power estimation.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_TJ_VALUE <value>
```

**Default Value**

25
1.13.41. POWER_TOGGLE_RATE

Specifies the toggle rate assumed by power estimation for the signals generated by this node or entity. The units for this value are transitions per second and the value must be positive. The value provided should be the expected time-averaged toggle rate, rather than worst case (highest possible) toggle rate. A different assignment, Toggle Rate, applies to I/O pins only and is used by the Fitter and by I/O Assignment Analysis to verify signal integrity under worst case conditions (highest possible toggle rate). Use the Synchronizer Toggle Rate if you want to configure the data rates used for Metastability Reporting in the Timing Analyzer.

**Type**

Double

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

**Syntax**

```text
set_instance_assignment -name POWER_TOGGLE_RATE -to <to> <value>
```
1.13.42. POWER_TOGGLE_RATE_PERCENTAGE

Specifies the toggle rate, as a percentage of clock domain frequency, assumed by power estimation for the signals generated by this node or entity. This percentage acts as a multiplier for the clock domain frequency of the given node. For example, a toggle rate percentage of 12.5 on a node with a clock domain frequency of 96 MHz would result in a toggle rate of 12 million transitions per second. The percentage value must be positive and can take on values greater than 100. The value provided should be representative of the expected time-averaged toggle rate, rather than worst case (highest possible) toggle rate.

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

**Syntax**

```
set_instance_assignment -name POWER_TOGGLE_RATE_PERCENTAGE -to <to> <value>
```
1.13.43. POWER_USE_CUSTOM_COOLING_SOLUTION

Specifies whether a custom cooling solution is used during power estimation. For a custom cooling solution, you must specify the case-to-heat sink, junction-to-case and heat sink-to-ambient thermal resistances.

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_USE_CUSTOM_COOLING_SOLUTION <value>
```

**Default Value**

Off
1.13.44. POWER_USE_DEVICE_CHARACTERISTICS

Specifies the device characteristics to be used during power estimation. Estimates are based on average power consumed by typical silicon at nominal operating conditions. For FPGA board power supply design, change to MAXIMUM to get worst-case values.

**Type**

Enumeration

**Values**

- MAXIMUM
- TYPICAL

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_USE_DEVICE_CHARACTERISTICS <value>
```
1.13.45. POWER_USE_INPUT_FILES

Specifies whether or not Signal Activity Files or VCD files should be used to initialize the toggle rates and static probabilities that will be used during power estimation.

**Type**
Boolean

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_USE_INPUT_FILES <value>
```

**Default Value**
Off
1.13.46. POWER_USE_PVA

Specifies whether or not Power Vectorless Activity should be used to fill in undefined toggle rates and static probabilities.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_USE_PVA <value>
```

**Default Value**

On
1.13.47. POWER_USE_TA_VALUE

Specifies the ambient temperature value, in degrees Celsius, used during power estimation.

**Type**
Integer

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_USE_TA_VALUE <value>
```

**Default Value**
50
1.13.48. POWER_VCCAUX_USER_OPTION

Allows you to specify settings for the VCCAUX power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_VCCAUX_USER_OPTION <value>
```
1.13.49. **POWER_VCCA_GXBL_USER_OPTION**

Allows you to specify settings for the VCCA_GXBL power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_VCCA_GXBL_USER_OPTION <value>
```
1.13.50. POWER_VCCA_GXBR_USER_OPTION

Allows you to specify settings for the VCCA_GXBR power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_VCCA_GXBR_USER_OPTION <value>
```
1.13.51. POWER_VCCA_GXB_USER_OPTION

Allows you to specify settings for the VCCA_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_VCCA_GXB_USER_OPTION <value>
```
1.13.52. POWER_VCCA_L_USER_OPTION

Allows you to specify settings for the VCCA_L power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```bash
set_global_assignment -name POWER_VCCA_L_USER_OPTION <value>
```
1.13.53. POWER_VCCA_R_USER_OPTION

Allows you to specify settings for the VCCA_R power rail supply. Refer to the device datasheet for the current device family for more details.

Type
String

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

set_global_assignment -name POWER_VCCA_R_USER_OPTION <value>
1.13.54. POWER_VCCCB_USER_OPTION

Allows you to specify settings for the VCCCB power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_VCCCB_USER_OPTION <value>
```
1.13.55. POWER_VCCH_GXBL_USER_OPTION

Allows you to specify settings for the VCCH_GXBL power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_VCCH_GXBL_USER_OPTION <value>
```
1.13.56. POWER_VCCH_GXBR_USER_OPTION

Allows you to specify settings for the VCCH_GXBR power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_VCCH_GXBR_USER_OPTION <value>
```
1.13.57. POWER_VCCH_GXB_USER_OPTION

Allows you to specify settings for the VCCH_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_VCCH_GXB_USER_OPTION <value>
```
1.13.58. POWER_VCCIO_USER_OPTION

Allows you to specify settings for the VCCIO power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_VCCIO_USER_OPTION <value>
```
1.13.59. POWER_VCCL_GXB_USER_OPTION

Allows you to specify settings for the VCCL_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_VCCL_GXB_USER_OPTION <value>
```
1.13.60. **POWER_VCCPD_USER_OPTION**

Allows you to specify settings for the VCCPD power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_VCCPD_USER_OPTION <value>
```
1.13.61. POWER_VCCR_GXBL_USER_OPTION

Allows you to specify settings for the VCCR_GXBL power rail supply. Refer to the device datasheet for the current device family for more details.

Type
String

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```python
set_global_assignment -name POWER_VCCR_GXBL_USER_OPTION <value>
```
1.13.62. POWER_VCCR_GXBR_USER_OPTION

Allows you to specify settings for the VCCR_GXBR power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name POWER_VCCR_GXBR_USER_OPTION <value>
```
1.13.63. POWER_VCCR_GXB_USER_OPTION

Allows you to specify settings for the VCCR_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name POWER_VCCR_GXB_USER_OPTION <value>
```
1.13.64. **POWER_VCCT_GXBL_USER_OPTION**

Allows you to specify settings for the VCCT_GXBL power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```tcl
cset_global_assignment -name POWER_VCCT_GXBL_USER_OPTION <value>
```
1.13.65. POWER_VCCT_GXBR_USER_OPTION

Allows you to specify settings for the VCCT_GXBR power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```bash
set_global_assignment -name POWER_VCCT_GXBR_USER_OPTION <value>
```
1.13.66. POWER_VCCT_GXB_USER_OPTION

Allows you to specify settings for the VCCT_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name POWER_VCCT_GXB_USER_OPTION <value>
```
1.13.67. POWER_VCD_FILE_END_TIME

Specifies the time at which toggle rates and static probabilities should stop being calculated for the output signals contained in the VCD files.

**Type**

Time

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

**Syntax**

```
set_global_assignment -name POWER_VCD_FILE_END_TIME -entity <entity name> -
section_id <section identifier> <value>
```
1.13.68. POWER_VCD_FILE_START_TIME

Specifies the time at which toggle rates and static probabilities should start to be calculated for the output signals contained in the VCD files.

**Type**

Time

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

**Syntax**

```
set_global_assignment -name POWER_VCD_FILE_START_TIME -entity <entity name> -section_id <section identifier> <value>
```
1.13.69. POWER_VCD_FILTER_GLITCHES

Specifies whether or not glitch filtering should be used when reading in VCD files.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name POWER_VCD_FILTER_GLITCHES <value>
```

**Default Value**

On
1.13.70. VCCAUX_SHARED_USER_VOLTAGE

Specifies the voltage of the VCCAUX_SHARED power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCAUX_SHARED_USER_VOLTAGE <value>
```
1.13.71. VCCAUX_USER_VOLTAGE

Specifies the voltage of the VCCAUX power rail supply. Refer to the device datasheet for the current device family for more details.

Type
String

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name VCCAUX_USER_VOLTAGE <value>
```
1.13.72. VCCA_FPLL_USER_VOLTAGE

Specifies the voltage of the VCCA_FPLL power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCA_FPLL_USER_VOLTAGE <value>
```
1.13.73. VCCA_GTBR_USER_VOLTAGE

Specifies the voltage of the VCCA_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name VCCA_GTBR_USER_VOLTAGE <value>
```
1.13.74. VCCA_GTB_USER_VOLTAGE

Specifies the voltage of the VCCA_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name VCCA_GTB_USER_VOLTAGE <value>
```
1.13.75. VCCA_GXBL_USER_VOLTAGE

Specifies the voltage of the VCCA_GXBL power rail supply. Refer to the device datasheet for the current device family for more details.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```set_global_assignment -name VCCA_GXBL_USER_VOLTAGE <value>```
1.13.76. VCCA_GXBR_USER_VOLTAGE

Specifies the voltage of the VCCA_GXBR power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCA_GXBR_USER_VOLTAGE <value>
```
1.13.77. VCCA_GXB_USER_VOLTAGE

Specifies the voltage of the VCCA_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name VCCA_GXB_USER_VOLTAGE <value>
```
1.13.78. VCCA_L_USER_VOLTAGE

Specifies the default voltage of the VCCA_L power rail supply, which is applied if all
transceivers on the left side of the device are powered and unused. To configure a
transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device
datasheet for the current device family for more details.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

set_global_assignment -name VCCA_L_USER_VOLTAGE <value>
1.13.79. **VCCA_PLL_USER_VOLTAGE**

Specifies the voltage of the VCCA_PLL power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCA_PLL_USER_VOLTAGE <value>
```
1.13.80. VCCA_R_USER_VOLTAGE

Specifications the default voltage of the VCCA_R power rail supply, which is applied if all transceivers on the right side of the device are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

**Type**
- String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
- The value of this assignment is case sensitive.
- This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCA_R_USER_VOLTAGE <value>
```
1.13.81. VCCA_USER_VOLTAGE

Specifications the voltage of the VCCA power rail supply. For devices in the Arria II family, this voltage is applied if the transceivers are powered. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCA_USER_VOLTAGE <value>
```
1.13.82. **VCCBAT_USER_VOLTAGE**

Specifies the voltage of the VCCBAT power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCBAT_USER_VOLTAGE <value>
```
1.13.83. VCCCB_USER_VOLTAGE

Specifies the voltage of the VCCCB power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCCB_USER_VOLTAGE <value>
```
1.13.84. VCCD_FPLL_USER_VOLTAGE

Specifies the voltage of the VCCD_FPLL power rail supply. Refer to the device datasheet for the current device family for more details.

Type
String

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name VCCD_FPLL_USER_VOLTAGE <value>
```
1.13.85. VCCD_PLL_USER_VOLTAGE

Specifies the voltage of the VCCD_PLL power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCD_PLL_USER_VOLTAGE <value>
```
1.13.86. VCCD_USER_VOLTAGE

Specifies the voltage of the VCCD power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCD_USER_VOLTAGE <value>
```
1.13.87. VCCEH_GXBL_USER_VOLTAGE

Specifies the default voltage of the VCCEH_GXBL power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

Type

String

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name VCCEH_GXBL_USER_VOLTAGE <value>
```
1.13.88. VCCEH_GXBR_USER_VOLTAGE

Specifies the default voltage of the VCCEH_GXBR power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name VCCEH_GXBR_USER_VOLTAGE <value>
```
1.13.89. VCCEH_GXB_USER_VOLTAGE

Specifies the default voltage of the VCCEH_GXB power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCEH_GXB_USER_VOLTAGE <value>
```
1.13.90. **VCCERAM_USER_VOLTAGE**

Specifies the voltage of the VCCERAM power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCERAM_USER_VOLTAGE <value>
```
1.13.91. VCCE_GXBL_USER_VOLTAGE

Specifies the default voltage of the VCCE_GXBL power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name VCCE_GXBL_USER_VOLTAGE <value>
```

1.13.92. VCCE_GXBR_USER_VOLTAGE

Specifies the default voltage of the VCCE_GXBR power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```shell
set_global_assignment -name VCCE_GXBR_USER_VOLTAGE <value>
```
1.13.93. VCCE_GXB_USER_VOLTAGE

Specifies the default voltage of the VCCE_GXB power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name VCCE_GXB_USER_VOLTAGE <value>
```
1.13.94. VCCE_USER_VOLTAGE

Specifies the voltage of the VCCE power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCE_USER_VOLTAGE <value>
```
1.13.95. VCCHIP_L_USER_VOLTAGE

Specifies the voltage of the VCCHIP_L power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCHIP_L_USER_VOLTAGE <value>
```
1.13.96. VCCHIP_R_USER_VOLTAGE

Specifies the voltage of the VCCHIP_R power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name VCCHIP_R_USER_VOLTAGE <value>
```
1.13.97. VCCHIP_USER_VOLTAGE

Specifies the voltage of the VCCHIP power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name VCCHIP_USER_VOLTAGE <value>
```
1.13.98. VCCHSSI_L_USER_VOLTAGE

Specifies the voltage of the VCCHSSI_L power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name VCCHSSI_L_USER_VOLTAGE <value>
```
1.13.99. VCCHSSI_R_USER_VOLTAGE

Specifies the voltage of the VCCHSSI_R power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCHSSI_R_USER_VOLTAGE <value>
```
1.13.100. VCCH_GTBR_USER_VOLTAGE

Specifies the voltage of the VCCH_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

Type
String

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```bash
set_global_assignment -name VCCH_GTBR_USER_VOLTAGE <value>
```
1.13.101. VCCH_GTB_USER_VOLTAGE

Specifies the voltage of the VCCH_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

Type
String

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

set_global_assignment -name VCCH_GTB_USER_VOLTAGE <value>
### 1.13.102. VCCH\_GXBL\_USER\_VOLTAGE

Specifies the default voltage of the VCCH\_GXBL power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```bash
set_global_assignment -name VCCH\_GXBL\_USER\_VOLTAGE <value>
```
1.13.103. VCCH_GXBR_USER_VOLTAGE

Specifies the default voltage of the VCCH_GXBR power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```plaintext
set_global_assignment -name VCCH_GXBR_USER_VOLTAGE <value>
```
1.13.104. VCCH_GXB_USER_VOLTAGE

Specifies the voltage of the VCCH_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name VCCH_GXB_USER_VOLTAGE <value>
```
1.13.105. VCCH_L_USER_VOLTAGE

Specifies the default voltage of the VCCH_L power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCH_L_USER_VOLTAGE <value>
```
1.13.106. VCCH_R_USER_VOLTAGE

Specifies the default voltage of the VCCH_R power rail supplies, which is applied if all transceivers in the corresponding transceiver block are powered and unused. To configure a transceiver for your intended protocol, use the ALTGX MegaWizard. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCH_R_USER_VOLTAGE <value>
```
1.13.107. VCCINT_USER_VOLTAGE

Specifies the voltage of the VCCINT power rail supply. Refer to the device datasheet for the current device family for more details.

Type
String

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name VCCINT_USER_VOLTAGE <value>
```
1.13.108. VCCIOREF_HPS_USER_VOLTAGE

Specifies the voltage of the VCCIOREF_HPS power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCIOREF_HPS_USER_VOLTAGE <value>
```
1.13.109. VCCIO_HPS_USER_VOLTAGE

Specifies the voltage of the VCCIO_HPS power rail supply. Refer to the device datasheet for the current device family for more details.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

set_global_assignment -name VCCIO_HPS_USER_VOLTAGE <value>
### 1.13.110. VCCIO_USER_VOLTAGE

Specifies the voltage of the VCCIO power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name VCCIO_USER_VOLTAGE <value>
```
1.13.111. VCCL_GTBL_USER_VOLTAGE

Specifies the voltage of the VCCL_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCL_GTBL_USER_VOLTAGE <value>
```
1.13.112. VCCL_GTBR_USER_VOLTAGE

Specifies the voltage of the VCCL_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCL_GTBR_USER_VOLTAGE <value>
```
1.13.113. VCCL_GTB_USER_VOLTAGE

Specifies the voltage of the VCCL_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

Type

String

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name VCCL_GTB_USER_VOLTAGE <value>
```
1.13.114. VCCL_GXBL_USER_VOLTAGE

Specifies the voltage of the VCCL_GXBL power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCL_GXBL_USER_VOLTAGE <value>
```
1.13.115. VCCL_GXBR_USER_VOLTAGE

Specifies the voltage of the VCCL_GXBR power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCL_GXBR_USER_VOLTAGE <value>
```
1.13.116. VCCL_GXB_USER_VOLTAGE

Specifies the voltage of the VCCL_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

Type
String

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name VCCL_GXB_USER_VOLTAGE <value>
```
1.13.117. VCCL_HPS_USER_VOLTAGE

Specifies the voltage of the VCCL_HPS power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCL_HPS_USER_VOLTAGE <value>
```
1.13.118. VCCL_USER_VOLTAGE

Specifies the voltage of the VCCL power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCL_USER_VOLTAGE <value>
```
1.13.119. **VCCPD_USER_VOLTAGE**

Specifies the voltage of the VCCPD power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCPD_USER_VOLTAGE <value>
```
1.13.120. VCCPGM_USER_VOLTAGE

Specifies the voltage of the VCCPGM power rail supply. Refer to the device datasheet for the current device family for more details.

Type
String

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```bash
set_global_assignment -name VCCPGM_USER_VOLTAGE <value>
```
1.13.121. **VCCPLL_HPS_USER_VOLTAGE**

Specifies the voltage of the VCCPLL_HPS power rail supply. For more information, refer to the respective device datasheet.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCPLL_HPS_USER_VOLTAGE <value>
```
1.13.122. VCCPT_USER_VOLTAGE

Specifies the voltage of the VCCPT power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCPT_USER_VOLTAGE <value>
```
1.13.123. VCCP_USER_VOLTAGE

Specifies the voltage of the VCCP power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCP_USER_VOLTAGE <value>
```
1.13.124. **VCCRSTCLK_HPS_USER_VOLTAGE**

Specifies the voltage of the VCCRSTCLK_HPS power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCRSTCLK_HPS_USER_VOLTAGE <value>
```
1.13.125. VCCR_GTBL_USER_VOLTAGE

Specifies the voltage of the VCCR_GTBl power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCR_GTBL_USER_VOLTAGE <value>
```
1.13.126. VCCR_GTBR_USER_VOLTAGE

Specifies the voltage of the VCCR_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name VCCR_GTBR_USER_VOLTAGE <value>
```
1.13.127. **VCCR_GTB_USER_VOLTAGE**

Specifies the voltage of the VCCR_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCR_GTB_USER_VOLTAGE <value>
```
1.13.128. VCCR_GXBL_USER_VOLTAGE

Specifies the voltage of the VCCR_GXBL power rail supply. Refer to the device datasheet for the current device family for more details.

Type
String

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```sh
set_global_assignment -name VCCR_GXBL_USER_VOLTAGE <value>
```
1.13.129. VCCR_GXBR_USER_VOLTAGE

Specifies the voltage of the VCCR_GXBR power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCR_GXBR_USER_VOLTAGE <value>
```
1.13.130. VCCR_GXB_USER_VOLTAGE

Specifies the voltage of the VCCR_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCR_GXB_USER_VOLTAGE <value>
```
1.13.131. VCCR_L_USER_VOLTAGE

Specifies the voltage of the VCCR_L power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive. This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCR_L_USER_VOLTAGE <value>
```
1.13.132. VCCR_R_USER_VOLTAGE

Specifies the voltage of the VCC\textsubscript{R} power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCR_R_USER_VOLTAGE <value>
```
1.13.133. VCCR_USER_VOLTAGE

Specifies the voltage of the VCCR power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCR_USER_VOLTAGE <value>
```
1.13.134. VCCT_GTBL_USER_VOLTAGE

Specifies the voltage of the VCCT_GTBL power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name VCCT_GTBL_USER_VOLTAGE <value>
```
1.13.135. VCCT_GTBR_USER_VOLTAGE

Specifies the voltage of the VCCT_GTBR power rail supply. Refer to the device datasheet for the current device family for more details.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```set_global_assignment -name VCCT_GTBR_USER_VOLTAGE <value>```
1.13.136. VCCT_GTB_USER_VOLTAGE

Specifies the voltage of the VCCT_GTB power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCT_GTB_USER_VOLTAGE <value>
```
1.13.137. VCCT_GXBL_USER_VOLTAGE

Specifies the voltage of the VCCT_GXBL power rail supply. Refer to the device datasheet for the current device family for more details.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name VCCT_GXBL_USER_VOLTAGE <value>
```
1.13.138. VCCT_GXBR_USER_VOLTAGE

Specifies the voltage of the VCCT_GXBR power rail supply. Refer to the device datasheet for the current device family for more details.

Type

String

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Notes

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name VCCT_GXBR_USER_VOLTAGE <value>
```
1.13.139. **VCCT_GXB_USER_VOLTAGE**

Specifies the voltage of the VCCT_GXB power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCT_GXB_USER_VOLTAGE <value>
```
1.13.140. VCCT_L_USER_VOLTAGE

Specifies the voltage of the VCCT_L power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name VCCT_L_USER_VOLTAGE <value>
```
1.13.141. VCCT_R_USER_VOLTAGE

Specifies the voltage of the VCCT_R power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCT_R_USER_VOLTAGE <value>
```
1.13.142. VCCT_USER_VOLTAGE

Specifies the voltage of the VCCT power rail supply. Refer to the device datasheet for the current device family for more details.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCCT_USER_VOLTAGE <value>
```
### 1.13.143. **VCC_HPS_USER_VOLTAGE**

Specifies the voltage of the VCC_HPS power rail supply. For more information, refer to the respective device datasheet.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name VCC_HPS_USER_VOLTAGE <value>
```
1.13.144. VCC_USER_VOLTAGE

Specifies the voltage of the VCC power rail supply. Refer to the device datasheet for the current device family for more details.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name VCC_USER_VOLTAGE <value>
```
1.14. Programmer Assignments

1.14.1. GENERATE_CONFIG_HEXOUT_FILE

Generates a Hexadecimal (Intel-format) Output File (.hexout) containing configuration data that can be programmed into a parallel data source, such as an EPROM or a mass storage device, which then in turn configures the target device.

**Type**

Boolean

**Device Support**

- Enhanced Configuration Devices

**Notes**

None

**Syntax**

```plaintext
set_global_assignment -name GENERATE_CONFIG_HEXOUT_FILE <value>
```

**Default Value**

Off
1.14.2. GENERATE_CONFIG_ISC_FILE

Generates an In System Configuration File (.isc) containing configuration data that an intelligent external controller can use to configure the target device.

Type
Boolean

Device Support
• Enhanced Configuration Devices

Notes
None

Syntax

```
set_global_assignment -name GENERATE_CONFIG_ISC_FILE <value>
```

Default Value
Off
1.14.3. GENERATE_CONFIG_JAM_FILE

Generate a JEDEC STAPL Format File (.jam) containing configuration data that an intelligent external controller can use to configure the target device.

**Type**

Boolean

**Device Support**

- EPC2
- Enhanced Configuration Devices

**Notes**

None

**Syntax**

```
set_global_assignment -name GENERATE_CONFIG_JAM_FILE <value>
```

**Default Value**

Off
1.14.4. GENERATE_CONFIG_JBC_FILE

Generate a compressed Jam STAPL Byte Code 2.0 File (.jbc) containing configuration data that an intelligent external controller can use to configure the target device.

**Type**
Boolean

**Device Support**
- EPC2
- Enhanced Configuration Devices

**Notes**
None

**Syntax**

```text
set_global_assignment -name GENERATE_CONFIG_JBC_FILE <value>
```

**Default Value**
Off
1.14.5. GENERATE_CONFIG_JBC_FILE_COMPRESSED

Generate a compressed Jam STAPL Byte Code 2.0 File (.jbc) containing configuration data that an intelligent external controller can use to configure the target device.

Type
Boolean

Device Support
- EPC2
- Enhanced Configuration Devices

Notes
None

Syntax
set_global_assignment -name GENERATE_CONFIG_JBC_FILE_COMPRESSED <value>

Default Value
On
1.14.6. GENERATE_CONFIG_SVF_FILE

Generates a Serial Vector Format File (.svf) containing configuration data that an intelligent external controller can use to configure the target device.

Type
Boolean

Device Support
- EPC2
- Enhanced Configuration Devices

Notes
None

Syntax

```
set_global_assignment -name GENERATE_CONFIG_SVF_FILE <value>
```

Default Value
Off
1.14.7. GENERATE_JAM_FILE

Directs the programmer to generate a JEDEC JESD71 STAPL Format File (.jam) containing configuration data that an intelligent external controller can use to configure the target device.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

None

**Syntax**

```
set_global_assignment -name GENERATE_JAM_FILE <value>
```

**Default Value**

Off
1.14.8. GENERATE_JBC_FILE

Directs the programmer to generate a compressed JAM Byte Code File (.jbc) containing configuration data that an intelligent external controller can use to configure the target device.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

None

**Syntax**

```
set_global_assignment -name GENERATE_JBC_FILE <value>
```

**Default Value**

Off
1.14.9. GENERATE_JBC_FILE_COMPRESSED

Generate a compressed JAM Byte Code File (.jbc) containing configuration data that an intelligent external controller can use to configure the target device.

**Type**
Boolean

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**
None

**Syntax**

```plaintext
set_global_assignment -name GENERATE_JBC_FILE_COMPRESSED <value>
```

**Default Value**
On
1.14.10. GENERATE_SVF_FILE

Directs the programmer to generate a Serial Vector Format File (.svf) containing configuration data that an intelligent external controller can use to configure the target device.

**Type**
Boolean

**Device Support**
- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**
None

**Syntax**

```
set_global_assignment -name GENERATE_SVF_FILE <value>
```

**Default Value**
Off
1.14.11. HPS_EARLY_IO_RELEASE

Release the HPS shared I/O bank after the IOCSR programming

**Type**

Boolean

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```text
set_global_assignment -name HPS_EARLY_IO_RELEASE <value>
```

**Default Value**

Off
1.14.12. MERGE_HEX_FILE

Uses the Hexadecimal (Intel-Format) File (.hex) and the programmable logic Partial SRAM Object File (.psof) to create passive programming files.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```plaintext
set_global_assignment -name MERGE_HEX_FILE <value>
```

**Default Value**

Off
1.15. Project-Wide Assignments

1.15.1. AHDL_FILE

Associates an AHDL source file with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name AHDL_FILE <value>
```
1.15.2. **AHDL_TEXT_DESIGN_OUTPUT_FILE**

Associates an AHDL Text Design Output File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name AHDL_TEXT_DESIGN_OUTPUT_FILE <value>
```
1.15.3. ALLOW_DSP_RETIMING

Allow retiming through DSP blocks.

Type

Boolean

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name ALLOW_DSP_RETIMING <value>
```

Default Value

Off
1.15.4. ALLOW_RAM_RETIMING

Allow retiming through RAM blocks.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ALLOW_RAM_RETIMING <value>
```

**Default Value**
Off
1.15.5. ASM_FILE

Associates an Assembly source file with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name ASM_FILE <value>
```
1.15.6. AUTO_EXPORT_VER_COMPATIBLE_DB

Automatically exports version-compatible database files when compilation completes.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is not copied when you create a companion revision for HardCopy II devices.

**Syntax**

```plaintext
set_global_assignment -name AUTO_EXPORT_VER_COMPATIBLE_DB <value>
```

**Default Value**

Off
1.15.7. BASE_REVISION_PROJECT_OUTPUT_DIRECTORY

Specifies the directory where project output files such as the Text-Format Report Files (.rpt) and Equation Files (.eqn) were saved for the base revision. By default, all project output files are saved in the project directory.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name BASE_REVISION_PROJECT_OUTPUT_DIRECTORY <value>
```
1.15.8. BDF_FILE

Associates a Block Design File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name BDF_FILE <value>
```
1.15.9. BINARY_FILE

Associates a binary file with this project.

Type
File name

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```plaintext
set_global_assignment -name BINARY_FILE <value>
```
1.15.10. BSF_FILE

Associates a Block Symbol File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name BSF_FILE <value>
```
1.15.11. CDC_MISC_FILE

Associates a CDC file with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name CDC_MISC_FILE <value>
```
1.15.12. CDC_SYSTEMVERILOG_FILE

Associates a CDC SystemVerilog HDL source file with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name CDC_SYSTEMVERILOG_FILE <value>
```
1.15.13. CDC_VERILOG_FILE

Associates a CDC Verilog HDL source file with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name CDC_VERILOG_FILE <value>
```
## 1.15.14. CDF_FILE

Associates a Chain Description File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name CDF_FILE <value>
```
1.15.15. COMMAND_MACRO_FILE

Associates a script file or ModelSim Macro File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name COMMAND_MACRO_FILE <value>
```
1.15.16. CPP_FILE

Associates a C++ source file with this project.

Type
File name

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name CPP_FILE <value>
```
1.15.17.CPP_INCLUDE_FILE

Associates a C++ include file with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name CPP_INCLUDE_FILE <value>
```
1.15.18. CUSP_FILE

Associates a C++ source file with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name CUSP_FILE <value>
```
1.15.19. C_FILE

Associates a C source file with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name C_FILE <value>
```
1.15.20. DEPENDENCY_FILE

Associates a Dependency file with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name DEPENDENCY_FILE <value>
```
1.15.21. DESIGN_ASSISTANT_INCLUDE_IP_BLOCKS

Choose whether IP blocks and their contents should be considered by Design Assistant rule checks, when they are inside a scope that is not excluded by a DESIGN_ASSISTANT_EXCLUDE assignment.

Old Name
DESIGN_ASISTANT_INCLUDE_IP_BLOCKS

Type
Boolean

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name DESIGN_ASSISTANT_INCLUDE_IP_BLOCKS <value>
```

Default Value
Off
1.15.22. DESIGN_ASSISTANT_MAX_VIOLATIONS_PER_RULE

The maximum number of rule violation messages generated by Design Assistant for each rule.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name DESIGN_ASSISTANT_MAX_VIOLATIONS_PER_RULE <value>
```

**Default Value**

5000
1.15.23. DESIGN_ASSISTANT_WAIVER_FILE

Waiver file for Design Assistant rule checker

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name DESIGN_ASSISTANT_WAIVER_FILE <value>
```

**Default Value**

da_drc.dawf
1.15.24. **DRC_RAM_INFERENCE_HIGH_FANOUT_NET_THRESHOLD**

Specifies the number of fanout for a net to be considered as a high fanout net in RAM inference.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name DRC_RAM_INFERENCE_HIGH_FANOUT_NET_THRESHOLD <value>
```

**Default Value**

15
1.15.25. DSPBUILDER_FILE

Associates a DSPBuilder source file with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name DSPBUILDER_FILE <value>
```
1.15.26. EDIF_FILE

Associates an EDIF source file with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name EDIF_FILE <value>
```
1.15.27. ELF_FILE

Associates an ELF file with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```bash
set_global_assignment -name ELF_FILE <value>
```
1.15.28. ENABLE_COMPACT_REPORT_TABLE

Allows you to view the report table in compact format.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```bash
set_global_assignment -name ENABLE_COMPACT_REPORT_TABLE <value>
```

**Default Value**

Off
1.15.29. ENABLE_FIT_RPTRESOURCE_BY_ENTITY

Allows Fitter Resource Utilization by Entity table to be visible in the fitter reports.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**
```
set_global_assignment -name ENABLE_FIT_RPTRESOURCE_BY_ENTITY <value>
```

**Default Value**
Off
1.15.30. ENABLE_REDUCED_MEMORY_MODE

Determine whether to enable compiler to run in reduced memory mode. This assignment controls a small number of memory-intensive fitter optimizations. Therefore, enabling the reduced memory mode may slightly impact the performance of your design.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```plaintext
set_global_assignment -name ENABLE_REDUCED_MEMORY_MODE <value>
```

**Default Value**

Off
1.15.31. EQUATION_FILE

Associates an Equation File with this project.

Type
File name

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

set_global_assignment -name EQUATION_FILE <value>
1.15.32. ERROR_ON_INVALID_ENTITY_NAME

Issue an error instead of a warning if an invalid TOP_LEVEL_ENTITY value or entity field on an instance assignment is found.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```plaintext
set_global_assignment -name ERROR_ON_INVALID_ENTITY_NAME <value>
```

**Default Value**

Off
1.15.33. EXPORT_PARTITION_SNAPSHOT_FINAL

Export specific partition(s) for the final snapshot of the design after the fitter

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_instance_assignment -name EXPORT_PARTITION_SNAPSHOT_FINAL -to <to> -entity <entity name> <value>
```
1.15.34. EXPORT_PARTITION_SNAPSHOT_SYNTHESIZED

Export specific partition(s) for the synthesized snapshot of the design after synthesis

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_instance_assignment -name EXPORT_PARTITION_SNAPSHOT_SYNTHESIZED -to <to> -entity <entity name> <value>
```
1.15.35. FLOW_DISABLE_ASSEMBLER

Allows you to turn on or turn off the Assembler during compilation.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name FLOW_DISABLE_ASSEMBLER <value>
```

**Default Value**

Off
1.15.36. FLOW_ENABLE_DESIGN_ASSISTANT

Allows you to run design assistant check during compilation.

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name FLOW_ENABLE_DESIGN_ASSISTANT <value>
```
1.15.37. FLOW_ENABLE_EDA_NETLIST_WRITER

Allows you to turn on or turn off the EDA Netlist Writer during compilation.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name FLOW_ENABLE_EDA_NETLIST_WRITER <value>
```

**Default Value**

Off
1.15.38. FLOW_ENABLE_INTERACTIVE_TIMING_ANALYZER

Allows you to turn on or turn off the interactive Timing Analyzer after compilation.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name FLOW_ENABLE_INTERACTIVE_TIMING_ANALYZER <value>
```

**Default Value**

On
1.15.39. FLOW_ENABLE_IO_ASSIGNMENT_ANALYSIS

Allows you to run I/O assignment analysis before compilation

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name FLOW_ENABLE_IO_ASSIGNMENT_ANALYSIS <value>
```

**Default Value**

Off
1.15.40. FLOW_ENABLE_PARALLEL_MODULES

Allows you to run Assembler and the Timing Analyzer in parallel during compilation.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name FLOW_ENABLE_PARALLEL_MODULES <value>
```

**Default Value**
On
1.15.41. FLOW_ENABLE_POWER_ANALYZER

Allows you to turn on or turn off the Power Analyzer during compilation.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name FLOW_ENABLE_POWER_ANALYZER <value>
```

**Default Value**

Off
1.15.42. FLOW_ENABLE_RTL_VIEWER

Allows the Netlist Viewers to process the schematic during design compilation. Turning on this option reduces the time required to open the Netlist Viewers at the expense of increased compilation time.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name FLOW_ENABLE_RTL_VIEWER <value>
```

**Default Value**

Off
1.15.43. GDF_FILE

Associates a GDF source file with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_global_assignment -name GDF_FILE <value>
```
1.15.44. HEX_FILE

Associates a Hexadecimal source file with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name HEX_FILE <value>
```
1.15.45. HEX_OUTPUT_FILE

Associates a Hexadecimal Output File with this project.

Type
File name

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

set_global_assignment -name HEX_OUTPUT_FILE <value>
1.15.46. HPS_ISW_DATA

Hard processor system (HPS) software configuration data.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name HPS_ISW_DATA -entity <entity name> <value>
set_instance_assignment -name HPS_ISW_DATA -to <to> -entity <entity name> <value>
```
1.15.47. HPS_ISW_EMIF

Hard processor system (HPS) EMIF configuration data.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```bash
set_global_assignment -name HPS_ISW_EMIF -entity <entity name> <value>
set_instance_assignment -name HPS_ISW_EMIF -to <to> -entity <entity name> <value>
```
1.15.48. HPS_ISW_FILE

Associates a hard processor system (HPS) initial software configuration file with an HPS entity.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name HPS_ISW_FILE -entity <entity name> <value>
set_instance_assignment -name HPS_ISW_FILE -to <to> -entity <entity name> <value>
```
1.15.49. HTML_FILE

Associates an HTML file with this project.

Type
File name

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

set_global_assignment -name HTML_FILE <value>
1.15.50. HTML_REPORT_FILE

Associates an HTML Report File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name HTML_REPORT_FILE <value>
```
1.15.51. INCLUDE_FILE

Associates an Include File with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name INCLUDE_FILE <value>
```
1.15.52. INVALID_DESIGN_SOURCE

Design source files contain invalid settings. Assembler and database export are disallowed.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name INVALID_DESIGN_SOURCE <value>
```

**Default Value**

Off
1.15.53. IPX_FILE

Associates a Quartus Prime IP-XACT description file with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name IPX_FILE <value>
```
1.15.54. IP_COMPONENT_AUTHOR

Specifies the IP component author

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name IP_COMPONENT_AUTHOR <value>
set_global_assignment -name IP_COMPONENT_AUTHOR -entity <entity name> <value>
set_instance_assignment -name IP_COMPONENT_AUTHOR -to <to> -entity <entity name> <value>
```
1.15.55. IP_COMPONENT_DESCRIPTION

Specifies the IP component description

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name IP_COMPONENT_DESCRIPTION <value>
set_global_assignment -name IP_COMPONENT_DESCRIPTION -entity <entity name> <value>
set_instance_assignment -name IP_COMPONENT_DESCRIPTION -to <to> -entity <entity name> <value>
```
1.15.56. IP_COMPONENT_DISPLAY_NAME

Specifies the IP component display name

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name IP_COMPONENT_DISPLAY_NAME <value>
set_global_assignment -name IP_COMPONENT_DISPLAY_NAME -entity <entity name> <value>
set_instance_assignment -name IP_COMPONENTDISPLAY_NAME -to <to> -entity <entity name> <value>
```
1.15.57. IP_COMPONENT_DOCUMENTATION_LINK

Specifies a documentation link for the IP component

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name IP_COMPONENT_DOCUMENTATION_LINK <value>
set_global_assignment -name IP_COMPONENT_DOCUMENTATION_LINK -entity <entity name> <value>
set_instance_assignment -name IP_COMPONENT_DOCUMENTATION_LINK -to <to> -entity <entity name> <value>
```
1.15.58. IP_COMPONENT_GROUP

Specifies the group in the Component Library that includes this IP component

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_global_assignment -name IP_COMPONENT_GROUP <value>
set_global_assignment -name IP_COMPONENT_GROUP -entity <entity name> <value>
set_instance_assignment -name IP_COMPONENT_GROUP -to <to> -entity <entity name> <value>
```
1.15.59. IP_COMPONENT_INTERNAL

Specifies if the IP is an internal component.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

**Syntax**

```
set_global_assignment -name IP_COMPONENT_INTERNAL <value>
set_global_assignment -name IP_COMPONENT_INTERNAL -entity <entity name> <value>
set_instance_assignment -name IP_COMPONENT_INTERNAL -to <to> -entity <entity name> <value>
```

**Default Value**

Off
1.15.60. IP_COMPONENT_NAME

Specifies the IP component name

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

set_global_assignment -name IP_COMPONENT_NAME <value>
set_global_assignment -name IP_COMPONENT_NAME -entity <entity name> <value>
set_instance_assignment -name IP_COMPONENT_NAME -to <to> -entity <entity name> <value>
1.15.61. IP_COMPONENT_PARAMETER

Specifies the parameter, value, and display name of an IP component parameter

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_global_assignment -name IP_COMPONENT_PARAMETER <value>
set_global_assignment -name IP_COMPONENT_PARAMETER -entity <entity name> <value>
set_instance_assignment -name IP_COMPONENT_PARAMETER -to <to> -entity <entity name> <value>
```
1.15.62. IP_COMPONENT_REPORT_HIERARCHY

Specifies the if the IP component should report its hierarchy

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

**Syntax**

```plaintext
set_global_assignment -name IP_COMPONENT_REPORT_HIERARCHY <value>
set_global_assignment -name IP_COMPONENT_REPORT_HIERARCHY -entity <entity name> <value>
set_instance_assignment -name IP_COMPONENT_REPORT_HIERARCHY -to <to> -entity <entity name> <value>
```

**Default Value**

Off
1.15.63. IP_COMPONENT_VERSION

Specifies the IP component version

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name IP_COMPONENT_VERSION <value>
set_global_assignment -name IP_COMPONENT_VERSION -entity <entity name> <value>
set_instance_assignment -name IP_COMPONENT_VERSION -to <to> -entity <entity name> <value>
```
1.15.64. IP_FILE

Associates a Qsys IP file (.ip) with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name IP_FILE <value>
```
1.15.65. IP_GENERATED_DEVICE_FAMILY

Specifies the device families for which the IP core was generated for.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_global_assignment -name IP_GENERATED_DEVICE_FAMILY <value>
set_global_assignment -name IP_GENERATED_DEVICE_FAMILY -entity <entity name> <value>
set_instance_assignment -name IP_GENERATED_DEVICE_FAMILY -to <to> -entity <entity name> <value>
```
1.15.66. IP_QSYS_MODE

Mode used to generate a QIP

Type
String

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```text
set_global_assignment -name IP_QSYS_MODE <value>
set_global_assignment -name IP_QSYS_MODE -entity <entity name> <value>
set_instance_assignment -name IP_QSYS_MODE -to <to> -entity <entity name> <value>
```
1.15.67. IP_TARGETEDDEVICE_FAMILY

Specifies the device family for which the IP core was targeted.

Type

String

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Notes

The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name IP_TARGETEDDEVICE_FAMILY <value>
set_global_assignment -name IP_TARGETEDDEVICE_FAMILY -entity <entity name> <value>
set_instance_assignment -name IP_TARGETEDDEVICE_FAMILY -to <to> -entity <entity name> <value>
```
1.15.68. **IP_TARGETED_PART_TRAIT**

Specifies a part trait for which IP core was targeted.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name IP_TARGETED_PART_TRAIT <value>
set_global_assignment -name IP_TARGETED_PART_TRAIT -entity <entity name> <value>
set_instance_assignment -name IP_TARGETED_PART_TRAIT -to <to> -entity <entity name> <value>
```
1.15.69. IP_TOOL_ENV

Specifies the tool which generated the IP core.

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name IP_TOOL_ENV <value>
set_global_assignment -name IP_TOOL_ENV -entity <entity name> <value>
set_instance_assignment -name IP_TOOL_ENV -to <to> -entity <entity name> <value>
```
1.15.70. IP_TOOL_HIERARCHY_LEVELS

Specifies the number of levels of hierarchy from the IP root.

Type
Integer

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```plaintext
set_global_assignment -name IP_TOOL_HIERARCHY_LEVELS <value>
set_global_assignment -name IP_TOOL_HIERARCHY_LEVELS -entity <entity name> <value>
set_instance_assignment -name IP_TOOL_HIERARCHY_LEVELS -to <to> -entity <entity name> <value>
```
1.15.71. IP_TOOL_NAME

Specifies the IP core name.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_global_assignment -name IP_TOOL_NAME <value>
set_global_assignment -name IP_TOOL_NAME -entity <entity name> <value>
set_instance_assignment -name IP_TOOL_NAME -to <to> -entity <entity name> <value>
```
1.15.72. IP_TOOL_VENDOR_NAME

Specifies the IP core vendor name

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name IP_TOOL_VENDOR_NAME <value>
set_global_assignment -name IP_TOOL_VENDOR_NAME -entity <entity name> <value>
set_instance_assignment -name IP_TOOL_VENDOR_NAME -to <to> -entity <entity name> <value>
```
1.15.73. IP_TOOL_VERSION

Specifies the IP core version

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```bash
set_global_assignment -name IP_TOOL_VERSION <value>
set_global_assignment -name IP_TOOL_VERSION -entity <entity name> <value>
set_instance_assignment -name IP_TOOL_VERSION -to <to> -entity <entity name> <value>
```
1.15.74. **IP_TOOL_VERSION_CREATED**

Specifies the IP core version used when created

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name IP_TOOL_VERSION_CREATED <value>
set_global_assignment -name IP_TOOL_VERSION_CREATED -entity <entity name> <value>
set_instance_assignment -name IP_TOOL_VERSION_CREATED -to <to> -entity <entity name> <value>
```
1.15.75. IP_TOP_LEVEL_COMPONENT_NAME

Specifies the top-level component name in a QIP or SIP file

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_global_assignment -name IP_TOP_LEVEL_COMPONENT_NAME <value>
set_global_assignment -name IP_TOP_LEVEL_COMPONENT_NAME -entity <entity name> <value>
set_instance_assignment -name IP_TOP_LEVEL_COMPONENT_NAME -to <to> -entity <entity name> <value>
```
1.15.76. IP_TOP_LEVEL_ENTITY_NAME

Specifies the top-level entity name in a QIP or SIP file

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_global_assignment -name IP_TOP_LEVEL_ENTITY_NAME <value>
set_global_assignment -name IP_TOP_LEVEL_ENTITY_NAME -entity <entity name> <value>
set_instance_assignment -name IP_TOP_LEVEL_ENTITY_NAME -to <to> -entity <entity name> <value>
```
1.15.77. JAM_FILE

Associates a Jam File with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name JAM_FILE <value>
```
1.15.78. JBC_FILE

Associates a Jam Byte-Code File with this project.

Type

File name

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Notes

The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name JBC_FILE <value>
```
1.15.79. LICENSE_FILE

Associates a License File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name LICENSE_FILE <value>
```
1.15.80. LMF_FILE

Associates a Library Mapping File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name LMF_FILE <value>
```
1.15.81. LOGIC_ANALYZER_INTERFACE_FILE

Associates a Logic Analyzer Interface file with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name LOGIC_ANALYZER_INTERFACE_FILE <value>
```
1.15.82. MAP_FILE

EPC16 addresses used

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name MAP_FILE <value>
```
1.15.83. MAX_IGNORED_ASGN_MSG

Allows you to specify the maximum number of ignored assignment info messages in read-only partitions. Use -1 for unlimited.

Type

Integer

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Notes

None

Syntax

```
set_global_assignment -name MAX_IGNORED_ASGN_MSG <value>
```

Default Value

10
1.15.84. MESSAGE_DISABLE

Tells the compiler to suppress the specified user message(s).

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment supports Fitter wildcards.

This assignment supports synthesis wildcards.

**Syntax**

```plaintext
set_global_assignment -name MESSAGE_DISABLE <value>
set_global_assignment -name MESSAGE_DISABLE -entity <entity name> <value>
set_instance_assignment -name MESSAGE_DISABLE -to <to> -entity <entity name> <value>
```
1.15.85. MESSAGE_ENABLE

Tells the compiler to enable the specified user message(s).

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment supports Fitter wildcards.

This assignment supports synthesis wildcards.

**Syntax**

```plaintext
set_global_assignment -name MESSAGE_ENABLE <value>
set_global_assignment -name MESSAGE_ENABLE -entity <entity name> <value>
set_instance_assignment -name MESSAGE_ENABLE -to <to> -entity <entity name> <value>
```
1.15.86. MIF_FILE

Associates a Memory Initialization File with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name MIF_FILE <value>
```
1.15.87. MISC_FILE

Associates a file with this project. Files assigned to this assignment will be archived by the Project Archive command if the 'Project source and settings files' file subset is selected.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name MISC_FILE <value>
```
1.15.88. NUM_PARALLEL_PROCESSORS

Specifies the maximum number of processors allocated for parallel compilation on a single machine. For parallel compilation you can use all available processors on your machine, or specify the number of processors you want to use. For example, if you have a quad-core processor machine and want to leave one processor free for other tasks, you specify '3' as the setting of this option. A setting of '1' disables parallel compilation.

**Old Name**

MAX_PROCESSORS_USED_FOR_MULTITHREADING

**Type**

String

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name NUM_PARALLEL_PROCESSORS <value>
```
1.15.89. OBJECT_FILE

Associates an Object file with this project.

Type

File name

Device Support

• This setting can be used in projects targeting any Intel FPGA device family.

Notes

The value of this assignment is case sensitive.

Syntax

set_global_assignment -name OBJECT_FILE <value>
1.15.90. OCP_FILE

Specifies the Intel FPGA IP Evaluation Mode file generated by the MegaWizard. This file is used by Quartus to allow compilation and sof generation of the core without a license.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name OCP_FILE <value>
```
1.15.91. PARTIAL_SRAM_OBJECT_FILE

Associates a Partial SRAM Object File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name PARTIAL_SRAM_OBJECT_FILE <value>
```
1.15.92. PIN_FILE

Associates a Pin-Out File with this project.

Type
File name

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```text
set_global_assignment -name PIN_FILE <value>
```
1.15.93. POWER_INPUT_FILE

Associates a Power Input File (.pwf) with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name POWER_INPUT_FILE <value>
```
1.15.94. PPF_FILE

Specifies the name of the MegaWizard generated .ppf file containing core specific pin assignments. This file will be loaded by Pin Planner.

Type
File name

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name PPF_FILE <value>
```
1.15.95. PROGRAMMER_OBJECT_FILE

Associates a Programmer Object File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```bash
set_global_assignment -name PROGRAMMER_OBJECT_FILE <value>
```
### 1.15.96. PROJECT_OUTPUT_DIRECTORY

Specifies the directory in which to save all project output files such as the Text-Format Report Files (.rpt) and Equation Files (.eqn). By default, all project output files are saved in the project directory.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name PROJECT_OUTPUT_DIRECTORY <value>
```
1.15.97. PROJECT_USE_SIMPLIFIED_NAMES

Determines whether to use the simplified naming scheme.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name PROJECT_USE_SIMPLIFIED_NAMES <value>
```

**Default Value**

Off
1.15.98. PROMOTE_WARNING_TO_ERROR

Issue an error if a warning with the given message ID is displayed.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```shell
set_global_assignment -name PROMOTE_WARNING_TO_ERROR <value>
```
1.15.99. QARLOG_FILE

Associates an Archive Log file with this project.

Type
File name

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name QARLOG_FILE <value>
```
1.15.100. QAR_FILE

Associates an Archive file with this project.

Type

File name

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Notes

The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name QAR_FILE <value>
```
1.15.101. QIP_FILE

Associates a Quartus Prime IP file with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```markdown
set_global_assignment -name QIP_FILE <value>
```
1.15.102. QSYS_FILE

Associates a Qsys file (.qsys) with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name QSYS_FILE <value>
```
1.15.103. QUARTUS_PTF_FILE

Associates a Peripheral Template File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name QUARTUS_PTF_FILE <value>
```
1.15.104. QUARTUS_SBD_FILE

Associates a Quartus Prime System Build Descriptor File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name QUARTUS_SBD_FILE <value>
```
1.15.105. QUARTUS_STANDARD_DELAY_FILE

Associates a Quartus Prime Standard Delay Format File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name QUARTUS_STANDARD_DELAY_FILE <value>
```
1.15.106. RAW_BINARY_FILE

Associates a Raw Binary File with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name RAW_BINARY_FILE <value>
```
1.15.107. READ_OR_WRITE_IN_BYTE_ADDRESS

Determines whether to read or write Hexadecimal(.hex) File in byte addressable mode for this project.

**Type**

Enumeration

**Values**

- Off
- On
- Use global settings

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name READ_OR_WRITE_IN_BYTE_ADDRESS <value>
```

**Default Value**

Use global settings
### 1.15.108. REVISION_TYPE

Describes the type of revision. The possible revision types are BASE, RECONFIGURABLE, AGGREGATE, CVP, and MASK. The default type is BASE.

**Type**

Enumeration

**Values**

- PR_Base
- PR_Impl
- PR_Syn

**Device Support**

- Intel Arria 10
- Intel Cyclone 10 GX

**Notes**

None

**Syntax**

```
set_global_assignment -name REVISION_TYPE <value>
```
1.15.109. **RUN_FULL_COMPILE_ON_DEVICE_CHANGE**

Run Full Compilation when the device changes

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name RUN_FULL_COMPILE_ON_DEVICE_CHANGE <value>
```

**Default Value**
On
**1.15.110. SBI_FILE**

Associates a Slave Binary Image File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_global_assignment -name SBI_FILE <value>
```
1.15.111. SDC_ENTITY_FILE

Associates a Synopsys Design Constraint File (.sdc) with an entity.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name SDC_ENTITY_FILE -entity <entity name> <value>
set_instance_assignment -name SDC_ENTITY_FILE -to <to> -entity <entity name> <value>
set_global_assignment -name SDC_ENTITY_FILE <value>
```
1.15.112. SDC_ENTITY_HELPER_FILE

Associates a file "sourced" into a Synopsys Design Constraint File (.sdc) with an entity. Helper files are usually TCL (.tcl) files.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_global_assignment -name SDC_ENTITY_HELPER_FILE -entity <entity name> <value>
set_instance_assignment -name SDC_ENTITY_HELPER_FILE -to <to> -entity <entity name> <value>
set_global_assignment -name SDC_ENTITY_HELPER_FILE <value>
```
1.15.113. SDC_FILE

Associates a Synopsys Design Constraint File (.sdc) with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name SDC_FILE <value>
```
1.15.114. SDF_OUTPUT_FILE

Associates a Standard Delay Format Output File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name SDF_OUTPUT_FILE <value>
```
1.15.115. SERIAL_BITSTREAM_FILE

Associates a Serial Bitstream File with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name SERIAL_BITSTREAM_FILE <value>
```
1.15.116. SIGNALTAP_FILE

Associates a Signal Tap file with this project.

Type
File name

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```plaintext
set_global_assignment -name SIGNALTAP_FILE <value>
```
1.15.117. SIP_FILE

Associates a Simulation IP File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name SIP_FILE <value>
```
1.15.118. SLD_FILE

Associates a file with this project. Files assigned to this assignment will be archived by the Project Archive command if the 'Project source and settings files' file subset is selected.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name SLD_FILE <value>
```
1.15.119. SMF_FILE

Associates a State Machine file (.smf) with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name SMF_FILE <value>
```
1.15.120. SOFTWARE_LIBRARY_FILE

Associates a Software library file with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name SOFTWARE_LIBRARY_FILE <value>
```
1.15.121. SOPCINFO_FILE

Associates a Qsys or SOPC Builder report file with this project. If you select the Project source and settings files option, the Project Archive command will archive the files assigned to this assignment.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_global_assignment -name SOPCINFO_FILE <value>
```
1.15.122. SOPC_FILE

Associates a SOPC Builder file (.sopc) with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name SOPC_FILE <value>
```
1.15.123. SOURCE_TCL_SCRIPT_FILE

Runs Tcl script file. This assignment has the same effect as 'source <filename>'.

Type
File name

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name SOURCE_TCL_SCRIPT_FILE <value>
```
1.15.124. SPD_FILE

Associates a Simulation Package Descriptor File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name SPD_FILE <value>
```
1.15.125. SPYGLASS_MISC_FILE

Associates a Spyglass file with this project.

Type
File name

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name SPYGLASS_MISC_FILE <value>
```
1.15.126. **SPYGLASS_SYSTEMVERILOG_FILE**

Associates a Spyglass SystemVerilog HDL source file with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name SPYGLASS_SYSTEMVERILOG_FILE <value>
```
1.15.127. SPYGLASS_VERILOG_FILE

Associates a Spyglass Verilog HDL source file with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name SPYGLASS_VERILOG_FILE <value>
```
1.15.128. SRAM_OBJECT_FILE

Associates an SRAM Object File with this project.

Type
File name

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

set_global_assignment -name SRAM_OBJECT_FILE <value>
1.15.129. SRECORDS_FILE

Associates a Motorola S-Record file with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_global_assignment -name SRECORDS_FILE <value>
```
1.15.130. SVF_FILE

Associates a Serial Vector Format File with this project.

Type

File name

Device Support

• This setting can be used in projects targeting any Intel FPGA device family.

Notes

The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name SVF_FILE <value>
```
1.15.131. **SYM_FILE**

Associates a Symbol File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_global_assignment -name SYM_FILE <value>
```
1.15.132. SYNTHESIS_ONLY_QIP

Determines whether a Quartus Prime IP File is not for simulation.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name SYNTHESIS_ONLY_QIP <value>
```
1.15.133. SYSTEMVERILOG_FILE

Associates a SystemVerilog HDL source file with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```bash
set_global_assignment -name SYSTEMVERILOG_FILE <value>
```
1.15.134. TCL_ENTITY_FILE

Associates a TCL File (.tcl) with an entity. These files are often "sourced" into Synopsys Design Constraint Files (.sdc) that were also associated with the same entity.

Type
File name

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name TCL_ENTITY_FILE -entity <entity name> <value>
set_instance_assignment -name TCL_ENTITY_FILE -to <to> -entity <entity name> <value>
set_global_assignment -name TCL_ENTITY_FILE <value>
```
1.15.135. TCL_SCRIPT_FILE

Associates a Tcl script file with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name TCL_SCRIPT_FILE <value>
```
1.15.136. TEMPLATE_FILE

Associates a Template File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name TEMPLATE_FILE <value>
```
1.15.137. TEXT_FILE

Associates a text file with this project.

Type
File name

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

set_global_assignment -name TEXT_FILE <value>
1.15.138. TEXT_FORMAT_REPORT_FILE

Associates a text-format Report File with this project.

Type
File name

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name TEXT_FORMAT_REPORT_FILE <value>
```
1.15.139. TIMING_ANALYSIS_OUTPUT_FILE

Associates a Timing Analysis Output File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name TIMING_ANALYSIS_OUTPUT_FILE <value>
```
1.15.140. USE_CHECKERED_PATTERN_AS_UNINITIALIZED_RAM_CONTENT

Loads a checkered pattern as initial RAM content into all RAM blocks without specified RAM content that supports content initialization. Turning on this option does not affect simulation, which may cause on-chip behavior to differ from simulation results.

**Type**

Enumeration

**Values**

- 0000
- 0101
- 1010
- 1111
- OFF
- ON
- RANDOM

**Device Support**

- Intel Agilex
- Intel Arria 10
- Intel Cyclone 10 GX
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name USE_CHECKERED_PATTERN_AS_UNINITIALIZED_RAM_CONTENT <value>
```

**Default Value**

OFF
1.15.141. VCD_FILE

Associates a Verilog Value Change Dump File with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name VCD_FILE <value>
```
1.15.142. VECTOR_TABLE_OUTPUT_FILE

Associates a Vector Table Output File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name VECTOR_TABLE_OUTPUT_FILE <value>
```
1.15.143. VECTOR_TEXT_FILE

Associates a text-format Vector File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name VECTOR_TEXT_FILE <value>
```
1.15.144. VECTOR_WAVEFORM_FILE

Associates a Vector Waveform File with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name VECTOR_WAVEFORM_FILE <value>
```
1.15.145. VERILOG_FILE

Associates a Verilog HDL source file with this project.

Type
File name

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

set_global_assignment -name VERILOG_FILE <value>
1.15.146. VERILOG_INCLUDE_FILE

Associates a Verilog Include file with this project.

**Old Name**
VERILOG_VH_FILE

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name VERILOG_INCLUDE_FILE <value>
```
1.15.147. VERILOG_OUTPUT_FILE

Associates a Verilog Output File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name VERILOG_OUTPUT_FILE <value>
```
1.15.148. VERILOG_TEST_BENCH_FILE

Associates a Verilog HDL Test Bench File (.vt) with this project.

Type
File name

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```
set_global_assignment -name VERILOG_TEST_BENCH_FILE <value>
```
1.15.149. VER_COMPATIBLE_DB_DIR

Specifies the directory to which version-compatible database files should be saved

Type

File name

Device Support

• This setting can be used in projects targeting any Intel FPGA device family.

Notes

The value of this assignment is case sensitive.

This assignment is not copied when you create a companion revision for HardCopy II devices.

Syntax

```
set_global_assignment -name VER_COMPATIBLE_DB_DIR <value>
```

Default Value

export_db
1.15.150. VHDL_FILE

Associates a VHDL source file with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_global_assignment -name VHDL_FILE <value>
```
1.15.151. VHDL_OUTPUT_FILE

Associates a VHDL Output File with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```script
class set_global_assignment -name VHDL_OUTPUT_FILE <value>
```
1.15.152. VHDL_TEST_BENCH_FILE

Associates a VHDL Test Bench File (.vht) with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```python
set_global_assignment -name VHDL_TEST_BENCH_FILE <value>
```
1.15.153. VQM_FILE

Associates a structural Verilog HDL source file with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name VQM_FILE <value>
```
1.15.154. ZIP_VECTOR_WAVEFORM_FILE

Associates a Compressed Vector Waveform File with this project.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name ZIP_VECTOR_WAVEFORM_FILE <value>
```
1.16. Retimer Assignments

1.16.1. HYPER_RETIMER_ADD_PIPELINING

Describes the maximum number of additional registers allowed to be inserted by Auto-Pipelining.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Stratix 10

**INTEGER_RANGE**

0, 100

**Notes**

This assignment supports wildcards.

This assignment is included in the Fitter report.

**Syntax**

```
set_instance_assignment -name HYPER_RETIMER_ADD_PIPELINING -to <to> -entity <entity name> <value>
```
1.16.2. HYPER_RETIMER_ADD_PIPELINING_GROUP

Describes the group name for Auto-Pipelining. Signals in the same group will always have the same number of pipelining stages inserted. Signals without a group assignment will be automatically assigned a group tied to its parent instance.

**Type**
String

**Device Support**
- Intel Agilex
- Intel Stratix 10

**Notes**
This assignment supports wildcards.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name HYPER_RETIMER_ADD_PIPELINING_GROUP <value>
set_instance_assignment -name HYPER_RETIMER_ADD_PIPELINING_GROUP -to <to> -entity <entity name> <value>
```
1.16.3. HYPER_RETIMER_ENABLE_ADD_PIPELINING

Turns on the Auto-Pipelining and Latency-Insensitive False Path feature. For Auto-Pipelining, use in conjunction with assignment "Maximum Additional Pipelining" and optionally "Additional Pipelining Group".

**Type**
Boolean

**Device Support**
- Intel Agilex
- Intel Stratix 10

**Notes**
This assignment supports wildcards.
This assignment is included in the Fitter report.

**Syntax**
```
set_global_assignment -name HYPER_RETIMER_ENABLE_ADD_PIPELINING <value>
```

**Default Value**
On
1.16.4. HYPER_RETIMER_FAST_FORWARD_ADD_PIPELINING_MAX

Set the maximum number of additional pipeline stages that the Fast Forward Compilation flow may explore.

**Type**

Integer

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment supports wildcards.

This assignment is included in the Fitter report.

**Syntax**

```plaintext
set_global_assignment -name HYPER_RETIMER_FAST_FORWARD_ADD_PIPELINING_MAX <value>
set_instance_assignment -name HYPER_RETIMER_FAST_FORWARD_ADD_PIPELINING_MAX -to <to> -entity <entity name> <value>
```

**Default Value**

-1
1.16.5. HYPER RETIMER FAST FORWARD ASYNCH CLEAR

Control how Fast Forward Compile handles registers with asynchronous clear signals.

**Type**
Enumeration

**Values**
- Auto
- Preserve

**Device Support**
- Intel Agilex
- Intel Stratix 10

**Notes**
This assignment supports wildcards.
This assignment is included in the Fitter report.

**Syntax**
```plaintext
set_global_assignment -name HYPER_RETIMER_FAST_FORWARD_ASYNCH_CLEAR <value>
set_instance_assignment -name HYPER_RETIMER_FAST_FORWARD_ASYNCH_CLEAR -to <to> -entity <entity name> <value>
```

**Default Value**
Auto
1.16.6. HYPER_RETIMER_FAST_FORWARD_DSP_BLOCKS

Fast Forward Compile will analyze DSP blocks that are limiting performance and assume that they can be fully registered.

Type
Boolean

Device Support
- Intel Agilex
- Intel Stratix 10

Notes
This assignment supports wildcards.
This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name HYPER_RETIMER_FAST_FORWARD_DSP_BLOCKS <value>
set_instance_assignment -name HYPER_RETIMER_FAST_FORWARD_DSP_BLOCKS -to <to> -entity <entity name> <value>
```

Default Value
On
1.16.7. HYPER_RETIMER_FAST_FORWARD_RAM_BLOCKS

Fast Forward Compile will analyze RAM blocks that are limiting performance and assume that they can be fully registered.

Type
Boolean

Device Support
• Intel Agilex
• Intel Stratix 10

Notes
This assignment supports wildcards.

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name HYPER_RETIMER_FAST_FORWARD_RAM_BLOCKS <value>
set_instance_assignment -name HYPER_RETIMER_FAST_FORWARD_RAM_BLOCKS -to <to> -entity <entity name> <value>
```

Default Value
On
1.16.8. HYPER_RETIMER_FAST_FORWARD_USER_PRESERVE_RESTRICTION

Controls how Fast Forward Compile handles restrictions due to user-preserve directives.

Type

Enumeration

Values

- Auto
- Preserve

Device Support

- Intel Agilex
- Intel Stratix 10

Notes

This assignment supports wildcards.

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name HYPER_RETIMER_FAST_FORWARD_USER_PRESERVE_RESTRICTION <value>
set_instance_assignment -name HYPER_RETIMER_FAST_FORWARD_USER_PRESERVE_RESTRICTION -to <to> -entity <entity name> <value>
```

Default Value

Auto
1.17. Retimer Fast Forward Assignments

1.17.1. CRITICAL_CHAINVIEWER

Enable Critical Chain visualization in the Fast Forward Timing Closure Recommendations report

**Type**

Boolean

**Device Support**

- Intel Agilex
- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name CRITICAL_CHAIN_VIEWER <value>
```

**Default Value**

On
1.17.2. FLOW_ENABLE_HYPER RETIMER_FAST_FORWARD

Allows you to turn on or turn off Fast Forward analysis during compilation.

Old Name

HYPER RETIMER_FAST_FORWARD

Type

Boolean

Device Support

• Intel Agilex
• Intel Stratix 10

Notes

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name FLOW_ENABLE_HYPER RETIMER_FAST_FORWARD <value>
```
1.17.3. HYPER_RETIMER_FAST_FORWARD_CUT_ALL_CLOCK_TRANSFERS

Cut all clock transfers in Fast Forward Compilation flow.

**Type**

Boolean

**Device Support**

- Intel Stratix 10

**Notes**

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name HYPER_RETIMER_FAST_FORWARD_CUT_ALL_CLOCK_TRANSFERS <value>
```

**Default Value**

On
1.17.4. HYPER_RETIMER_FAST_FORWARD_ON_HIERARCHY

Enables you to run or ignore Fast Forward analysis on specific instances of a design. Partitions are suggested on instances targeted by this feature to prevent optimizations across boundaries. If using without boundaries this feature will provide a best effort suggestion with potential cross-hierarchy optimizations.

Type

Boolean

Device Support

- Intel Agilex
- Intel Stratix 10

Notes

This assignment supports wildcards.

This assignment is included in the Fitter report.

Syntax

```
set_global_assignment -name HYPER_RETIMER_FAST_FORWARD_ON_HIERARCHY <value>
set_instance_assignment -name HYPER_RETIMER_FAST_FORWARD_ON_HIERARCHY -to <to> -entity <entity name> <value>
```
1.18. Signal Tap Assignments

1.18.1. CREATE_PARTITION_BOUNDARY_PORTS

Creates boundary ports on ancestor partition(s) by the specified name

Type

String

Device Support

• This setting can be used in projects targeting any Intel FPGA device family.

Notes

The value of this assignment is case sensitive.

Syntax

set_instance_assignment -name CREATE_PARTITION_BOUNDARY_PORTS -to <to> <value>
1.18.2. ENABLE_LOGIC_ANALYZER_INTERFACE

Enables Logic Analyzer Interface for compilation

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name ENABLE_LOGIC_ANALYZER_INTERFACE <value>
```
1.18.3. ENABLE_SIGNALTAP

   Enables the Signal Tap Logic Analyzer for compilation

   **Type**
   Boolean

   **Device Support**
   • This setting can be used in projects targeting any Intel FPGA device family.

   **Notes**
   This assignment is included in the Fitter report.

   **Syntax**

   ```
   set_global_assignment -name ENABLE_SIGNALTAP <value>
   ```
1.18.4. PRESERVE_FOR_DEBUG

Preserves a signal for debug, will have no effect unless PRESERVE_FOR_DEBUG_ENABLE is set to ON for the project or entity containing the signal.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment supports Fitter wildcards.
This assignment supports synthesis wildcards.

**Syntax**

```plaintext
set_global_assignment -name PRESERVE_FOR_DEBUG -entity <entity name> <value>
set_instance_assignment -name PRESERVE_FOR_DEBUG -to <to> -entity <entity name> <value>
```

**Example**

```plaintext
set_instance_assignment -name preserve_for_debug on -to foo
```
1.18.5. PRESERVE_FOR_DEBUG_ENABLE

Tells the compiler to keep all signals marked as PRESERVE_FOR_DEBUG either project wide or within the specified entity.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment supports Fitter wildcards.
This assignment is included in the Analysis & Synthesis report.
This assignment supports synthesis wildcards.

**Syntax**

```
set_global_assignment -name PRESERVE_FOR_DEBUG_ENABLE <value>
set_global_assignment -name PRESERVE_FOR_DEBUG_ENABLE -entity <entity name> <value>
set_instance_assignment -name PRESERVE_FOR_DEBUG_ENABLE -to <to> -entity <entity name> <value>
```

**Example**

```
set_global_assignment -name preserve_for_debug_enable on
set_instance_assignment -name preserve_for_debug_enable on -to foo
```
1.18.6. STP_FILE

Associates a Signal Tap Logic Analyzer File with this project.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```bash
set_global_assignment -name STP_FILE <value>
```
1.18.7. USE_LOGIC_ANALYZER_INTERFACE_FILE

Specifies the Logic Analyzer Interface File to be used for compilation.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name USE_LOGIC_ANALYZER_INTERFACE_FILE <value>
```
1.18.8. USE_SIGNALTAP_FILE

Specifies the Signal Tap Logic Analyzer File to be used for compilation.

**Type**
File name

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.
This assignment is included in the Fitter report.

**Syntax**

```
set_global_assignment -name USE_SIGNALTAP_FILE <value>
```
1.19. Simulator Assignments

1.19.1. ACTION

Specifies the breakpoint's action when triggered.

**Type**

Enumeration

**Values**

- Give Error
- Give Info
- Give Warning
- Stop

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name ACTION -section_id <section identifier> <value>
```
1.19.2. ADD_DEFAULT_PINS_TO_SIMULATION_OUTPUT_WAVEFORMS

Adds output pins to the simulation vector output waveforms automatically.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name ADD_DEFAULT_PINS_TO_SIMULATION_OUTPUT_WAVEFORMS <value>
```

**Default Value**

On
1.19.3. ADD_TO_SIMULATION_OUTPUT_WAVEFORMS

Adds the signal to the list of signals for which output waveforms are shown in the simulation report. This option makes a node observable during simulation.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```bash
set_instance_assignment -name ADD_TO_SIMULATION_OUTPUT_WAVEFORMS -to <to> -entity <entity name> <value>
```
1.19.4. ALIAS

Specifies an alias for the full hierarchical name of the node.

Type
String

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

```
set_instance_assignment -name ALIAS -to <to> -entity <entity name> <value>
```
1.19.5. AUTO_USE_SIMULATION_PDB_NETLIST

Automatically saves/loads simulation netlist to/from external file

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name AUTO_USE_SIMULATION_PDB_NETLIST <value>
```

**Default Value**

Off
1.19.6. BREAKPOINT_STATE

Specifies the state of a breakpoint as either enabled or disabled.

Type

Enumeration

Values

- Disabled
- Enabled

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```
set_global_assignment -name BREAKPOINT_STATE -section_id <section identifier> <value>
```
1.19.7. CHECK_OUTPUTS

Checks expected outputs vs. actual outputs in the simulation report.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name CHECK_OUTPUTS <value>
```

**Default Value**

Off
1.19.8. END_TIME

Specifies the end time for simulation.

Type
Time

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
None

Syntax

```
set_global_assignment -name END_TIME <value>
```
1.19.9. EXTERNAL_PIN_CONNECTION

Specifies an external pin connection between an output pin and an input pin. This option is used during simulations only.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_instance_assignment -name EXTERNAL_PIN_CONNECTION -to <to> -entity <entity name> <value>
```
1.19.10. GLITCH_DETECTION

Monitors the design for user-defined glitches (spikes).

Type
Boolean

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Notes
None

Syntax

set_global_assignment -name GLITCH_DETECTION <value>

Default Value
Off
1.19.11. GLITCH_INTERVAL

Allows you to detect glitches and specify the time interval that defines a glitch. If two logic level transitions occur in a period shorter than the specified time period, the resulting glitch is detected and reported in the Processing tab of the Messages window.

Type

Time

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Notes

None

Syntax

```
set_global_assignment -name GLITCH_INTERVAL <value>
```

Default Value

1ns
1.19.12. IMMEDIATE_ASSERTION_FAIL_ACTION

Specifies the immediate assertion's action when the assertion fails.

Type

Enumeration

Values
- Give Error
- Give Info
- Give Warning
- Stop

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```set_global_assignment -name IMMEDIATE_ASSERTION_FAIL_ACTION -section_id <section identifier> <value>```
1.19.13. IMMEDIATE_ASSERTION_FAIL_MESSAGE

Specifies the immediate assertion's message when the assertion fails.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name IMMEDIATE_ASSERTION_FAIL_MESSAGE -section_id <section identifier> <value>
```
1.19.14. IMMEDIATE_ASSERTION_PASS_MESSAGE

Specifies the immediate assertion's message when the assertion passes.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name IMMEDIATE_ASSERTION_PASS_MESSAGE -section_id <section identifier> <value>
```
1.19.15. IMMEDIATE_ASSERTION_STATE

Specifies the state of an immediate assertion as either enabled or disabled.

**Type**

Enumeration

**Values**

- Disabled
- Enabled

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name IMMEDIATE_ASSERTION_STATE -section_id <section_identifier> <value>
```
1.19.16. IMMEDIATE_ASSERTION_TEST_CONDITION

Specifies the immediate assertion's test condition.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```bash
set_global_assignment -name IMMEDIATE_ASSERTION_TEST_CONDITION -section_id <section_identifier> <value>
```
1.19.17. INCREMENTAL_VECTOR_INPUT_SOURCE

Specifies the source of input vectors to be used for simulation.

Type
File name

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Notes
The value of this assignment is case sensitive.

Syntax

set_global_assignment -name INCREMENTAL_VECTOR_INPUT_SOURCE <value>
1.19.18. PASSIVE_RESISTOR

Specifies whether an output or bidirectional pin has a pull-up or pull-down resistor. This option is used in functional simulations only.

**Type**

Enumeration

**Values**

- Pull-down
- Pull-up

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_instance_assignment -name PASSIVE_RESISTOR -to <to> -entity <entity name> <value>
```
1.19.19. SETUP_HOLD_DETECTION

Detects setup and hold time violations.

Type

Boolean

Device Support

• This setting can be used in projects targeting any Intel FPGA device family.

Notes

None

Syntax

set_global_assignment -name SETUP_HOLD_DETECTION <value>

Default Value

Off
1.19.20. SETUP_HOLD_DETECTION_INPUT_REGISTERS_BIDIR_PINS_DISABLED

Disables setup and hold time violations detection in input registers of bi-directional pins.

Type
Boolean

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```
set_global_assignment -name
SETUP_HOLD_DETECTION_INPUT_REGISTERS_BIDIR_PINS_DISABLED <value>
```

Default Value

Off
1.19.21. SETUP_HOLD_TIME_VIOLATION_DETECTION

Enables setup and hold time violation detection during simulation.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_instance_assignment -name SETUP_HOLD_TIME_VIOLATION_DETECTION -to <to> -
entity <entity name> <value>
```
1.19.22. SIMULATION_BUS_CHANNEL_GROUPING

Automatically groups bus channels in the output waveforms which are shown in the simulation report.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name SIMULATION_BUS_CHANNEL_GROUPING <value>
```

**Default Value**

Off
1.9.23. SIMULATION_COMPARE_SIGNAL

Specifies the signal to be compared in a waveform comparison.

Type

Boolean

Device Support

• This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```plaintext
set_instance_assignment -name SIMULATION_COMPARE_SIGNAL -to <to> -entity <entity name> <value>
```
1.19.24. SIMULATIONCOMPLETECOVERAGEREPORT_PANEL

Display report on output ports that toggle between 1 and 0 during simulation.

Type

Boolean

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Syntax

set_global_assignment -name SIMULATIONCOMPLETECOVERAGEREPORT_PANEL <value>

Default Value

On
1.19.25. SIMULATION_COVERAGE

Reports 'coverage,' that is, the ratio of output ports that toggle between 1 and 0 during simulation, compared to the total number of output ports present in the netlist, expressed as a percentage.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```plaintext
set_global_assignment -name SIMULATION_COVERAGE <value>
```

**Default Value**

On
1.19.26. SIMULATION_DEFAULT_VECTORCOMPARE_TOLERANCE

Specifies the default comparison timing tolerance to be used in a waveform comparison.

**Type**
Time

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```plaintext
set_global_assignment -name SIMULATION_DEFAULT_VECTORCOMPARE_TOLERANCE <value>
```
1.19.27. SIMULATION_MISSING_0_VALUE_COVERAGE_REPORT_PANEL

Display report on output ports that do not toggle to 0 during simulation.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name SIMULATION_MISSING_0_VALUE_COVERAGE_REPORT_PANEL <value>
```

**Default Value**

On
1.19.28. SIMULATION_MISSING_1_VALUE_COVERAGE_REPORT_PANEL

Display report on output ports that do not toggle to 1 during simulation.

Type

Boolean

Device Support

- This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```
set_global_assignment -name SIMULATION_MISSING_1_VALUE_COVERAGE_REPORT_PANEL <value>
```

Default Value

On
1.19.29. SIMULATION_MODE

Specifies the type of simulation to perform for the current Simulation focus.

**Type**

Enumeration

**Values**

- Functional
- Timing
- Timing using Fast Timing Model

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name SIMULATION_MODE <value>
```

**Default Value**

TIMING
1.19.30. SIMULATION_NETLIST_VIEWER

Enables the Simulation Netlist Viewer.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```plaintext
set_global_assignment -name SIMULATION_NETLIST_VIEWER <value>
```

**Default Value**

Off
1.19.31. SIMULATION_SIGNAL_COMPARE_TOLERANCE

Specifies the comparison timing tolerance to be used for each signal in a waveform comparison.

**Type**

Time

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_instance_assignment -name SIMULATION_SIGNAL_COMPARE_TOLERANCE -to <to> -entity <entity name> <value>
```
1.19.32. SIMULATION_VDB_RESULT_FLUSH

Flushes signal transitions from memory to disk for memory optimization

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

None

**Syntax**

```
set_global_assignment -name SIMULATION_VDB_RESULT_FLUSH <value>
```

**Default Value**

On

MNL-1088 | 2021.06.21

1.19.33. SIMULATION_VECTOR_COMPARE_BEGIN_TIME

Specifies the begin time at which waveform comparison on simulation results should start.

**Type**

Time

**Device Support**

• This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name SIMULATION_VECTOR_COMPARE_BEGIN_TIME <value>
```
1.19.34. SIMULATION_VECTOR_COMPARE_END_TIME

Specifies the end time at which waveform comparison on simulation results should stop.

**Type**
Time

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```bash
set_global_assignment -name SIMULATION_VECTOR_COMPARE_END_TIME <value>
```
1.19.35. SIMULATION_VECTOR_COMPARE_RULE_FOR_0

Specifies vector values that match with expected strong low value (0) in the waveform file

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name SIMULATION_VECTOR_COMPARE_RULE_FOR_0 <value>
```
1.19.36. SIMULATION_VECTOR_COMPARE_RULE_FOR_1

Specifies vector values that match with expected strong high value (1) in the waveform file

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```bash
set_global_assignment -name SIMULATION_VECTOR_COMPARE_RULE_FOR_1 <value>
```
1.19.37. SIMULATION_VECTOR_COMPARE_RULE_FOR_DC

Specifies vector values that match with expected don't care value (DC) in the waveform file

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name SIMULATION_VECTOR_COMPARE_RULE_FOR_DC <value>
```
1.19.38. SIMULATION_VECTOR_COMPARE_RULE_FOR_H

Specifies vector values that match with expected weak high value (H) in the waveform file.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name SIMULATION_VECTOR_COMPARE_RULE_FOR_H <value>
```
1.19.39. SIMULATION_VECTORCOMPARE_RULE_FOR_L

Specifies vector values that match with expected weak low value (L) in the waveform file

Type
String

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```
set_global_assignment -name SIMULATION_VECTORCOMPARE_RULE_FOR_L <value>
```
1.19.40. SIMULATION_VECTOR_COMPARE_RULE_FOR_U

Specifies vector values that match with expected uninitialized value (U) in the waveform file

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name SIMULATION_VECTOR_COMPARE_RULE_FOR_U <value>
```
1.19.41. SIMULATION_VECTORCOMPARE_RULE_FOR_W

Specifies vector values that match with expected weak unknown value (W) in the waveform file

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name SIMULATION_VECTOR_COMPARE_RULE_FOR_W <value>
```
1.19.42. SIMULATION VECTOR_COMPARE_RULE_FOR_X

Specifies vector values that match with expected unknown value (X) in the waveform file

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```plaintext
set_global_assignment -name SIMULATION_VECTOR_COMPARE_RULE_FOR_X <value>
```
1.19.43. SIMULATION_VECTORCOMPARE_RULE_FOR_Z

Specifies vector values that match with expected high impedance value (Z) in the waveform file

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name SIMULATION_VECTOR_COMPARE_RULE_FOR_Z <value>
```
1.19.44. SIM_BEHAVIOR_SIMULATION

Perform QUASAR Behavior simulation to simulate a verilog design

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name SIM_BEHAVIOR_SIMULATION <value>
```
1.19.45. SIM_COMPILE_HDL_FILES

Collect a list of HDL files for compilation in QUASAR

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name SIM_COMPILE_HDL_FILES <value>
```
1.19.46. **SIM_HDL_TOP_MODULE_NAME**

Top level module name provided from user to determine starting point of simulation

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name SIM_HDL_TOP_MODULE_NAME <value>
```
1.19.47. SIM_OVERWRITE_WAVEFORM_INPUTS

Overwrite simulation input file with simulation results.

**Type**
Boolean

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name SIM_OVERWRITE_WAVEFORM_INPUTS <value>
```
1.19.48. SIM_TAPREGISTER_D_Q_PORTS

Adds the D and Q ports of a register node to the list of signals for which output waveforms are shown in the simulation report. This option makes the D and Q ports of a register node observable during Functional Simulation.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_instance_assignment -name SIM_TAPREGISTER_D_Q_PORTS -to <to> -entity <entity name> <value>
```
1.19.49. SIM_VECTOR_COMPARED_CLOCK_DUTY_CYCLE

Specifies the duty cycle of compared clock used to trigger waveform comparison.

**Type**

Integer

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```plaintext
set_global_assignment -name SIM_VECTOR_COMPARED_CLOCK_DUTY_CYCLE -section_id <section identifier> <value>
```

**Default Value**

50, requires section identifier
1.19.50. SIM_VECTOR_COMPARED_CLOCK_OFFSET

Specifies the offset of compared clock used to trigger waveform comparison.

**Type**

Time

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```plaintext
set_global_assignment -name SIM_VECTOR_COMPARED_CLOCK_OFFSET -section_id <section identifier> <value>
```

**Default Value**

0ns, requires section identifier
1.19.51. SIM_VECTOR_COMPARED_CLOCK_PERIOD

Specifies the period of compared clock used to trigger waveform comparison.

**Type**

Time

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name SIM_VECTOR_COMPARED_CLOCK_PERIOD -section_id <section identifier> <value>
```
1.19.52. START_TIME

Specifies the start time for simulation.

**Type**
Time

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Syntax**

```
set_global_assignment -name START_TIME <value>
```

**Default Value**

0ns
1.19.53. TRIGGER_EQUATION

Specifies the breakpoint's trigger equation.

**Type**

String

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```plaintext
set_global_assignment -name TRIGGER_EQUATION -section_id <section identifier> <value>
```
1.19.54. TRIGGER_VECTOR_COMPARE_ON_SIGNAL

Trigger vector comparison with the specified signal.

Type
Boolean

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```
set_instance_assignment -name TRIGGER_VECTOR_COMPARE_ON_SIGNAL -to <to> -entity <entity name> <value>
```
1.19.55. USER_MESSAGE

Specifies the breakpoint's message when triggered.

**Type**
String

**Device Support**
- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**
The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name USER_MESSAGE -section_id <section identifier>
<value>
```
1.19.56. VECTOR_COMPARE_TRIGGER_MODE

Specifies the comparison mode to trigger vector comparison.

Type

Enumeration

Values
- ALL_EDGE
- INPUT_EDGE
- SELECTED_EDGE

Device Support
- This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```
set_global_assignment -name VECTOR_COMPARE_TRIGGER_MODE <value>
```

Default Value

INPUT_EDGE
1.19.57. VECTOR_INPUT_SOURCE

    Specifies the source of input vectors to be used for simulation.

    **Type**
    File name

    **Device Support**
    • This setting can be used in projects targeting any Intel FPGA device family.

    **Notes**
    The value of this assignment is case sensitive.

    **Syntax**

    set_global_assignment -name VECTOR_INPUT_SOURCE <value>
1.19.58. VECTOR_OUTPUT_DESTINATION

Specifies the output vector file for the current simulation.

**Type**

File name

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

The value of this assignment is case sensitive.

**Syntax**

```
set_global_assignment -name VECTOR_OUTPUT_DESTINATION <value>
```
1.19.59. VECTOR_OUTPUT_FORMAT

Specifies the format of simulation results.

Type
Enumeration

Values
• CVWF
• VCD
• VWF

Device Support
• This setting can be used in projects targeting any Intel FPGA device family.

Syntax

```
set_global_assignment -name VECTOR_OUTPUT_FORMAT <value>
```
1.19.60. X_ON_VIOLATION_OPTION

Gives user the option to see 'X' or valid data at the output of registers in the event of a timing violation during simulation.

**Type**

Boolean

**Device Support**

- This setting can be used in projects targeting any Intel FPGA device family.

**Notes**

This assignment supports wildcards.

**Syntax**

```plaintext
set_instance_assignment -name X_ON_VIOLATION_OPTION -to <to> -entity <entity name> <value>
```