16. Programmable Power and Temperature-Sensing Diodes in Stratix III Devices

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Introduction

The total power of an FPGA includes static power and dynamic power. Static power is the power consumed by the FPGA when it is programmed but no clocks are operating. Dynamic power is comprised of switching power when the device is configured and running. Dynamic power is calculated with the Equation 16–1:

Equation 16–1. Dynamic Power Equation

$$P = \frac{1}{2} CV^2 \times \text{frequency} \times \text{toggle rate}$$

Equation 16–1 shows that the frequency and toggle rate are design-dependent. However, voltage can be varied to lower dynamic power consumption by the square value of the voltage difference. Stratix® III devices minimize static and dynamic power with advanced process optimizations, selectable core voltage, and programmable power technology. These technologies enable Stratix III designs to optimally meet design-specific performance requirements with the lowest possible power.

The Quartus® II software optimizes all designs with Stratix III power technology to ensure performance is met at the lowest power consumption. This automatic process allows you to concentrate on the functionality of your design, instead of the power consumption of the design.

Power consumption also affects thermal management. Stratix III offers a temperature sensing diode (TSD), which you can use with external circuitry to monitor the device junction temperature for activities such as controlling air flow to the FPGA.

Stratix III Power Technology

The following section provides details about Stratix III selectable core voltage and programmable power technology.

Selectable Core Voltage

Altera offers a series of low-voltage Stratix products that have the ability to power the core logic of the device with either a 0.9-V or 1.1-V power supply. This power supply, called V_{CCL}, powers the logic array block (LAB), memory logic array block (MLAB), digital signal processing (DSP) blocks, TriMatrix™ memory blocks, clock networks, and routing lines. The periphery, consisting of the I/O registers and their routing connections are powered by V_{CC} with a 1.1-V power supply. You can use the same 1.1-V power supply if you want both V_{CC} and V_{CCL} to be 1.1 V.

Lowering the core voltage reduces both static and dynamic power, but causes a reduction in performance. You need to set the correct core supply voltage in the Quartus II software settings under **Operating Conditions**, since the Quartus II software analyzes the core power consumption and timing delays based on this selection. When you compile a design, you can select either 0.9-V or 1.1-V core voltage. You can compare the power and performance trade-offs of a 0.9-V core voltage compilation result and a 1.1-V core voltage compilation result and then choose the most desirable core voltage for your design. By default, the Quartus II software sets the core voltage to 1.1 V.

Ensure that the board has a separate 0.9-V power supply to utilize the lower voltage option and be sure to connect V_{CCL} to the voltage level that you set in the Quartus II software. The Stratix III device cannot distinguish which core voltage level is used on the board. Connecting to the wrong voltage level gives you different timing delays and power consumption than what is reported by the Quartus II software.

For information about selectable core voltage performance and power effects on sample designs, refer to *AN 437: Power Optimization Techniques*.

Programmable Power Technology

In addition to the variable core voltage, Stratix III devices also offer the ability to configure portions of the core, called tiles, for high-speed or low-power mode of operation performed by the Quartus II software without user intervention. This programmable power technology, used to reduce static power, uses an on-chip voltage regulator powered by V_{CCPT}. In a design compilation, the Quartus II software determines whether a tile needs to be in high-speed or low-power mode based on the timing constraints of the design.

For more information about how the Quartus II software uses programmable power technology when compiling a design, refer to *AN 437: Power Optimization Techniques*.

A Stratix III tile can consist of the following:

- MLAB/LAB pairs with routing to the pair
- MLAB/LAB pairs with routing to the pair and to adjacent DSP/memory block routing
- TriMatrix memory blocks
- DSP blocks
- I/O interfaces

All blocks and routing associated with the tile share the same setting of either high speed or low power. Tiles that include DSP blocks, memory blocks, or I/O interfaces are set to high-speed mode by default for optimum performance when used in the design. Unused DSP blocks, memory blocks, and I/O elements are set to low-power mode to minimize static power. Clock networks do not support programmable power technology.

With programmable power technology, faster speed grade FPGAs may require less power, as there are fewer high-speed MLAB and LAB pairs, compared to slower speed grade FPGAs. The slower speed grade device may need to use more high-speed MLAB and LAB pairs to meet the performance requirements, while the faster speed grade device can meet the performance requirements with MLAB and LAB pairs in low-power mode.

The Quartus II software sets unshared inputs and unused device resources in the design to low-power mode to reduce static and dynamic power. The Quartus II software sets the following resources to low power when they are not used in the design:

- LABs and MLABs
- TriMatrix memory blocks
- External memory interface circuitry
- DSP blocks
- phase-locked loop (PLL)
- serializer/deserializer (SERDES) and DPA blocks

If the PLL is instantiated in the design, asserting a reset high keeps the PLL in low power.

Relationship Between Selectable Core Voltage and Programmable Power Technology

Table 16–1 shows available Stratix III programmable power capabilities. You can speed grade considerations to the permutations to give you flexibility in designing your system.

Table 16–1. Stratix III Programmable Power Capabilities

	Selectable Core Voltage	Programmable Power Technology
LAB	Yes	Yes
Routing	Yes	Yes
Memory Blocks	Yes	Fixed setting *(1)*
DSP Blocks	Yes	Fixed setting *(1)*
Global Clock Networks	Yes	No
I/O Elements (IOE)	No	Fixed setting *(1)*

Note to Table 16–1:

(1) Tiles with DSP blocks, memory blocks, and I/O elements that are used in the design are always set to high-speed mode. Unused DSP blocks, memory blocks, and I/O interfaces are set to low-power mode by default.

Stratix III External Power Supply Requirements

This section describes the different external power supplies needed to power Stratix III devices. Table 16–2 lists the external power supply pins for Stratix III devices. Some of the power supply pins can be supplied with the same external power supply, provided they need the same voltage level, as noted in the recommended board connection column.

For possible values of each power supply, refer to the *DC and Switching Characteristics of Stratix III Devices* chapter in volume 2 of the *Stratix III Device Handbook*.

For detailed guidelines about how to connect and isolate VCCL and VCC power supply pins, refer to the *Stratix III Device Family Pin Connections Guidelines* .

Table 16–2. Stratix III Power Supply Requirements

Power Supply Pin	Recommended Board Connection	Description
VCCL	VCCL	Selectable core voltage power supply
VCC	VCC	I/O registers power supply
VCCD_PLL	VCCD_PLL	PLL digital power supply
VCCA_PLL	VCCA_PLL *(1)*	PLL analog power supply
VCCPT		Power supply for programmable power technology
VCCPGM	VCCPGM	Configuration pins power supply
VCCPD	VCCPD *(2)*	I/O pre-driver power supply
VCCIO	VCCIO *(3)*	I/O power supply
VCC_CLKIN		Differential clock input pins power supply (top and bottom I/O banks only)
VCCBAT	VCCBAT	Battery back-up power supply for design security volatile key register
VREF	VREF *(4)*	Power supply for voltage-referenced I/O standards
GND	GND	Ground

Notes to Table 16–2:

(1) You can minimize the number of external power sources by driving the left column and supplies with the same voltage regulator. Note that separate power planes, decoupling capacitors, and ferrite beads are required for VCCA_PLL and VCCPT when implementing this scheme.

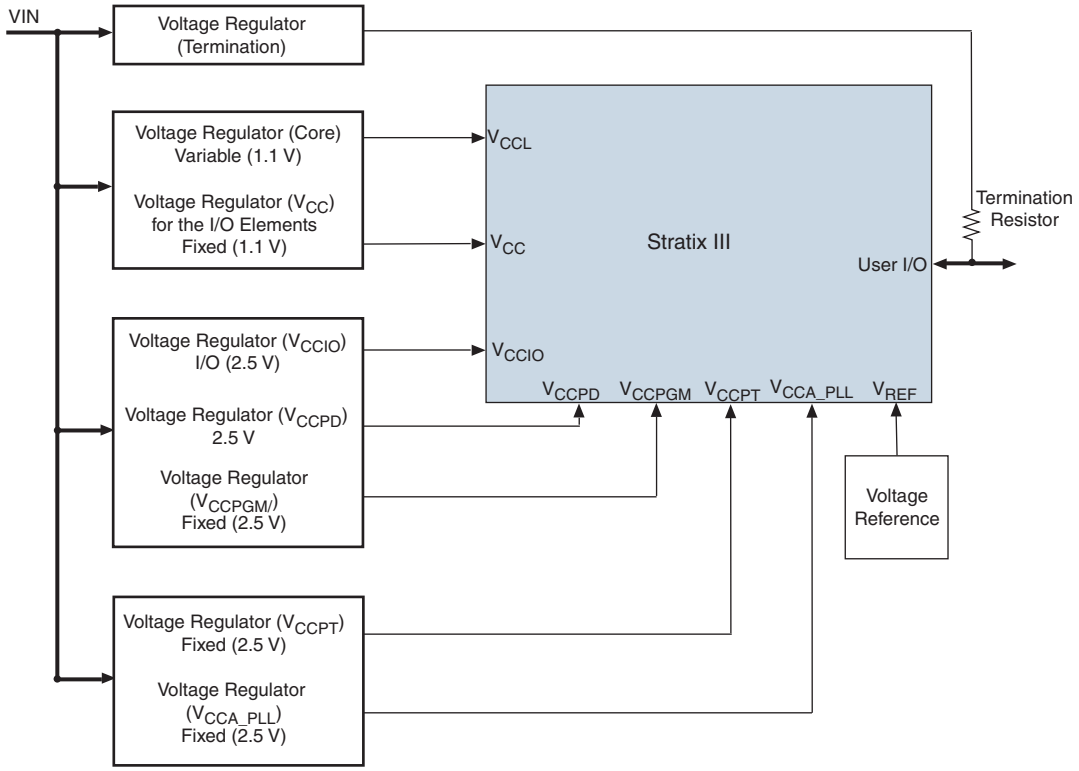
(2) V_{CCPD} can be either 2.5 V, 3.0 V, or 3.3 V. For a 3.3-V standard, V_{CCPD} = 3.3 V. For a 3.0-V I/O standard, V_{CCPD} = 3.0 V. For 2.5 V and below I/O standards, V_{CCPD} = 2.5 V.

(3) This scheme is for VCCIO = 2.5 V.

(4) There is one VREF pin per I/O bank. Use an external power supply or a resistor divider network to supply this voltage.

Figure 16–1 shows an example of power management for Stratix III devices.

Figure 16–1. Stratix III Power Management Example *(Note 1)*, *(2)*



Notes to Figure 16–1:

(1) When V_{CCL} = 0.9 V, you need a separate voltage regulator.

(2) When V_{CCL} = 0.9 V, V_{CCPT} and V_{CC} must be ramped before V_{CCL} to minimize V_{CCL} standby current during V_{CCPT} and V_{CC} ramping to full rail.

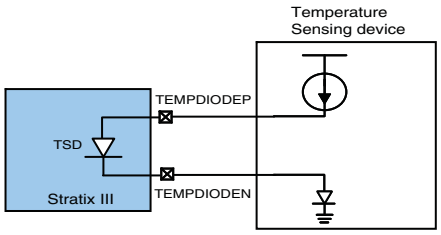
Temperature Sensing Diode

Knowing the junction temperature is crucial for thermal management. A Stratix III device monitors its die temperature with an embedded temperature sensing diode (TSD). This is done by sensing the voltage level across the TSD. Each temperature level produces a unique voltage across the diode. Use an external analog-to-digital converter that measures the voltage difference across the TSD and then converts it to a temperature reading.

External Pin Connections

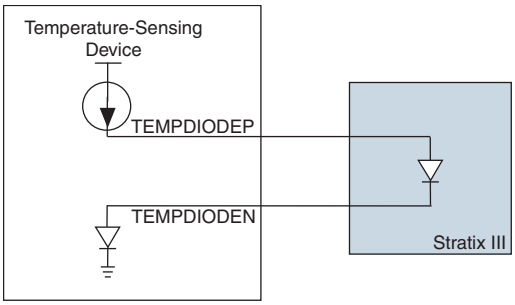
The Stratix III TSD, located in the top-right corner of the die, requires two pins for voltage reference. Connect the TEMPDIODEP and TEMPDIODEN pins to the external analog-to-digital converter, as shown in Figure 16–2.

Figure 16–2. TEMPDIODEP and TEMPDIODEN External Pin Connections



The TSD is a very sensitive circuit which can be influenced by the noise coupled from traces on the board, and possibly within the device package itself, depending on device usage. The interfacing device registers temperature based on milivolts of difference as seen at the TSD. Switching I/O near the TSD pins can affect the temperature reading. Altera recommends you take temperature readings during periods of no activity in the device (for example, standby mode where no clocks are toggling in the device), such as when the nearby I/Os are at a DC state and the clock networks in the device are disabled.

Figure 16–3. TSD Connections



Conclusion

As process geometries get smaller, power and thermal management is becoming more crucial in FPGA designs. Stratix III devices offer programmable power technology and selectable core voltage options for low-power operation. Use these features, along with speed grade choices, in different permutations to get the best power and performance combination. Taking advantage of the silicon, the Quartus II software is able to manipulate designs to use the best combination to achieve the lowest power at the required performance.

For thermal management, use the Stratix III temperature sensing diode with an external analog-to-digital converter in production devices. This allows you to easily incorporate this feature in your designs. Being able to monitor the junction temperature of the device at any time also allows you to control air flow to the device and save power for the whole system.

Chapter Revision History

Table 16–3 shows the revision history for this document.

Table 16–3. Chapter Revision History

Date and Revision	Changes Made	Summary of Changes
February 2009, version 1.5	Removed “Referenced Documents” section.	—
October 2008, version 1.4	■ Updated “Introduction”, “Temperature Sensing Diode”, “External Pin Connections”, and “Conclusion” sections. ■ Updated new Document Format.	—
May 2008, version 1.3	■ Updated Figure 16–1. ■ Updated Table 16–2. ■ Updated “External Pin Connections” section.	—
October 2007, version 1.2	■ Added material to note 3 of Table 16–2. ■ Updated Figure 16–1 and Figure 16–3. ■ Removed old version of Figure 16-2. ■ Removed section “Architecture Description”. ■ Removed material from the sections “Introduction”, “Temperature Sensing Diode”, “External Pin Connections”, and “Conclusion”. ■ Added new section “Referenced Documents”. ■ Added live links for references.	Minor update.
May 2007, version 1.1	Replaced all instances of VCCR with VCCPT	Minor update.
November 2006, version 1.0	Initial Release.	—