3. MultiTrack Interconnect in Stratix III Devices

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Introduction

Stratix® III devices contain a two-dimensional row- and column-based architecture to implement custom logic. A series of column and row interconnects of varying length and speed provides signal interconnects between logic array blocks (LABs), memory block structures, digital signal processing (DSP) blocks, and input/output elements (IOE). These blocks communicate with themselves and to one another through a fabric of routing wires. This chapter provides details on the Stratix III core routing structure. It also describes how Stratix III block types interface to this fabric.

In the Stratix III architecture, connections between adaptive logic modules (ALMs), TriMatrix memory, DSP blocks, and device I/O pins are provided by the MultiTrack interconnect structure with DirectDrive technology. The MultiTrack interconnect consists of continuous, performance-optimized routing lines of different lengths and speeds used for inter- and intra-design block connectivity. The Quartus® II Compiler automatically routes critical design paths on faster interconnects to improve design performance.

DirectDrive technology is a deterministic routing technology that ensures identical routing resource usage for any function regardless of placement in the device. The MultiTrack interconnect and DirectDrive technology simplify the integration stage of block-based designing by eliminating the re-optimization cycles that typically follow design changes and additions.

The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and repeatable performance when migrating through different device densities.

Row Interconnects

Dedicated row interconnects route signals to and from LABs, DSP blocks, and TriMatrix memory blocks in the same row. These row interconnect resources include:

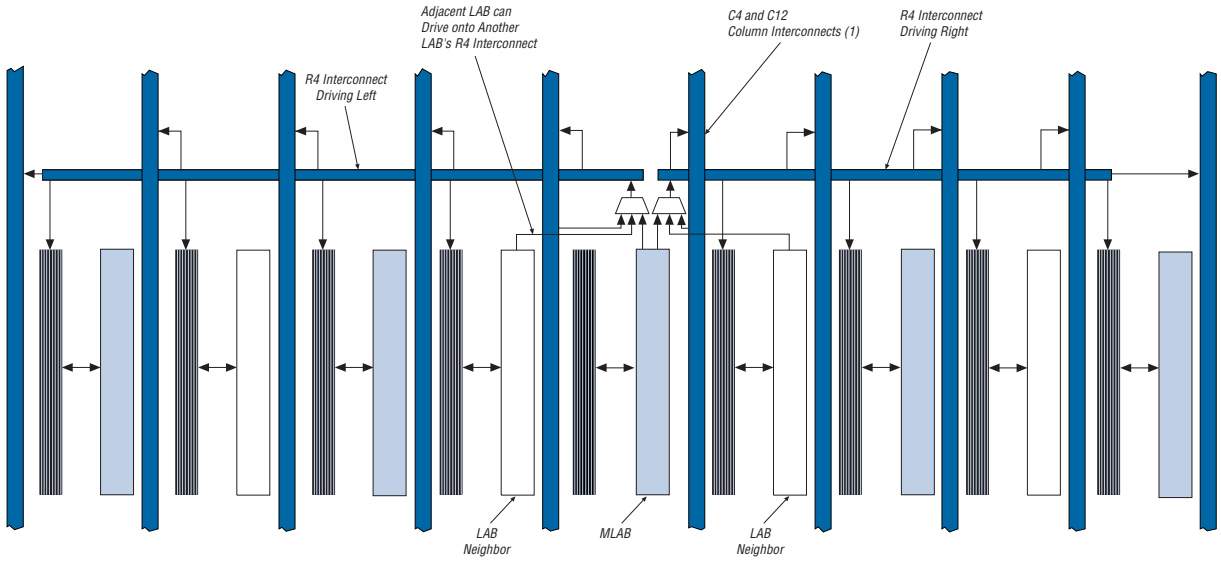
- Direct link interconnects between LABs and adjacent blocks
- R4 interconnects traversing four blocks to the right or left
- R20 row interconnects for high-speed access across the length of the device

The direct link interconnect allows a LAB, DSP block, or TriMatrix memory block to drive into the local interconnect of its left and right neighbors. This capability provides fast communication between adjacent LABs and blocks without using row interconnect resources. The direct link interconnect is the fastest way to communicate between two adjacent blocks.

The R4 interconnects span a combination of four LABs, memory logic array blocks (MLAB), DSP blocks, M9K blocks, and M144K blocks. Use these resources for fast row connections in a four-LAB region. Figure 3–1 shows R4 interconnect connections from a LAB. R4 interconnects can drive and be driven by DSP blocks and RAM blocks and row IOEs. For LAB interfacing, a primary LAB or LAB neighbor can drive a given R4

interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they drive. R4 interconnects can also drive C4 and C12 (column interconnects) for connections from one row to another. Additionally, R4 interconnects can drive R20 interconnects.

Figure 3–1. R4 Interconnect Connections *(Note 1)*, *(2)*



Notes to Figure 3–1

(1) C4 and C12 interconnects can drive R4 interconnects.

(2) This pattern is repeated for every LAB in the LAB row.

R20 row interconnects span 20 LABs and provide the fastest resource for row connections between distant LABs, TriMatrix memory, DSP blocks, and row IOEs. R20 row interconnects drive LAB local interconnects via R4 and C4 interconnects. R20 interconnects can drive R20, R4, C12, and C4 interconnects.

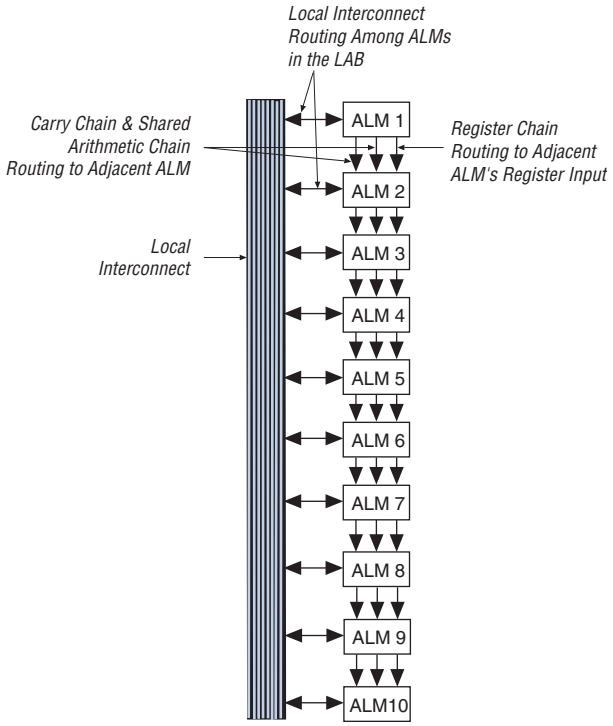
Column Interconnects

The column interconnect operates similarly to the row interconnect. It vertically routes signals to and from LABs, TriMatrix memory, DSP blocks, and IOEs. Each column of LABs is served by a dedicated column interconnect. These column interconnect resources include:

- Shared arithmetic chain interconnects in a LAB and from LAB to LAB
- Carry chain interconnects in a LAB and from LAB to LAB
- Register chain interconnects in a LAB
- C4 interconnects traversing a distance of four blocks in the same device column
- C12 column interconnects for high-speed vertical routing through the device

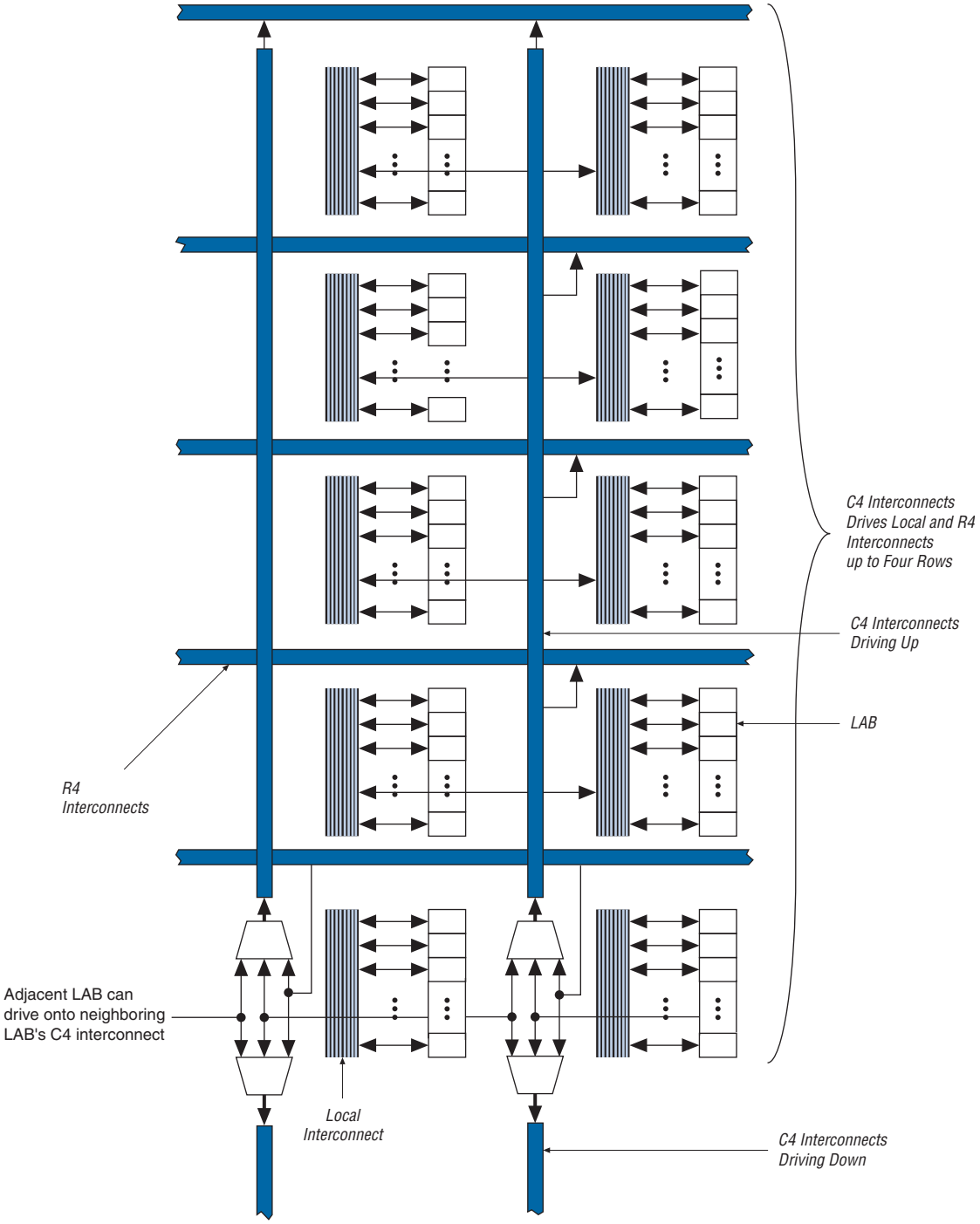
Stratix III devices include an enhanced interconnect structure in LABs for routing-shared arithmetic chains and carry chains for efficient arithmetic functions. The register chain connection allows the register output of one ALM to connect directly to the register input of the next ALM in the LAB for fast shift registers. These ALM-to-ALM connections bypass the local interconnect. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 3–2 shows the shared arithmetic chain, carry chain, and register chain interconnects.

Figure 3–2. Shared Arithmetic Chain, Carry Chain, and Register Chain Interconnects



The C4 interconnects span four adjacent interfaces in the same device column. C4 interconnects also pass by M144K and DSP blocks. A single M144K block utilizes eight adjacent interfaces in the same column. A DSP block utilizes four adjacent interfaces in the same column. Figure 3–3 shows the C4 interconnect connections from a LAB in a column. The C4 interconnects can drive and be driven by all types of architecture blocks, including DSP blocks, TriMatrix memory blocks, and column and row IOEs. For LAB interconnection, a primary LAB or its LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Figure 3–3. C4 Interconnect Connections *(Note 1)*



Note to Figure 3–3:

(1) Each C4 interconnect can drive either up or down four rows.

C12 column interconnects span a length of 12 LABs and provide the fastest resource for column connections between distant LABs, TriMatrix memory blocks, DSP blocks, and IOEs. C12 interconnects drive LAB local interconnects via C4 and R4 interconnects and do not drive LAB local interconnects directly.

All embedded blocks communicate with the logic array through interconnects similar to LAB-to-LAB interfaces. Each block (for example, TriMatrix memory blocks and DSP blocks) connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. These blocks also have direct link interconnects for fast connections to and from a neighboring LAB.

Table 3–1 shows the Stratix III device's routing scheme.

Table 3–1. Stratix III Device Routing Scheme

Source	Destination															
	Shared Arithmetic Chain	Carry Chain	Register Chain	Local Interconnect	Direct Link Interconnect	R4 Interconnect	R20 Interconnect	C4 Interconnect	C12 Interconnect	ALM	MLAB RAM Block	M9K RAM Block	M144K Block	DSP Blocks	Column IOE	Row IOE
Shared arithmetic chain	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—
Carry chain	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—
Register chain	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	—
Local interconnect	—	—	—	—	—	—	—	—	—	✓	✓	✓	✓	✓	✓	✓
Direct link interconnect	—	—	—	✓	—	—	—	—	—	—	—	—	—	—	—	—
R4 interconnect	—	—	—	✓	—	✓	✓	✓	✓	—	—	—	—	—	—	—
R20 interconnect	—	—	—	✓	—	✓	✓	✓	✓	—	—	—	—	—	—	—
C4 interconnect	—	—	—	✓	—	✓	—	✓	—	—	—	—	—	—	—	—
C12 interconnect	—	—	—	✓	—	✓	✓	✓	✓	—	—	—	—	—	—	—
ALM	✓	✓	✓	✓	✓	✓	—	✓	—	—	—	—	—	—	—	—
MLAB RAM block	—	—	—	✓	✓	✓	—	✓	—	—	—	—	—	—	—	—
M9K RAM block	—	—	—	—	✓	✓	—	✓	—	—	—	—	—	—	—	—
M144K block	—	—	—	—	✓	✓	—	✓	—	—	—	—	—	—	—	—
DSP blocks	—	—	—	—	✓	✓	—	✓	—	—	—	—	—	—	—	—
Column IOE	—	—	—	—	—	—	—	✓	✓	—	—	—	—	—	—	—
Row IOE	—	—	—	—	✓	✓	✓	✓	—	—	—	—	—	—	—	—

Notes to Table 3–1:

(1) Except column IOE local interconnects.
(2) Row IOE local interconnects.
(3) Column IOE local interconnects.

The R4 and C4 interconnects provide superior and flexible routing capabilities. Stratix III has a three-sided routing architecture which allows the interconnect wires from each LAB to reach the adjacent LABs to its right and left. A given LAB can drive 32 other LABs using one R4 or C4 interconnect, in one hop. This routing scheme improves efficiency and flexibility by placing all the critical LABs within one hop of the routing interconnects.

Table 3–2 shows how many LABs are reachable within one, two, or three hops using the R4 and C4 interconnects.

Table 3–2. Number of LABs reachable using C4 and R4 interconnects

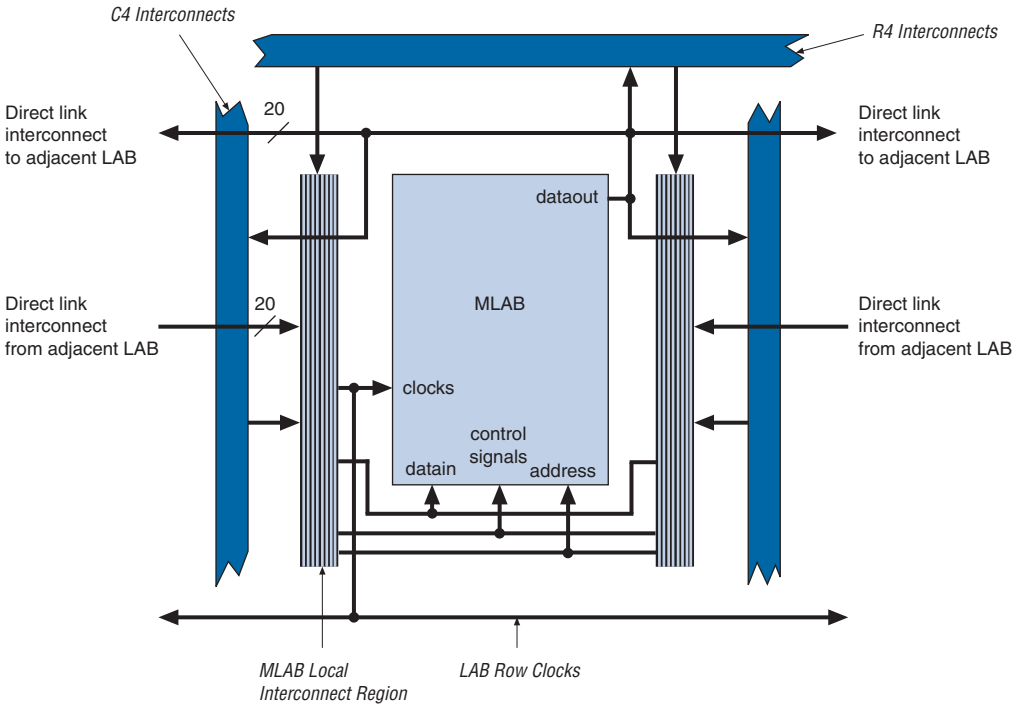
Hops	Number of LABs
1	34
2	96
3	160

Memory Block Interface

TriMatrix memory consists of three types of RAM blocks: MLAB, M9K, and M144K. This section provides a brief overview of how the different memory blocks interface to the routing structure.

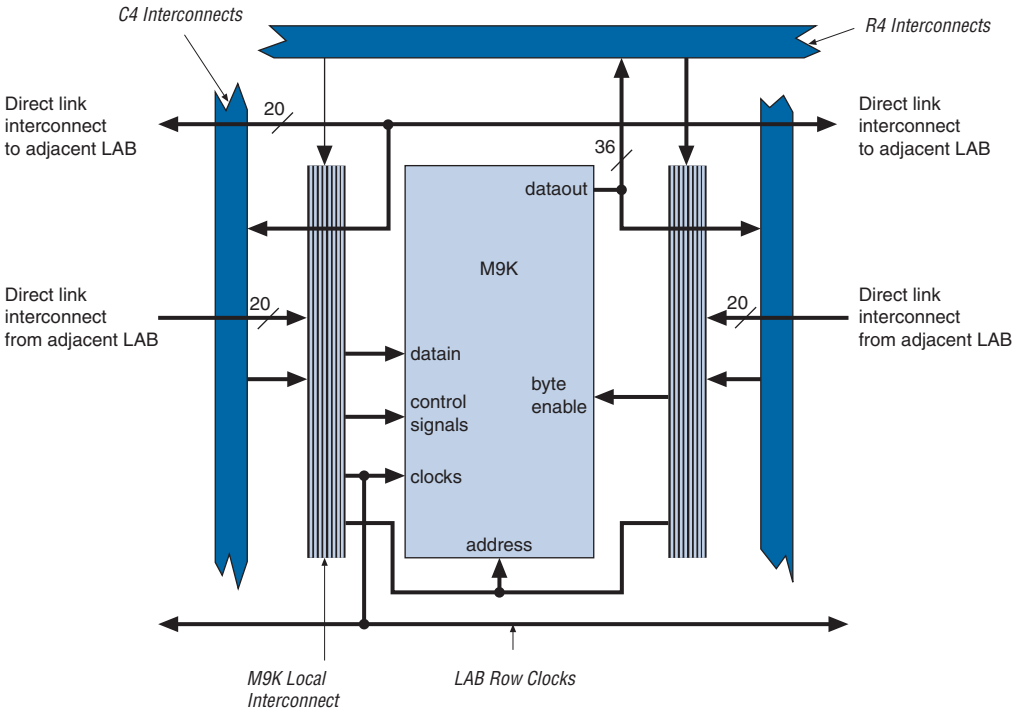
The RAM blocks in Stratix III devices have local interconnects to allow ALMs and interconnects to drive into RAM blocks. The MLAB RAM block local interconnect is driven by the R4, C4, and direct link interconnects from adjacent LABs. The MLAB RAM blocks can communicate with LABs on either the left or right side through these row interconnects or with LAB columns on the left or right side with the column interconnects. Each MLAB RAM block has up to 20 direct link input connections from the left adjacent LAB and another 20 from the right adjacent LAB. MLAB RAM outputs can also connect to left and right LABs through a direct link interconnect. The MLAB RAM block has equal opportunity for access and performance to and from LABs on either its left or right side. Figure 3–4 shows the MLAB RAM block to LAB row interface.

Figure 3–4. MLAB RAM Block LAB Row Interface



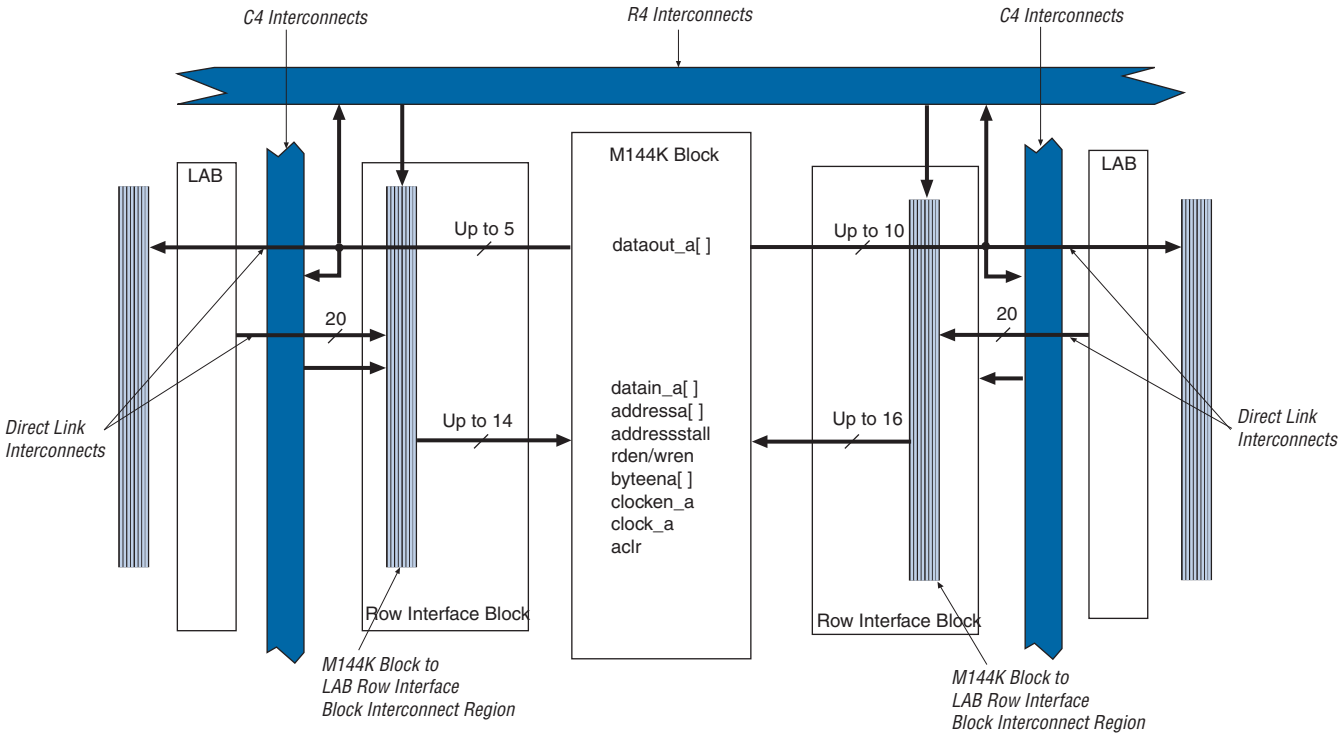
The M9K RAM block local interconnect is driven by the R4, C4, and direct link interconnects from adjacent LABs. The M9K RAM blocks can communicate with LABs on either the left or right side through these row resources or with LAB columns on either the right or left with the column resources. Up to 20 direct link input connections to the M9K RAM Block are possible from the left adjacent LABs and another 20 possible from the right adjacent LAB. M9K RAM block outputs can also connect to left and right LABs through direct link interconnect. Figure 3–5 shows the M9K RAM block to logic array interface.

Figure 3–5. M9K RAM Block LAB Row Interface



The M144K blocks use eight interfaces in the same device column. The M144K block local interconnects are driven by R4, C4, and direct link interconnects from adjacent LABs on either the right or left side of the MRAM block. Up to 20 direct link input connections to the M144K block are possible from the left adjacent LABs and another 20 possible from the right adjacent LAB. M144K block outputs can also connect to the LABs on the block's left and right sides through direct link interconnect. Figure 3–6 shows the interface between the M144K RAM block and the logic array.

Figure 3–6. M144K Row Unit Interface to Interconnect



DSP Block Interface

Stratix III device DSP block input registers can generate a shift register that cascades down in the same DSP block column. Dedicated connections between DSP blocks provide fast connections between the shift register inputs to cascade the shift register chains. You can cascade registers within multiple DSP blocks for 9-bit or 18-bit finite impulse response (FIR) filters larger than four taps, with additional adder stages implemented in ALMs. If the DSP block is configured as 36-bit blocks, the adder, subtractor, or accumulator stages are implemented in ALMs. Each DSP block can route the shift register chain out of the block to cascade multiple columns of DSP blocks.

The DSP block is divided into four block units that interface with four LAB rows on the left and right. You can consider each block unit as two 18-bit multipliers followed by an adder with 72 inputs and 36 outputs. A local interconnect region is associated with each DSP block. Like a LAB, this interconnect region can be fed with 20 direct link interconnects from the LAB to the left or right of the DSP block in the same row. R4 and C4 routing resources can access the DSP block's local interconnect region.

These outputs work similarly to LAB outputs. Eighteen outputs from the DSP block can drive to the left LAB through direct link interconnects and eighteen can drive to the right LAB though direct link interconnects. All 36 outputs can drive to R4 and C4 routing interconnects. Outputs can drive right- or left-column routing. Figure 3–7 and Figure 3–8 show the DSP block interfaces to LAB rows.

Figure 3–7. High-Level View, DSP Block Interface to Interconnect

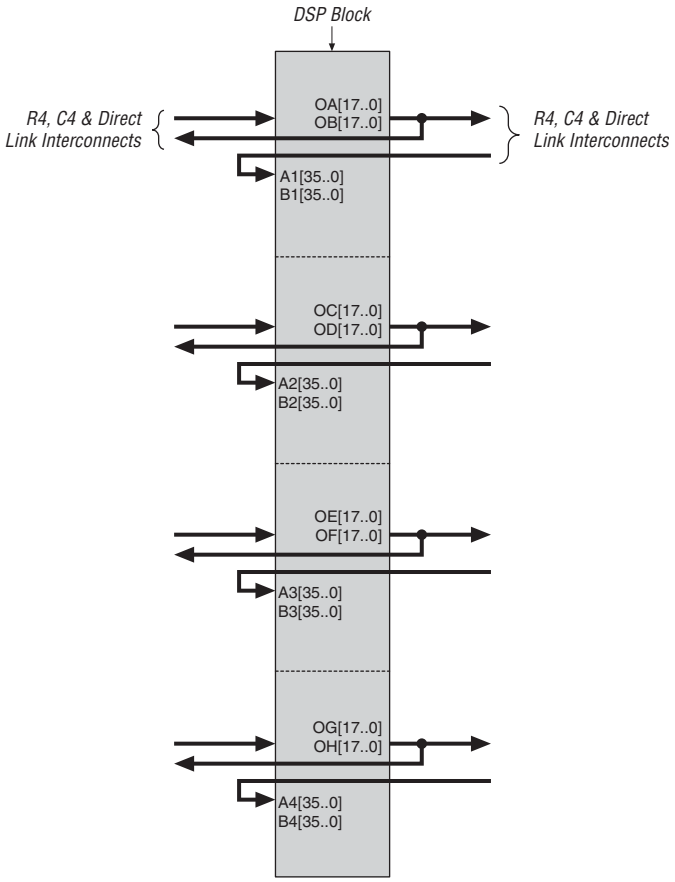
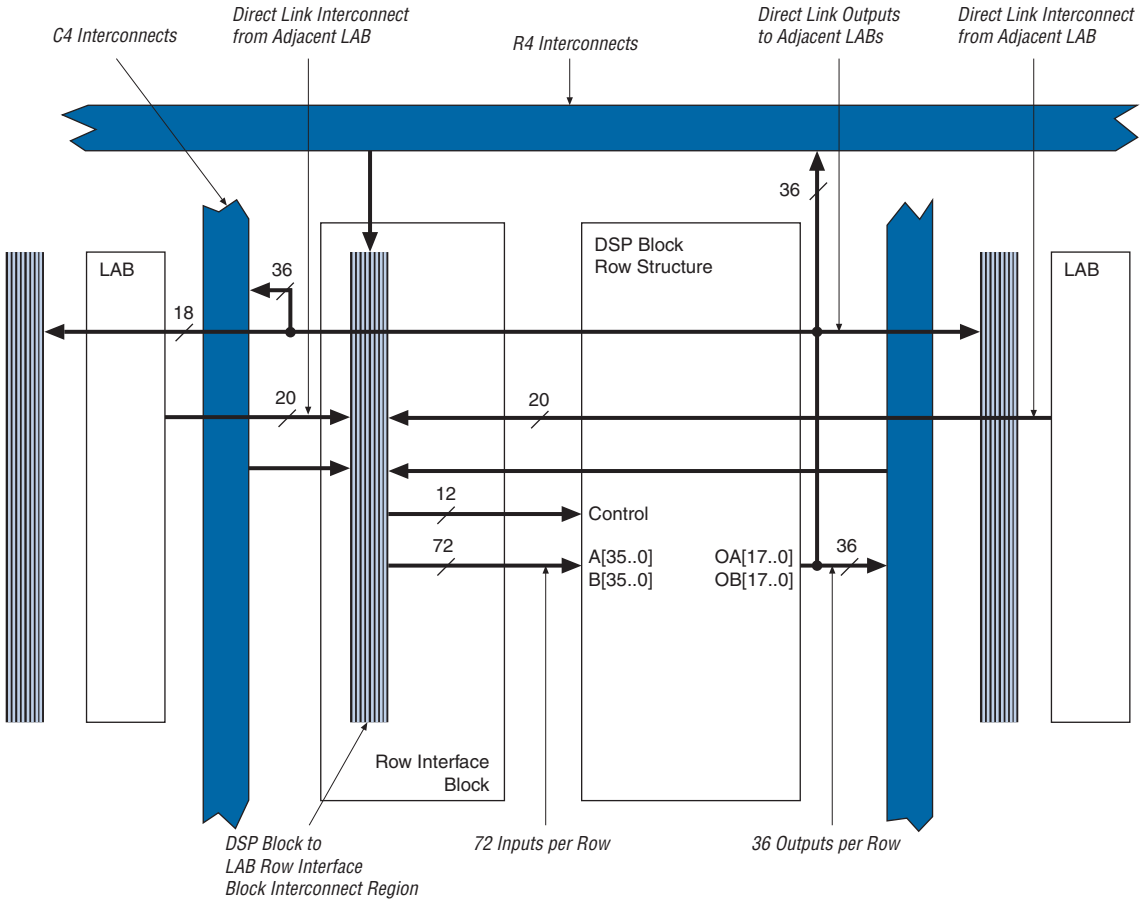


Figure 3–8. Detailed View, DSP Block Interface to Interconnect



I/O Block Connections to Interconnect

The IOEs are located in I/O blocks around the periphery of the Stratix III device. There are up to four IOEs per row I/O block and four IOEs per column I/O block. The row I/O blocks drive row, column, or direct link interconnects. The column I/O blocks drive column interconnects. Figure 3–9 shows how a row I/O block connects to the logic array. Figure 3–10 shows how a column I/O block connects to the logic array.

Figure 3–9. Row I/O Block Connection to Interconnect

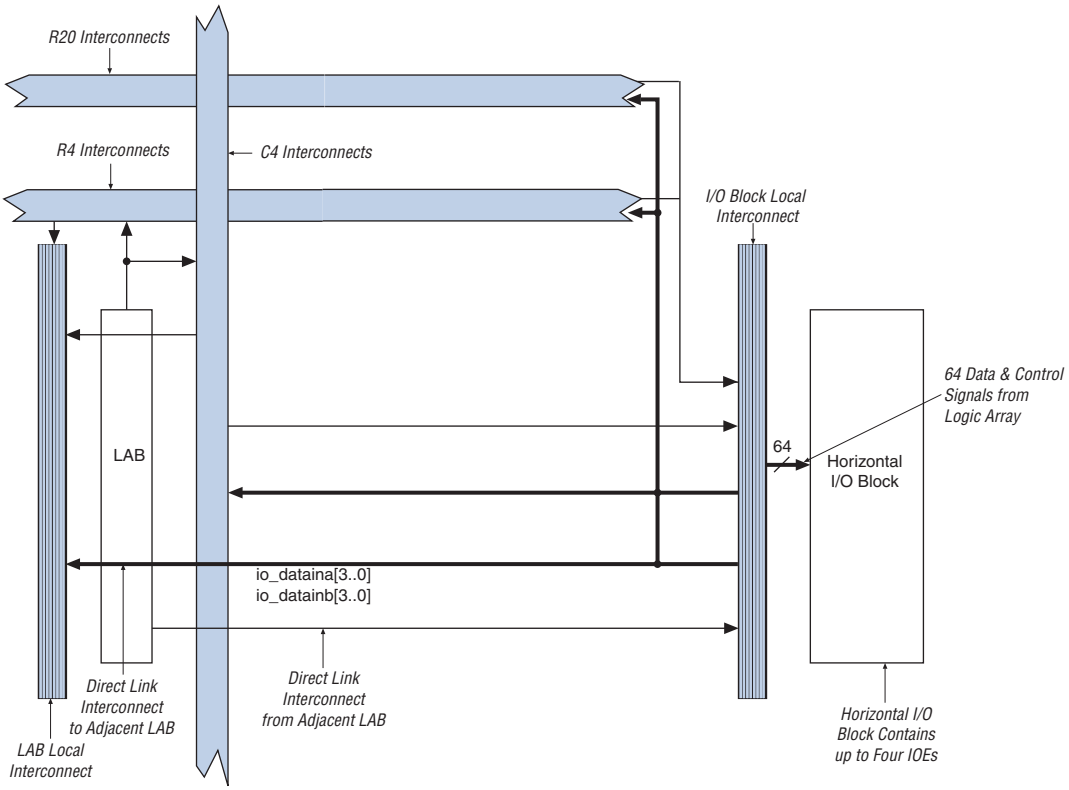
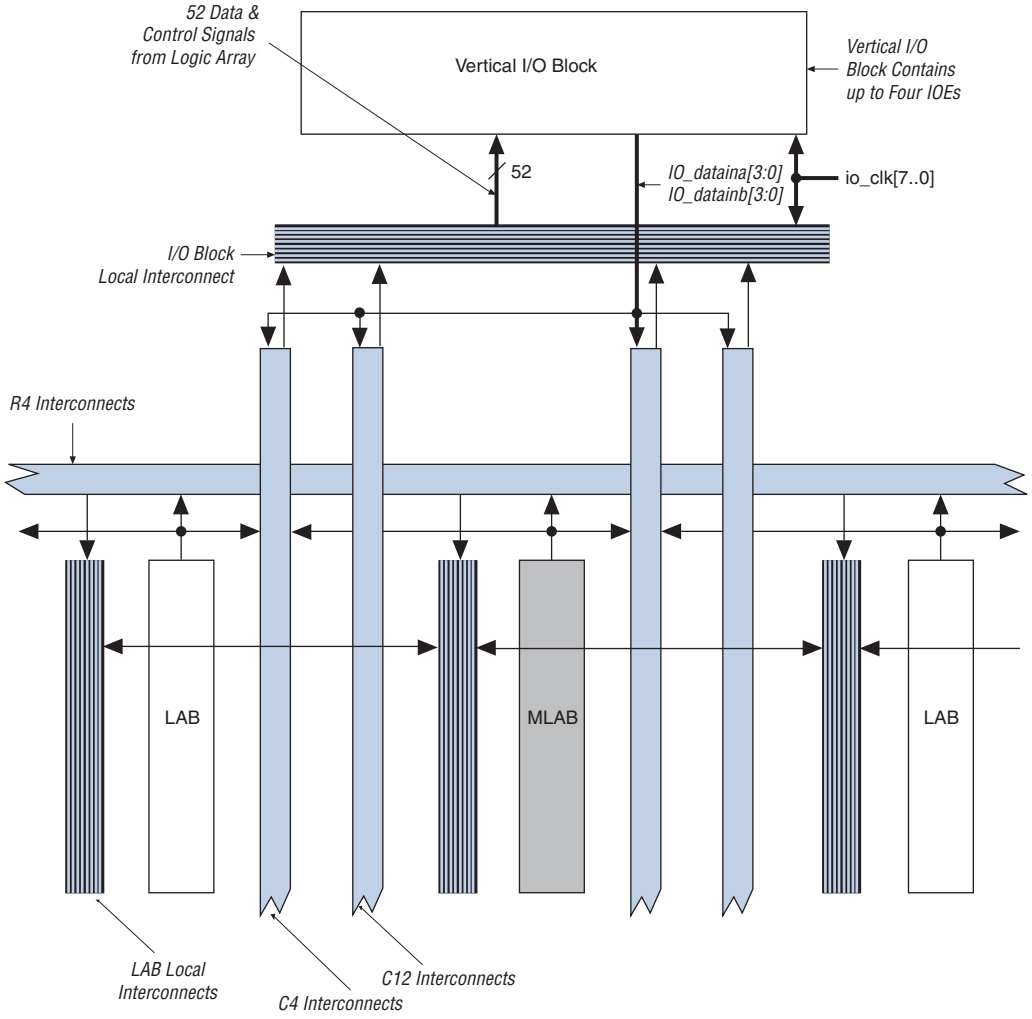


Figure 3–10. Column I/O Block Connection to Interconnect



Conclusion

Stratix III devices consist of an array of logic blocks such as LABs, TriMatrix memory, DSP blocks, and IOEs. These blocks communicate with themselves and one another through the MultiTrack interconnect structures. The Quartus II compiler automatically routes critical design paths on faster interconnects to improve design performance and optimize the device resources.

Chapter Revision History

Table 3–3 shows the revision history for this document.

Table 3–3. Chapter Revision History

Date and Revision	Changes Made	Summary of Changes
October 2008, version 1.2	Updated New Document Format.	—
October 2007, version 1.1	■ Minor formatting changes. ■ Added section “Chapter Revision History”. ■ Added live links for references.	Minor formatting changes.
November 2006, version 1.0	Initial Release.	—