1. Introduction

SIIGX51001-1.6

The Stratix® II GX family of devices is Altera's third generation of FPGAs to combine high-speed serial transceivers with a scalable, high-performance logic array. Stratix II GX devices include 4 to 20 high-speed transceiver channels, each incorporating clock and data recovery unit (CRU) technology and embedded SERDES capability at data rates of up to 6.375 gigabits per second (Gbps). The transceivers are grouped into four-channel transceiver blocks and are designed for low power consumption and small die size. The Stratix II GX FPGA technology is built upon the Stratix II architecture and offers a 1.2-V logic array with unmatched performance, flexibility, and time-to-market capabilities. This scalable, high-performance architecture makes Stratix II GX devices ideal for high-speed backplane interface, chip-to-chip, and communications protocol-bridging applications.

Features

This section lists the Stratix II GX device features.

- Main device features:
  - TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers with performance up to 550 MHz
  - Up to 16 global clock networks with up to 32 regional clock networks per device region
  - High-speed DSP blocks provide dedicated implementation of multipliers (at up to 450 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
  - Up to four enhanced PLLs per device provide spread spectrum, programmable bandwidth, clock switch-over, real-time PLL reconfiguration, and advanced multiplication and phase shifting
  - Support for numerous single-ended and differential I/O standards
  - High-speed source-synchronous differential I/O support on up to 71 channels
  - Support for source-synchronous bus standards, including SPI-4 Phase 2 (POS-PHY Level 4), SFI-4.1, XSBI, UTOPIA IV, NPSI, and CSIX-L1
  - Support for high-speed external memory, including quad data rate (QDR and QDRII) SRAM, double data rate (DDR and DDR2) SDRAM, and single data rate (SDR) SDRAM

- Support for multiple intellectual property megafunctions from Altera® MegaCore® functions and Altera Megafunction Partners Program (AMPP^{SM}) megafunctions
- Support for design security using configuration bitstream encryption
- Support for remote configuration updates

- Transceiver block features:
  - High-speed serial transceiver channels with clock data recovery (CDR) provide 600-megabits per second (Mbps) to 6.375-Gbps full-duplex transceiver operation per channel
  - Devices available with 4, 8, 12, 16, or 20 high-speed serial transceiver channels providing up to 255 Gbps of serial bandwidth (full duplex)
  - Dynamically programmable voltage output differential (V_{OD}) and pre-emphasis settings for improved signal integrity
  - Support for CDR-based serial protocols, including PCI Express, Gigabit Ethernet, SDI, Altera's SerialLite II, XAUI, CEI-6G, CPRI, Serial RapidIO, SONET/SDH
  - Dynamic reconfiguration of transceiver channels to switch between multiple protocols and data rates
  - Individual transmitter and receiver channel power-down capability for reduced power consumption during non-operation
  - Adaptive equalization (AEQ) capability at the receiver to compensate for changing link characteristics
  - Selectable on-chip termination resistors (100, 120, or 150 Ω) for improved signal integrity on a variety of transmission media
  - Programmable transceiver-to-FPGA interface with support for 8-, 10-, 16-, 20-, 32-, and 40-bit wide data transfer
  - 1.2- and 1.5-V pseudo current mode logic (PCML) for 600 Mbps to 6.375 Gbps (AC coupling)
  - Receiver indicator for loss of signal (available only in PIPE mode)
  - Built-in self test (BIST)
  - Hot socketing for hot plug-in or hot swap and power sequencing support without the use of external devices
  - Rate matcher, byte-reordering, bit-reordering, pattern detector, and word aligner support programmable patterns
  - Dedicated circuitry that is compliant with PIPE, XAUI, and GIGE
  - Built-in byte ordering so that a frame or packet always starts in a known byte lane
  - Transmitters with two PLL inputs for each transceiver block with independent clock dividers to provide varying clock rates on each of its transmitters

- 8B/10B encoder and decoder perform 8-bit to 10-bit encoding and 10-bit to 8-bit decoding
- Phase compensation FIFO buffer performs clock domain translation between the transceiver block and the logic array
- Receiver FIFO resynchronizes the received data with the local reference clock
- Channel aligner compliant with XAUI

Certain transceiver blocks can be bypassed. Refer to the *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook* for more details.

Table 1–1 lists the Stratix II GX device features.

Table 1–1. Stratix II GX Device Features (Part 1 of 2)

Feature	EP2SGX30C/D		EP2SGX60C/D/E			EP2SGX90E/F		EP2SGX130/G
	C	D	C	D	E	E	F	G
ALMs	13,552		24,176			36,384		53,016
Equivalent LEs	33,880		60,440			90,960		132,540
Transceiver channels	4	8	4	8	12	12	16	20
Transceiver data rate	600 Mbps to 6.375 Gbps		600 Mbps to 6.375 Gbps			600 Mbps to 6.375 Gbps		600 Mbps to 6.375 Gbps
Source-synchronous receive channels *(1)*	31		31	31	42	47	59	73
Source-synchronous transmit channels	29		29	29	42	45	59	71
M512 RAM blocks (32 × 18 bits)	202		329			488		699
M4K RAM blocks (128 × 36 bits)	144		255			408		609
M-RAM blocks (4K × 144 bits)	1		2			4		6
Total RAM bits	1,369,728		2,544,192			4,520,448		6,747,840
Embedded multipliers (18 × 18)	64		144			192		252
DSP blocks	16		36			48		63
PLLs	4		4	4	8	8		8
Maximum user I/O pins	361		364	364	534	558	650	734

Table 1–1. Stratix II GX Device Features (Part 2 of 2)

Feature	EP2SGX30C/D		EP2SGX60C/D/E			EP2SGX90E/F		EP2SGX130/G
	C	D	C	D	E	E	F	G
Package	780-pin FineLine BGA		780-pin FineLine BGA		1,152-pin FineLine BGA	1,152-pin FineLine BGA	1,508-pin FineLine BGA	1,508-pin FineLine BGA

Note to Table 1–1:
(1) Includes two sets of dual-purpose differential pins that can be used as two additional channels for the differential receiver or differential clock inputs.

Stratix II GX devices are available in space-saving FineLine BGA packages (refer to Table 1–2). All Stratix II GX devices support vertical migration within the same package. Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities. For I/O pin migration across densities, you must cross-reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins are migratable. Table 1–3 lists the Stratix II GX device package sizes.

Table 1–2. Stratix II GX Package Options (Pin Counts and Transceiver Channels)

Device	Transceiver Channels	Source-Synchronous Channels		Maximum User I/O Pin Count		
		Receive *(1)*	Transmit	780-Pin FineLine BGA (29 mm)	1,152-Pin FineLine BGA (35 mm)	1,508-Pin FineLine BGA (40 mm)
EP2SGX30C	4	31	29	361	—	—
EP2SGX60C	4	31	29	364	—	—
EP2SGX30D	8	31	29	361	—	—
EP2SGX60D	8	31	29	364	—	—
EP2SGX60E	12	42	42	—	534	—
EP2SGX90E	12	47	45	—	558	—
EP2SGX90F	16	59	59	—	—	650
EP2SGX130G	20	73	71	—	—	734

Note to Table 1–2:
(1) Includes two differential clock inputs that can also be used as two additional channels for the differential receiver.

Table 1–3. Stratix II GX FineLine BGA Package Sizes			
Dimension	**780 Pins**	**1,152 Pins**	**1,508 Pins**
Pitch (mm)	1.00	1.00	1.00
Area (mm^2)	841	1,225	1,600
Length width (mm × mm)	29 × 29	35 × 35	40 × 40

Referenced Document

This chapter references the following document:

- *Stratix II GX Architecture* chapter in volume 1 of the *Stratix II GX Device Handbook*

Document Revision History

Table 1–4 shows the revision history for this chapter.

Table 1–4. Document Revision History		
Date and Document Version	**Changes Made**	**Summary of Changes**
October 2007, v1.6	Updated "Features" section.	
	Minor text edits.	
August 2007, v1.5	Added "Referenced Documents" section.	
	Minor text edits.	
February 2007, v1.4	• Changed 622 Mbps to 600 Mbps on page 1-2 and Table 1–1. • Deleted "DC coupling" from the Transceiver Block Features list. • Changed 4 to 6 in the PLLs row (columns 3 and 4) of Table 1–1.	
	Added the "Document Revision History" section to this chapter.	Added support information for the Stratix II GX device.
June 2006, v1.3	• Updated Table 1–2.	
April 2006, v1.2	• Updated Table 1–1. • Updated Table 1–2.	Updated numbers for receiver channels and user I/O pin counts in Table 1–2.
February 2006, v1.1	• Updated Table 1–1.	
October 2005 v1.0	Added chapter to the *Stratix II GX Device Handbook*.	