5. High-Speed Differential I/O Interfaces with DPA in Stratix II and Stratix II GX Devices

SII52005-2.2

Introduction

Stratix® II and Stratix® II GX device family offers up to 1-Gbps differential I/O capabilities to support source-synchronous communication protocols such as HyperTransport™ technology, Rapid I/O, XSBI, and SPI.

Stratix II and Stratix II GX devices have the following dedicated circuitry for high-speed differential I/O support:

- Differential I/O buffer
- Transmit serializer
- Receive deserializer
- Data realignment circuit
- Dynamic phase aligner (DPA)
- Synchronizer (FIFO buffer)
- Analog PLLs (fast PLLs)

For high-speed differential interfaces, Stratix II and Stratix II GX devices can accommodate different differential I/O standards, including the following:

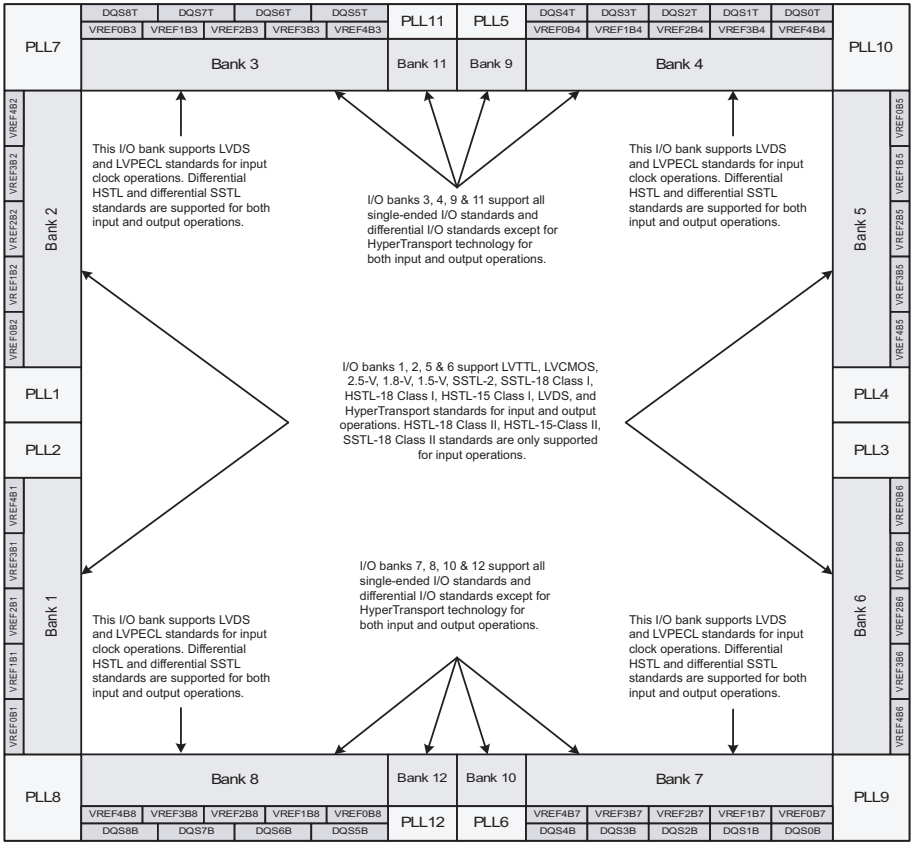
- LVDS
- HyperTransport technology
- HSTL
- SSTL
- LVPECL

HSTL, SSTL, and LVPECL I/O standards can be used only for PLL clock inputs and outputs in differential mode.

I/O Banks

Stratix II and Stratix II GX inputs and outputs are partitioned into banks located on the periphery of the die. The inputs and outputs that support LVDS and HyperTransport technology are located in row I/O banks, two on the left and two on the right side of the Stratix II device and two on the left side of the Stratix II GX device. LVPECL, HSTL, and SSTL standards are supported on certain top and bottom banks of the die (banks 9 to 12) when used as differential clock inputs/outputs. Differential HSTL and SSTL standards can be supported on banks 3, 4, 7, and 8 if the pins on these banks are used as DQS/DQSn pins. Figures 5–1 and 5–2 show where the banks and the PLLs are located on the die.

Figure 5–1. Stratix II I/O Banks *Note (1), (2), (3), (4), (5), (6), and (7)*



Notes to Figure 5–1:

(1) Figure 5–1 is a top view of the silicon die that corresponds to a reverse view for flip-chip packages. It is a graphical representation only. See the pin list and Quartus II software for exact locations.

(2) Depending on the size of the device, different device members have different numbers of V_{REF} groups.

(3) Banks 9 through 12 are enhanced PLL external clock output banks. These PLL banks utilize the adjacent V_{REF} group when voltage-referenced standards are implemented. For example, if an SSTL input is implemented in PLL bank 10, the voltage level at VREFB7 is the reference voltage level for the SSTL input.

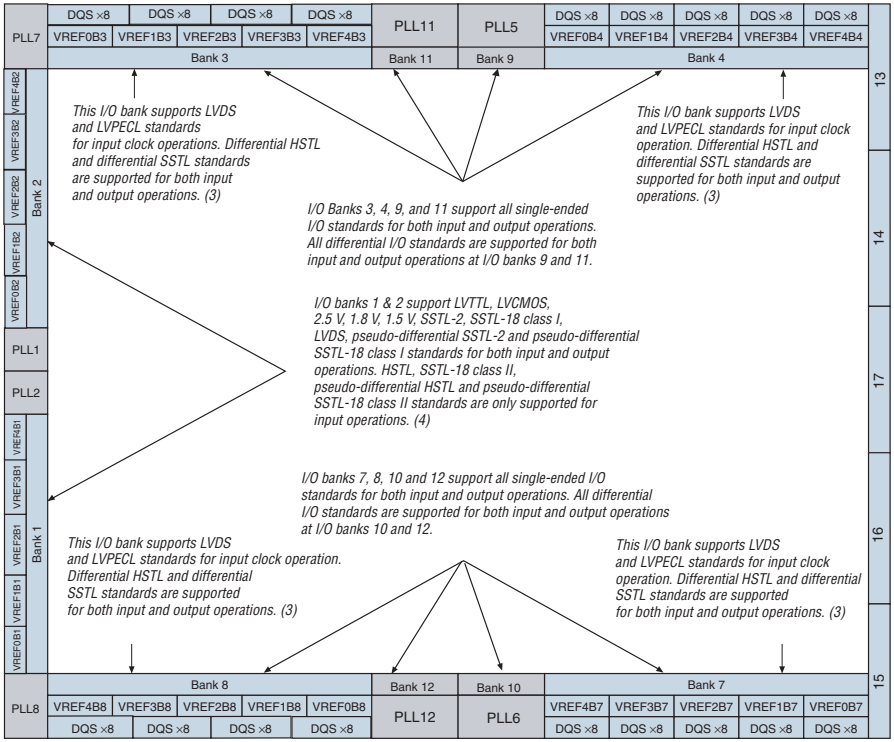
(4) Differential HSTL and differential SSTL standards are available for bidirectional operations on DQS pin and input-only operations on PLL clock input pins; LVDS, LVPECL, and HyperTransport standards are available for input-only operations on PLL clock input pins. See the *Selectable I/O standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* for more details.

(5) Quartus II software does not support differential SSTL and differential HSTL standards at left/right I/O banks. See the *Selectable I/O standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* if you need to implement these standards at these I/O banks.

(6) Banks 11 and 12 are available only in EP2S60, EP2S90, EP2S130, and EP2S180 devices.

(7) PLLs 7, 8, 9, 10, 11, and 12 are available only in EP2S60, EP2S90, EP2S130, and EP2S180 devices.

***Figure 5–2. Stratix II GX I/O Banks** Note (1), (2), (3), (4), (5), (6), and (7)*



Notes to Figure 5–2:

(1) Figure 5–2 is a top view of the silicon die which corresponds to a reverse view for flip-chip packages. It is a graphical representation only.

(2) Depending on size of the device, different device members have different number of V_{REF} groups. Refer to the pin list and the Quartus II software for exact locations.

(3) Banks 9 through 12 are enhanced PLL external clock output banks.

(4) Horizontal I/O banks feature transceiver and DPA circuitry for high speed differential I/O standards.

(5) Quartus II software does not support differential SSTL and differential HSTL standards at left/right I/O banks. Refer to the "Differential Pin Placement Guidelines" on page 5–21 if you need to implement these standards at these I/O banks.

(6) Banks 11 and 12 are available only in EP2SGX60C/D/E, EP2SGX90E/F, and EP2SGX130G.

(7) PLLs 7, 8, 11, and 12 are available only in EP2SGX60C/D/E, EP2SGXE/F, and EP2SGX130G.

Table 5–1 lists the differential I/O standards supported by each bank.

Table 5–1. Supported Differential I/O Types

Bank	Row I/O (Banks 1, 2, 5 and 6) (2)			Column I/O (Banks, 3, 4 and 7 through 12)		
Type	Clock Inputs	Clock Outputs	Data or Regular I/O Pins	Clock Inputs	Clock Outputs	Data or Regular I/O Pins
Differential HSTL				✓	✓	(1)
Differential SSTL				✓	✓	(1)
LVPECL				✓	✓	
LVDS	✓	✓	✓	✓	✓	
HyperTransport technology	✓	✓	✓			

Note to Table 5–1:
(1) Used as both inputs and outputs on the DQS/DQSn pins.
(2) Banks 5 and 6 are not available in Stratix II GX devices.

Table 5–2 shows the total number of differential channels available in Stratix II devices. The available channels are divided evenly between the left and right banks of the die. Non-dedicated clocks in the left and right banks can also be used as data receiver channels. The total number of receiver channels includes these four non-dedicated clock channels. Pin migration is available for different size devices in the same package.

Table 5–2. Differential Channels in Stratix II Devices (Part 1 of 2) Notes (1), (2), and (3)

Device	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA Within the 1,508-pin Fin
EP2S15	38 transmitters 42 receivers		38 transmitters 42 receivers			
EP2S30	38 transmitters 42 receivers		58 transmitters 62 receivers			
EP2S60	38 transmitters 42 receivers		58 transmitters 62 receivers		84 transmitters 84 receivers	
EP2S90		38 transmitters 42 receivers		64 transmitters 68 receivers	90 transmitters 94 receivers	118 transmitters 118 receivers
EP2S130				64 transmitters 68 receivers	88 transmitters 92 receivers	156 transmitters 156 receivers

Table 5–2. Differential Channels in Stratix II Devices (Part 2 of 2) Notes (1), (2), and (3)						
Device	**484-Pin FineLine BGA**	**484-Pin Hybrid FineLine BGA**	**672-Pin FineLine BGA**	**780-Pin FineLine BGA**	**1,020-Pin FineLine BGA**	**1,508-Pin FineLine BGA Within the 1,508-pin Fin**
EP2S180					88 transmitters 92 receivers	156 transmitters 156 receivers

Notes to Table 5–2:
(1) Pin count does not include dedicated PLL input pins.
(2) The total number of receiver channels includes the four non-dedicated clock channels that can optionally be used as data channels.
(3) Within the 1,508-pin FineLine BGA package, 92 receiver channels and 92 transmitter channels are vertically migratable.

Table 5–3 shows the total number of differential channels available in Stratix II GX devices. Non-dedicated clocks in the left bank can also be used as data receiver channels. The total number of receiver channels includes these four non-dedicated clock channels. Pin migration is available for different size devices in the same package.

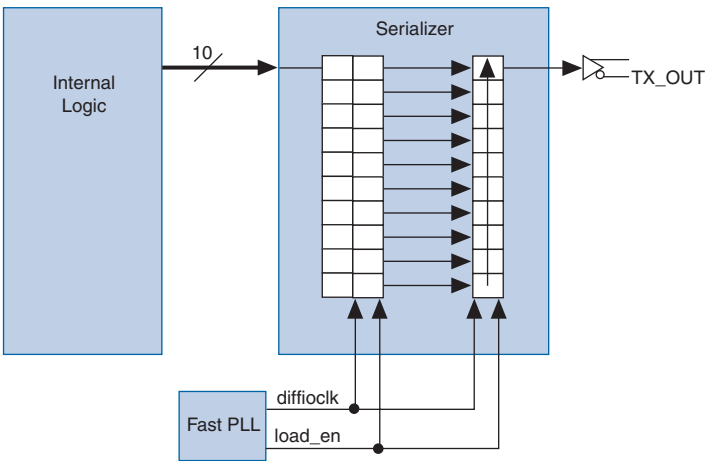
Table 5–3. Differential Channels in Stratix II GX Devices Notes (1), (2), (3)			
Device	**780-Pin FineLine BGA**	**1,152-Pin FineLine BGA**	**1,508-Pin FineLine BGA**
EP2SGX30	29 transmitters 31receivers		
EP2SGX60	29 transmitters 31 receivers	42 transmitters 42 receivers	
EP2SGX90		45 transmitters 47 receivers	59 transmitters 59 receivers
EP2SGX130			71 transmitters 73 receivers

Notes to Table 5–3:
(1) Pin count does not include dedicated PLL input pins.
(2) The total number of receiver channels includes the four non-dedicated clock channels that can optionally be used as data channels.
(3) EP2SGX30CF780 devices with four transceiver channels are vertically migratable to EP2SGX60CF780 devices with four transceiver channels. EP2SGX30DF780 devices with eight transceiver channels are vertically migratable to EP2SGX60DF780 devices with eight transceiver channels. EP2SGX60EF1152 devices with 12 transceiver channels are vertically migratable to EP2SGX90EF1152 devices with 12 transceiver channels. EP2SGX90FF1508 devices with 16 transceiver channels are vertically migratable to EP2SGX130GF1508 devices with 20 transceiver channels.

Differential Transmitter

The Stratix II and Stratix II GX transmitter has dedicated circuitry to provide support for LVDS and HyperTransport signaling. The dedicated circuitry consists of a differential buffer, a serializer, and a shared fast PLL. The differential buffer can drive out LVDS or HyperTransport signal levels that are statically set in the Quartus® II software. The serializer takes data from a parallel bus up to 10 bits wide from the internal logic, clocks it into the load registers, and serializes it using the shift registers before sending the data to the differential buffer. The most significant bit (MSB) is transmitted first. The load and shift registers are clocked by the `diffioclk` (a fast PLL clock running at the serial rate) and controlled by the load enable signal generated from the fast PLL. The serialization factor can be statically set to ×4, ×5, ×6, ×7, ×8, ×9, or ×10 using the Quartus II software. The load enable signal is automatically generated by the fast PLL and is derived from the serialization factor setting. Figure 5–3 is a block diagram of the Stratix II transmitter.

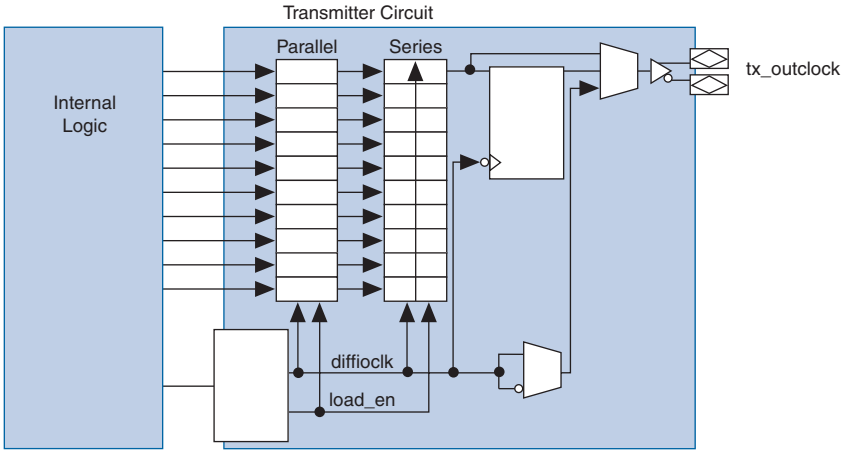
Figure 5–3. Transmitter Block Diagram



Each Stratix II and Stratix II GX transmitter data channel can be configured to operate as a transmitter clock output. This flexibility allows the designer to place the output clock near the data outputs to simplify board layout and reduce clock-to-data skew. Different applications often require specific clock to data alignments or specific data rate to clock rate factors. The transmitter can output a clock signal at the same rate as the data with a maximum frequency of 717 MHz. The output clock can also be divided by a factor of 2, 4, 8, or 10, depending on the serialization factor. The phase of the clock in relation to the data can be set at 0° or 180° (edge or center aligned). The fast PLL provides additional support for

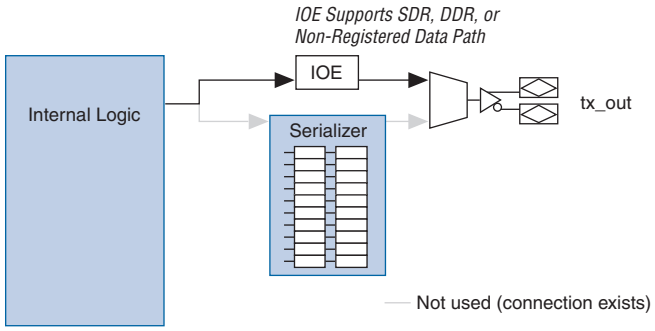
other phase shifts in 45° increments. These settings are made statically in the Quartus II MegaWizard® software. Figure 5–4 shows the transmitter in clock output mode.

Figure 5–4. Transmitter in Clock Output Mode



The serializer can be bypassed to support DDR (×2) and SDR (×1) operations. The I/O element (IOE) contains two data output registers that each can operate in either DDR or SDR mode. The clock source for the registers in the IOE can come from any routing resource, from the fast PLL, or from the enhanced PLL. Figure 5–5 shows the bypass path.

Figure 5–5. Serializer Bypass



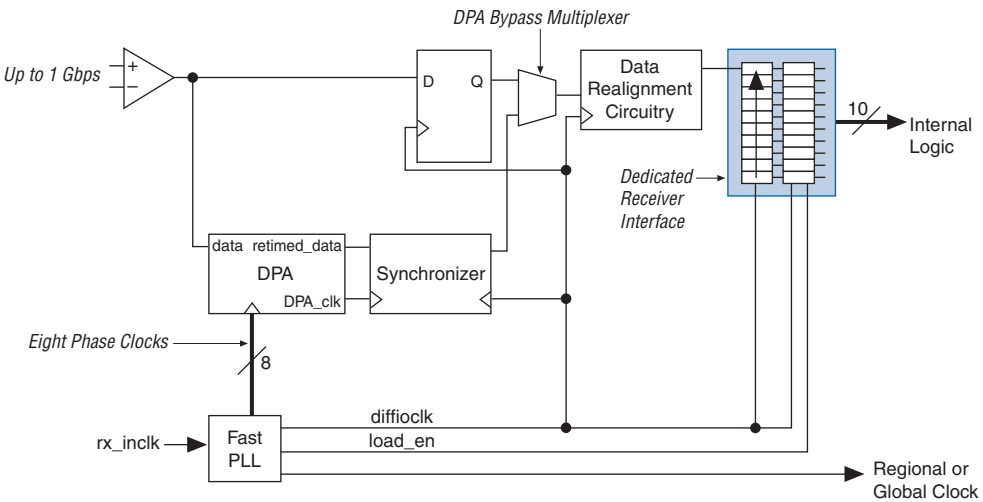
Differential Receiver

The receiver has dedicated circuitry to support high-speed LVDS and HyperTransport signaling, along with enhanced data reception. Each receiver consists of a differential buffer, dynamic phase aligner (DPA), synchronization FIFO buffer, data realignment circuit, deserializer, and a shared fast PLL. The differential buffer receives LVDS or HyperTransport signal levels, which are statically set by the Quartus II software. The DPA block aligns the incoming data to one of eight clock phases to maximize the receiver's skew margin. The DPA circuit can be bypassed on a channel-by-channel basis if it is not needed. Set the DPA bypass statically in the Quartus II MegaWizard Plug-In Manager or dynamically by using the optional RX_DPLL_ENABLE port.

The synchronizer circuit is a 1-bit wide by 6-bit deep FIFO buffer that compensates for any phase difference between the DPA block and the deserializer. If necessary, the data realignment circuit inserts a single bit of latency in the serial bit stream to align the word boundary. The deserializer includes shift registers and parallel load registers, and sends a maximum of 10 bits to the internal logic. The data path in the receiver is clocked by either the diffioclk signal or the DPA recovered clock. The deserialization factor can be statically set to 4, 5, 6, 7, 8, 9, or 10 by using the Quartus II software. The fast PLL automatically generates the load enable signal, which is derived from the deserialization factor setting.

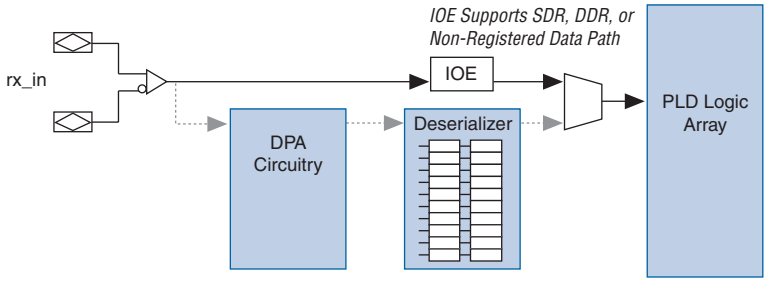
Figure 5–6 shows a block diagram of the receiver.

Figure 5–6. Receiver Block Diagram



The deserializer, like the serializer, can also be bypassed to support DDR (×2) and SDR (×1) operations. The DPA and data realignment circuit cannot be used when the deserializer is bypassed. The IOE contains two data input registers that can operate in DDR or SDR mode. The clock source for the registers in the IOE can come from any routing resource, from the fast PLL, or from the enhanced PLL. Figure 5–7 shows the bypass path.

Figure 5–7. Deserializer Bypass



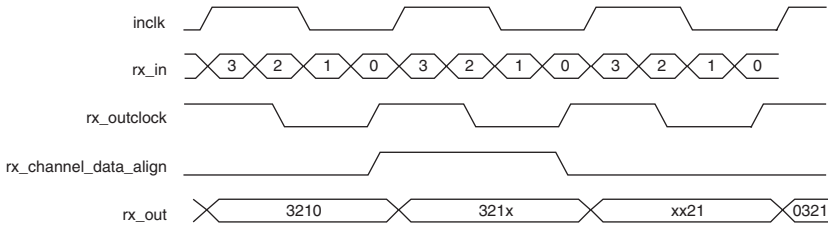
Receiver Data Realignment Circuit

The data realignment circuit aligns the word boundary of the incoming data by inserting bit latencies into the serial stream. An optional RX_CHANNEL_DATA_ALIGN port controls the bit insertion of each receiver independently controlled from the internal logic. The data slips one bit for every pulse on the RX_CHANNEL_DATA_ALIGN port. The following are requirements for the RX_CHANNEL_DATA_ALIGN port:

- The minimum pulse width is one period of the parallel clock in the logic array.
- The minimum low time between pulses is one period of parallel clock.
- There is no maximum high or low time.
- Valid data is available two parallel clock cycles after the rising edge of RX_CHANNEL_DATA_ALIGN.

Figure 5–8 shows receiver output (RX_OUT) after one bit slip pulse with the deserialization factor set to 4.

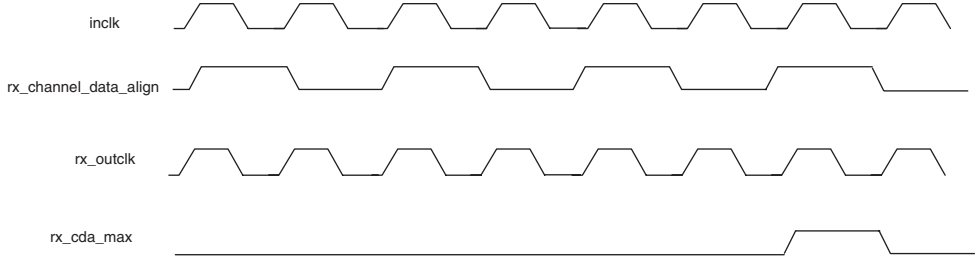
Figure 5–8. Data Realignment Timing



The data realignment circuit can have up to 11 bit-times of insertion before a rollover occurs. The programmable bit rollover point can be from 1 to 11 bit-times independent of the deserialization factor. An optional status port, rx_cda_max, is available to the FPGA from each channel to indicate when the preset rollover point is reached.

Figure 5–9 illustrates a preset value of four bit-times before rollover occurs. The rx_cda_max signal pulses for one rx_outclk cycle to indicate that the rollover has occurred.

Figure 5–9. Receiver Data Re-alignment Rollover

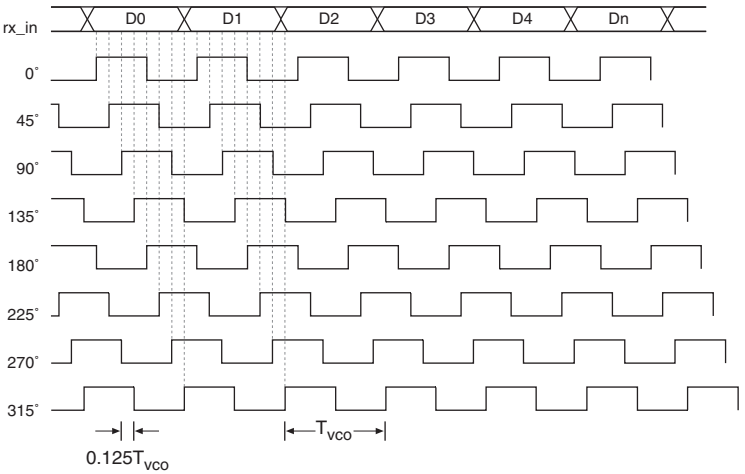


Dynamic Phase Aligner

The DPA block takes in high-speed serial data from the differential input buffer and selects one of eight phase clocks to sample the data. The DPA chooses a phase closest to the phase of the serial data. The maximum phase offset between the data and the phase-aligned clock is 1/8 UI, which is the maximum quantization error of the DPA. The eight phases

are equally divided, giving a 45-degree resolution. Figure 5–10 shows the possible phase relationships between the DPA clocks and the incoming serial data.

Figure 5–10. DPA Clock Phase to Data Bit Relationship



Each DPA block continuously monitors the phase of the incoming data stream and selects a new clock phase if needed. The selection of a new clock phase can be prevented by the optional RX_DPLL_HOLD port, which is available for each channel.

The DPA block requires a training pattern and a training sequence of at least 256 repetitions of the training pattern. The training pattern is not fixed, so you can use any training pattern with at least one transition on each channel. An optional output port, RX_DPA_LOCKED, is available to the internal logic, to indicate when the DPA block has settled on the closest phase to the incoming data phase. The RX_DPA_LOCKED de-asserts, depending on what is selected in the Quartus II MegaWizard Plug-In, when either a new phase is selected, or when the DPA has moved two phases in the same direction. The data may still be valid even when the RX_DPA_LOCKED is deasserted. Use data checkers to validate the data when RX_DPA_LOCKED is deasserted.

An independent reset port, RX_RESET, is available to reset the DPA circuitry. The DPA circuit must be retrained after reset.

Synchronizer

The synchronizer is a 1-bit × 6-bit deep FIFO buffer that compensates for the phase difference between the recovered clock from the DPA circuit and the `diffioclk` that clocks the rest of the logic in the receiver. The synchronizer can only compensate for phase differences, not frequency differences between the data and the receiver's `INCLK`. An optional port, `RX_FIFO_RESET`, is available to the internal logic to reset the synchronizer. The synchronizer is automatically reset when the DPA first locks to the incoming data. Altera® recommends using `RX_FIFO_RESET` to reset the synchronizer when the DPA signals a loss-of-lock condition beyond the initial locking condition.

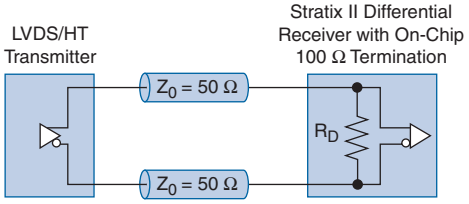
Differential I/O Termination

Stratix II and Stratix II GX devices provide an on-chip 100-Ω differential termination option on each differential receiver channel for LVDS and HyperTransport standards. The on-chip termination eliminates the need to supply an external termination resistor, simplifying the board design and reducing reflections caused by stubs between the buffer and the termination resistor. You can enable on-chip termination in the Quartus II assignments editor. Differential on-chip termination is supported across the full range of supported differential data rates.

For more information, refer to the High-Speed I/O Specifications section of the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook* or the High-Speed I/O Specifications section of the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook*.

Figure 5–11 illustrates on-chip termination.

Figure 5–11. On-Chip Differential Termination



On-chip differential termination is supported on all row I/O pins and on clock pins `CLK[0, 2, 8, 10]`. The clock pins `CLK[1, 3, 9, 11]`, and `FPLL[7..10]CLK`, and the clocks in the top and bottom I/O banks (`CLK[4..7, 12..15]`) do not support differential on-chip termination.

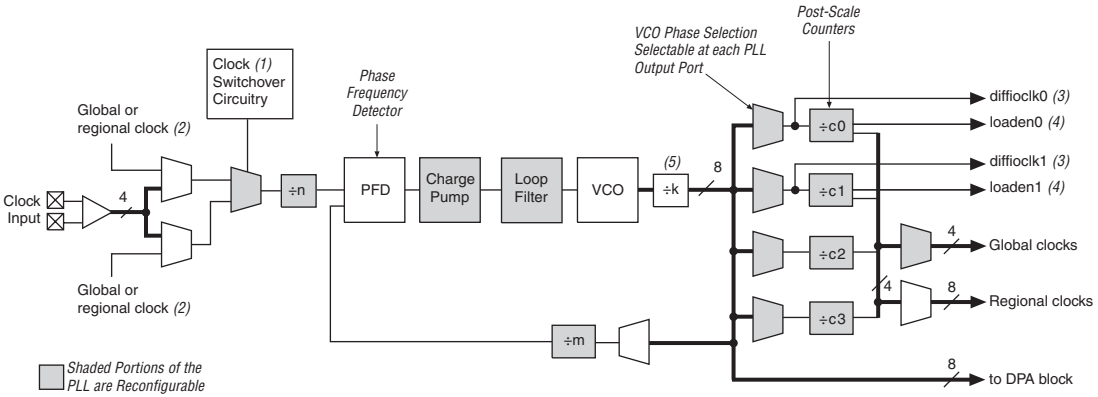
Fast PLL

The high-speed differential I/O receiver and transmitter channels use the fast PLL to generate the parallel global clocks (`rx-` or `tx-` clock) and high-speed clocks (`diffioclk`). Figure 5–12 shows the locations of the fast PLLs. The fast PLL VCO operates at the clock frequency of the data rate. Each fast PLL offers a single serial data rate support, but up to two separate serialization and/or deserialization factors (from the C0 and C1 fast PLL clock outputs) can be used. Clock switchover and dynamic fast PLL reconfiguration is available in high-speed differential I/O support mode.

For additional information on the fast PLL, refer to the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Handbook* or the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Handbook*.

Figure 5–12 shows a block diagram of the fast PLL in high-speed differential I/O support mode.

Figure 5–12. Fast PLL Block Diagram



Notes to Figure 5–12:

(1) Stratix II fast PLLs only support manual clock switchover.

(2) The global or regional clock input can be driven by an output from another PLL, a pin-driven dedicated global or regional clock, or through a clock control block provided the clock control block is fed by an output from another PLL or pin-driven dedicated global or regional clock.

(3) In high-speed differential I/O support mode, this high-speed PLL clock feeds the SERDES. Stratix II devices only support one rate of data transfer per fast PLL in high-speed differential I/O support mode.

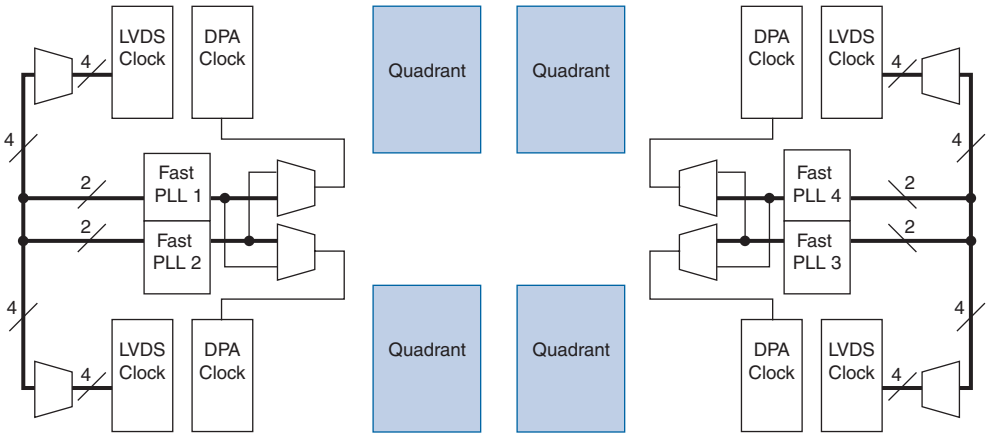
(4) This signal is a high-speed differential I/O support SERDES control signal.

(5) If the design enables this ÷2 counter, the device can use a VCO frequency range of 150 to 520 MHz.

Clocking

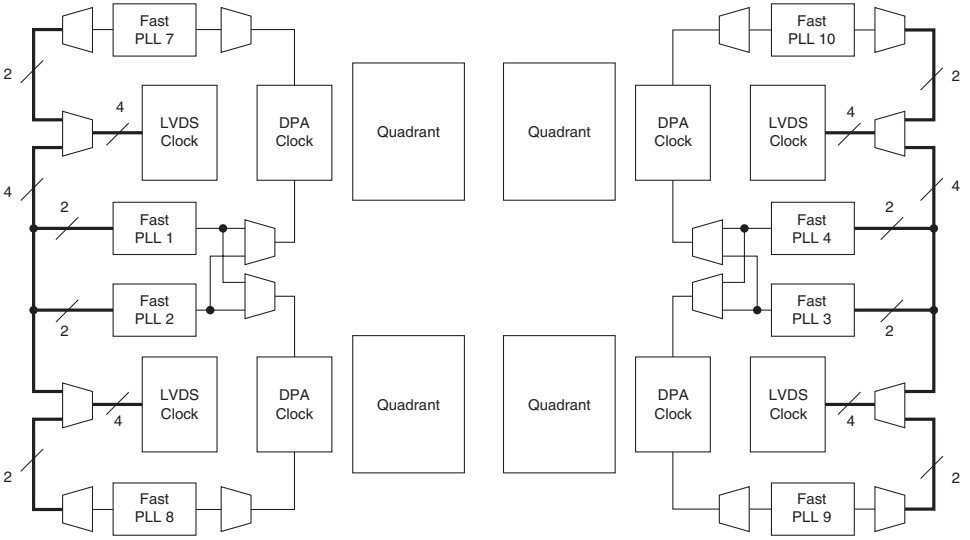
The fast PLLs feed in to the differential receiver and transmitter channels through the LVDS/DPA clock network. The center fast PLLs can independently feed the banks above and below them. The corner PLLs can feed only the banks adjacent to them. Figures 5–13 and 5–14 show the LVDS and DPA clock networks of the Stratix II devices.

Figure 5–13. Fast PLL and LVDS/DPA Clock for EP2S15, EP2S30, and EP2S60 Devices *Note (1)*



Note to Figure 5–13:
(1) Figure 5–13 applies to EP2S60 devices in the 484 and 672 pin packages.

Figure 5–14. Fast PLL and LVDS/DPA Clocks for EP2S60, EP2S90, EP2S130 and EP2S180 Devices Note (1)



Note to Figure 5–14:
(1) Figure 5–14 applies only to the EP2S60 in the 1020 Stratix II GX device.

Figures 5–15 and 5–16 show the Fast PLL and LVDS/DPA clock of the Stratix II GX devices.

Figure 5–15. Fast PLL and LVDS/DPA Clock for EP2SGX30C/D and EP2SGX60C/D Devices

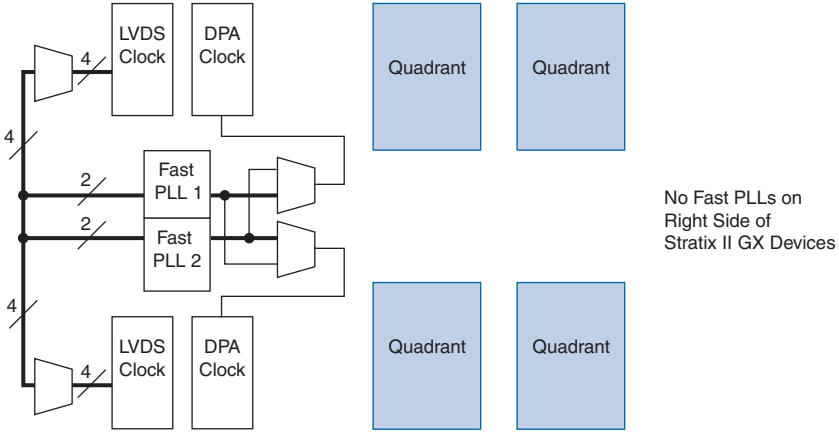
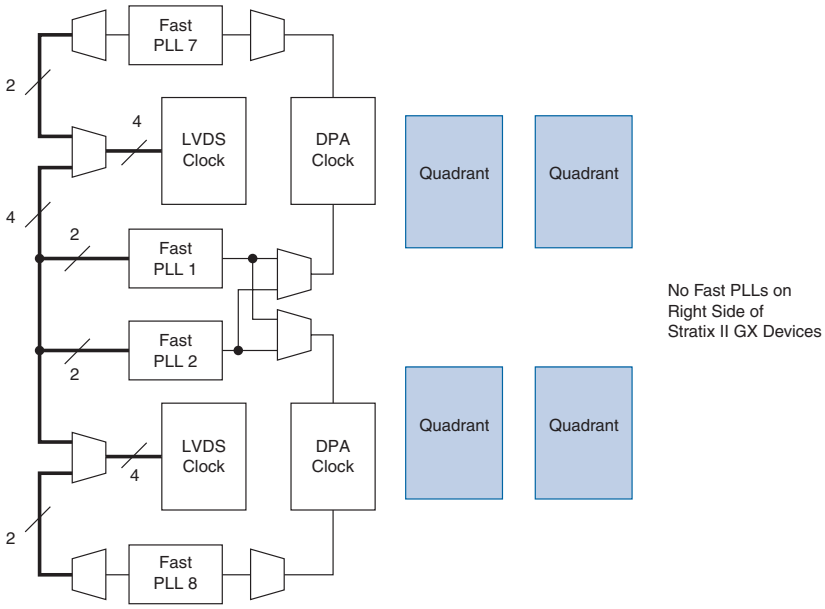


Figure 5–16. Fast PLL and LVDS/DPA Clocks for EP2SGX60E, EP2SGX90 and EP2SGX130 Devices



Source Synchronous Timing Budget

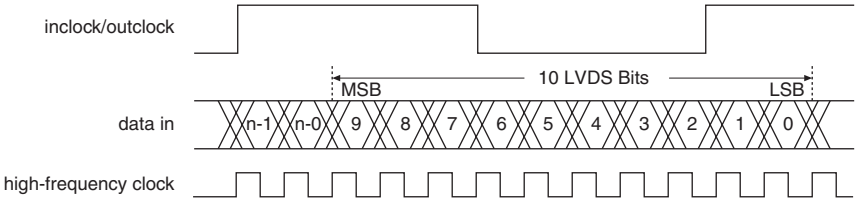
This section discusses the timing budget, waveforms, and specifications for source-synchronous signaling in Stratix II and Stratix II GX devices. LVDS and HyperTransport I/O standards enable high-speed data transmission. This high data transmission rate results in better overall system performance. To take advantage of fast system performance, it is important to understand how to analyze timing for these high-speed signals. Timing analysis for the differential block is different from traditional synchronous timing analysis techniques.

Rather than focusing on clock-to-output and setup times, source-synchronous timing analysis is based on the skew between the data and the clock signals. High-speed differential data transmission requires the use of timing parameters provided by IC vendors and is strongly influenced by board skew, cable skew, and clock jitter. This section defines the source-synchronous differential data orientation timing parameters, the timing budget definitions for Stratix II and Stratix II GX devices, and how to use these timing parameters to determine a design's maximum performance.

Differential Data Orientation

There is a set relationship between an external clock and the incoming data. For operation at 1 Gbps and SERDES factor of 10, the external clock is multiplied by 10, and phase-alignment can be set in the PLL to coincide with the sampling window of each data bit. The data is sampled on the falling edge of the multiplied clock. Figure 5–17 shows the data bit orientation of the ×10 mode.

Figure 5–17. Bit Orientation in the Quartus II Software



Differential I/O Bit Position

Data synchronization is necessary for successful data transmission at high frequencies. Figure 5–18 shows the data bit orientation for a channel operation. These figures are based on the following:

- SERDES factor equals clock multiplication factor
- Edge alignment is selected for phase alignment
- Implemented in hard SERDES

For other serialization factors use the Quartus II software tools and find the bit position within the word. The bit positions after deserialization are listed in Table 5–4.

Figure 5–18 also shows a functional waveform. Timing waveforms may produce different results. Altera recommends performing a timing simulation to predict actual device behavior.

Figure 5–18. Bit Order for One Channel of Differential Data

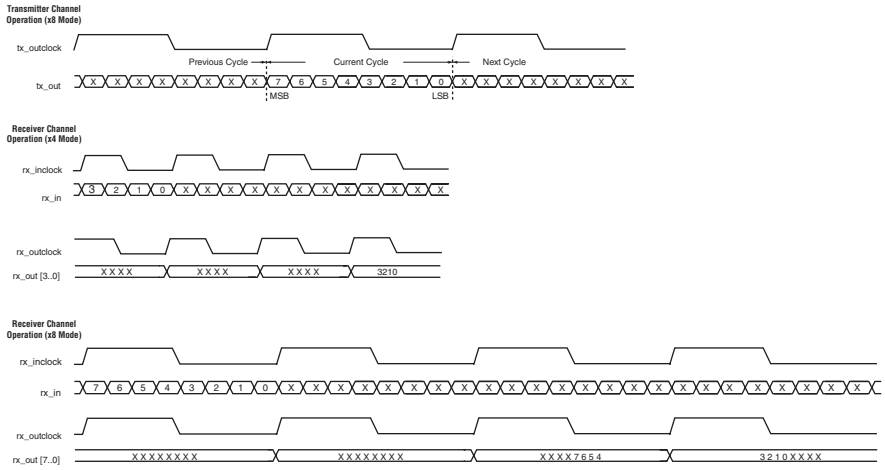


Table 5–4 shows the conventions for differential bit naming for 18 differential channels. The MSB and LSB positions increase with the number of channels used in a system.

Table 5–4. LVDS Bit Naming

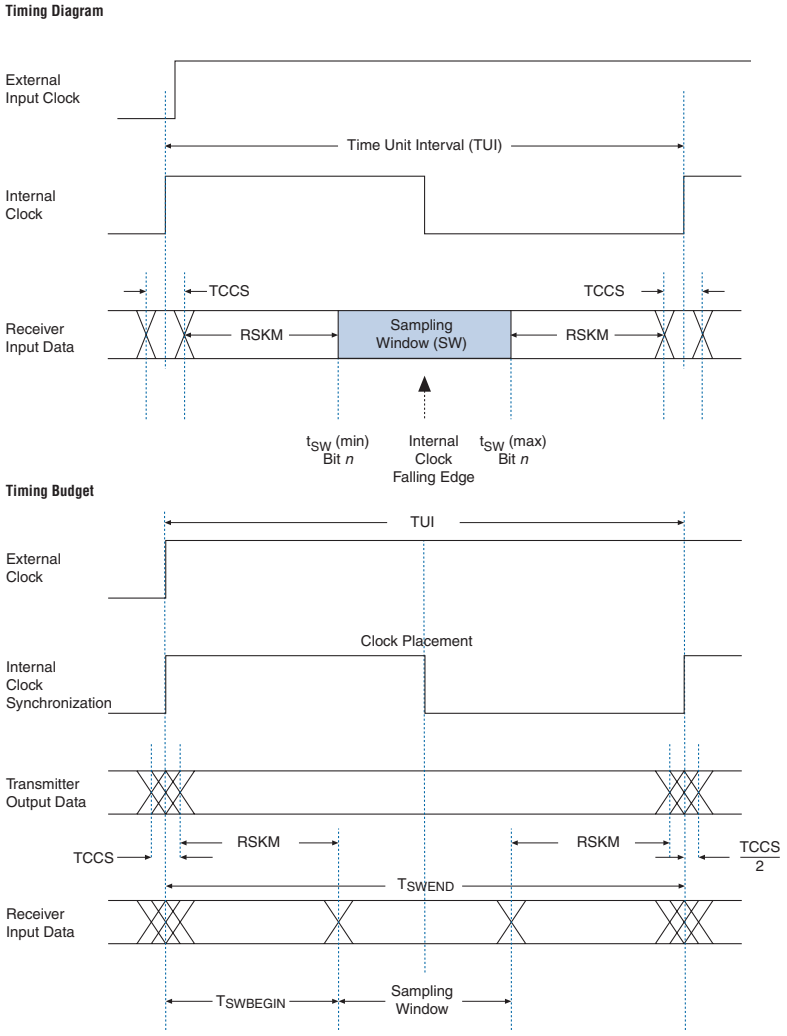
Receiver Channel Data Number	Internal 8-Bit Parallel Data	
	MSB Position	LSB Position
1	7	0
2	15	8
3	23	16
4	31	24
5	39	32
6	47	40
7	55	48
8	63	56
9	71	64
10	79	72
11	87	80
12	95	88
13	103	96
14	111	104
15	119	112
16	127	120
17	135	128
18	143	136

Receiver Skew Margin for Non-DPA

Changes in system environment, such as temperature, media (cable, connector, or PCB) loading effect, the receiver's setup and hold times, and internal skew, reduce the sampling window for the receiver. The timing margin between the receiver's clock input and the data input sampling window is called Receiver Skew Margin (RSKM). Figure 5–19 shows the relationship between the RSKM and the receiver's sampling window.

TCCS, RSKM, and the sampling window specifications are used for high-speed source-synchronous differential signals without DPA. When using DPA, these specifications are exchanged for the simpler single DPA jitter tolerance specification. For instance, the receiver skew is why each input with DPA selects a different phase of the clock, thus removing the requirement for this margin.

Figure 5–19. Differential High-Speed Timing Diagram and Timing Budget for Non-DPA



Differential Pin Placement Guidelines

In order to ensure proper high-speed operation, differential pin placement guidelines have been established. The Quartus II compiler automatically checks that these guidelines are followed and will issue an error message if these guidelines are not met. PLL driving distance information is separated into guidelines with and without DPA usage.

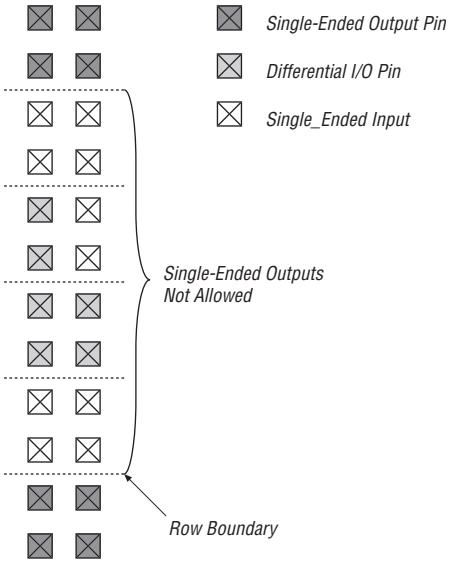
High-Speed Differential I/Os and Single-Ended I/Os

When a differential channel or channels of side banks are used (with or without DPA), you must adhere to the guidelines described in the following sections.

- Single-ended I/Os are allowed in the same bank as the LVDS channels (with or without DPA) as long as the single-ended I/O standard uses the same V_{CCIO} as the LVDS bank.
- Single-ended inputs can be in the same LAB row. Outputs cannot be on the same LAB row with LVDS I/Os. If input registers are used in the IOE, single-ended inputs cannot be in the same LAB row as an LVDS SERDES block.
- LVDS (non-SERDES) I/Os are allowed in the same row as LVDS SERDES but the use of IOE registers are not allowed.
- Single-ended outputs are limited to 120 mA drive strength on LVDS banks (with or without DPA).
    - LVTTL equation for maximum number of I/Os in an LVDS bank:
        - 120 mA = (number of LVTTL outputs) × (drive strength of each LVTTL output)
    - SSTL-2 equation:
        - 120 mA = (number of SSTL-2 I/Os) × (drive strength of each output) ÷ 2
    - LVTTL and SSTL-2 mix equation:
        - 120 mA= (total drive strength of all LVTTL outputs) + (total drive strength of all SSTL2 outputs) ÷ 2
- Single-ended inputs can be in the same LAB row as a differential channel using the SERDES circuitry; however, IOE input registers are not available for the single-ended I/Os placed in the same LAB row as differential I/Os. The same rule for input registers applies for non-SERDES differential inputs placed within the same LAB row as a SERDES differential channel. The input register must be implemented within the core logic. The same rule for input registers applies for non-SERDES differential inputs placed within the same LAB row as a SERDES differential channel.

- Single-ended output pins must be at least one LAB row away from differential output pins, as shown in Figure 5–20.

Figure 5–20. Single-Ended Output Pin Placement with Respect to Differential I/O Pins



DPA Usage Guidelines

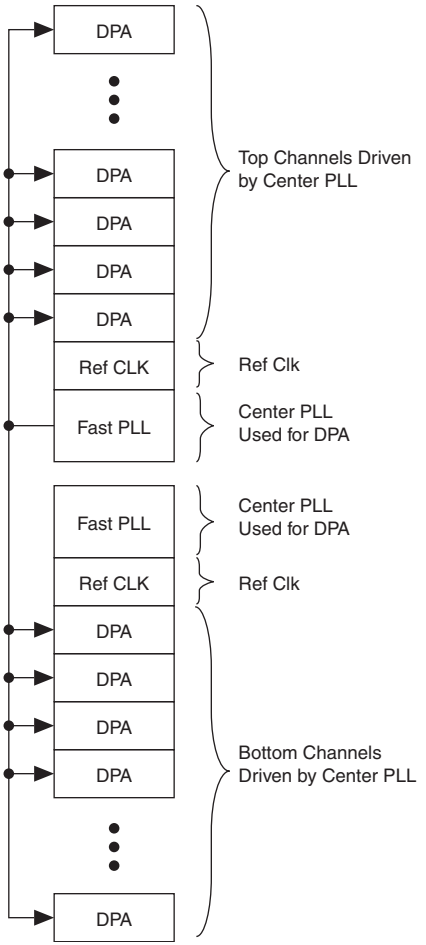
The Stratix II and Stratix II GX device have differential receivers and transmitters on the Row banks of the device. Each receiver has a dedicated DPA circuit to align the phase of the clock to the data phase of its associated channel. When a channel or channels of left or right banks are used in DPA mode, the guidelines listed below must be adhered to.

Fast PLL/DPA Channel Driving Distance

- Each fast PLL can drive up to 25 contiguous rows in DPA mode in a single bank (not including the reference clock row). The unbonded SERDES I/O rows are included in the 25 row calculation. These channels can be anywhere in the bank, their distance from the PLL is not relevant, but the channels must be within 25 rows of each other.

- Unused channels can be within the 25 row span, but all used channels must be in DPA mode from the same fast PLL. Center fast PLLs can drive two I/O banks simultaneously, up to 50 channels (25 on the upper bank and 25 on the lower bank) as shown in Figure 5–21.
- If one center fast PLL drives DPA channels in the upper and lower banks, the other center fast PLL cannot be used for DPA.

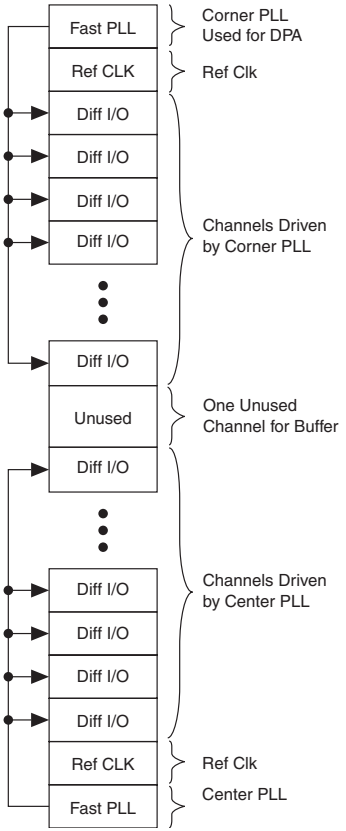
Figure 5–21. Driving Capabilities of a Center Fast PLL



Using Corner and Center Fast PLLs

- If a differential bank is being driven by two fast PLLs, where the corner PLL is driving one group and the center fast PLL is driving another group, there must be at least 1 row of separation between the two groups of DPA channels (see Figure 5–22). The two groups can operate at independent frequencies. Not all the channels are bonded out of the die. Each LAB row is considered a channel, whether or not it has I/O support.
- No separation is necessary if a single fast PLL is driving DPA channels as well as non-DPA channels as long as the DPA channels are contiguous.

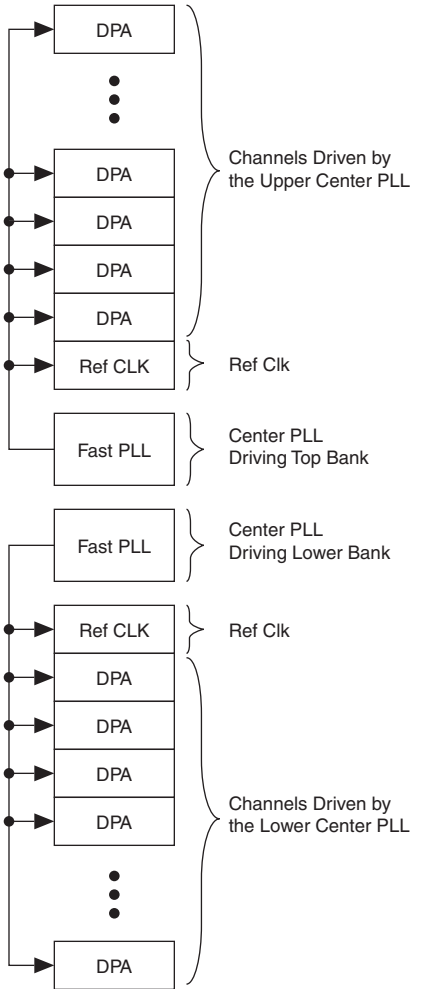
Figure 5–22. Usage of Corner and Center Fast PLLs Driving DPA Channels in a Single Bank



Using Both Center Fast PLLs

- Both center fast PLLs can be used for DPA as long as they drive DPA channels in their adjacent quadrant only. See Figure 5–23.
- Both center fast PLLs cannot be used for DPA if one of the fast PLLs drives the top and bottom banks, or if they are driving cross banks (e.g., the lower fast PLL drives the top bank and the top fast PLL drives the lower bank).

Figure 5–23. Center Fast PLL Usage When Driving DPA Channels



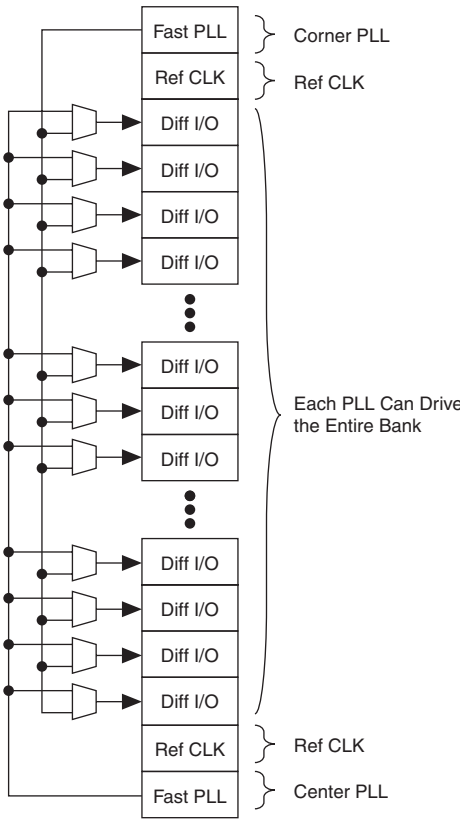
Non-DPA Differential I/O Usage Guidelines

When a differential channel or channels of left or right banks are used in non-DPA mode, you must adhere to the guidelines in the following sections.

Fast PLL/Differential I/O Driving Distance

- As shown in Figure 5–24, each fast PLL can drive all the channels in the entire bank.

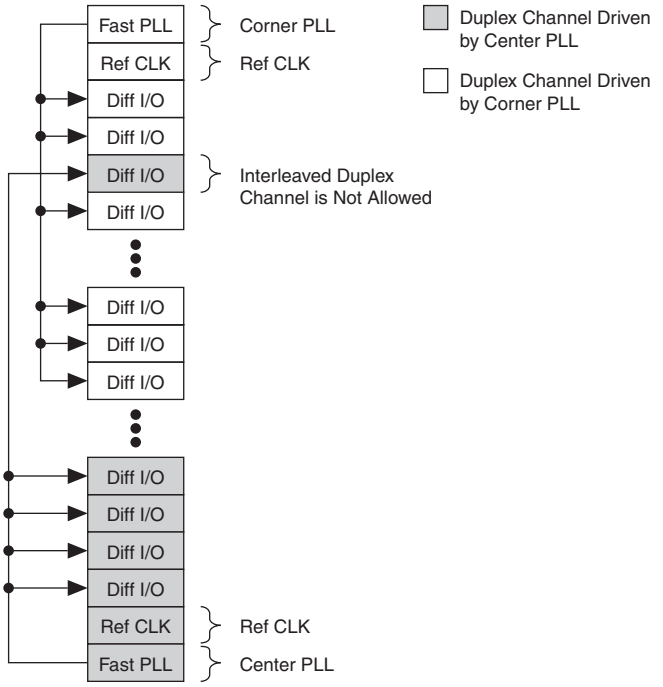
Figure 5–24. Fast PLL Driving Capability When Driving Non-DPA Differential Channels



Using Corner and Center Fast PLLs

- The corner and center fast PLLs can be used as long as the channels driven by separate fast PLLs do not have their transmitter or receiver channels interleaved. Figure 5–25 shows illegal placement of differential channels when using corner and center fast PLLs.
- If one fast PLL is driving transmitter channels only, and the other fast PLL drives receiver channels only, the channels driven by those fast PLLs can overlap each other.
- Center fast PLLs can be used for both transmitter and receiver channels.

Figure 5–25. Illegal Placement of Interlaced Duplex Channels in an I/O Bank



Board Design Considerations

This section explains how to achieve the optimal performance from the Stratix II and Stratix II GX high-speed I/O block and ensure first-time success in implementing a functional design with optimal signal quality.

For more information on board layout recommendations and I/O pin terminations, refer to *AN 224: High-Speed Board Layout Guidelines*.

To achieve the best performance from the device, pay attention to the impedances of traces and connectors, differential routing, and termination techniques.

Use this section together with the *Stratix II Device Family Data Sheet* in volume 1 of the *Stratix II Device Handbook*.

The Stratix II and Stratix II GX high-speed module generates signals that travel over the media at frequencies as high as one Gbps. Board designers should use the following guidelines:

- Base board designs on controlled differential impedance. Calculate and compare all parameters such as trace width, trace thickness, and the distance between two differential traces.
- Place external reference resistors as close to receiver input pins as possible.
- Use surface mount components.
- Avoid 90° or 45° corners.
- Use high-performance connectors such as HMZD or VHDM connectors for backplane designs. Two suppliers of high-performance connectors are Teradyne Corp (**www.teradyne.com**) and Tyco International Ltd. (**www.tyco.com**).
- Design backplane and card traces so that trace impedance matches the connector's or the termination's impedance.
- Keep an equal number of vias for both signal traces.
- Create equal trace lengths to avoid skew between signals. Unequal trace lengths also result in misplaced crossing points and system margins when the TCCS value increases.
- Limit vias, because they cause impedance discontinuities.
- Use the common bypass capacitor values such as 0.001, 0.01, and 0.1 µF to decouple the fast PLL power and ground planes. You can also use 0.0047 µF and 0.047 µF.
- Keep switching TTL signals away from differential signals to avoid possible noise coupling.
- Do not route TTL clock signals to areas under or above the differential signals.
- Route signals on adjacent layers orthogonally to each other.

Conclusion

Stratix II and Stratix II GX high-speed differential inputs and outputs, with their DPA and data realignment circuitry, allow users to build a robust multi-Gigabit system. The DPA circuitry allows users to compensate for any timing skews resulting from physical layouts. The data realignment circuitry allows the devices to align the data packet between the transmitter and receiver. Together with the on-chip differential termination, Stratix II and Stratix II GX devices can be used as a single-chip solution for high-speed applications.

Referenced Documents

This chapter references the following documents:

- *AN 224: High-Speed Board Layout Guidelines*
- *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Handbook*
- *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II GX Device Handbook*
- *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Handbook*
- *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II GX Handbook*
- *Selectable I/O standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook*
- *Stratix II Device Family Data Sheet* in volume 1 of the *Stratix II Device Handbook*

Document Revision History

Table 5–5 shows the revision history for this chapter.

Table 5–5. Document Revision History (Part 1 of 2)

Date and Document Version	Changes Made	Summary of Changes
January 2008, v2.2	Updated Figure 5–2.	—
	Added "Referenced Documents" section.	—
	Minor text edits.	—
	Added Figure 5–9.	—
	Updated "Receiver Data Realignment Circuit".	—
	For the *Stratix II GX Device Handbook* only: Formerly chapter 10. The chapter number changed due to the addition of the *Stratix II GX Dynamic Reconfiguration* chapter.	—
May 2007, v2.1	Updated entire chapter to include Stratix II GX information.	—
	Changed chapter part number.	—
	Fixed two types in "High-Speed Differential I/Os and Single-Ended I/Os" section	—

Table 5–5. Document Revision History (Part 2 of 2)

Date and Document Version	Changes Made	Summary of Changes
February 2007 v2.0	This chapter changed from High-Speed, Source-Synchronous Differential I/O Interfaces in Stratix II GX Devices to "High-Speed Differential I/O Interfaces with DPA in Stratix II and Stratix II GX Devices".	—
	Added the "Document Revision History" section to this chapter.	—
	Added "and Stratix II GX" after each instance of "Stratix II".	—
	Updated Figures 10–4, 10–20, 10–22.	—
	Updated Note (4) of Figure 10–2.	—
	Updated Table 10–1.	—
	Updated the following sections: • "I/O Banks" • "Differential I/O Termination" • "Fast PLL " • "Differential I/O Bit Position" • "DPA Usage Guidelines" • "Fast PLL/DPA Channel Driving Distance"	—
	Updated Note (1) of Tables 10–2 and 10–3.	—
	Added Note (5) to Figure 10–11.	—
	Added Table 10–3.	—
	Added Figures 10–14, 10–15, 10–19.	—
	Deleted old section called High-Speed Differential I/Os and Single-Ended I/Os and added a new "High-Speed Differential I/Os and Single-Ended I/Os" section.	—
	Deleted DPA and Single-Ended I/Os section.	—
	Updated title and added Note (1) to Figure 10–12.	—
	Added Note (1) to Figure 10–13.	—
April 2006, v1.2	• Updated all the MegaWizard Plug-In Manager figures to match the Quartus II software GUI. • Updated "Dedicated Source-Synchronous Circuitry" section, including Table 10–3.	—
February 2006, v1.1	• Updated chapter number from 9 to 10. • Updated Figures 10–11 and 10–12.	—
October 2005 v1.0	Added chapter to the *Stratix II GX Device Handbook*.	—