

## IEEE Std. 1149.1 JTAG Boundary- Scan Support

All Stratix® II devices provide Joint Test Action Group (JTAG) boundary-scan test (BST) circuitry that complies with the IEEE Std. 1149.1. JTAG boundary-scan testing can be performed either before or after, but not during configuration. Stratix II devices can also use the JTAG port for configuration with the Quartus® II software or hardware using either Jam Files (.jam) or Jam Byte-Code Files (.jbc).

Stratix II devices support IOE I/O standard setting reconfiguration through the JTAG BST chain. The JTAG chain can update the I/O standard for all input and output pins any time before or during user mode through the CONFIG\_IO instruction. You can use this capability for JTAG testing before configuration when some of the Stratix II pins drive or receive from other devices on the board using voltage-referenced standards. Because the Stratix II device may not be configured before JTAG testing, the I/O pins may not be configured for appropriate electrical standards for chip-to-chip communication. Programming those I/O standards via JTAG allows you to fully test I/O connections to other devices.

A device operating in JTAG mode uses four required pins, TDI, TDO, TMS, and TCK, and one optional pin, TRST. The TCK pin has an internal weak pull-down resistor, while the TDI, TMS and TRST pins have weak internal pull-ups. The JTAG input pins are powered by the 3.3-V VCCPD pins. The TDO output pin is powered by the VCCIO power supply of bank 4.

Stratix II devices also use the JTAG port to monitor the logic operation of the device with the SignalTap® II embedded logic analyzer. Stratix II devices support the JTAG instructions shown in [Table 3-1](#).



Stratix II, Stratix, Cyclone® II, and Cyclone devices must be within the first 17 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Stratix II, Stratix, Cyclone II, or Cyclone devices are in the 18th or further position, they fail configuration. This does not affect SignalTap II.

The Stratix II device instruction register length is 10 bits and the USERCODE register length is 32 bits. [Tables 3-2](#) and [3-3](#) show the boundary-scan register length and device IDCODE information for Stratix II devices.

<b>Table 3–1. Stratix II JTAG Instructions</b>		
<b>JTAG Instruction</b>	<b>Instruction Code</b>	<b>Description</b>
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap II embedded logic analyzer.
EXTEST (1)	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO.
HIGHZ (1)	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP (1)	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register.
ICR instructions		Used when configuring a Stratix II device via the JTAG port with a USB Blaster, MasterBlaster™, ByteBlasterMV™, or ByteBlaster II download cable, or when using a .jam or .jbc via an embedded processor or JRunner.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO (2)	00 0000 1101	Allows configuration of I/O standards through the JTAG chain for JTAG testing. Can be executed before, during, or after configuration. Stops configuration if executed during configuration. Once issued, the CONFIG_IO instruction holds nSTATUS low to reset the configuration device. nSTATUS is held low until the IOE configuration register is loaded and the TAP controller state machine transitions to the UPDATE_DR state.
SignalTap II instructions		Monitors internal device operation with the SignalTap II embedded logic analyzer.

**Notes to Table 3–1:**

- (1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.
- (2) For more information on using the CONFIG\_IO instruction, see the *MorphIO: An I/O Reconfiguration Solution for Altera Devices White Paper*.

The Quartus II software has an Auto Usercode feature where you can choose to use the checksum value of a programming file as the JTAG user code. If selected, the checksum is automatically loaded to the USERCODE register. Turn on the **Auto Usercode** option by clicking **Device & Pin Options**, then **General**, in the **Settings** dialog box (Assignments menu).

**Table 3–2. Stratix II Boundary-Scan Register Length**

Device	Boundary-Scan Register Length
EP2S15	1,140
EP2S30	1,692
EP2S60	2,196
EP2S90	2,748
EP2S130	3,420
EP2S180	3,948

**Table 3–3. 32-Bit Stratix II Device IDCODE**

Device	IDCODE (32 Bits) (1)			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) (2)
EP2S15	0000	0010 0000 1001 0001	000 0110 1110	1
EP2S30	0000	0010 0000 1001 0010	000 0110 1110	1
EP2S60	0001	0010 0000 1001 0011	000 0110 1110	1
EP2S90	0000	0010 0000 1001 0100	000 0110 1110	1
EP2S130	0000	0010 0000 1001 0101	000 0110 1110	1
EP2S180	0000	0010 0000 1001 0110	000 0110 1110	1

**Notes to Table 3–3:**

- (1) The most significant bit (MSB) is on the left.
- (2) The IDCODE's least significant bit (LSB) is always 1.



Stratix, Stratix II, Cyclone, and Cyclone II devices must be within the first 17 devices in a JTAG chain. All of these devices have the same JTAG controller. If any of the Stratix, Stratix II, Cyclone, and Cyclone II devices are in the 18th or after they fail configuration. This does not affect SignalTap II.



For more information on JTAG, see the following documents:

- The *IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing for Stratix II & Stratix II GX Devices* chapter of the *Stratix II Device Handbook, Volume 2* or the *Stratix II GX Device Handbook, Volume 2*
- Jam Programming & Test Language Specification

## SignalTap II Embedded Logic Analyzer

Stratix II devices feature the SignalTap II embedded logic analyzer, which monitors design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry. You can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages, such as FineLine BGA® packages, because it can be difficult to add a connection to a pin during the debugging process after a board is designed and manufactured.

## Configuration

The logic, circuitry, and interconnects in the Stratix II architecture are configured with CMOS SRAM elements. Altera® FPGA devices are reconfigurable and every device is tested with a high coverage production test program so you do not have to perform fault testing and can instead focus on simulation and design verification.

Stratix II devices are configured at system power-up with data stored in an Altera configuration device or provided by an external controller (e.g., a MAX® II device or microprocessor). Stratix II devices can be configured using the fast passive parallel (FPP), active serial (AS), passive serial (PS), passive parallel asynchronous (PPA), and JTAG configuration schemes. The Stratix II device's optimized interface allows microprocessors to configure it serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat Stratix II devices as memory and configure them by writing to a virtual memory location, making reconfiguration easy.

In addition to the number of configuration methods supported, Stratix II devices also offer the design security, decompression, and remote system upgrade features. The design security feature, using configuration bitstream encryption and AES technology, provides a mechanism to protect your designs. The decompression feature allows Stratix II FPGAs to receive a compressed configuration bitstream and decompress this data in real-time, reducing storage requirements and configuration time. The remote system upgrade feature allows real-time system upgrades from remote locations of your Stratix II designs. For more information, see [“Configuration Schemes” on page 3–7](#).

## Operating Modes

The Stratix II architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called command mode. Normal device operation is called user mode.

SRAM configuration elements allow Stratix II devices to be reconfigured in-circuit by loading new configuration data into the device. With real-time reconfiguration, the device is forced into command mode with a device pin. The configuration process loads different configuration data, reinitializes the device, and resumes user-mode operation. You can perform in-field upgrades by distributing new configuration files either within the system or remotely.

PORSEL is a dedicated input pin used to select POR delay times of 12 ms or 100 ms during power-up. When the PORSEL pin is connected to ground, the POR time is 100 ms; when the PORSEL pin is connected to  $V_{CC}$ , the POR time is 12 ms.

The nIO PULLUP pin is a dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose configuration I/O pins (nCS0, ASDO, DATA [7 . . 0], nWS, nRS, RDYnBSY, nCS, CS, RUnLU, PGM [2 . . 0], CLKUSR, INIT\_DONE, DEV\_OE, DEV\_CLR) are on or off before and during configuration. A logic high (1.5, 1.8, 2.5, 3.3 V) turns off the weak internal pull-ups, while a logic low turns them on.

Stratix II devices also offer a new power supply,  $V_{CCPD}$ , which must be connected to 3.3 V in order to power the 3.3-V/2.5-V buffer available on the configuration input pins and JTAG pins.  $V_{CCPD}$  applies to all the JTAG input pins (TCK, TMS, TDI, and TRST) and the configuration input pins when VCCSEL is connected to ground. See [Table 3–4](#) for more information on the pins affected by VCCSEL.

The VCCSEL pin allows the  $V_{CCIO}$  setting (of the banks where the configuration inputs reside) to be independent of the voltage required by the configuration inputs. Therefore, when selecting the  $V_{CCIO}$ , the  $V_{IL}$  and  $V_{IH}$  levels driven to the configuration inputs do not have to be a concern.

The PLL\_ENA pin and the configuration input pins (Table 3–4) have a dual buffer design: a 3.3-V/2.5-V input buffer and a 1.8-V/1.5-V input buffer. The VCCSEL input pin selects which input buffer is used. The 3.3-V/2.5-V input buffer is powered by V<sub>CCPD</sub>, while the 1.8-V/1.5-V input buffer is powered by V<sub>CCIO</sub>. Table 3–4 shows the pins affected by VCCSEL.

Pin	VCCSEL = LOW (connected to GND)	VCCSEL = HIGH (connected to V <sub>CCPD</sub> )
nSTATUS (when used as an input)	3.3/2.5-V input buffer is selected. Input buffer is powered by V <sub>CCPD</sub> .	1.8/1.5-V input buffer is selected. Input buffer is powered by V <sub>CCIO</sub> of the I/O bank.
nCONFIG		
CONF_DONE (when used as an input)		
DATA [7 . . 0]		
nCE		
DCLK (when used as an input)		
CS		
nWS		
nRS		
nCS		
CLKUSR		
DEV_OE		
DEV_CLRn		
RUnLU		
PLL_ENA		

VCCSEL is sampled during power-up. Therefore, the VCCSEL setting cannot change on the fly or during a reconfiguration. The VCCSEL input buffer is powered by V<sub>CCINT</sub> and must be hardwired to V<sub>CCPD</sub> or ground. A logic high VCCSEL connection selects the 1.8-V/1.5-V input buffer, and a logic low selects the 3.3-V/2.5-V input buffer. VCCSEL should be set to comply with the logic levels driven out of the configuration device or MAX<sup>®</sup> II/microprocessor.

If you need to support configuration input voltages of 3.3 V/2.5 V, you should set the VCCSEL to a logic low; you can set the V<sub>CCIO</sub> of the I/O bank that contains the configuration inputs to any supported voltage. If

you need to support configuration input voltages of 1.8 V/1.5 V, you should set the VCCSEL to a logic high and the V<sub>CCIO</sub> of the bank that contains the configuration inputs to 1.8 V/1.5 V.



For more information on multi-volt support, including information on using TDO and nCEO in multi-volt systems, refer to the *Stratix II Architecture* chapter in volume 1 of the *Stratix II Device Handbook*.

## Configuration Schemes

You can load the configuration data for a Stratix II device with one of five configuration schemes (see Table 3–5), chosen on the basis of the target application. You can use a configuration device, intelligent controller, or the JTAG port to configure a Stratix II device. A configuration device can automatically configure a Stratix II device at system power-up.

You can configure multiple Stratix II devices in any of the five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

Stratix II FPGAs offer the following:

- Configuration data decompression to reduce configuration file storage
- Design security using configuration data encryption to protect your designs
- Remote system upgrades for remotely updating your Stratix II designs

Table 3–5 summarizes which configuration features can be used in each configuration scheme.

Configuration Scheme	Configuration Method	Design Security	Decompression	Remote System Upgrade
FPP	MAX II device or microprocessor and flash device	✓ (1)	✓ (1)	✓
	Enhanced configuration device		✓ (2)	✓
AS	Serial configuration device	✓	✓	✓ (3)
PS	MAX II device or microprocessor and flash device	✓	✓	✓
	Enhanced configuration device	✓	✓	✓
	Download cable (4)	✓	✓	

**Table 3–5. Stratix II Configuration Features (Part 2 of 2)**

Configuration Scheme	Configuration Method	Design Security	Decompression	Remote System Upgrade
PPA	MAX II device or microprocessor and flash device			✓
JTAG	Download cable (4)			
	MAX II device or microprocessor and flash device			

**Notes for Table 3–5:**

- (1) In these modes, the host system must send a DCLK that is 4× the data rate.
- (2) The enhanced configuration device decompression feature is available, while the Stratix II decompression feature is not available.
- (3) Only remote update mode is supported when using the AS configuration scheme. Local update mode is not supported.
- (4) The supported download cables include the Altera USB Blaster universal serial bus (USB) port download cable, MasterBlaster serial/USB communications cable, ByteBlaster II parallel port download cable, and the ByteBlasterMV parallel port download cable.



See the *Configuring Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook* for more information about configuration schemes in Stratix II and Stratix II GX devices.

*Device Security Using Configuration Bitstream Encryption*

Stratix II FPGAs are the industry’s first FPGAs with the ability to decrypt a configuration bitstream using the Advanced Encryption Standard (AES) algorithm. When using the design security feature, a 128-bit security key is stored in the Stratix II FPGA. To successfully configure a Stratix II FPGA that has the design security feature enabled, it must be configured with a configuration file that was encrypted using the same 128-bit security key. The security key can be stored in non-volatile memory inside the Stratix II device. This non-volatile memory does not require any external devices, such as a battery back-up, for storage.





An encryption configuration file is the same size as a non-encryption configuration file. When using a serial configuration scheme such as passive serial (PS) or active serial (AS), configuration time is the same whether or not the design security feature is enabled. If the fast passive parallel (FPP) scheme is used with the design security or decompression feature, a  $4 \times$  DCLK is required. This results in a slower configuration time when compared to the configuration time of an FPGA that has neither the design security, nor decompression feature enabled. For more information about this feature, refer to *AN 341: Using the Design Security Feature in Stratix II Devices*. Contact your local Altera sales representative to request this document.

### *Device Configuration Data Decompression*

Stratix II FPGAs support decompression of configuration data, which saves configuration memory space and time. This feature allows you to store compressed configuration data in configuration devices or other memory, and transmit this compressed bit stream to Stratix II FPGAs. During configuration, the Stratix II FPGA decompresses the bit stream in real time and programs its SRAM cells.

Stratix II FPGAs support decompression in the FPP (when using a MAX II device/microprocessor and flash memory), AS and PS configuration schemes. Decompression is not supported in the PPA configuration scheme nor in JTAG-based configuration.

### *Remote System Upgrades*

Shortened design cycles, evolving standards, and system deployments in remote locations are difficult challenges faced by modern system designers. Stratix II devices can help effectively deal with these challenges with their inherent re-programmability and dedicated circuitry to perform remote system updates. Remote system updates help deliver feature enhancements and bug fixes without costly recalls, reduce time to market, and extend product life.

Stratix II FPGAs feature dedicated remote system upgrade circuitry to facilitate remote system updates. Soft logic (Nios<sup>®</sup> processor or user logic) implemented in the Stratix II device can download a new configuration image from a remote location, store it in configuration memory, and direct the dedicated remote system upgrade circuitry to initiate a reconfiguration cycle. The dedicated circuitry performs error detection during and after the configuration process, recovers from any error condition by reverting back to a safe configuration image, and provides

error status information. This dedicated remote system upgrade circuitry avoids system downtime and is the critical component for successful remote system upgrades.

RSC is supported in the following Stratix II configuration schemes: FPP, AS, PS, and PPA. RSC can also be implemented in conjunction with advanced Stratix II features such as real-time decompression of configuration data and design security using AES for secure and efficient field upgrades.



See the *Remote System Upgrades With Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook* for more information about remote configuration in Stratix II devices.

### Configuring Stratix II FPGAs with JRunner

JRunner is a software driver that configures Altera FPGAs, including Stratix II FPGAs, through the ByteBlaster II or ByteBlasterMV cables in JTAG mode. The programming input file supported is in Raw Binary File (**.rbf**) format. JRunner also requires a Chain Description File (**.cdf**) generated by the Quartus II software. JRunner is targeted for embedded JTAG configuration. The source code is developed for the Windows NT operating system (OS), but can be customized to run on other platforms.



For more information on the JRunner software driver, see the *JRunner Software Driver: An Embedded Solution to the JTAG Configuration White Paper* and the source files on the Altera web site (**www.altera.com**).

### Programming Serial Configuration Devices with SRunner

A serial configuration device can be programmed in-system by an external microprocessor using SRunner. SRunner is a software driver developed for embedded serial configuration device programming that can be easily customized to fit in different embedded systems. SRunner is able to read a **.rpd** file (Raw Programming Data) and write to the serial configuration devices. The serial configuration device programming time using SRunner is comparable to the programming time when using the Quartus II software.



For more information about SRunner, see the *SRunner: An Embedded Solution for EPCS Programming White Paper* and the source code on the Altera web site at **www.altera.com**.



For more information on programming serial configuration devices, see the Serial Configuration Devices (EPCS1 & EPCS4) Data Sheet in the *Configuration Handbook*.

## Configuring Stratix II FPGAs with the MicroBlaster Driver

The MicroBlaster™ software driver supports an RBF programming input file and is ideal for embedded FPP or PS configuration. The source code is developed for the Windows NT operating system, although it can be customized to run on other operating systems. For more information on the MicroBlaster software driver, see the *Configuring the MicroBlaster Fast Passive Parallel Software Driver White Paper* or the *Configuring the MicroBlaster Passive Serial Software Driver White Paper* on the Altera web site ([www.altera.com](http://www.altera.com)).

## PLL Reconfiguration

The phase-locked loops (PLLs) in the Stratix II device family support reconfiguration of their multiply, divide, VCO-phase selection, and bandwidth selection settings without reconfiguring the entire device. You can use either serial data from the logic array or regular I/O pins to program the PLL's counter settings in a serial chain. This option provides considerable flexibility for frequency synthesis, allowing real-time variation of the PLL frequency and delay. The rest of the device is functional while reconfiguring the PLL.



See the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook* or the *Stratix II GX Device Handbook* for more information on Stratix II PLLs.

## Temperature Sensing Diode (TSD)

Stratix II devices include a diode-connected transistor for use as a temperature sensor in power management. This diode is used with an external digital thermometer device. These devices steer bias current through the Stratix II diode, measuring forward voltage and converting this reading to temperature in the form of an 8-bit signed number (7 bits plus sign). The external device's output represents the junction temperature of the Stratix II device and can be used for intelligent power management.

The diode requires two pins (`tempdiodep` and `tempdioden`) on the Stratix II device to connect to the external temperature-sensing device, as shown in [Figure 3-1](#). The temperature sensing diode is a passive element and therefore can be used before the Stratix II device is powered.

**Figure 3–1. External Temperature-Sensing Diode**

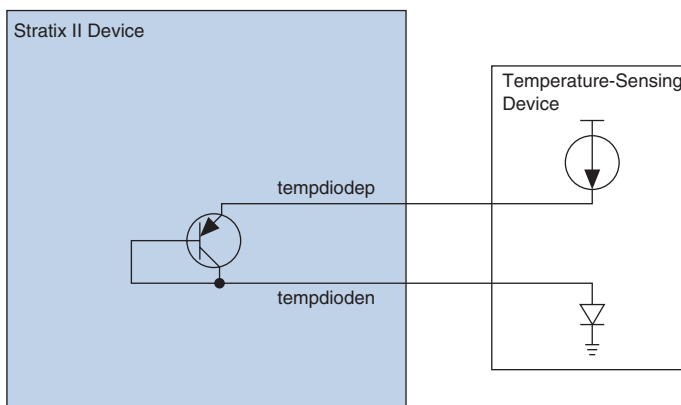


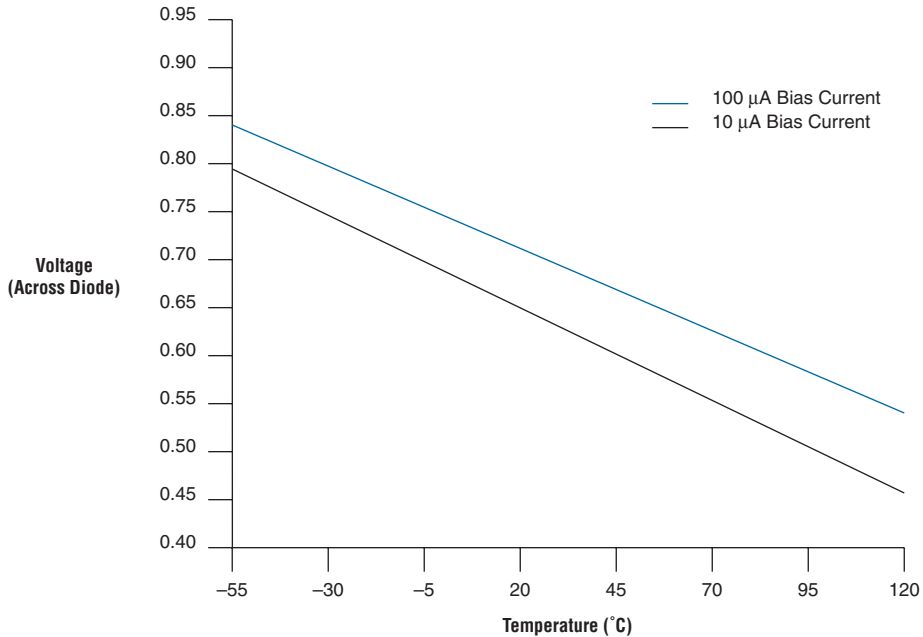
Table 3–6 shows the specifications for bias voltage and current of the Stratix II temperature sensing diode.

**Table 3–6. Temperature-Sensing Diode Electrical Characteristics**

Parameter	Minimum	Typical	Maximum	Unit
IBIAS high	80	100	120	μA
IBIAS low	8	10	12	μA
VBP - VBN	0.3		0.9	V
VBN		0.7		V
Series resistance			3	Ω

The temperature-sensing diode works for the entire operating range, as shown in [Figure 3–2](#).

**Figure 3–2. Temperature vs. Temperature-Sensing Diode Voltage**



The temperature sensing diode is a very sensitive circuit which can be influenced by noise coupled from other traces on the board, and possibly within the device package itself, depending on device usage. The interfacing device registers temperature based on millivolts of difference as seen at the TSD. Switching I/O near the TSD pins can affect the temperature reading. Altera recommends you take temperature readings during periods of no activity in the device (for example, standby mode where no clocks are toggling in the device), such as when the nearby I/Os are at a DC state, and disable clock networks in the device.

## Automated Single Event Upset (SEU) Detection

Stratix II devices offer on-chip circuitry for automated checking of single event upset (SEU) detection. Some applications that require the device to operate error free at high elevations or in close proximity to Earth's North or South Pole require periodic checks to ensure continued data integrity. The error detection cyclic redundancy check (CRC) feature controlled by

the Device & Pin Options dialog box in the Quartus II software uses a 32-bit CRC circuit to ensure data reliability and is one of the best options for mitigating SEU.

You can implement the error detection CRC feature with existing circuitry in Stratix II devices, eliminating the need for external logic. For Stratix II devices, CRC is computed by the device during configuration and checked against an automatically computed CRC during normal operation. The CRC\_ERROR pin reports a soft error when configuration SRAM data is corrupted, triggering device reconfiguration.

### Custom-Built Circuitry

Dedicated circuitry is built in the Stratix II devices to perform error detection automatically. This error detection circuitry in Stratix II devices constantly checks for errors in the configuration SRAM cells while the device is in user mode. You can monitor one external pin for the error and use it to trigger a re-configuration cycle. You can select the desired time between checks by adjusting a built-in clock divider.

### Software Interface

In the Quartus II software version 4.1 and later, you can turn on the automated error detection CRC feature in the Device & Pin Options dialog box. This dialog box allows you to enable the feature and set the internal frequency of the CRC between 400 kHz to 50 MHz. This controls the rate that the CRC circuitry verifies the internal configuration SRAM bits in the FPGA device.

For more information on CRC, refer to *AN 357: Error Detection Using CRC in Altera FPGA Devices*.

## Document Revision History

Table 3–7 shows the revision history for this chapter.

<i>Table 3–7. Document Revision History (Part 1 of 2)</i>		
<b>Date and Document Version</b>	<b>Changes Made</b>	<b>Summary of Changes</b>
May 2007, v4.2	Moved Document Revision History section to the end of the chapter.	—
	Updated the “Temperature Sensing Diode (TSD)” section.	—

**Table 3–7. Document Revision History (Part 2 of 2)**

<b>Date and Document Version</b>	<b>Changes Made</b>	<b>Summary of Changes</b>
April 2006, v4.1	Updated “Device Security Using Configuration Bitstream Encryption” section.	—
December 2005, v4.0	Updated “Software Interface” section.	—
May 2005, v3.0	<ul style="list-style-type: none"> <li>● Updated “IEEE Std. 1149.1 JTAG Boundary-Scan Support” section.</li> <li>● Updated “Operating Modes” section.</li> </ul>	—
January 2005, v2.1	Updated JTAG chain device limits.	—
January 2005, v2.0	Updated Table 3–3.	—
July 2004, v1.1	<ul style="list-style-type: none"> <li>● Added “Automated Single Event Upset (SEU) Detection” section.</li> <li>● Updated “Device Security Using Configuration Bitstream Encryption” section.</li> <li>● Updated Figure 3–2.</li> </ul>	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—

