

Introduction

The Stratix® II FPGA family is based on a 1.2-V, 90-nm, all-layer copper SRAM process and features a new logic structure that maximizes performance, and enables device densities approaching 180,000 equivalent logic elements (LEs). Stratix II devices offer up to 9 Mbits of on-chip, TriMatrix™ memory for demanding, memory intensive applications and has up to 96 DSP blocks with up to 384 (18-bit × 18-bit) multipliers for efficient implementation of high performance filters and other DSP functions. Various high-speed external memory interfaces are supported, including double data rate (DDR) SDRAM and DDR2 SDRAM, RLDRAM II, quad data rate (QDR) II SRAM, and single data rate (SDR) SDRAM. Stratix II devices support various I/O standards along with support for 1-gigabit per second (Gbps) source synchronous signaling with DPA circuitry. Stratix II devices offer a complete clock management solution with internal clock frequency of up to 550 MHz and up to 12 phase-locked loops (PLLs). Stratix II devices are also the industry's first FPGAs with the ability to decrypt a configuration bitstream using the Advanced Encryption Standard (AES) algorithm to protect designs.

Features

The Stratix II family offers the following features:

- 15,600 to 179,400 equivalent LEs; see [Table 1-1](#)
- New and innovative adaptive logic module (ALM), the basic building block of the Stratix II architecture, maximizes performance and resource usage efficiency
- Up to 9,383,040 RAM bits (1,172,880 bytes) available without reducing logic resources
- TriMatrix memory consisting of three RAM block sizes to implement true dual-port memory and first-in first-out (FIFO) buffers
- High-speed DSP blocks provide dedicated implementation of multipliers (at up to 450 MHz), multiply-accumulate functions, and finite impulse response (FIR) filters
- Up to 16 global clocks with 24 clocking resources per device region
- Clock control blocks support dynamic clock network enable/disable, which allows clock networks to power down to reduce power consumption in user mode
- Up to 12 PLLs (four enhanced PLLs and eight fast PLLs) per device provide spread spectrum, programmable bandwidth, clock switch-over, real-time PLL reconfiguration, and advanced multiplication and phase shifting

- Support for numerous single-ended and differential I/O standards
- High-speed differential I/O support with DPA circuitry for 1-Gbps performance
- Support for high-speed networking and communications bus standards including Parallel RapidIO, SPI-4 Phase 2 (POS-PHY Level 4), HyperTransport™ technology, and SFI-4
- Support for high-speed external memory, including DDR and DDR2 SDRAM, RLDRAM II, QDR II SRAM, and SDR SDRAM
- Support for multiple intellectual property megafunctions from Altera MegaCore® functions and Altera Megafunction Partners Program (AMPPSM) megafunctions
- Support for design security using configuration bitstream encryption
- Support for remote configuration updates

Table 1–1. Stratix II FPGA Family Features

Feature	EP2S15	EP2S30	EP2S60	EP2S90	EP2S130	EP2S180
ALMs	6,240	13,552	24,176	36,384	53,016	71,760
Adaptive look-up tables (ALUTs) (1)	12,480	27,104	48,352	72,768	106,032	143,520
Equivalent LEs (2)	15,600	33,880	60,440	90,960	132,540	179,400
M512 RAM blocks	104	202	329	488	699	930
M4K RAM blocks	78	144	255	408	609	768
M-RAM blocks	0	1	2	4	6	9
Total RAM bits	419,328	1,369,728	2,544,192	4,520,488	6,747,840	9,383,040
DSP blocks	12	16	36	48	63	96
18-bit × 18-bit multipliers (3)	48	64	144	192	252	384
Enhanced PLLs	2	2	4	4	4	4
Fast PLLs	4	4	8	8	8	8
Maximum user I/O pins	366	500	718	902	1,126	1,170

Notes to Table 1–1:

- (1) One ALM contains two ALUTs. The ALUT is the cell used in the Quartus® II software for logic synthesis.
- (2) This is the equivalent number of LEs in a Stratix device (four-input LUT-based architecture).
- (3) These multipliers are implemented using the DSP blocks.

Stratix II devices are available in space-saving FineLine BGA® packages (see [Tables 1–2](#) and [1–3](#)).

Table 1–2. Stratix II Package Options & I/O Pin Counts *Notes (1), (2)*

Device	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S15	342		366			
EP2S30	342		500			
EP2S60 (3)	334		492		718	
EP2S90 (3)		308		534	758	902
EP2S130 (3)				534	742	1,126
EP2S180 (3)					742	1,170

Notes to Table 1–2:

- (1) All I/O pin counts include eight dedicated clock input pins (clk1p, clk1n, clk3p, clk3n, clk9p, clk9n, clk11p, and clk11n) that can be used for data inputs.
- (2) The Quartus II software I/O pin counts include one additional pin, PLL_ENA, which is not available as general-purpose I/O pins. The PLL_ENA pin can only be used to enable the PLLs within the device.
- (3) The I/O pin counts for the EP2S60, EP2S90, EP2S130, and EP2S180 devices in the 1020-pin and 1508-pin packages include eight dedicated fast PLL clock inputs (FPLL7CLKp/n, FPLL8CLKp/n, FPLL9CLKp/n, and FPLL10CLKp/n) that can be used for data inputs.

Table 1–3. Stratix II FineLine BGA Package Sizes

Dimension	484 Pin	484-Pin Hybrid	672 Pin	780 Pin	1,020 Pin	1,508 Pin
Pitch (mm)	1.00	1.00	1.00	1.00	1.00	1.00
Area (mm ²)	529	729	729	841	1,089	1,600
Length × width (mm × mm)	23 × 23	27 × 27	27 × 27	29 × 29	33 × 33	40 × 40

All Stratix II devices support vertical migration within the same package (for example, you can migrate between the EP2S15, EP2S30, and EP2S60 devices in the 672-pin FineLine BGA package). Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities.

To ensure that a board layout supports migratable densities within one package offering, enable the applicable vertical migration path within the Quartus II software (Assignments menu > Device > Migration Devices).

After compilation, check the information messages for a full list of I/O, DQ, LVDS, and other pins that are not available because of the selected migration path.

Table 1–4 lists the Stratix II device package offerings and shows the total number of non-migratable user I/O pins when migrating from one density device to a larger density device. Additional I/O pins may not be migratable if migrating from the larger device to the smaller density device.



When moving from one density to a larger density, the larger density device may have fewer user I/O pins. The larger device requires more power and ground pins to support the additional logic within the device. Use the Quartus II Pin Planner to determine which user I/O pins are migratable between the two devices.

Vertical Migration Path	484-Pin FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1020-Pin FineLine BGA	1508-Pin FineLine BGA
EP2S15 to EP2S30	0 (1)	0			
EP2S15 to EP2S60	8 (1)	0			
EP2S30 to EP2S60	8 (1)	8			
EP2S60 to EP2S90				0	
EP2S60 to EP2S130				0	
EP2S60 to EP2S180				0	
EP2S90 to EP2S130			0 (1)	16	17
EP2S90 to EP2S180				16	0
EP2S130 to EP2S180				0	0

Note to Table 1–4:

- (1) Some of the DQ/DQS pins are not migratable. Refer to the Quartus II software information messages for more detailed information.



To determine if your user I/O assignments are correct, run the I/O Assignment Analysis command in the Quartus II software (Processing > Start > Start I/O Assignment Analysis).



Refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook* for more information on pin migration.

Stratix II devices are available in up to three speed grades, -3, -4, and -5, with -3 being the fastest. Table 1-5 shows Stratix II device speed-grade offerings.

Table 1-5. Stratix II Device Speed Grades

Device	Temperature Grade	484-Pin FineLine BGA	484-Pin Hybrid FineLine BGA	672-Pin FineLine BGA	780-Pin FineLine BGA	1,020-Pin FineLine BGA	1,508-Pin FineLine BGA
EP2S15	Commercial	-3, -4, -5		-3, -4, -5			
	Industrial	-4		-4			
EP2S30	Commercial	-3, -4, -5		-3, -4, -5			
	Industrial	-4		-4			
EP2S60	Commercial	-3, -4, -5		-3, -4, -5		-3, -4, -5	
	Industrial	-4		-4		-4	
EP2S90	Commercial		-4, -5		-4, -5	-3, -4, -5	-3, -4, -5
	Industrial					-4	-4
EP2S130	Commercial				-4, -5	-3, -4, -5	-3, -4, -5
	Industrial					-4	-4
EP2S180	Commercial					-3, -4, -5	-3, -4, -5
	Industrial					-4	-4

Document Revision History

Table 1–6 shows the revision history for this chapter.

Date and Document Version	Changes Made	Summary of Changes
May 2007, v4.2	Moved Document Revision History to the end of the chapter.	—
April 2006, v4.1	<ul style="list-style-type: none"> ● Updated “Features” section. ● Removed Note 4 from Table 1–2. ● Updated Table 1–4. 	—
December 2005, v4.0	<ul style="list-style-type: none"> ● Updated Tables 1–2, 1–4, and 1–5. ● Updated Figure 2–43. 	—
July 2005, v3.1	<ul style="list-style-type: none"> ● Added vertical migration information, including Table 1–4. ● Updated Table 1–5. 	—
May 2005, v3.0	<ul style="list-style-type: none"> ● Updated “Features” section. ● Updated Table 1–2. 	—
March 2005, v2.1	Updated “Introduction” and “Features” sections.	—
January 2005, v2.0	Added note to Table 1–2.	—
October 2004, v1.2	Updated Tables 1–2, 1–3, and 1–5.	—
July 2004, v1.1	<ul style="list-style-type: none"> ● Updated Tables 1–1 and 1–2. ● Updated “Features” section. 	—
February 2004, v1.0	Added document to the Stratix II Device Handbook.	—