3. External Memory Interfaces in Stratix & Stratix GX Devices

Introduction

Stratix® and Stratix GX devices support a broad range of external memory interfaces such as double data rate (DDR) SDRAM, RLDRAM II, quad data rate (QDR) SRAM, QDRII SRAM, zero bus turnaround (ZBT) SRAM, and single data rate (SDR) SDRAM. The dedicated phase-shift circuitry allows the Stratix and Stratix GX devices to interface at twice the system clock speed with an external memory (up to 200 MHz/400 Mbps).

Typical I/O architectures transmit a single data word on each positive clock edge and are limited to the associated clock speed using this protocol. To achieve a 400-megabits per second (Mbps) transfer rate, a SDR system requires a 400-MHz clock. Many new applications have introduced a DDR I/O architecture as an alternative to SDR architectures. While SDR architectures capture data on one edge of a clock, the DDR architectures captures data on both the rising and falling edges of the clock, doubling the throughput for a given clock frequency and accelerating performance. For example, a 200-MHz clock can capture a 400-Mbps data stream, enhancing system performance and simplifying board design.

Most current memory architectures use a DDR I/O interface. These DDR memory standards cover a broad range of applications for embedded processor systems, image processing, storage, communications, and networking. This chapter describes the hardware features in Stratix and Stratix GX devices that facilitate the high-speed memory interfacing for each memory standard. It then briefly explains how each memory standard uses the features of the Stratix and Stratix GX devices.

You can use this document with *AN 329: ZBT SRAM Controller Reference Design for Stratix & Stratix GX Devices, AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices*, and *AN 349: QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

External Memory Standards

The following sections provide an overview on using the Stratix and Stratix GX device external memory interfacing features.

DDR SDRAM

DDR SDRAM is a memory architecture that transmits and receives data at twice the clock speed of traditional SDR architectures. These devices transfer data on both the rising and falling edge of the clock signal.

Interface Pins

DDR devices use interface pins including data, data strobe, clock, command, and address pins. Data is sent and captured at twice the clock rate by transferring data on both the positive and negative edge of a clock. The commands and addresses only use one active edge of a clock.

Connect the memory device's DQ and DQS pins to the DQ and DQS pins, respectively, as listed in the Stratix and Stratix GX devices pin table. DDR SDRAM also uses active-high data mask pins for writes. You can connect DM pins to any of the I/O pins in the same bank as the DQ pins of the FPGA. There is one DM pin per DQS/DQ group.

DDR SDRAM ×16 devices use two DQS pins, and each DQS pin is associated with eight DQ pins. However, this is not the same as the ×16 mode in Stratix and Stratix GX devices. To support a ×16 DDR SDRAM, you need to configure the Stratix and Stratix GX FPGAs to use two sets of DQ pins in ×8 mode. Similarly if your ×32 memory device uses four DQS pins where each DQS pin is associated with eight DQ pins, you need to configure the Stratix and Stratix GX FPGA to use four sets of pins in ×8 mode.

You can also use any I/O pins in banks 1, 2, 5, or 6 to interface with DDR SDRAM devices. These banks do not have dedicated circuitry, though.

You can also use any of the user I/O pins for commands and addresses to the DDR SDRAM.

For more information, see *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices*.

If the DDR SDRAM device supports ECC, the design uses a DQS/DQ group for ECC pins. You can use any of the user I/O pins for commands and addresses.

Because of the symmetrical setup and hold time for the command and address pins at the memory, you might need to generate these signals from the system clock's negative edge.

The clocks to the SDRAM device are called CK and CK#. Use any of the user I/O pins via the DDR registers to generate the CK and CK# signals to meet the DDR SDRAM t_{DQSS} requirement. The memory device's t_{DQSS} requires that the DQS signal's positive edge write operations must be within 25% of the positive edge of the DDR SDRAM clock input. Using user I/O pins for CK and CK# ensures that any PVT variations seen by the DQS signal are tracked by these pins, too.

Read & Write Operations

When reading from the DDR SDRAM, the DQS signal coming into the Stratix and Stratix GX device is edge-aligned with the DQ pins. The dedicated circuitry center-aligns the DQS signal with respect to the DQ signals and the shifted DQS bus drives the clock input of the DDR input registers. The DDR input registers bring the data from the DQ signals to the device. The system clock clocks the DQS output enable and output paths. The -90° shifted clock clocks the DQ output enable and output paths. Figure 3–1 shows an example of the DQ and DQS relationship during a burst-of-two read. It shows where the DQS signal is center-aligned in the IOE.

Figure 3–1. Example of Where a DQS Signal is Center-Aligned in the IOE
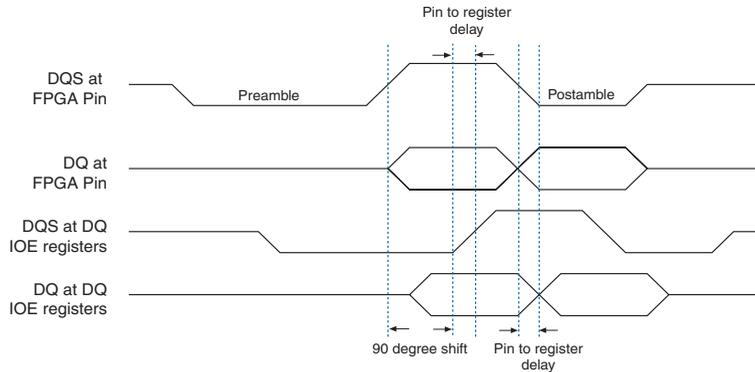
When writing to the DDR SDRAM, the DQS signal must be center-aligned with the DQ pins. Two PLL outputs are needed to generate the DQS signal and to clock the DQ pins. The DQS are clocked by the 0° phase-shift PLL output, while the DQ pins are clocked by the -90° phase-shifted PLL output. Figure 3–2 shows the DQS and DQ relationship during a DDR SDRAM burst-of-two write.

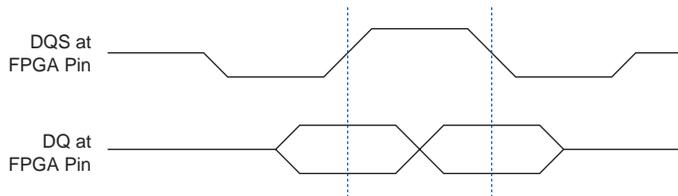*Figure 3–2. DQ & DQS Relationship During a Burst-of-Two Write*

Figure 3–3 shows DDR SDRAM interfacing from the I/O through the dedicated circuitry to the logic array. When the DQS pin acts as an input strobe, the dedicated circuitry shifts the incoming DQS pin by either 72° or 90° and clocks the DDR input registers. Because of the DDR input registers architecture in Stratix and Stratix GX devices, the shifted DQS signal must be inverted. The DDR registers outputs are sent to two LE registers to be synchronized with the system clock.

Refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix Device Handbook* for frequency limits regarding the 72 and 90° phase shift for DQS.

Figure 3–3. DDR SDRAM Interfacing
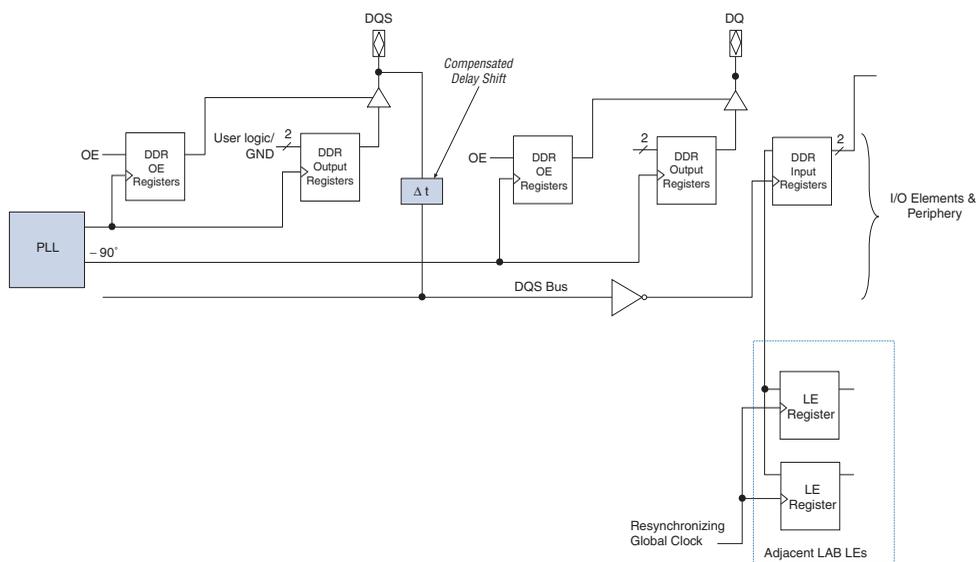
For more information on DDR SDRAM specifications, see JEDEC standard publications JESD79C from **www.jedec.org**, or see *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices*.

RLDRAM II

RLDRAM II provides fast random access as well as high bandwidth and high density, making this memory technology ideal for high-speed network and communication data storage applications. The fast random access speeds in RLDRAM II devices make them a viable alternative to SRAM devices at a lower cost. Additionally, RLDRAM II devices have minimal latency to support designs that require fast response times.

Interface Pins

RLDRAM II devices use interface pins such as data, clock, command, and address pins. There are two types of RLDRAM II memory: common I/O (CIO) and separate I/O (SIO). The data pins in RLDRAM II CIO device are bidirectional while the data pins in a RLDRAM II SIO device are uni-directional. Instead of bidirectional data strobes, RLDRAM II uses differential free-running read and write clocks to accompany the data. As in DDR SDRAM, data is sent and captured at twice the clock rate by transferring data on both the positive and negative edge of a clock. The commands and addresses still only use one active edge of a clock.

If the data pins are bidirectional, connect them to the Stratix and Stratix GX device DQ pins. If the data pins are uni-directional, connect the RLDRAM II device Q ports to the Stratix and Stratix GX device DQ pins and connect the D ports to any user I/O pins in I/O banks 3, 4, 7, and 8. RLDRAM II also uses active-high data mask pins for writes. You can connect DM pins to any of the I/O pins in the same bank as the DQ pins of the FPGA. When interfacing with SIO devices, connect the DM pins to any of the I/O pins in the same bank as the D pins. There is one DM pin per DQS/DQ group.

Connect the read clock pins (QK) to Stratix and Stratix GX device DQS pins. You must configure the DQS signals as bidirectional pins. However, since QK pins are output-only pins from the memory, RLDRAM memory interfacing in Stratix and Stratix GX devices requires that you ground the DQS and DQSn pin output enables. The Stratix and Stratix GX devices use the shifted QK signal from the DQS logic block to capture data. You can leave the QK# signal of the RLDRAM II device unconnected.

RLDRAM II devices have both input clocks (CK and CK#) and write clocks (DK and DK#). Use the external clock buffer to generate CK, CK#, DK, and DK# to meet the CK, CK#, DK, and DK# skew requirements from the RLDRAM II device. If you are interfacing with multiple RLDRAM II devices, perform IBIS simulations to analyze the loading effects on the clock pair.

You can use any of the user I/O pins for commands and addresses. RLDRAM II also offers QVLD pins to indicate the read data availability. Connect the QVLD pins to the Stratix and Stratix GX device DQVLD pins, listed in the pin table.

Read & Write Operations

When reading from the RLDRAM II device, data is sent edge-aligned with the read clock QK or QK# signal. When writing to the RLDRAM II device, data must be center-aligned with the write clock (DK or DK# signal). The Stratix and Stratix GX device RLDRAM II interface uses the

same scheme as in DDR SDRAM interfaces whereby the dedicated circuitry is used during reads to center-align the data and the read clock inside the FPGA and the PLL center-aligns the data and write clock outputs. The data and clock relationship for reads and writes in RLDRAM II is similar to those in DDR SDRAM as already depicted in Figure 3–1 on page 3–3 and Figure 3–3 on page 3–4.

QDR & QDRII SRAM

QDR SRAM provides independent read and write ports that eliminate the need for bus turnaround. The memory uses two sets of clocks: K and Kn for write access, and optional C and Cn for read accesses, where Kn and Cn are the inverse of the K and C clocks, respectively. You can use differential HSTL I/O pins to drive the QDR SRAM clock into the Stratix and Stratix GX devices. The separate write data and read data ports permit a transfer rate up to four words on every cycle through the DDR circuitry. Stratix and Stratix GX devices support both burst-of-two and burst-of-four QDR SRAM architectures, with clock cycles up to 167 MHz using the 1.5-V HSTL Class I or Class II I/O standard. Figure 3–4 shows the block diagram for QDR SRAM burst-of-two architecture.

Figure 3–4. QDR SRAM Block Diagram for Burst-of-Two Architecture
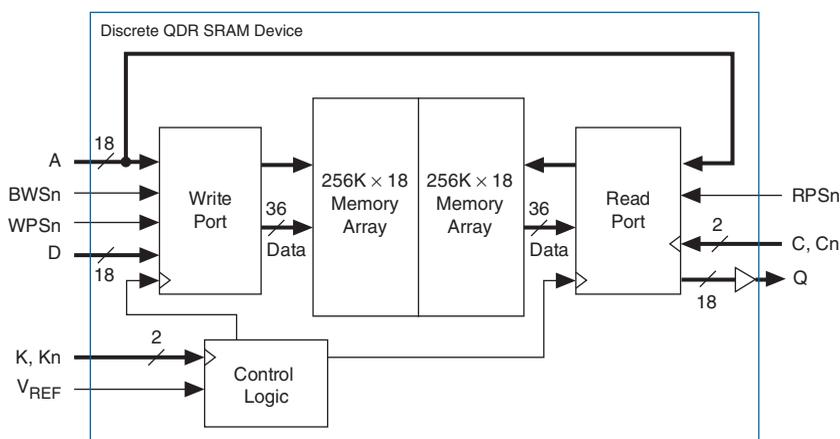
QDRII SRAM is a second generation of QDR SRAM devices. It can transfer four words per clock cycle, fulfilling the requirements facing next-generation communications system designers. QDRII SRAM devices provide concurrent reads and writes, zero latency, and increased data throughput. Stratix and Stratix GX devices support QDRII SRAM at speeds up to 200 MHz since the timing requirements for QDRII SRAM are not as strict as QDR SRAM.

Interface Pins

QDR and QDRII SRAM uses two separate, uni-directional data ports for read and write operations, enabling quad data-rate data transfer. Both QDR and QDRII SRAM use shared address lines for reads and writes. Stratix and Stratix GX devices utilize dedicated DDR I/O circuitry for the input and output data bus and the K and Kn output clock signals.

Both QDR and QDRII SRAM burst-of-two devices sample the read address on the rising edge of the K clock and sample the write address on the rising edge of the Kn clock while QDR and QDRII SRAM burst-of-four devices sample both read and write addresses on the K clock's rising edge. You can use any of the Stratix and Stratix GX device user I/O pins in I/O banks 3, 4, 7, and 8 for the D write data ports, commands, and addresses.

QDR SRAM uses the following clock signals: input clocks K and Kn and output clocks C and Cn. In addition to the aforementioned two pairs of clocks, QDRII SRAM also uses echo clocks CQ and CQn. Clocks Cn, Kn, and CQn are logical complements of clocks C, K, and CQ respectively. Clocks C, Cn, K, and Kn are inputs to the QDRII SRAM while clocks CQ and CQn are outputs from the QDRII SRAM. Stratix and Stratix GX devices use single-clock mode for single-device QDR and QDRII SRAM interfacing where the K and Kn are used for both read and write operations, and the C and Cn clocks are unused. Use both C or Cn and K or Kn clocks when interfacing with a bank of multiple QDRII SRAM devices with a single controller.

You can generate C, Cn, K, and Kn clocks using any of the I/O registers in I/O banks 3, 4, 7, or 8 via the DDR registers. Due to strict skew requirements between K and Kn signals, use adjacent pins to generate the clock pair. Surround the pair with buffer pins tied to V_{CC} and ground for better noise immunity from other signals.

In general, all output signals to the QDR and QDRII SRAM should use the top and bottom banks (I/O banks 3, 4, 7, or 8). You can place the input signals from the QDR and QDRII SRAM in any I/O banks.

Read & Write Operations

Figure 3–5 shows the data and clock relationships in QDRII SRAM devices at the memory pins during reads. QDR and QDRII SRAM devices send data within a t_{CO} time after each rising edge of the input clock C or Cn in multi-clock mode, or the input clock K or Kn in single clock mode. Data is valid until t_{DOH} time, after each rising edge of the C or Cn in multi-

clock mode, or K or Kn in single clock mode. The edge-aligned CQ and CQn clocks accompany the read data for data capture in Stratix and Stratix GX devices.

Figure 3–5. Data & Clock Relationship During a QDRII SRAM Read   Note (1)
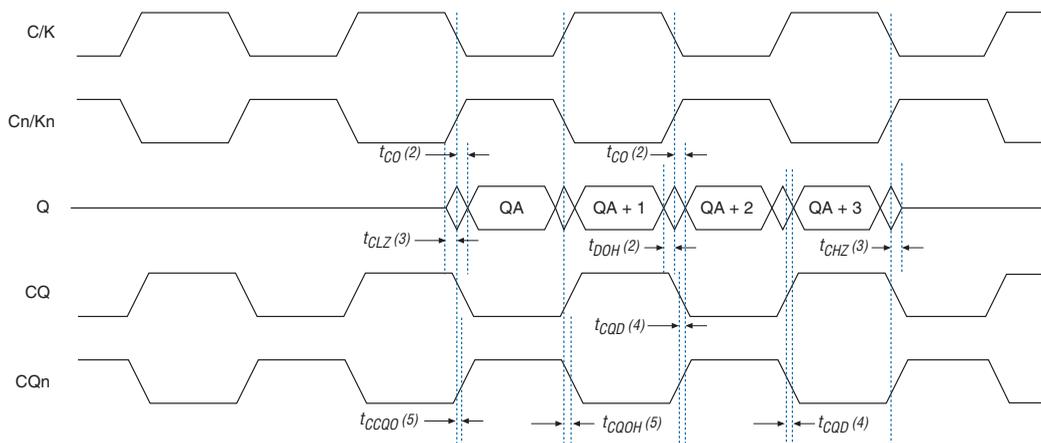
Notes to Figure 3–5:
(1)   The timing parameter nomenclature is based on the Cypress QDRII SRAM data sheet for CY7C1313V18.
(2)   CO is the data clock-to-out time and t_{DOH} is the data output hold time between burst.
(3) t_{CLZ} and t_{CHZ} are bus turn-on and turn-off times respectively.
(4) t_{CQD} is the skew between CQn and data edges.
(5) t_{CQQO} and t_{CQOH} are skew between the C or Cn (or K or Kn in single-clock mode) and the CQ or CQn clocks.

When writing to QDRII SRAM devices, data is generated by the write clock, while the K clock is 90° shifted from the write clock, creating a center-aligned arrangement.

Go to **www.qdrsram.com** for the QDR SRAM and QDRII SRAM specifications. For more information on QDR and QDRII SRAM interfaces in Stratix and Stratix GX devices, see *AN 349: QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

ZBT SRAM

ZBT SRAM eliminate dead bus cycles when turning a bidirectional bus around between reads and writes or between writes and reads. ZBT allows for 100% bus utilization because ZBT SRAM can be read or written on every clock cycle. Bus contention can occur when shifting from a write cycle to a read cycle or vice versa with no idle cycles in between. ZBT SRAM allows small amounts of bus contention. To avoid bus contention, the output clock-to-low-impedance time (t_{ZX}) must be greater

than the clock-to-high-impedance time (t_{XZ}). Stratix and Stratix GX device I/O pins can interface with ZBT SRAM devices at up to 200 MHz and can meet ZBT t_{CO} and t_{SU} timing requirements by controlling phase delay in clocks to the OE or output and input registers using an enhanced PLL. Figure 3–6 shows a flow-through ZBT SRAM operation where A1 and A3 are read addresses and A2 and A4 are write addresses. For pipelined ZBT SRAM operation, data is delayed by another clock cycle. Stratix and Stratix GX devices support up to 200-MHz ZBT SRAM operation using the 2.5-V or 3.3-V LVTTL I/O standard.

Figure 3–6. t_{ZX} & t_{XZ} Timing Diagram
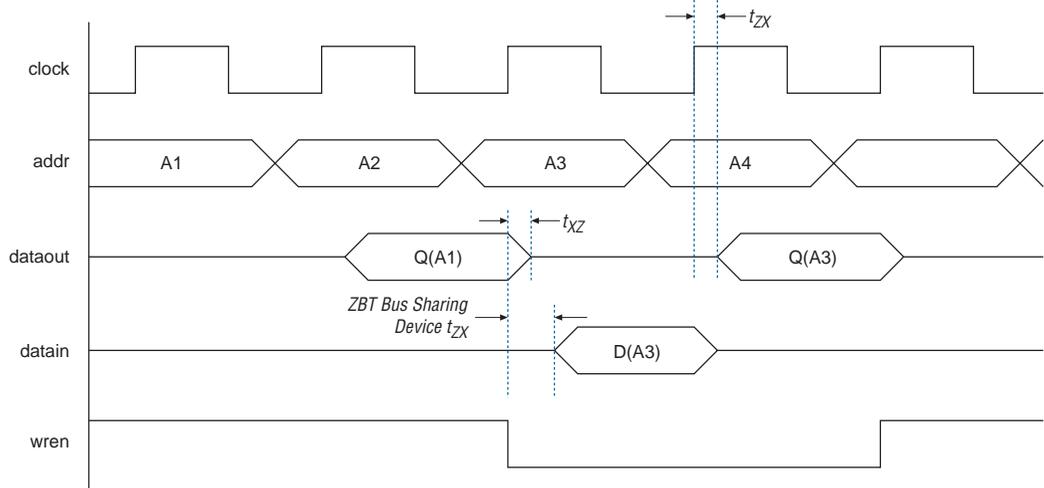
Interface Pins

ZBT SRAM uses one system clock input for all clocking purposes. Only the rising edge of this clock is used, since ZBT SRAM uses a single data rate scheme. The data bus, DQ, is bidirectional. There are three control signals to the ZBT SRAM: RW_N, BW_N, and ADV_LD_N. You can use any of the Stratix and Stratix GX device user I/O pins to interface to the ZBT SRAM device.

For more information on ZBT SRAM Interfaces in Stratix devices, see *AN 329: ZBT SRAM Controller Reference Design for Stratix & Stratix GX Devices*.

DDR Memory Support Overview

Table 3–1 shows the external RAM support in Stratix EP1S10 through EP1S40 devices and all Stratix GX devices. Table 3–2 shows the external RAM support in Stratix EP1S60 and EP1S80 devices.

Table 3–1. External RAM Support in Stratix EP1S10 through EP1S40 & All Stratix GX Devices

DDR Memory Type	I/O Standard	Maximum Clock Rate (MHz)						
		-5 Speed Grade	-6 Speed Grade		-7 Speed Grade		-8 Speed Grade	
		Flip-Chip	Flip-Chip	Wire-Bond	Flip-Chip	Wire-Bond	Flip-Chip	Wire-Bond
DDR SDRAM *(1)*, *(2)*	SSTL-2	200	167	133	133	100	100	100
DDR SDRAM - side banks *(2)*, *(3)*, *(4)*	SSTL-2	150	133	110	133	100	100	100
RLDRAM II *(4)*	1.8-V HSTL	200	*(5)*	*(5)*	*(5)*	*(5)*	*(5)*	*(5)*
QDR SRAM *(6)*	1.5-V HSTL	167	167	133	133	100	100	100
QDRII SRAM *(6)*	1.5-V HSTL	200	167	133	133	100	100	100
ZBT SRAM *(7)*	LVTTL	200	200	200	167	167	133	133

Notes to Table 3–1:

(1)   These maximum clock rates apply if the Stratix device uses DQS phase-shift circuitry to interface with DDR SDRAM. DQS phase-shift circuitry is only available on the top and bottom I/O banks (I/O banks 3, 4, 7, and 8).
(2)   For more information on DDR SDRAM, see *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices.*
(3)   DDR SDRAM is supported on the Stratix device side I/O banks (I/O banks 1, 2, 5, and 6) without dedicated DQS phase-shift circuitry. The read DQS signal is ignored in this mode.
(4)   These performance specifications are preliminary.
(5)   This device does not support RLDRAM II.
(6)   For more information on QDR or QDRII SRAM, see *AN 349: QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices*.
(7)   For more information on ZBT SRAM, see *AN 329: ZBT SRAM Controller Reference Design for Stratix and Stratix GX Devices*.

Table 3–2. External RAM Support in Stratix EP1S60 & EP1S80   (Part 1 of 2)

DDR Memory Type	I/O Standard	Maximum Clock Rate (MHz)		
		-5 Speed Grade	-6 Speed Grade	-7 Speed Grade
DDR SDRAM *(1)*, *(2)*	SSTL-2	167	167	133
DDR SDRAM - side banks *(2)*, *(3)*	SSTL-2	150	133	133
QDR SRAM *(4)*	1.5-V HSTL	133	133	133
QDRII SRAM *(4)*	1.5-V HSTL	167	167	133

Table 3–2. External RAM Support in Stratix EP1S60 & EP1S80   (Part 2 of 2)

DDR Memory Type	I/O Standard	Maximum Clock Rate (MHz)		
		-5 Speed Grade	-6 Speed Grade	-7 Speed Grade
ZBT SRAM *(5)*	LVTTL	200	200	167

Notes to Table 3–2:

(1)   These maximum clock rates apply if the Stratix device uses DQS phase-shift circuitry to interface with DDR SDRAM. DQS phase-shift circuitry is only available on the top and bottom I/O banks (I/O banks 3, 4, 7, and 8).

(2)   For more information on DDR SDRAM, see *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices.*

(3)   DDR SDRAM is supported on the side banks (I/O banks 1, 2, 5, and 6) with no dedicated DQS phase-shift circuitry. The read DQS signal is ignored in this mode.

(4)   For more information on QDR or QDRII SRAM, see *AN 349: QDR SRAM Controller Reference Design for Stratix & Stratix GX Devices.*

(5)   For more information on ZBT SRAM, see *AN 329: ZBT SRAM Controller Reference Design for Stratix and Stratix GX Devices.*

Stratix and Stratix GX devices support the data strobe or read clock signal (DQS) used in DDR SDRAM, and RLDRAM II devices. DQS signals are associated with a group of data (DQ) pins.

Stratix and Stratix GX devices contain dedicated circuitry to shift the incoming DQS signals by 0°, 72°, and 90°. The DQS phase-shift circuitry uses a frequency reference to dynamically generate control signals for the delay chains in each of the DQS pins, allowing it to compensate for process, voltage, and temperature (PVT) variations. The dedicated circuitry also creates consistent margins that meet your data sampling window requirements.

Refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix Device Handbook* for frequency limits regarding the 72 and 90° phase shift for DQS.

In addition to the DQS dedicated phase-shift circuitry, every I/O element (IOE) in Stratix and Stratix GX devices contains six registers and one latch to achieve DDR operation. There is also a programmable delay chain in the IOE that can help reduce contention when interfacing with ZBT SRAM devices.

DDR Memory Interface Pins

Stratix and Stratix GX devices use data (DQ), data strobe (DQS), and clock pins to interface with DDR SDRAM and RLDRAM II devices. This section explains the pins used in the DDR SDRAM and RLDRAM II interfaces. For QDR, QDRII, and ZBT SRAM interfaces, see the "External Memory Standards" section.

Figure 3–7 shows the DQ and DQS pins in ×8 mode.

Figure 3–7. Stratix & Stratix GX Device DQ & DQS Groups in × 8 Mode

Top or Bottom I/O Bank

DQ Pins (1)   DQS Pin
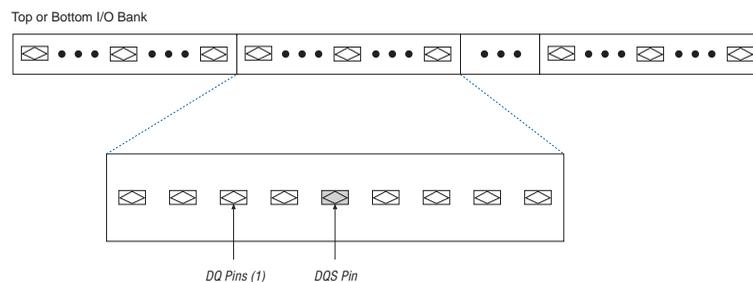
Note to Figure 3–7:
(1)   There are at least eight DQ pins per group.

Data & Data Strobe Pins

Stratix and Stratix GX data pins for the DDR memory interfaces are called DQ pins. The Stratix and Stratix GX device I/O banks at the top (I/O banks 3 and 4) and the bottom (I/O banks 7 and 8) of the device support DDR SDRAM and RLDRAM II up to 200 MHz. These pins support DQS signals with DQ bus modes of ×8, ×16, or ×32. Stratix and Stratix GX devices can support either bidirectional data strobes or uni-directional read clocks. Depending on the external memory interface, either the memory device's read data strobes or read clocks feed the DQS pins.

For ×8 mode, there are up to 20 groups of programmable DQS and DQ pins—10 groups in I/O banks 3 and 4 and 10 groups in I/O banks 7 and 8 (see Table 3–3). Each group consists of one DQS pin and a set of eight DQ pins.

For ×16 mode, there are up to eight groups of programmable DQS and DQ pins—four groups in I/O banks 3 and 4, and four groups in I/O banks 7 and 8. The EP1S20 device supports seven ×16 mode groups. The EP1S10 device does not support ×16 mode. All other devices support the full eight groups. See Table 3–3. Each group consists of one DQS and 16 DQ pins. In ×16 mode, DQS1T, DQS3T, DQS6T, and DQS8T pins on the top side of the device, and DQS1B, DQS3B, DQS6B, and DQS8B pins on the

bottom side of the device are dedicated DQS pins. The DQS2T, DQS7T, DQS2B, and DQS7B pins are dedicated DQS pins for ×32 mode, and each group consists of one DQS and 32 DQ pins.

Table 3–3. DQS & DQ Bus Mode Support *Note (1)*		Number of ×8 Groups	Number of ×16 Groups	Number of ×32 Groups
Device	**Package**			
EP1S10	672-pin BGA 672-pin FineLine BGA®	12 *(2)*	0	0
	484-pin FineLine BGA 780-pin FineLine BGA	16 *(3)*	0	4
EP1S20	484-pin FineLine BGA	18 *(4)*	7 *(5)*	4
	672-pin BGA 672-pin FineLine BGA	16 *(3)*	7 *(5)*	4
	780-pin FineLine BGA	20	7 *(5)*	4
EP1S25	672-pin BGA 672-pin FineLine BGA	16 *(3)*	8	4
	780-pin FineLine BGA 1,020-pin FineLine BGA	20	8	4
EP1S30	956-pin BGA 780-pin FineLine BGA 1,020-pin FineLine BGA	20	8	4
EP1S40	956-pin BGA 1,020-pin FineLine BGA 1,508-pin FineLine BGA	20	8	4
EP1S60	956-pin BGA 1,020-pin FineLine BGA 1,508-pin FineLine BGA	20	8	4
EP1S80	956-pin BGA 1,508-pin FineLine BGA 1,923-pin FineLine BGA	20	8	4

Notes to Table 3–3:
(1) For V_{REF} guidelines, see the *Selectable I/O Standards in Stratix & Stratix GX Devices* chapter of the *Stratix Device Handbook, Volume 2* or the *Stratix GX Handbook, Volume 2*.
(2) These packages have six groups in I/O banks 3 and 4 and six groups in I/O banks 7 and 8.
(3) These packages have eight groups in I/O banks 3 and 4 and eight groups in I/O banks 7 and 8.
(4) This package has nine groups in I/O banks 3 and 4 and nine groups in I/O banks 7 and 8.
(5) These packages have three groups in I/O banks 3 and 4 and four groups in I/O banks 7 and 8.

The DQS pins are marked in the Stratix and Stratix GX device pin table as `DQS[9..0]T` or `DQS[9..0]B`, where `T` stands for top and `B` for bottom. The corresponding DQ pins are marked as `DQ[9..0]T[7..0]`, where `[9..0]` indicates which DQS group the pins belong to. The numbering scheme starts from right to left on the package bottom view. When not used as DQ or DQS pins, these pins are available as user I/O pins.

You can also create a design in a mode other than the ×8, ×16, or ×32 mode. The Quartus® II software uses the next larger mode with the unused DQ pins available as regular use I/O pins. For example, if you create a design for ×9 mode for an RLDRAM II interface (nine DQ pins driven by one DQS pin), the Quartus II software implements a ×16 mode with seven DQ pins unconnected to the DQS bus. These seven unused DQ pins can be used as regular I/O pins.

☞   On the top and bottom side of the device, the DQ and DQS pins must be configured as bidirectional DDR pins to enable the DQS phase-shift circuitry. If you only want to use the DQ and/or DQS pins as inputs, you need to set the output enable of the DQ and/or DQS pins to ground. Use the `altdqs` and `altdq` megafunctions to configure the DQS and DQ pins, respectively. However, you should use the Altera® IP Toolbench to create the data path for your memory interfaces.

Stratix and Stratix GX device side I/O banks (I/O banks 1, 2, 5, and 6) support SDR SDRAM, ZBT SRAM, QDR SRAM, QDRII SRAM, and DDR SDRAM interfaces and can use any of the user I/O pins in these banks for the interface. Since these I/O banks do not have any dedicated circuitry for memory interfacing, they can support DDR SDRAM up to 150 MHz in -5 speed grade devices. However, these I/O banks do not support the HSTL-18 Class II I/O standard, which is required to interface with RLDRAM II.

Clock Pins

You can use any of the DDR I/O registers in the top or bottom bank of the device (I/O banks 3, 4, 7, or 8) to generate clocks to the memory device. You can also use any of the DDR I/O registers in the side I/O banks 1, 2, 5, or 6 to generate clocks for DDR SDRAM interfaces on the side I/O banks (not using the DQS circuitry).

Command & Address Pins

You can use any of the user I/O pins in the top or bottom bank of the device (I/O banks 3, 4, 7, or 8) for commands and addresses. For DDR SDRAM, you can also use any of the user I/O pins in the side I/O banks 1, 2, 5, or 6, regardless of whether you use the DQS phase-shift circuitry or not.

Other Pins (Parity, DM, ECC & QVLD Pins)

You can use any of the DQ pins for the parity pins in Stratix and Stratix GX devices. However, this may mean that you are using the next larger DQS/DQ mode. For example, if you need a parity bit for each byte of data, you are actually going to have nine DQ pins per DQS pin. The Quartus II software then implements a ×16 mode, with the seven unused DQ pins available as user I/O pins.

The data mask (DM) pins are only required when writing to DDR SDRAM and RLDRAM II devices. A low signal on the DM pins indicates that the write is valid. If the DM signal is high, the memory masks the DQ signals. You can use any of the I/O pins in the same bank as the DQ pins for the DM signals. Each group of DQS and DQ signals requires a DM pin. The DDR register, clocked by the –90° shifted clock, creates the DM signals, similar to DQ output signals.

Some DDR SDRAM devices support error correction coding (ECC), which is a method of detecting and automatically correcting errors in data transmission. Connect the DDR ECC pins to a Stratix and Stratix GX device DQS/DQ group. In 72-bit DDR SDRAM, there are eight ECC pins in addition to the 64 data pins. The memory controller needs extra logic to encode and decode the ECC data.

QVLD pins are used in RLDRAM II interfacing to indicate the read data availability. There is one QVLD pin per RLDRAM II device. A high on QVLD indicates that the memory is outputting the data requested. Similar to DQ inputs, this signal is edge-aligned with the RLDRAM II read clocks, QK and QK#, and is sent half a clock cycle before data starts coming out of the memory. You can connect QVLD pins to any of the I/O pins in the same bank as the DQ pins for the QVLD signals.

DQS Phase-Shift Circuitry

Two single phase-shifting reference circuits are located on the top and bottom of the Stratix and Stratix GX devices. Each circuit is driven by a system reference clock that is of the same frequency as the DQS signal. Clock pins CLK[15..12]p feed the phase-shift circuitry on the top of the device and clock pins CLK[7..4]p feed the phase-shift circuitry on the

bottom of the device. The phase-shift circuitry cannot be fed from other sources such as the LE or the PLL internal output clocks. This phase-shift circuitry is used for DDR SDRAM and RLDRAM II interfaces. For best performance, turn off the input reference clock to the DQS phase-shift circuitry when reading from the DDR SDRAM or RLDRAM II. This is to avoid any DLL jitter incorrectly shifting the DQS signal while the FPGA is capturing data.

☞ The I/O pins in I/O banks 1, 2, 5, and 6 can interface with the DDR SDRAM at up to 150 MHz. See *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices*.

A compensated delay element on each DQS pin allows for either a 90° or a 72° phase shift, which automatically centers input DQS signals with the data valid window of their corresponding DQ data signals. The DQS signals drive a local DQS bus within the top and bottom I/O banks. This DQS bus is an additional resource to the I/O clocks and clocks DQ input registers with the DQS signal.

☜ Refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix Device Handbook* for frequency limits regarding the 72 and 90° phase shift for DQS.

The phase-shifting reference circuit on the top of the device controls the compensated delay elements for all 10 DQS pins located at the top of the device. The phase-shifting reference circuit on the bottom of the device controls the compensated delay elements for all 10 DQS pins located on the bottom of the device. All 10 delay elements (DQS signals) on either the top or bottom of the device shift by the same degree amount. For example, all 10 DQS pins on the top of the device can be shifted by 90° and all 10 DQS pins on the bottom of the device can be shifted by 72°. The reference circuit requires a maximum of 256 system reference clock cycles to set the correct phase on the DQS delay elements.

☞ This applies only to the initial phase calculation. Altera recommends that you enable the DLL during the refresh cycle of the DDR SDRAM. Enabling the DLL for the duration of the minimum refresh time is sufficient for recalculating the phase shift.

Figure 3–8 shows the phase-shift reference circuit control of each DQS delay shift on the top of the device. This same circuit is duplicated on the bottom of the device.

Figure 3–8. DQS & DQSn Pins & the DQS Phase-Shift Circuitry   *Note (1)*
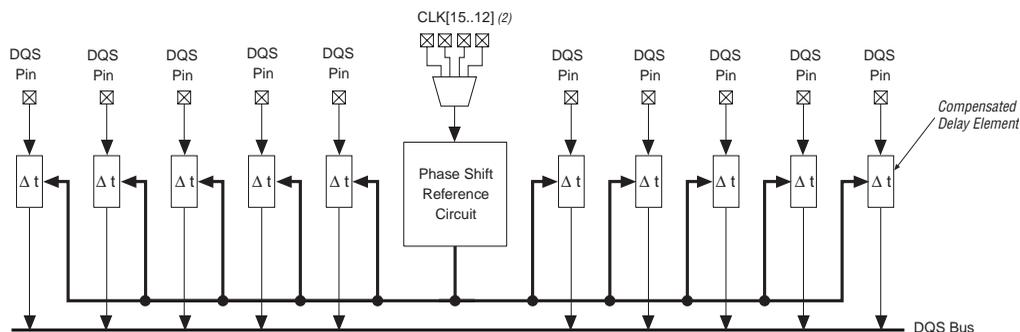
Notes to Figure 3–8:
(1)   There are up to 10 DQS and DQSn pins available on the top or the bottom of the Stratix and Stratix GX devices.
(2)   Clock pins CLK[15..12]p feed the phase-shift circuitry on the top of the device and clock pins CLK[7..4]p feed the phase circuitry on the bottom of the device. The reference clock can also be used in the logic array.

The phase-shift circuitry is only used during read transactions where the DQS pins are acting as input clocks or strobes. The phase-shift circuitry can shift the incoming DQS signal by 0°, 72°, and 90°. The shifted DQS signal is then inverted and used as a clock or a strobe at the DQ IOE input registers.

Refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix Device Handbook* for frequency limits regarding the 72 and 90° phase shift for DQS.

The DQS phase-shift circuitry is bypassed when 0° shift is chosen. The routing delay between the pins and the IOE registers is matched with high precision for both the DQ and DQS signal when the 72° or 90° phase shift is used. With the 0° phase shift, the skew between DQ and the DQS signals at the IOE register has been minimized. See Table 3–4 for the Quartus II software reported number on the DQ and DQS path to the IOE when the DQS is set to 0° phase shift.

Table 3–4. Quartus II Reported Number on the DQS Path to the IOE   *Note (1)*

Speed Grade	DQ2IOE	DQS2IOE	Unit
-5	0.908	1.008	ns
-6	0.956	1.061	ns
-7	1.098	1.281	ns

Table 3–4. Quartus II Reported Number on the DQS Path to the IOE *Note (1)*

Speed Grade	DQ2IOE	DQS2IOE	Unit
-8	1.293	1.635	ns

Note to Table 3–4:

(1)   These are reported by Quartus II version 4.0. Check the latest version of the Quartus II software for the most current information.

To generate the correct phase shift, you must provide a clock signal of the same frequency as the DQS signal to the DQS phase-shift circuitry. Any of the CLK[15..12]p clock pins can feed the phase circuitry on the top of the device (I/O banks 3 and 4) and any of the CLK[7..4]p clock pins can feed the phase circuitry on the bottom of the device (I/O banks 7 and 8). Both the top and bottom phase-shift circuits need unique clock pins for the reference clock. You cannot use any internal clock sources to feed the phase-shift circuitry, but you can route internal clock sources off-chip and then back into one of the allowable clock input pins.

DLL

The DQS phase-shift circuitry uses a DLL to dynamically measure the clock period needed by the DQS pin (see Figure 3–9). The DQS phase-shift circuitry then uses the clock period to generate the correct phase shift. The DLL in the Stratix and Stratix GX devices DQS phase-shift circuitry can operate between 100 and 200 MHz. The phase-shift circuitry needs a maximum of 256 clock cycles to calculate the correct phase shift. Data sent during these clock cycles may not be properly captured.

☞   You can still use the DQS phase-shift circuitry for DDR SDRAM interfaces that are less than 100 MHz. The DQS signal is shifted by about 2.5 ns. This shifted DQS signal is not in the center of the DQ signals, but it is shifted enough to capture the correct data in this low-frequency application.

Figure 3–9. Simplified Diagram of the DQS Phase-Shift Circuitry
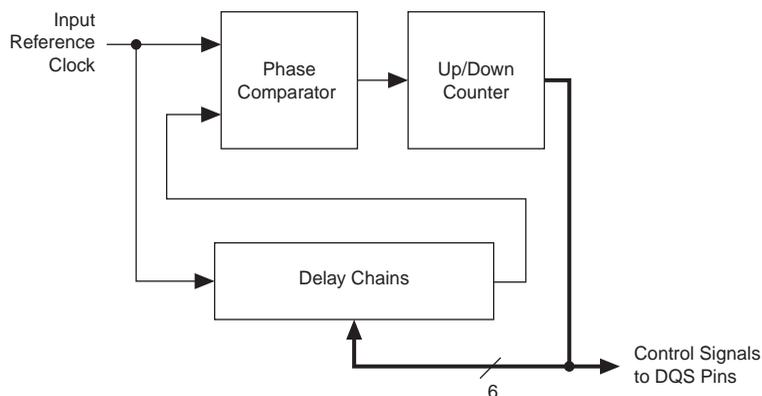
The input reference clock goes into the DLL to a chain of delay elements. The phase comparator compares the signal coming out of the end of the delay element chain to the input reference clock. The phase comparator then issues the upndn signal to the up/down counter. This signal increments or decrements a six-bit delay setting (control signals to DQS pins) that increases or decreases the delay through the delay element chain to bring the input reference clock and the signals coming out of the delay element chain in phase.

The shifted DQS signal then goes to the DQS bus to clock the IOE input registers of the DQ pins. It cannot go into the logic array for other purposes.

For external memory interfaces that use a bidirectional read strobe like DDR SDRAM, the DQS signal is low before going to or coming from a high-impedance state (see Figure 3–1 on page 3–3). The state where DQS is low just after a high-impedance state is called the preamble and the state where DQS is low just before it returns to high-impedance state is called the postamble. There are preamble and postamble specifications for both read and write operations in DDR SDRAM. To ensure data is not lost when there is noise on the DQS line at the end of a read postamble time, you need to add soft postamble circuitry to disable the clocks at the DQ IOE registers.

For more information, the DQS Postamble soft logic is described in *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices*. The Altera DDR SDRAM controller MegaCore® generates this logic as open-source code.

DDR Registers

Each Stratix and Stratix GX IOE contains six registers and one latch. Two registers and a latch are used for input, two registers are used for output, and two registers are used for output enable control. The second output enable register provides the write preamble for the DQS strobe in the DDR external memory interfaces. This negative-edge output enable register extends the high-impedance state of the pin by a half clock cycle to provide the external memory's DQS preamble time specification. Figure 3–10 shows the six registers and the latch in the Stratix and Stratix GX IOE and Figure 3–11 shows how the second OE register extends the DQS high impedance state by half a clock cycle during a write operation.

Figure 3–10. Bidirectional DDR I/O Path in Stratix & Stratix GX Devices   *Note (1)*
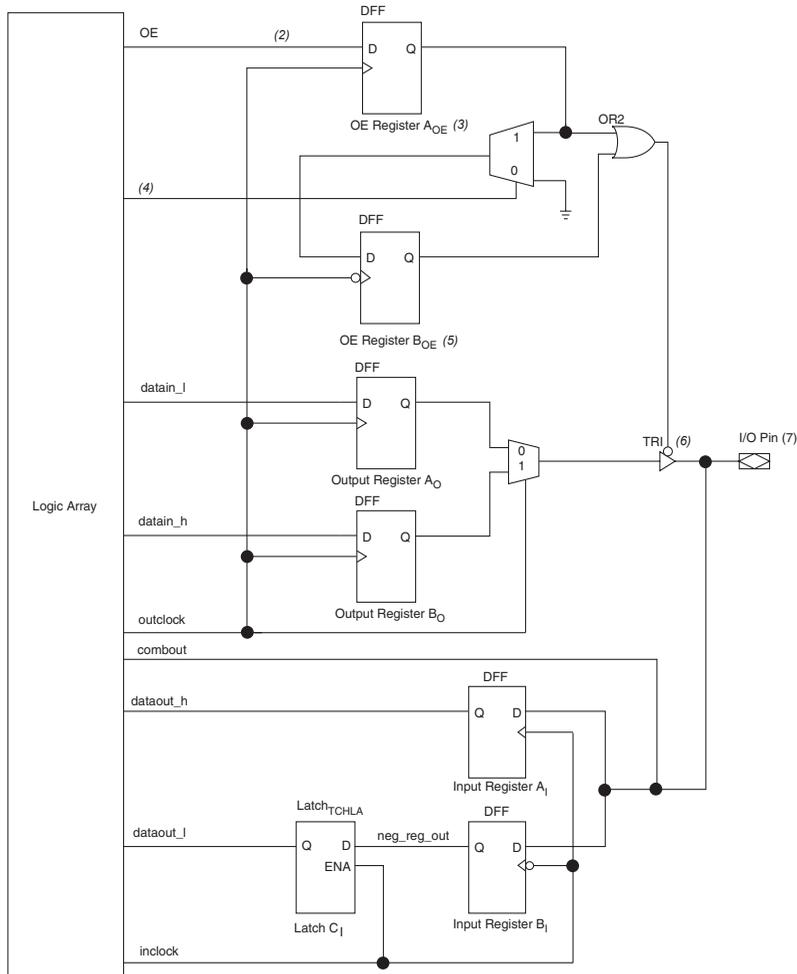
Notes to Figure 3–10:
(1)   All control signals can be inverted at the IOE. No programmable delay chains are shown in this diagram.
(2)   The OE signal is active low, but the Quartus II software implements this as active high and automatically adds an inverter before input to the A_{OE} register during compilation.
(3)   The A_{OE} register generates the enable signal for general-purpose DDR I/O applications.
(4)   This select line is to choose whether the OE signal should be delayed by half-a-clock cycle.
(5)   The B_{OE} register generates the delayed enable signal for the write strobes and write clock for memory interfaces.
(6)   The tristate enable is active low by default. You can design it to be active high. The combinational control path for the tristate is not shown in this diagram.
(7)   You can also have combinational output to the I/O pin; this path is not shown in the diagram.

Figure 3–11. Extending the OE Disable by Half-a-Clock Cycle for a Write Transaction   Note (1)
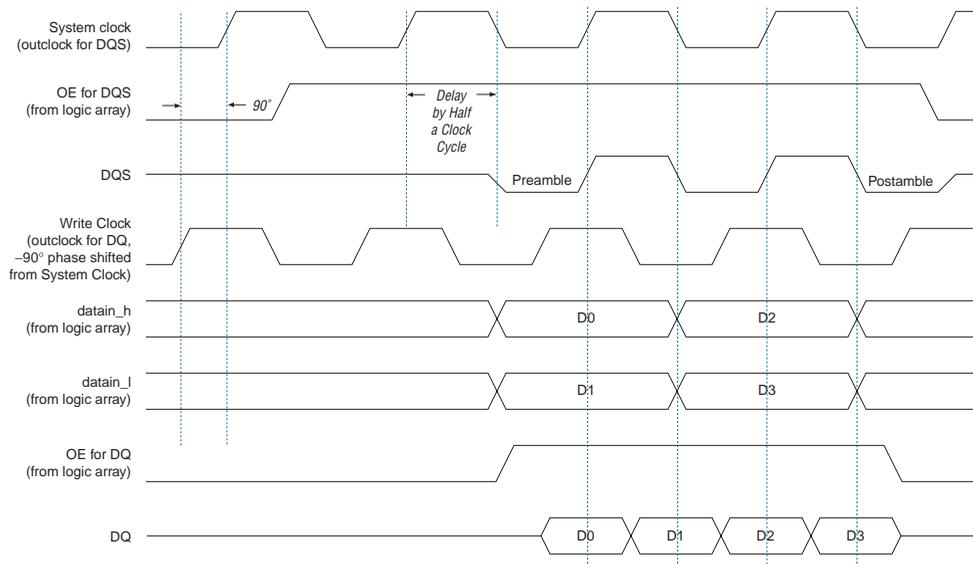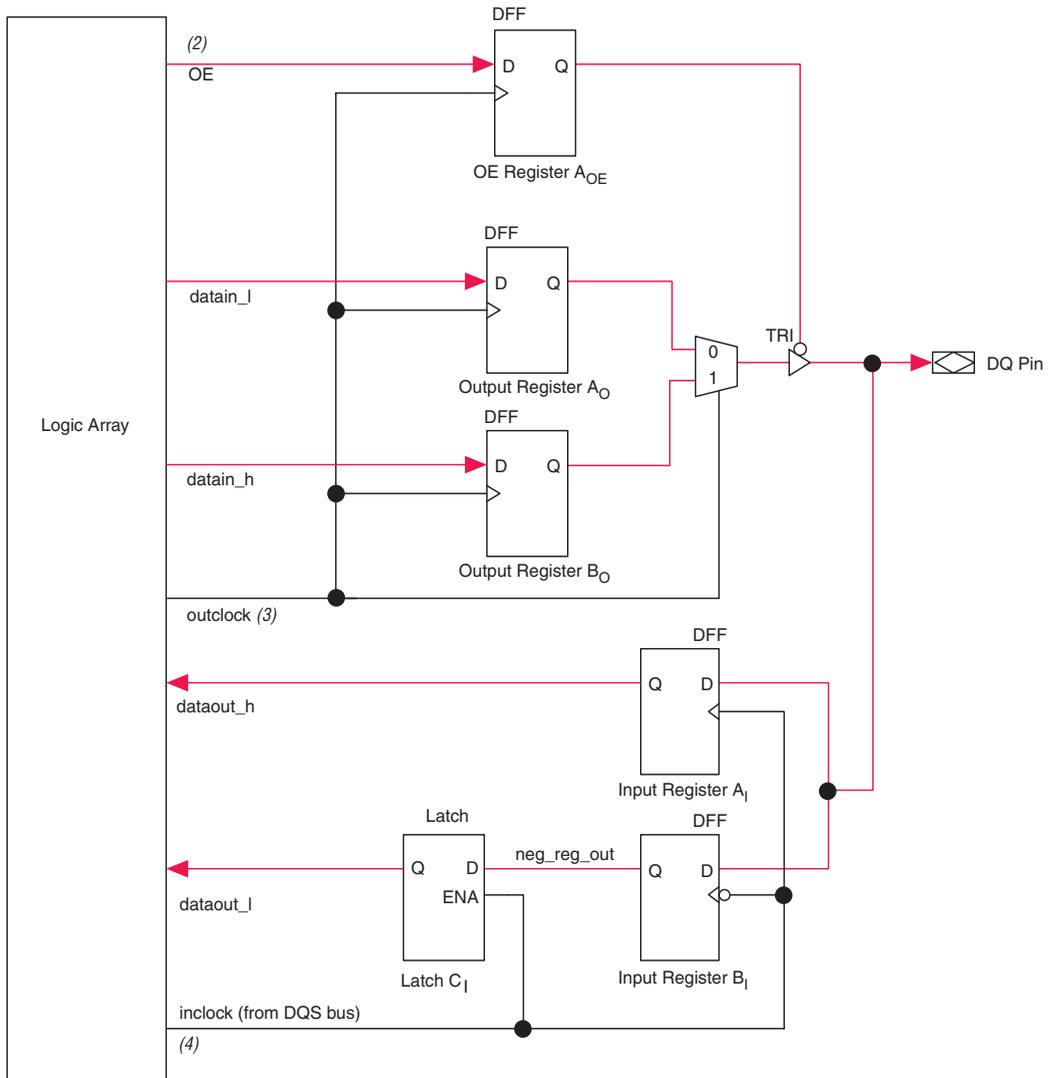

Note to Figure 3–11:
(1)   The waveform reflects the software simulation result. The OE signal is an active low on the device. However, the Quartus II software implements this signal as an active high and automatically adds an inverter before the A_{OE} register D input.

Figures 3–12 and 3–13 summarize the IOE registers used for the DQ and DQS signals.
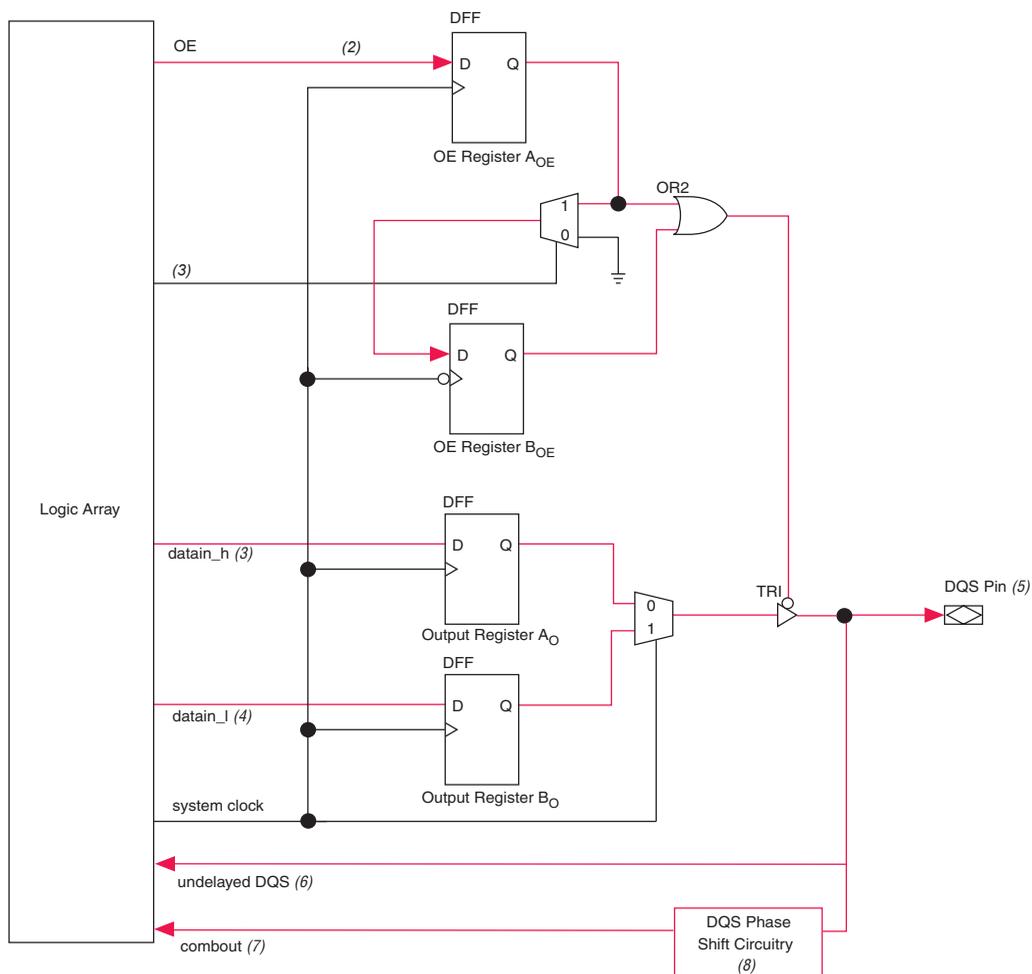
Figure 3–12. DQ Configuration in Stratix & Stratix GX IOE   *Note (1)*

Notes to Figure 3–12:

(1)   You can use the `altdq` megafunction to generate the DQ signals.

(2)   The `OE` signal is active low, but the Quartus II software implements this as active high and automatically adds an inverter before the `OE` register A_{OE} during compilation.

(3)   The `outclock` signal is phase shifted –90° from the system clock.

(4)   The shifted DQS signal must be inverted before going to the IOE. The inversion is automatic if you use the `altdq` megafunction to generate the DQ signals.

Figure 3–13. DQS Configuration in Stratix & Stratix GX IOE   *Note (1)*
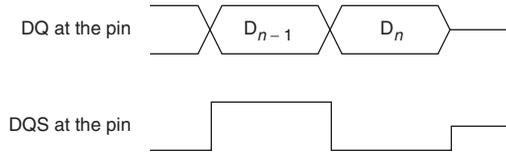

Notes to Figure 3–13:

(1) You can use the `altdqs` megafunction to generate the DQS signals.

(2) The `OE` signal is active low, but the Quartus II software implements this as active high and automatically adds an inverter before `OE` register A$_{OE}$ during compilation.

(3) The select line can be chosen in the `altdqs` MegaWizard Plug-In Manager.

(4) The `datain_l` and `datain_h` pins are usually connected to V$_{CC}$ and ground, respectively.

(5) DQS postamble handling is not shown in this diagram. For more information, see *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices*.

(6) This undelayed DQS signal goes to the LE for the soft postamble circuitry.

(7) You must invert this signal before it reaches the DQ IOE. This signal is automatically inverted if you use the `altdq` megafunction to generate the DQ signals. Connect this port to the `inclock` port in the `altdq` megafunction.

(8) DQS phase-shift circuitry is only available on DQS pins.

The Stratix and Stratix GX DDR IOE structure requires you to invert the incoming DQS signal by using a NOT gate to ensure proper data transfer. The `altdq` megafunction automatically adds the inverter when it generates the DQ signals. As shown in Figure 3–10, the `inclock` signal's rising edge clocks the A_I register, `inclock` signal's falling edge clocks the B_I register, and latch C_I is opened when `inclock` is one. In a DDR memory read operation, the last data coincides with DQS being low. If you do not invert the DQS pin, you do not get this last data because the latch does not open until the next rising edge of the DQS signal. The NOT gate is inserted automatically if the `altdq` megafunction is used; otherwise you need to add the NOT gate manually.
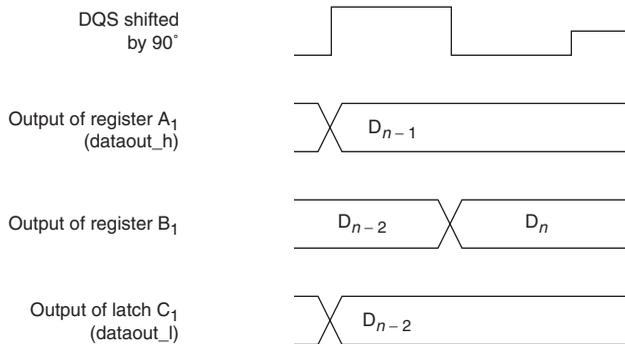
Figure 3–14 shows waveforms of the circuit shown in Figure 3–12. The second set of waveforms in Figure 3–14 shows what happens if the shifted DQS signal is not inverted; the last data, D_n, does not get latched into the logic array as DQS goes to tristate after the read postamble time. The third set of waveforms in Figure 3–14 shows a proper read operation with the DQS signal inverted after the 90° shift; the last data D_n does get latched. In this case the outputs of register A_I and latch C_I, which correspond to `dataout_h` and `dataout_l` ports, are now switched because of the DQS inversion.

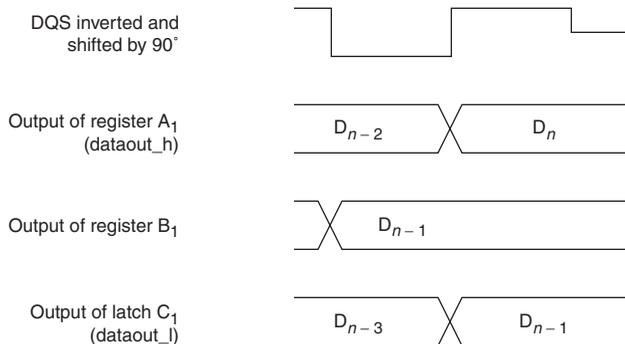*Figure 3–14. DQ Captures with Non-Inverted & Inverted Shifted DQS*

DQ & DQS Signals

DQ at the pin

DQS at the pin

D_{n-1} D_n

Shifted DQS Signal is Not Inverted

DQS shifted by 90˚

Output of register A_1 (dataout_h) D_{n-1}

Output of register B_1 D_{n-2} D_n

Output of latch C_1 (dataout_l) D_{n-2}

Shifted DQS Signal is Inverted

DQS inverted and shifted by 90˚

Output of register A_1 (dataout_h) D_{n-2} D_n

Output of register B_1 D_{n-1}

Output of latch C_1 (dataout_l) D_{n-3} D_{n-1}

PLL

When using the Stratix and Stratix GX top and bottom I/O banks (I/O banks 3, 4, 7, or 8) to interface with a DDR memory, at least one PLL with two outputs is needed to generate the system clock and the write clock. The system clock generates the DQS write signals, commands, and addresses. The write clock is –90° shifted from the system clock and generates the DQ signals during writes.

When using the Stratix and Stratix GX side I/O banks 1, 2, 5, or 6 to interface with DDR SDRAM devices, two PLLs may be needed per I/O bank for best performance. The side I/O banks do not have dedicated circuitry, so one PLL captures data from the DDR SDRAM and another PLL generates the write signals, commands, and addresses to the DDR SDRAM device. Stratix and Stratix GX devices side I/O banks can support DDR SDRAM up to 150 MHz.

For more information, see *AN 342: Interfacing DDR SDRAM with Stratix & Stratix GX Devices*.

Conclusion

Stratix and Stratix GX devices support SDR SDRAM, DDR SDRAM, RLDRAM II, QDR SDRAM, QDRII SRAM, and ZBT SRAM external memories. Stratix and Stratix GX devices feature high-speed interfaces that transfer data between external memory devices at up to 200 MHz/400 Mbps. Phase-shift circuitry in the Stratix and Stratix GX devices allows you to ensure that clock edges are properly aligned.