9. Implementing SFI-4 in Stratix & Stratix GX Devices

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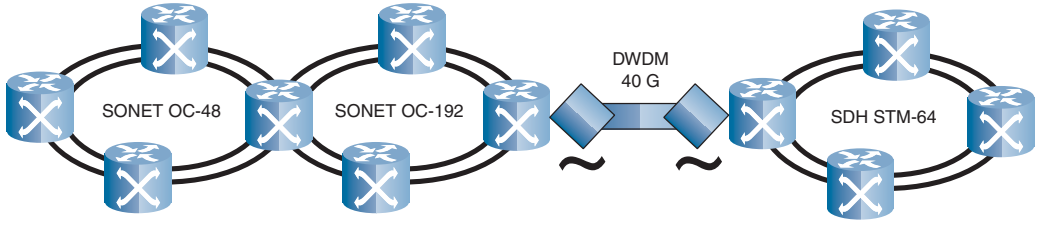
Introduction

The growth of the Internet has created huge bandwidth demands as voice, video, and data push the limits of the existing wide area network (WAN) backbones. To facilitate this bandwidth growth, speeds of OC-192 and higher are being deployed in WAN backbones (see Figure 9–1). Today's carrier backbone networks are supported by SONET/SDH transmission technology. SONET/SDH is a transmission technology for transporting optical signals at speeds ranging from 51 megabits per second (Mbps) up to 40 gigabits per second (Gbps). SONET/SDH rings make up the majority of the existing backbone infrastructure of the Internet and the public switched telephone network (PSTN).

The Optical Internetworking Forum (OIF) standard SFI-4 is a 16-bit LVDS interface used in an OC-192 SONET system to link the framer and the serializer/deserializer (SERDES). Stratix® and Stratix GX devices support the required data rates of up to 622.08 Mbps along with the one-to-one relationship required between clock frequency and data rate. The fast phase-locked loop (PLL) was designed to support the high clock frequencies and the one-to-one relationship (between clock and data rate) needed for interfaces such as XSBI and SFI-4. Support for SFI-4 extends the reach of high-density programmable logic from the backplane to the physical layer (PHY) devices.

This chapter focuses on the implementation of the interface between the SERDES and the framer.

Figure 9–1. WAN Backbone



A SONET/SDH transmission network is composed of several pieces of equipment, including terminal multiplexers, add-drop multiplexers, and repeater and digital cross-connect systems. SONET is the standard used in North America and SDH is the standard used outside North America.

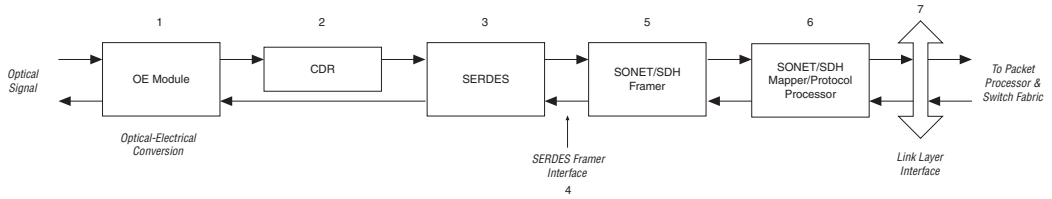
The SONET/SDH specification outlines the frame format, multiplexing method, synchronization method, and optical interface between the equipment, as well as the specific optical interface.

SONET/SDH continues to play a key role in the next generation of networks for many carriers. In the core network, the carriers offer services such as telephone, dedicated leased lines, and Internet protocol (IP) data, which are continuously transmitted. The individual data channels are not transmitted on separate lines; instead, they are multiplexed into higher speeds and transmitted on SONET/SDH networks at the corresponding transmission speed.

Figure 9–2 shows a typical SONET/SDH line card. The system operates as follows:

1. The SONET/SDH line card first takes a high-speed serial optical signal and converts it into a high-speed serial electrical signal. The devices are called physical media dependent (PMD) devices.
2. The system then recovers the clock from the electrical data using a clock data recovery (CDR) unit.
3. The SERDES parallelizes the data so that it can be manipulated easily at lower clock rates.
4. The interface between the SERDES and framer is called the SERDES framer interface. The interface requirements are defined by the OIF.
5. The framer identifies the beginning of the SONET/SDH frames and monitors the performance of the system.
6. The mapper following the framer maps asynchronous transfer mode (ATM) cells, IP packets, or T/E carrier signals into the SONET frame.
7. The PHY-link layer interface provides a bus interface to packet/cell processors or other link-layer devices.

Figure 9–2. SONET/SDH Line Card

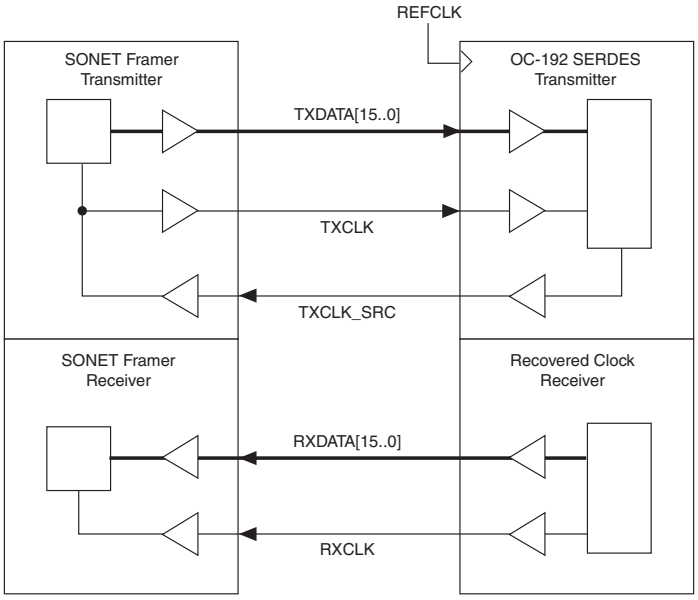


The OIF has defined the electrical interface (SFI) between the SONET/SDH framer and high-speed SERDES devices. To keep up with evolving transmission speeds and technology enhancements, different versions of electrical interfaces are defined. SFI-4 is the version of SFI that acts as an interface between an OC-192 SERDES and SONET framer, as shown in Figure 9–2. An aggregate of 9953.28 Mbps is transferred in each direction. With their differential I/O capabilities, Stratix and Stratix GX devices are ideally suited to support the framer side of the SFI-4 interface. Support for SFI-4 extends the reach of high-density programmable logic from the backplane to the PHY devices.

System Topology

The SFI-4 interface uses 16 channels of source-synchronous LVDS to interface between a SONET framer and an OC-192 SERDES. Figure 9–3 shows the SFI-4 interface.

Figure 9–3. SFI-4 Interface Signals



The framer transmits outbound data via TXDATA[15..0] and is received at the SERDES using TXCLK. TXCLK is derived from TXCLK_SRC, which is provided by the OC-192 SERDES. The framer receives incoming data on RXDATA[15..0] from the OC-192 SERDES. The data received is latched on the rising edge of RXCLK. Table 9–1 provides the data rates and clock frequencies specified by SFI-4. The modes of TXCLK are specified by the SFI-4 standard. In required mode (622 MHz clock mode or ×1 mode), TXCLK should run at 622.08 MHz. In optional mode (311 MHz clock mode or ×2 mode), TXCLK should run at 311.04 MHz.

Table 9–1. SFI-4 Interface Data Rates & Clock Frequencies

Signal	Performance
TXDATA[15..0]	622.08 Mbps
TXCLK	622.08 MHz or 311.04 MHz
TXCLK_SRC	622.08 MHz
RXDATA[15..0]	622.08 Mbps
RXCLK	622.08 MHz
REFCLK	622.08 MHz

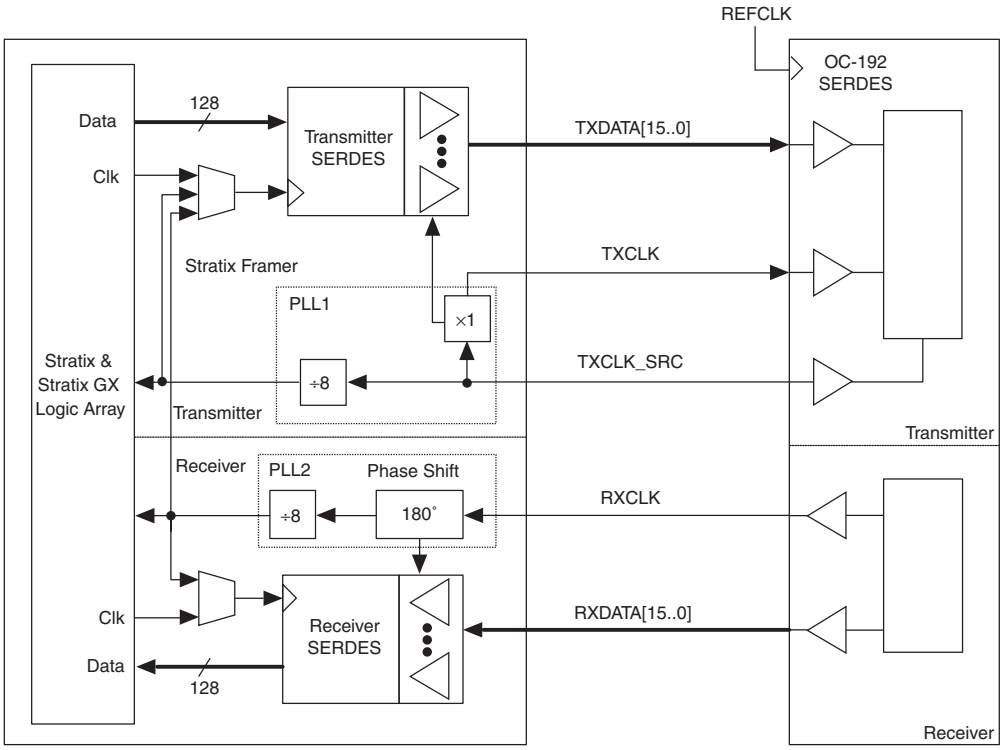
Interface Implementation in Stratix & Stratix GX Devices

The 16-bit full-duplex LVDS implementation of the framer part of the SFI-4 interface is shown in Figure 9–4. Stratix devices support source-synchronous interfacing and LVDS differential signaling up to 840 Mbps. Stratix devices have embedded SERDES circuitry for serial and parallel data conversion.

The source-synchronous I/O implemented in Stratix GX devices optionally includes dynamic phase alignment (DPA). DPA automatically and continuously tracks fluctuations caused by system variations and self-adjusts to eliminate the phase skew between the multiplied clock and the serial data, allowing for data rates of 1 Gbps. In non DPA mode the I/O behaves similarly to that of the Stratix I/O. This document assumes that DPA is disabled. However, it is simple to implement the same system with DPA enabled to take advantage of its features. For more information on DPA, see the *Stratix GX Transceivers* chapter in the *Stratix GX Device Handbook, Volume 1*.

The fast PLL enables 622.08 Mbps data transmission by transmitting and receiving a differential clock at rates of up to 645 MHz. The clocks required in the SERDES for parallel and serial data conversion can be configured from the received `RXCLK` (divided down), the `TXCLK_SRC` (divided down), or the asynchronous core clock. See Figure 9–4.

Figure 9–4. Implementation of SFI-4 Interface Using Stratix & Stratix GX Devices



For details on differential I/O buffers, SERDES, and clock dividers using PLLs, see the *High-Speed Differential I/O Interfaces in Stratix Devices* chapter in the *Stratix Device Handbook* or the *Stratix GX Device Handbook*.

Figure 9–5 shows the transmitter block (from Figure 9–4) of the SFI-4 framer interface implemented in Stratix and Stratix GX devices. The data starts in the logic array and goes into the Stratix and Stratix GX SERDES block. The transmitter SERDES of the framer converts the parallel data to serial data for the 16 TXDATA channels (TXDATA[15..0]). A fast PLL is used to generate TXCLK from TXCLK_SRC. The fast PLL keeps the TXDATA and TXCLK edge-aligned. A divided down (÷8) clock generated from TXCLK_SRC is used to convert the parallel data to serial in the transmitter SERDES. The divided down clock also clocks some of the logic in the logic array.

Figure 9–5. Framer Transmitter Interface in Stratix & Stratix GX Devices

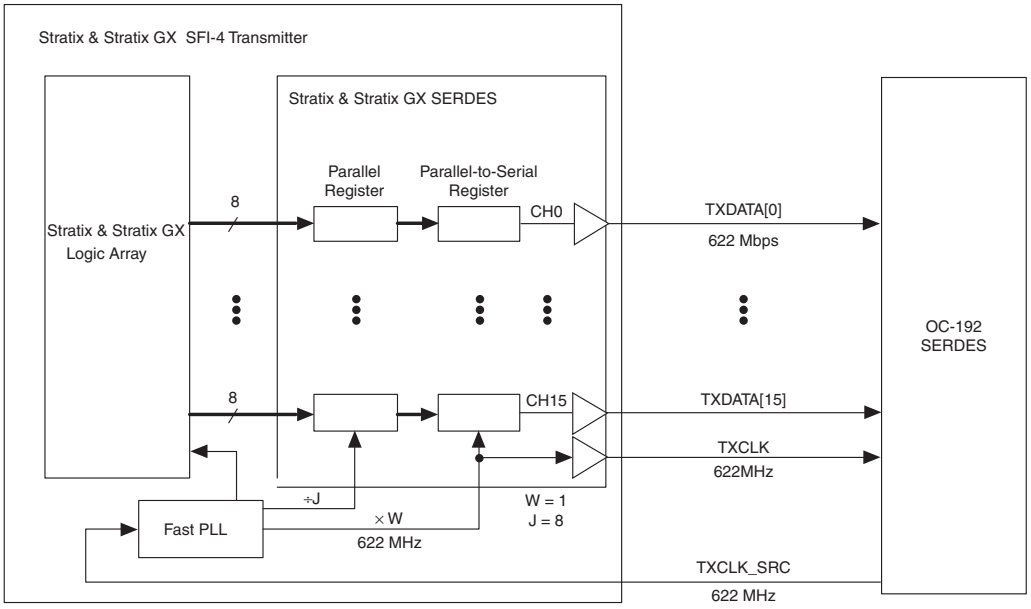
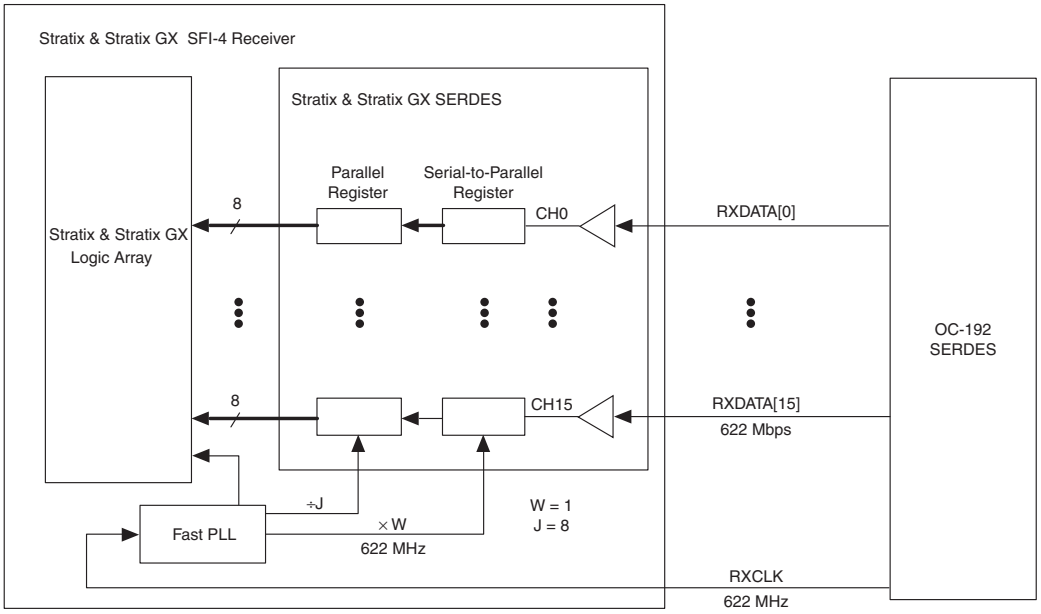


Figure 9–6 shows the receiver block (from Figure 9–4) of the SFI-4 framer interface implemented in Stratix and Stratix GX devices. RXDATA[15..0] is received from the OC-192 SERDES on the differential I/O pins of the Stratix or Stratix GX device. The receiver SERDES converts the high-speed serial data to parallel. You can generate the clocks required in the SERDES for parallel and serial data conversion from the received RXCLK. RXCLK is inverted (phase-shifted by 180°) to capture received data. While normal I/O operation guarantees that data is captured, it does not guarantee the parallelization boundary, which is randomly determined based on the power up of both communicating devices. The SERDES has embedded data realignment capability, which can be used to save logic elements (LEs).

Figure 9–6. Framer Receiver Interface in Stratix & Stratix GX Devices



Note to Figure 9–6:
(1) The figure shows Stratix GX DPA disabled.

For more information on the byte-alignment feature in Stratix and Stratix GX devices, see the *High-Speed Differential I/O Interfaces in Stratix Devices* chapter in the *Stratix Device Handbook* or the *Stratix GX Device Handbook*.

Tables 9–2 and 9–3 list the number of SFI-4 cores that can be implemented in Stratix and Stratix GX devices. See the *High-Speed Differential I/O Interfaces in Stratix Devices* chapter in the *Stratix Device Handbook* or the *Stratix GX Device Handbook* for the package type and the maximum number of channels supported by each package.

Table 9–2. Stratix SFI-4 Core Support

Stratix Device	Number of LVDS Channels (Receiver/Transmitter) (1)	Number of PLLs	Number of SFI-4 Interfaces (Maximum)
EP1S10	44/44	4	2
EP1S20	66/66	4	2
EP1S25	78/78	4	2
EP1S30	82/82	8	4
EP1S40	90/90	8	4
EP1S60	116/116	8	4
EP1S80	152/156	8	4

Note to Table 9–2:

(1) The LVDS channels can go up to 840 Mbps (or 1 Gbps using DPA in Stratix GX devices). This number includes both high speed and low speed channels. The high speed LVDS channels can go up to 840 Mbps. The low speed LVDS channels can go up to 462 Mbps. The *High-Speed Differential I/O Support* chapters in the *Stratix Device Handbook, Volume 1* and the *Stratix GX Device Handbook, Volume 1* and the device pin-outs on the web (**www.altera.com**) specify which channels are high and low speed.

Table 9–3. Stratix GX SFI-4 Core Support

Stratix GX Device	Number of LVDS Channels (Receiver/Transmitter) (1)	Number of PLLs	Number of SFI-4 Interfaces (Maximum)
EP1SGX10	22/22	2	1
EP1SGX25	39/39	2	2
EP1SGX40	45/45	4	2

Note to Table 9–3:

(1) The LVDS channels can go up to 840 Mbps, or 1 Gbps using DPA. This number includes both high speed and low speed channels. The high speed LVDS channels can go up to 840 Mbps. The low speed LVDS channels can go up to 462 Mbps. The *High-Speed Differential I/O Support* chapter in the *Stratix Device Handbook, Volume 1* and the *Stratix GX Device Handbook, Volume 1* and the device pin-outs on the web (**www.altera.com**) specify which channels are high and low speed.

AC Timing Specifications

Figures 9–7 through 9–9 and Tables 9–4 through 9–6 illustrate the timing characteristics of SFI-4 at the framer. Stratix and Stratix GX devices support all the timing requirements needed to support transmitter and receiver functions of a SFI-4 framer; only framer-related timing specifications are applicable.

For details on the timing specifications of LVDS I/O standards in Stratix and Stratix GX devices, see the *Stratix Device Family Data Sheet* section of the *Stratix Device Handbook, Volume 1* and the *High-Speed Differential I/O Interfaces in Stratix Devices* chapter or the *Stratix GX Device Family Data Sheet* section of the *Stratix GX Device Handbook, Volume 1* and the *High-Speed Differential I/O Interfaces in Stratix Devices* chapter

Figure 9–7 shows the timing diagram for the Stratix and Stratix GX framer transmitter ×1 (622 MHz clock) mode.

Figure 9–7. Framer Transmitter × 1 (622 MHz Clock) Mode Timing Diagram

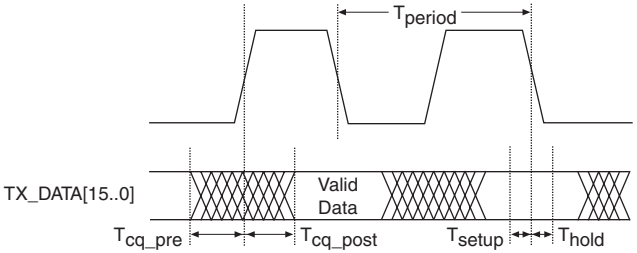


Table 9–4 lists the timing specifications for the SFI-4 framer transmitter in ×1 (622 MHz clock) mode.

Table 9–4. SFI-4 Framer Transmitter × 1 (622 MHz Clock) Mode Timing Specifications

Parameter	Value			Unit
	Min	Typ	Max	
TX_CLK (T_{period})		1,608		ps
Data invalid window before the rising edge (T_{cq_pre})			200	ps
Data invalid window after the rising edge (T_{cq_post})			200	ps
TX_CLK duty cycle	40		60	%
Framer transmitter channel-to-channel skew			200	ps

Figure 9–8 shows the timing diagram for the SFI-4 framer transmitter in ×2 (311 MHz clock) mode

Figure 9–8. Framer Transmitter × 2 (311 MHz Clock) Mode Timing Diagram

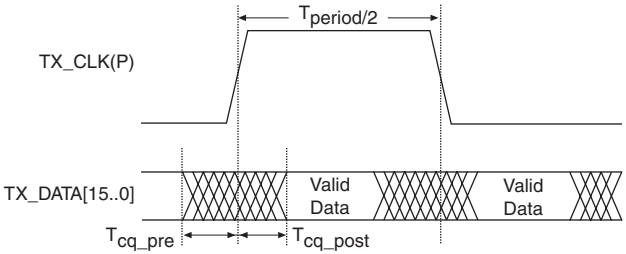


Table 9–5 lists the timing specifications for the SFI-4 framer transmitter in ×2 (311 MHz clock) mode.

Table 9–5. SFI-4 Framer Transmitter × 2 (311 MHz Clock) Mode Timing Specifications

Parameter	Value			Unit
	Min	Typ	Max	
TX_CLK (T_{period})		3,215		ps
Data invalid window before the rising edge (T_{cq_pre})			200	ps
Data invalid window after the rising edge (T_{cq_post})			200	ps
TX_CLK duty cycle	48		52	%
Framer transmitter channel-to-channel skew			200	ps

Figure 9–9 shows the timing diagram for the SFI-4 framer receiver.

Figure 9–9. Framer Receiver Timing Diagram

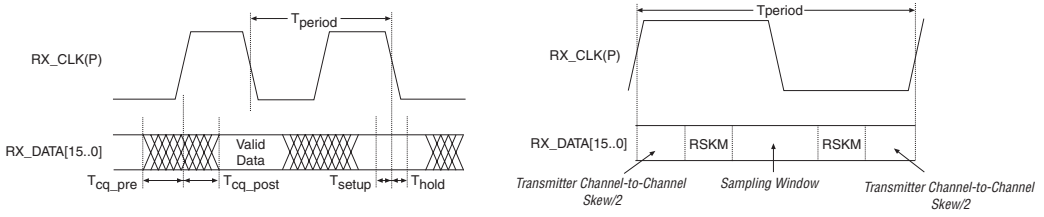


Table 9–6 lists the timing specifications for the SFI-4 framer receiver.

Table 9–6. Framer Receiver Timing Specifications

Parameter	Value			Unit
	Min	Typ	Max	
RX_CLK (T_{period})		1,608		ps
Data invalid window before the rising edge (T_{cq_pre})			200	ps
Data invalid window after the rising edge (T_{cq_post})			200	ps
RX_CLK duty cycle	45		55	%
Data set-up time (T_{setup})	300			ps
Data hold time (T_{hold})	300			ps
Framer sampling window	600			ps
Receiver skew margin (RSKM)			304	ps

Electrical Specifications

SFI-4 uses LVDS as a high-speed data transfer mechanism to implement the SFI-4 interface. Table 9–7 lists the DC electrical characteristics for the interface, which are based on the IEEE Std. 1596.3-1996 7 specification. For more information on the voltage specification of LVDS I/O standards in Stratix and Stratix GX devices, see the *Stratix Device Family Data Sheet* section of the *Stratix Device Handbook, Volume 1* and the *High-Speed Differential I/O Interfaces in Stratix Devices* chapter or the *Stratix GX Device Family Data Sheet* section of the *Stratix GX Device Handbook, Volume 1* and the *High-Speed Differential I/O Interfaces in Stratix Devices* chapter.

Table 9–7. Framer LVDS DC Specifications

Parameter	Value			Unit
	Min	Typ	Max	
Output differential voltage (V_{OD})	250		600 *(1)*	mV
Output offset voltage (V_{OS})	1,125		1,375	mV
Output Impedance, single ended	40		140	W
Change in V_{OD} between ‘0’ and '1'			50	mV
Change in V_{OD} between '1' and '0'			50	mV
Input voltage range (V_I)	0		2,400	mV
Differential impedance		100		W
Input differential voltage (V_{ID})	100		600	mV
Receiver differential input impedance	70		130	W
Ground potential difference (between PCS and PMA)			50	mV
Rise and fall times (20% to 80%)	100		400	ps

Note to Table 9–7:
(1) The IEEE standard requires 400 mV. A larger swing is encouraged, but not required.

Software Implementation

The SFI-4 interface uses a 16-bit LVDS I/O interface. The Altera® Quartus® II software version 2.0 supports Stratix and Stratix GX devices, allowing you to implement LVDS I/O buffers through the Quartus II Assignment Organizer.

For information on the Quartus II Assignment Organizer, see the Quartus II Software Help.

Conclusion

SFI-4 is the standard interface between SONET framers and optical SERDES for OC-192 interfaces. With embedded SERDES and fast PLLs, Stratix and Stratix GX devices can easily support the SFI-4 framer interface, enabling
10-Gbps (OC-192) data transfer rates. Stratix and Stratix GX I/O supports the required data rates of up to 622.08 Mbps. Stratix and Stratix GX fast PLLs are designed to support the high clock frequencies and one-to-one relationship needed for interfaces such as XSBI and SFI-4. Stratix and Stratix GX devices can support multiple SFI-4 functions on one device.