Upcoming Stratix IV Device Features

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This document lists the Stratix® IV device family features that include transceivers, LVDS and memory interfaces, which will be enabled in the future Quartus® II software versions. It is intended to provide a high level overview of the upcoming features.

Stratix IV Device Features

The following items show the current and future support for Stratix IV GX device features:

The following items show the current and future support for Stratix IV GT device features:

The following items show the current and future support for Stratix IV E device features:

Stratix IV GX Device Enhancements

Item 1. Clock Data Recover (CDR) Block and Receiver Input Buffer Offset Cancellation

Current Support	Stratix IV GX devices provide an offset cancellation circuit per transceiver channel to counter the offset variations due to process, voltage, and temperature. This feature is currently disabled in the Quartus II software.
Future Support	The Quartus II software will allow you to enable this circuit and control it through the dynamic reconfiguration controller.

Item 2. Low Uncertainty Latency Option

Current Support	This option is primarily intended for use in systems implementing CPRI/OBSAI or similar protocols that require deterministic latency. To reduce the uncertainty in PMA and PCS data paths, the following features are independently available: ■ Receiver phase compensation FIFO can be configured in registered mode ■ Ability to connect receiver word aligner output to transmit bit slipper input to make latency inserted due to word alignment deterministic
Future Support	The following options will be available to further reduce the uncertainty in PMA and PCS data paths: ■ The transmit phase compensation FIFOs configured in registered mode ■ The feedback path for the CMU PLL, which compensates for the uncertainty caused by the parallel divider in the block.

Item 3. Multi-Channel Bonding

Current Support	The Quartus II software allows the following bonded configurations: ■ ×4 bonded configuration in Basic, XAUI, and PCI Express (PIPE) functional modes. Both PCS and PMA functional blocks are bonded in these modes. ■ ×4 bonded configuration in (OIF) CEI PHY interface functional mode. Only the PMA functional blocks are bonded in this mode. ■ ×8 bonded configuration in Basic mode and PCI Express (PIPE) Gen.1 ×8 functional mode only. ■ ×N (up to full-side) bonded configuration for Basic PMA direct bonded functional mode.
Future Support	Based on characterization results, the Quartus II software will support the bonding of PCS and PMA functional blocks in more than eight transceiver channels up to full-side bonding. SFI-S is a good example that requires ×12 bonded configuration with both PCS and PMA bonded.

Item 4. Flexible Master/Slave Configuration

Current Support	The Quartus II software requires the lower transceiver block to be the master for basic ×8 (PCS and PMA bonded) mode and PCI Express (PIPE) ×8 configuration. The master transceiver block provides all the shared control signals and clocks to the adjacent transceiver block. The current Quartus II software requires the physical `channel0` in the master transceiver block to be assigned as the logical `channel0` of a ×8 link.
Future Support	Based on characterization, the Quartus II software will allow: ■ Any of the two transceiver blocks of a ×8 link to be configured as the master transceiver block ■ Any channel within a ×8 bonded configuration to be assigned as logical `channel0`

Item 5. Dynamic Reconfiguration for Stratix IV GX Devices

Current Support	Stratix IV GX devices provide the option to dynamically reconfigure the following: ■ PMA settings → Pre-emphasis settings → Equalization settings → DC gain settings → Voltage Output Differential (VOD) settings ■ Transceiver channels → Channel functional mode → Channel PLL select between two CMU PLLs within a transceiver block → Channel data rate switching → CMU PLL settings For more details, refer to the *Stratix IV Dynamic Reconfiguration* chapter in the *Stratix IV Device Handbook*.
Future Support	Stratix IV GX devices provide the option to dynamically reconfigure the following: ■ Bonded configurations ■ Adaptive equalization circuit ■ Channel PLL select between ATX PLLs and CMU PLLs from any transceiver block

Item 6. ATX PLL (also known as LC Tank PLL) Placement

Current Support	Manual placement of ATX PLLs is required to achieve low skew. Automatic placement of ATX PLLs is not optimized to achieve low skew. Refer to the *Manual Placement of CMU and ATX PLLs in Stratix IV Devices* white paper on this topic for more details.
Future Support	Based on the design, the ATX PLL location will be automatically picked by the Quartus II software for low skew. This feature will simplify use of ATX PLLs in your design.

Item 7. Adaptive Equalization

Current Support	None
Future Support	The adaptive equalization feature will enable the Stratix IV GX transceiver to adapt to changing data rates and backplane characteristics by dynamically tuning the equalization settings of the receiver without user intervention. The adaptive equalization block in Stratix IV GX devices will consume lower power compared to Stratix II GX devices. It will also support a standby mode for lower power consumption. In standby mode, the adaptive equalization block locks in the selected equalization settings instead of continuously tuning the equalization settings for the receiver.

Item 8. Decision Feedback Equalization

Current Support	None
Future Support	High-speed signals transmitted across a backplane experience signal attenuation due to skin effect, dielectric losses, and crosstalk. The Stratix IV GX device will provide multi-tap decision feedback equalization (DFE) to primarily compensate the backplane attenuation due to crosstalk. DFE is effective in canceling out post cursor inter-symbol interference by boosting only the high frequency components of a signal without noise amplification. DFE can be used in conjunction with pre-emphasis, linear equalization (Manual Equalization), and adaptive equalization (AEQ).

Item 9. Electrical Idle in Basic Functional Mode

Current Support	The Quartus II software supports forcing the transmitter buffer into electrical idle in PCI Express (PIPE) functional mode In Stratix IV GX devices.
Future Support	In addition to the current support, the Quartus II software will support forcing the transmitter buffer into electrical idle in Basic functional modes.

Item 10. Signal Detect Capability in Basic Functional Mode

Current Support	In Stratix IV GX devices, signal detect capability is supported by the Quartus II software in PCI Express (PIPE) functional mode only.
Future Support	In addition to the current support, the Quartus II software will support signal detect capability in Basic functional modes.

Item 11. HyperTransport Support in Transceivers

Current Support	None
Future Support	The Quartus II software will provide HyperTransport 3.0 support at data rates between 600 Mbps to 3.2 Gbps (Gen1 and Gen3 data rates). Data rates less than 600 Mbps will be supported through over sampling. The transceiver will be configured in bonded channel configuration with PMA direct mode enabled. Support for AC coupling for HyperTransport functional mode will be determined after characterization.

Item 12. PCI Express Hard-IP Support for Stratix IV GX Devices

Current Support	Stratix IV GX devices provide support for PCI Express endpoint modes in Gen1 ×1, ×4, ×8 configurations and Gen2 ×1, ×4, ×8 configurations. The following modes are also supported: ■ Endpoint modes in Gen2 ×8 configuration. ■ Rootport modes in Gen1 ×1, ×4, ×8 and Gen2 ×1, ×4, ×8 configurations. ■ Runtime reconfiguration of PCI read only registers.
Future Support	In addition to the current support, Stratix IV GX devices will also support runtime switching between endpoint and rootport modes.

Item 13. On-Chip Scope

Current Support	None
Future Support	The on-chip scope (OCS) estimates the eye opening of the signal inside the chip at the input of the CDR block on the receive side using phase interpolation technique. It provides a way to assess the effectiveness of the receiver equalizer, thereby enabling system engineers to analyze and debug the signal integrity of a transmission link inside the chip. The OCS can be used in conjunction with the CDR block to select the optimum phase with the maximum eye opening.

Stratix IV GT Device Enhancements

Table 1 shows additional Stratix IV GT devices that will be supported.

Table 1. Support for Additional Device

Feature	EP4S100G3F45	EP4S100G4F45
Package	F1932	F1932
Logic Elements	291,200	353,600
Total Transceiver Channels	48	48
10G Transceiver Channels *(1)*	24	24
8G Transceiver Channels *(2)*	8	8

Table 1. Support for Additional Device

Feature	EP4S100G3F45	EP4S100G4F45
Clock Multiplier Unit (CMU) Channels (PMA-only) *(3)*	16	16

Notes to Table 1:

(1) 10G transceiver channels support data rates between 2.488 Gbps and 10.3125 Gbps.

(2) 8G transceiver channels support data rates between 2.488 Gbps and 8.5 Gbps. All 10G transceiver channels can also be configured as 8G transceiver channels.

(3) CMU channels that support data rates between 2.488 Gbps and 6.5 Gbps are PMA-only channels that do not have PCS circuitry. For more information, refer to *Stratix IV Transceiver Architecture* chapter in volume 2 of the *Stratix IV Device Handbook*.

Item 14 through Item 17 show current and future support for Stratix IV GT device features.

Item 14. Enhanced Data Rate Support for Stratix IV GT Devices

Current Support	Data rates up to 10.3125 Gbps are supported in Stratix IV GT devices.
Future Support	Data rate support will be enhanced to 11.3 Gbps.

Item 15. PCI Express Hard-IP Support for Stratix IV GT Devices

Current Support	Not enabled on any channels
Future Support	PCI Express Gen1 ×1, ×4 and Gen2 ×1, ×4 modes will be available in one transceiver block of the device. This support will be available for devices in F1932 pin packages only.

Item 16. Dynamic Reconfiguration for Stratix IV GT Devices

Current Support	Dynamic reconfiguration of pre-emphasis and VOD settings for the PMA are supported.
Future Support	Adaptive equalization and the ability to reconfigure it will be available for all transceiver blocks.

Item 17. Industrial Speed Grades for Stratix IV GT Devices

Current Support	None
Future Support	Industrial speed grades I1, I2 and I3 will be available that operate from 0°C–100°C.

Stratix IV E Device Enhancements

Item 18 shows the previous and updated offerings for the Stratix IV E devices that will be supported. The EP4SE820 device replaces the EP4SE680 device. All references to the EP4SE680 in the current Stratix IV Device handbook apply to the EP4SE820.

Item 18. Previous Stratix IV E Device Offering

Feature	EP4SE110	EP4SE230	EP4SE290			EP4SE360			EP4SE530			EP4SE680		
Package Pin Count	780	780	780	1152	1517	780	1152	1517	1152	1517	1760	1152	1517	1760
ALMs	42,240	91,200	116,480			141,440			212,480			272,440		
LEs	105,600	228,000	291,200			353,600			531,200			681,100		
High-Speed LVDS SERDES (up to 1.6 Gbps)	56	56	56	88	88	56	88	88	88	112	112	88	112	132
SPI-4.2 Links	3	3	3	4		3	4		4	6		4	6	7
M9K Blocks (256 × 36 bits)	660	1,235	936			1,248			1,280			1,529		

Item 18. Previous Stratix IV E Device Offering

Feature	EP4SE110	EP4SE230	EP4SE290			EP4SE360			EP4SE530			EP4SE680		
M144K Blocks (2048 × 72 bits)	16	22	36			48			64			64		
Total Memory (MLAB+M9K+ M144K) Kbits	9,564	17,133	17,248			22,564			27,376			31,491		
Embedded Multipliers (18 × 18)	512	1,288	832			1,040			1,024			1,360		
PLLs	4	4	4	8	12	4	8	12	8	12	12	8	12	12
User I/Os *(1)*	480	480	480	736	864	480	736	864	736	960	960	736	960	1,104

Note to Item 18:

(1) The user I/O count includes all general purpose I/Os and dual purpose configuration pins. Transceiver pins, dedicated configuration pins and dedicated clock pins are not included in the user I/O count.

Item 18. Updated Stratix IV E Device Offering

Feature	EP4SE230	EP4SE360		EP4SE530			EP4SE820		
Package Pin Count	780	780	1152	1152	1517	1760	1152	1517	1760
ALMs	91,200	141,440		212,480			325,220		
LEs	228,000	353,600		531,200			813,050		
High-Speed LVDS SERDES (up to 1.6 Gbps)	56	56	88	88	112	112	88	112	132
SPI-4.2 Links	3	3	4	4	6		4	6	6
M9K Blocks (256 × 36 bits)	1,235	1,248		1,280			1610		
M144K Blocks (2048 × 72 bits)	22	48		64			60		
Total Memory (MLAB+M9K+ M144K) Kbits	17,133	22,564		27,376			33,294		
Embedded Multipliers (18 × 18)	1,288	1,040		1,024			960		
PLLs	4	4	8	8	12	12	8	12	12
User I/Os *(1)*	488	488	744	744	976	976	744	976	1120
Speed Grade (fastest to slowest)	–2,–3, –4	–2,–3, –4	–2,–3, –4	–2,–3, –4	–2,–3, –4	–2,–3, –4	–3, –4	–3, –4	–3, –4

Note to Item 18:

(1) The user I/O count includes all general purpose I/Os, dedicated clock pins, and dual purpose configuration pins. Transceiver pins and dedicated configuration pins are not included in the user I/O count.

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