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1. Intel® Stratix® 10 E-Tile Transceiver PHY Overview

Intel® Stratix® 10 devices offer up to 144 transceivers with integrated high-speed analog signal conditioning and clock data recovery circuits for chip-to-chip, chip-to-module, and backplane applications.

Intel Stratix 10 devices contain a combination of GX, GXT, or GXE channels in addition to hardened IP blocks for PCI Express and Ethernet applications.

Intel Stratix 10 devices introduce several transceiver tile variants to support a wide variety of protocol implementations. These transceiver tile variants are L-, H-, and E-Tiles. This user guide focuses on E-Tile transceivers.

The full contents of the user guide are going through a final review and will be provided at a later date.