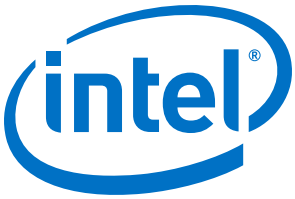

Intel Stratix 10 Embedded Memory User Guide

UG-S10MEMORY
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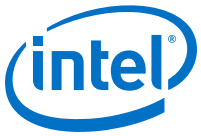
Contents

1 Stratix® 10 Embedded Memory Overview 4
1.1 Stratix 10 Embedded Memory Features 4
1.2 Stratix 10 Embedded Memory Capacity 6
2 Stratix 10 Embedded Memory Architecture and Features 8
2.1 Byte Enable in Stratix 10 Embedded Memory Blocks 8
2.1.1 Byte Enable Controls 8
2.1.2 Data Byte Output 9
2.1.3 Byte Enable Behavior 9
2.2 Address Clock Enable Support 9
2.3 Asynchronous Clear and Synchronous Clear 11
2.4 Memory Blocks Error Correction Code Support 12
2.4.1 Parity Bit 13
2.4.2 Error Correction Code Truth Table 13
2.5 Force-to-Zero 13
2.6 Coherent Read 14
2.7 Stratix 10 Embedded Memory Operation Modes 16
2.8 Stratix 10 Embedded Memory Clocking Modes 17
2.8.1 Single Clock Mode 18
2.8.2 Read/Write Clock Mode 18
2.8.3 Input/Output Clock Mode 18
2.8.4 Asynchronous/Synchronous Clears in Clocking Modes 18
2.8.5 Output Read Data in Simultaneous Read/Write 18
2.8.6 Independent Clock Enables in Clocking Modes 18
2.9 Stratix 10 Embedded Memory Configurations 19
2.9.1 Mixed-Width Port Configurations 19
2.9.2 Mixed-Width Ratio Configurations 19
2.10 Freeze Logic 19
2.11 Hardware Behavior 20
3 Stratix 10 Embedded Memory Design Considerations 21
3.1 Consider the Memory Block Selection 21
3.2 Customize Read-During-Write Behavior 21
3.2.1 Same-Port Read-During-Write Mode 22
3.2.2 Mixed-Port Read-During-Write Mode 23
3.3 Consider Power-Up State and Memory Initialization 25
3.4 Reduce Power Consumption 25
4 Stratix 10 Embedded Memory IP Core References 27
4.1 On-Chip Memory RAM and ROM IP Cores 27
4.1.1 On-Chip Memory RAM: 1-Port IP Core Parameters 28
4.1.2 On-Chip Memory RAM: 2-Port IP Core Parameters 30
4.1.3 On-Chip Memory RAM: 4-Port IP Core Parameters 36
4.1.4 On-Chip Memory ROM: 1-PORT IP Core Parameters 38
4.1.5 On-Chip Memory ROM: 2-PORT IP Core Parameters 40
4.1.6 On-Chip Memory RAM and ROM Interface Signals 42
4.2 Stratix 10 eSRAM IP Core 46



A Revision History for Stratix 10 Embedded Memory User Guide..... 48

1 Stratix® 10 Embedded Memory Overview

Stratix® 10 embedded memory blocks are flexible and provide an optimal amount of various sized memory arrays to fit your design requirements.

Related Links

HyperFlex Core Architecture, Stratix 10 Device Overview
Provides more information about Hyper-Registers and the HyperFlex core architecture. Hyper-Registers are additional registers available in every interconnect routing segment throughout the core fabric, including the routing segments connected to the memory logic array block (MLAB) and M20K block inputs and outputs.

1.1 Stratix 10 Embedded Memory Features

The Stratix 10 devices contain three types of memory blocks: Embedded SRAM (eSRAM) blocks, M20K blocks, and memory logic array blocks (MLABs).

- 45-Megabit (Mb) eSRAM blocks
  - Fast path, low latency, high bandwidth and very high random transaction rate (RTR) on-chip memory block
  - Each block consists of 8 channels and each channel has 40 banks.
  - Each bank is configurable to 2K depth and 72-bit data width
  - Supports only simple dual port RAM with concurrent read and write access per channel
- 20-kilobit (Kb) M20K blocks
  - Blocks of dedicated memory resources.
  - Ideal for larger memory arrays, while providing a large number of independent ports.
- 640-bit MLABs
  - Enhanced memory blocks configured from dual-purpose logic array blocks (LABs).
  - Ideal for wide and shallow memory arrays.
  - Optimized for implementation of shift registers for digital signal processing (DSP) applications, wide and shallow FIFO buffers, and filter delay lines.
  - Each MLAB is made up of ten adaptive logic modules (ALMs).

In Stratix 10 devices, you can configure each ALM in the MLAB as ten 32×2 blocks. The Stratix 10 devices provide one 32×20 simple dual-port SRAM block per MLAB.

The Stratix 10 embedded memory blocks support the following operation modes:

- Single-port RAM/ROM
- Simple dual-port RAM/ROM
- True dual-port RAM/ROM
- Simple quad-port RAM
- Shift-register
- FIFO

Table 1. Stratix 10 Embedded Memory Features

This table summarizes the features supported by the Stratix 10 embedded memory blocks.

Features	eSRAM	M20K	MLAB
Maximum operating frequency	750 MHz	1 GHz	1 GHz
Total RAM bits (including parity bits)	45 Mb	20,480 bits	640 bits
Byte enable	–	Supported	Supported
Packed mode	–	–	–
Address clock enable	–	Supported (only in simple dual-port RAM mode)	Supported
Simple dual-port mixed width	–	Supported	–
FIFO buffer mixed width	–	Supported	–
Memory Initialization File (.mif)	–	Supported	Supported
Dual-clock mode	–	Supported (only in simple dual-port RAM mode)	Supported
Full synchronous memory	–	Supported	Supported
Asynchronous memory	–	–	Only for flow-through read memory operations
Power-up state	–	Output ports are cleared	• Registered output ports are cleared • Unregistered output ports read memory contents
Asynchronous/Synchronous Clears	–	Output registers and output latches	Output registers and output latches
Write/read operation triggering	Rising clock edges	Rising clock edges	Rising clock edges
Same-port read-during-write	–	Output ports set to *New Data* or *Don't Care*	Output ports set to *Don't Care*

continued...

Features	eSRAM	M20K	MLAB
Mixed-port read-during-write	–	Output ports set to *Old Data* or *Don't Care*	Output ports set to *New Data*, *Old Data*, or *Don't Care*
Error Correction Code (ECC) support	• Soft IP using the Quartus® Prime software • Built-in support ×64-wide simple dual-port mode	• Soft IP using the Quartus Prime software • Hard IP • Built-in support ×32-wide simple dual-port mode • Parity bits	Soft IP using the Quartus Prime software
Coherent read	Write-forwarding feature • ON = New Data • OFF = Old Data	Supported	–

1.2 Stratix 10 Embedded Memory Capacity

Table 2. Embedded Memory Capacity and Distribution in Stratix 10 Devices

This table lists the embedded memory capacity for Stratix 10 GX, Stratix 10 SX, and Stratix 10 TX variants.

Variant	Product Line	eSRAM		M20K		MLAB		Total RAM Bit (Mbits)
		Block	RAM Bit (Mbits)	Block	RAM Bit (Mbits)	Block	RAM Bit (Mbits)	
Stratix 10 GX	GX 400	NA	NA	1,537	30	3,276	2	32
	GX 650	NA	NA	2,489	49	5,364	3	52
	GX 850	1	45	3,477	68	7,124	4	117
	GX 1100	1	45	4,401	86	9,540	6	137
	GX 1650	2	90	5,851	114	13,764	8	212
	GX 2100	2	90	6,501	127	17,316	11	228
	GX 2500	NA	NA	9,963	195	20,529	13	208
	GX 2800	NA	NA	11,721	229	23,796	15	244
	GX 4500	NA	NA	7,033	137	37,821	23	160
	GX 5500	NA	NA	7,033	137	47,700	29	166
Stratix 10 SX	SX 400	NA	NA	1,537	30	3,276	2	32
	SX 650	NA	NA	2,489	49	5,364	3	52
	SX 850	1	45	3,477	68	7,124	4	117
	SX 1100	1	45	4,401	86	9,540	6	137
	SX 1650	2	90	5,851	114	13,764	8	212
	SX 2100	2	90	6,501	127	17,316	11	228
	SX 2500	NA	NA	9,963	195	20,529	13	208
	SX 2800	NA	NA	11,721	229	23,796	15	244
	SX 4500	NA	NA	7,033	137	37,821	23	160
	SX 5500	NA	NA	7,033	137	47,700	29	166

continued...

Variant	Product Line	eSRAM		M20K		MLAB		Total RAM Bit (Mbits)
		Block	RAM Bit (Mbits)	Block	RAM Bit (Mbits)	Block	RAM Bit (Mbits)	
Stratix 10 TX	TX 1650	2	90	5,851	114	13,764	8	212
	TX 2100	2	90	6,501	127	17,316	11	228
	TX 2500	NA	NA	9,963	195	20,529	13	208
	TX 2800	NA	NA	11,721	229	23,796	15	244

2 Stratix 10 Embedded Memory Architecture and Features

The Stratix 10 embedded memory features include operation modes, clocking modes, and configurations.

2.1 Byte Enable in Stratix 10 Embedded Memory Blocks

The Stratix 10 embedded memory blocks support byte enable controls.

- The byte enable controls mask the input data so that only specific bytes of data are written. The unwritten bytes retain the values written previously.
- The write enable (`wren`) signal, together with the byte enable (`byteena`) signal, control the write operations on the embedded memory blocks. By default, the `byteena` signal is high (enabled) and only the `wren` signal controls the writing.
- The byte enable registers do not have a `clear` port.
- If you are using parity bits, the byte enable function controls 10-bit data. The function controls the data bits and the parity bits..
- Byte enables operate in a one-hot fashion. The LSB of the `byteena` signal corresponds to the LSB of the data bus.
- The byte enable signals are active high.

2.1.1 Byte Enable Controls

Table 3. Byte Enable Controls in ×10 Data Width (MLAB)

byteena[1:0]	Data Bits Written	
11 (default)	[9:5]	[4:0]
10	[9:5]	–
01	–	[4:0]
00	–	–

Table 4. Byte Enable Controls in ×20 Data Width (M20K)

byteena[1:0]	Data Bits Written	
11 (default)	[19:10]	[9:0]
10	[19:10]	–
01	–	[9:0]
00	–	–

Table 5. Byte Enable Controls in ×40 Data Width (M20K)

byteena[3:0]	Data Bits Written			
1111 (default)	[39:30]	[29:20]	[19:10]	[9:0]
1000	[39:30]	–	–	–
0100	–	[29:20]	–	–
0010	–	–	[19:10]	–
0001	–	–	–	[9:0]
0000	–	–	–	–

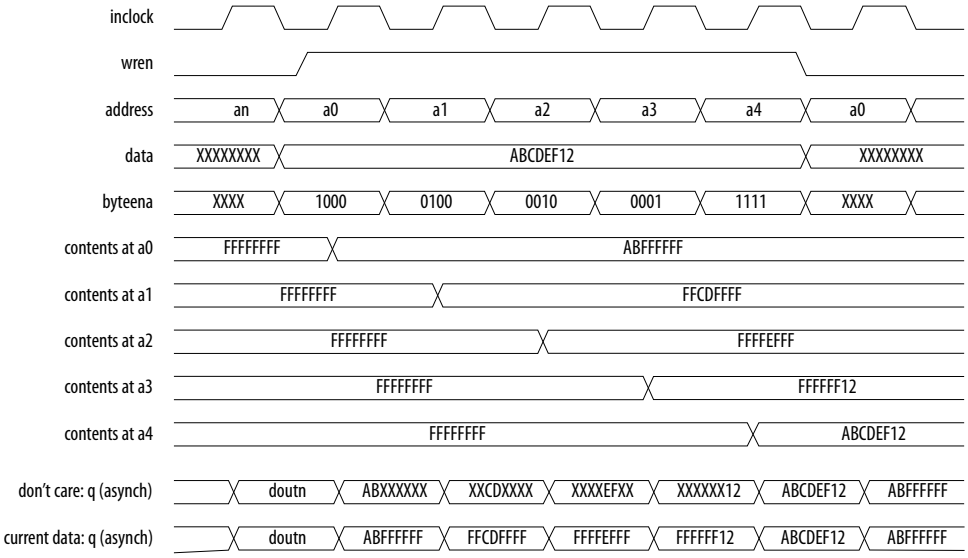
2.1.2 Data Byte Output

In M20K blocks or MLABs, when you deassert a byte-enable bit to 0 during a write cycle, the corresponding data byte output appears as either a *Don't Care* value, or the current data at that location. You can control the output value for the masked byte in the M20K blocks or MLABs by using the Quartus Prime software.

2.1.3 Byte Enable Behavior

Figure 1. Byte Enable Functional Waveform

This figure shows how the `wren` and `byteena` signals control the operations of the embedded memory blocks.



2.2 Address Clock Enable Support

Stratix 10 embedded memory blocks support address clock enable. When you enable address clock enable (`addressstall` = 1), it holds the previous address value.

Note: Only simple dual-port mode supports this feature.

When you configure the memory blocks in dual-port mode, each port has its own independent address clock enable.

Figure 2. Address Clock Enable

This figure shows an address clock enable block diagram.

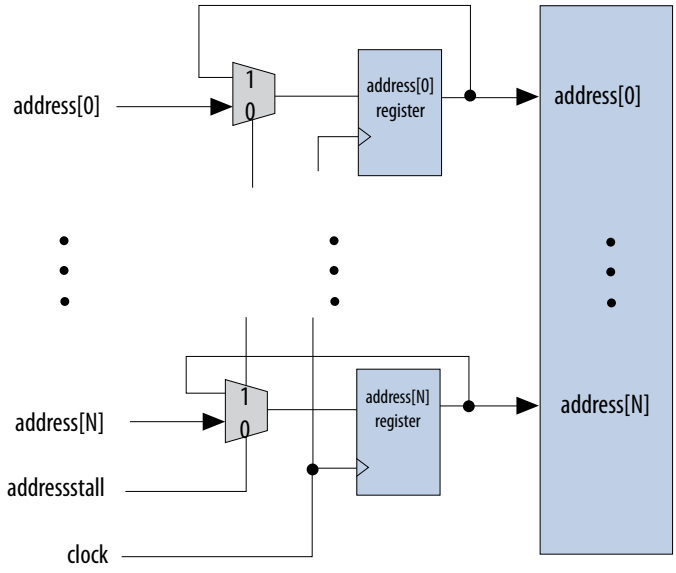


Figure 3. Address Clock Enable During Read Cycle

This figure shows the address clock enable behavior during read cycle.

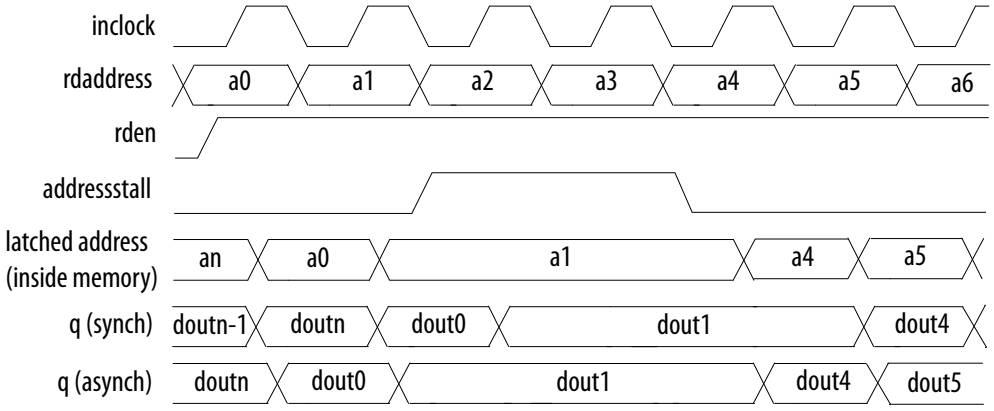
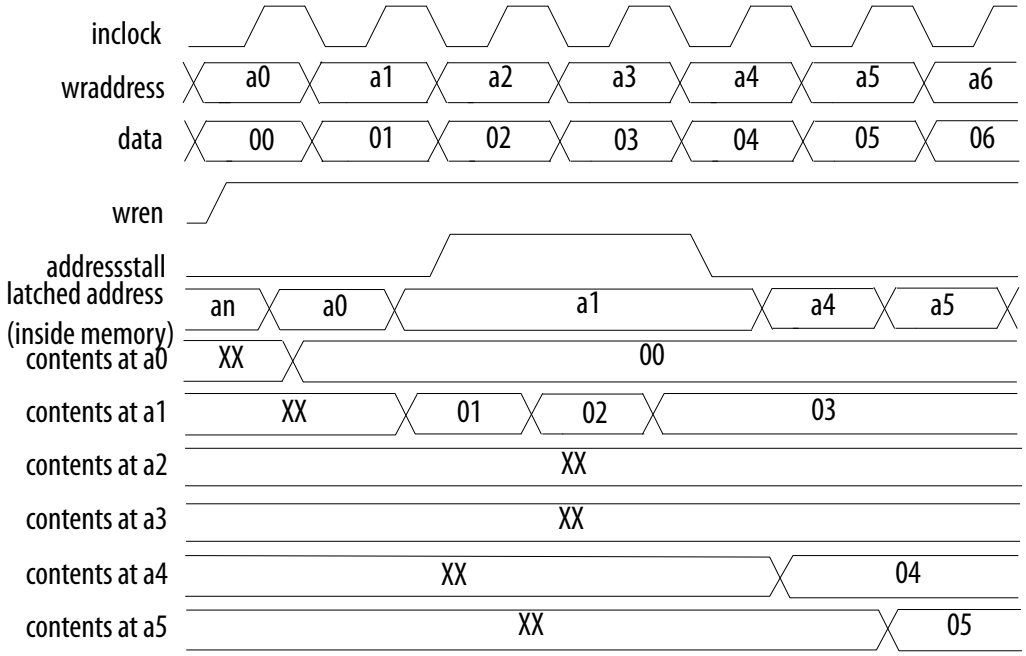


Figure 4. Address Clock Enable During Write Cycle

This figure shows the address clock enable behavior during write cycle.



2.3 Asynchronous Clear and Synchronous Clear

The embedded memory blocks support asynchronous clear and synchronous clear on output latches and output registers.

If your RAM does not use output registers, clear the RAM outputs using the output latch asynchronous clear (`aclr`). The (`aclr`) signal is generated at any time. The internal logic extends the clear pulse until the next rising edge of the output clock. When the `aclr` signal asserts, the outputs are cleared and stay cleared until the next read cycle.

Figure 5. Behavior of Asynchronous Clear and Synchronous Clear In Registered Mode

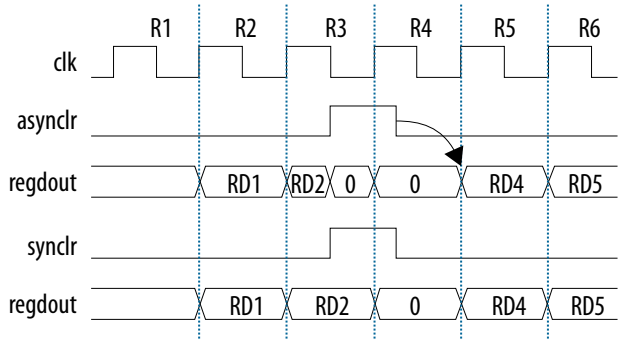
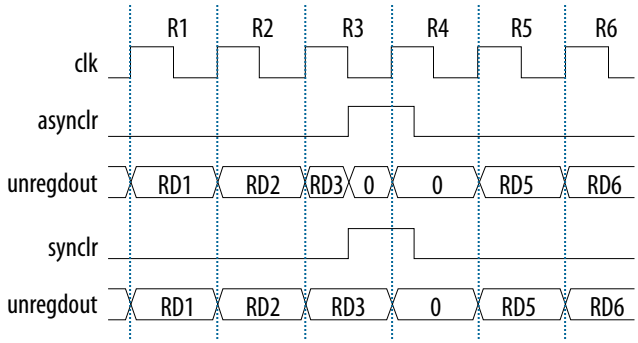


Figure 6. Behavior for Asynchronous Clear and Synchronous Clear In Unregistered Mode



2.4 Memory Blocks Error Correction Code Support

ECC detects and corrects data errors at the output of the memory.

Only M20K blocks and eSRAM blocks support the ECC feature.

If you engage the ECC feature, you cannot use the following features:

- Byte enable
- Read-during-write
- Coherent read

M20K Blocks

For M20K blocks, ECC performs single-error correction, double-adjacent-error correction, and triple-adjacent-error correction in a 32-bit word. However, ECC cannot guarantee detection or correction of non-adjacent two-bit or more errors.

The M20K blocks have built-in support for ECC when in ×32-wide simple dual-port mode.

- When you engage the ECC feature, the M20K runs slower than the non-ECC simple-dual port mode. However, you can enable optional ECC pipeline registers before the output decoder to achieve higher performance compared to non-pipeline ECC mode at the expense of one-cycle latency.
- Two ECC status flag signals—e (error) and ue (uncorrectable error) indicate the M20K ECC status. The status flags are part of the regular outputs from the memory block. When you engage ECC, you cannot access two of the parity bits because the ECC status flag replaces them.

eSRAM Blocks

For eSRAM blocks, ECC performs single-error correction and double-error correction in a 64-bit word.

The eSRAM blocks have built-in support for ECC when in ×64-wide simple dual-port mode.

- Two ECC status flag signals—e (error) and ue (uncorrectable error) indicate the eSRAM ECC status. .

2.4.1 Parity Bit

The following describes the parity bit support for M20K blocks:

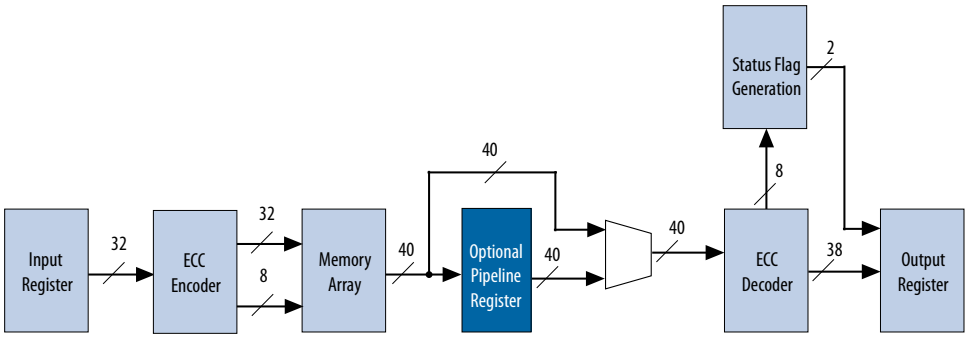
- 2 parity bits are associated with every 8 data bits in data widths of 10, 20, and 40.
- In non-parity data widths, the parity bits are skipped during read or write operations.
- Parity function is not performed on the parity bit.

2.4.2 Error Correction Code Truth Table

Table 6. ECC Status Flags Truth Table

e (error) (eccstatus[1])	ue (uncorrectable error) (eccstatus[0])	Status
0	0	No error.
0	1	Illegal.
1	0	An error is correctable. The error has been corrected at the outputs. The corrected data appears at the outputs; but the memory array has not been updated.
1	1	An error is uncorrectable. The uncorrectable data appears at the outputs.

Figure 7. ECC Block Diagram for M20K Memory



2.5 Force-to-Zero

The Force-to-Zero feature clears the read data output when you do not assert the read enable signal.

You have the option to turn on **Enable Force-to-Zero feature** in the parameter editors of the RAM/ROM IP cores. This feature is applicable only for M20K blocks.

Note: When you turn on **Enable Force-to-Zero feature**, the read enable signal does not retain previous values when you deassert the signal.

2.6 Coherent Read

You can use the coherent read feature to perform multiple operations correctly using internal forwarding.

The M20K memory block implements internal forwarding paths that allow read/modify/write operations on memories with 1 or 2 levels of pipelining. In coherent mode, data on the memory output reflect data written to the same address in current or previous clock cycles.

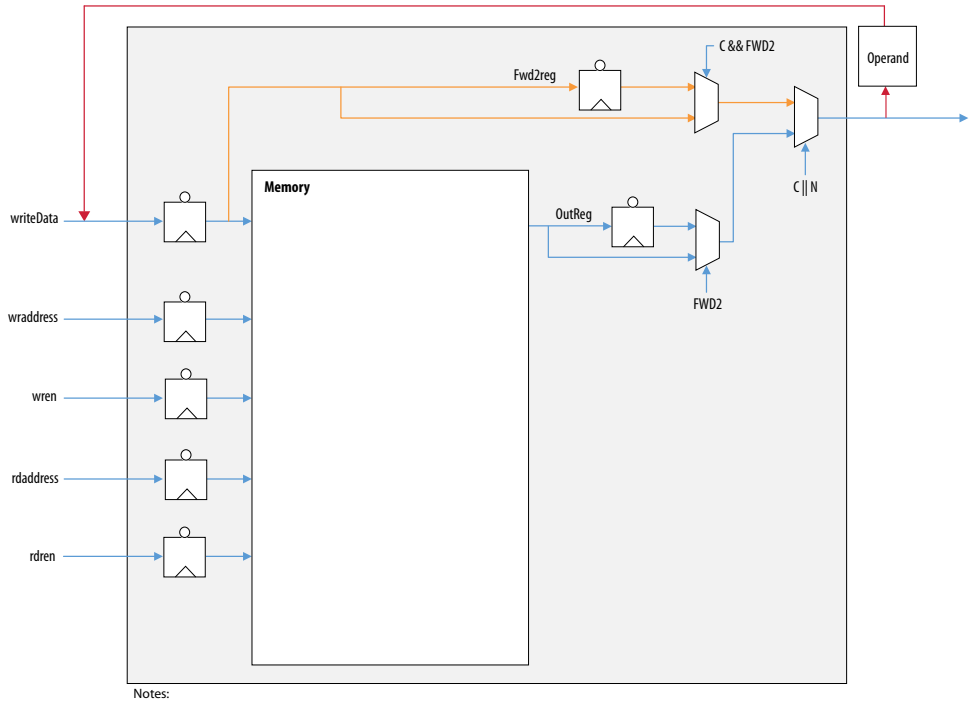
For example, this feature enables back-to-back increments to the same memory location. The M20K coherency logic does the following functions:

- In 1-level pipelining
  - Compares the current cycle read-address with the current cycle write-address.
  - Feeds through write data into read output if the current read-address and current write-address match.
- In 2-level pipelining
  - Compares the current cycle read-address with the previous cycle write-address.
  - Feeds through the previous cycle write pipelined data into read output if the current read-address and previous write-address match.

If you engage the coherent read feature, you cannot use the following features:

- Byte enable
- ECC
- Mixed-width configuration

Figure 8. Boundary of Internal Forwarding Implementation



Notes:
1. N = (rden_reg && wren && (rdAdd_reg == wrAdd)) ? 1 : 0.
2. C = (rden_reg && wren_reg && (rdAdd_reg == wrAdd_reg)) ? 1 : 0.
3. R = (forwarding_stage2) ? 1 : 0.
4. C is registered when forwarding_stage2 is selected.

Figure 9. 1-level pipelining Waveform

This figure shows the waveform of the 1-level pipelining with the read enable (rden) signal is high (enable).

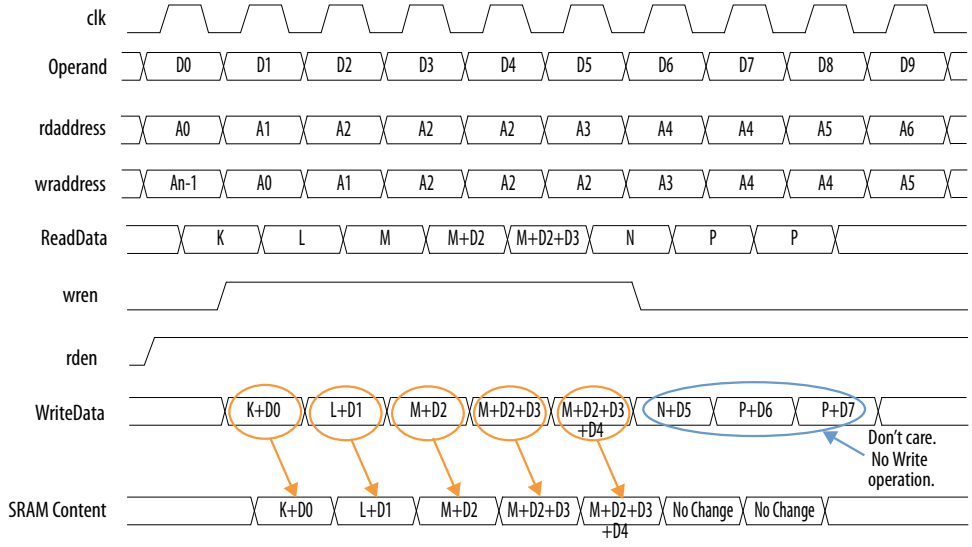
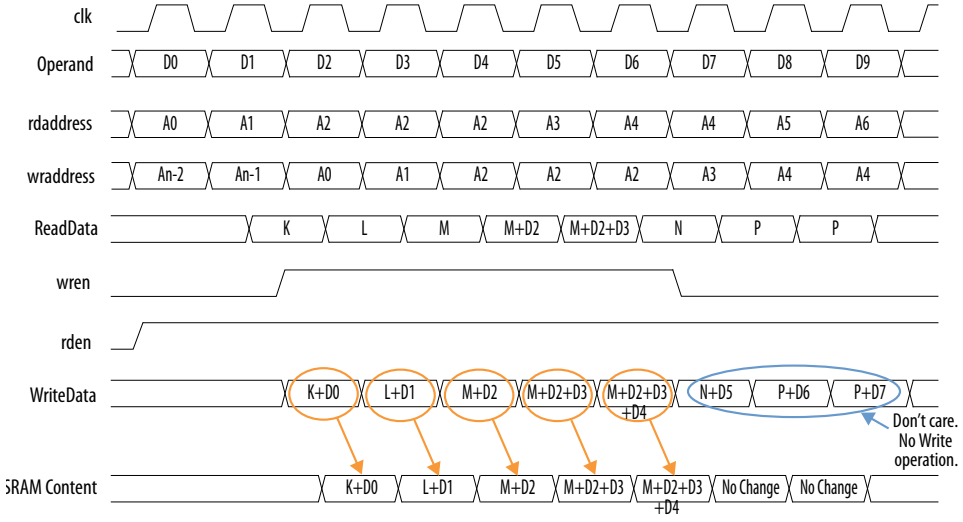


Figure 10. 2-level pipelining Waveform

This figure shows the waveform of the 2-level pipelining with the read enable (rden) signal is high (enable).



2.7 Stratix 10 Embedded Memory Operation Modes

Table 7. Stratix 10 Memory Operation Modes

This table lists and describes the memory modes that are supported in the Stratix 10 embedded memory blocks.

Operation Mode	M20K Support	MLAB Support	Description
Single-port RAM	Yes	Yes	You can perform only one read or one write operation at a time. Use the read enable port to control the RAM output ports behavior during a write operation: • To retain the previous values that are held during the most recent active read enable—create a read-enable port and perform the write operation with the read enable port deasserted. • To show the new data being written, the old data at that address, or a *Don't Care* value when read-during-write occurs at the same address location—do not create a read-enable signal, or activate the read enable during a write operation.
Simple dual-port RAM	Yes	Yes	You can simultaneously perform one read and one write operations to different locations where the write operation happens on port A and the read operation happens on port B.
True dual-port RAM	Yes	–	You can perform any combination of two port operations: two reads, two writes, or one read and one write at single clocking mode.
Simple quad-port RAM	Yes	–	You can simultaneously perform two read and two write operations to different locations where the write operation happens on port A and port B, and the read operation happens on port A1 and port B2 at single clocking mode.
Shift-register	Yes	Yes	Use the memory blocks as a shift-register block to save logic cells and routing resources.

continued...

Operation Mode	M20K Support	MLAB Support	Description
			This mode is useful in DSP applications that require local data storage such as finite impulse response (FIR) filters, pseudo-random number generators, multi-channel filtering, and auto- and cross- correlation functions. Traditionally, the local data storage is implemented with standard flip-flops that exhaust many logic cells for large shift registers. The input data width (w), the length of the taps (m), and the number of taps (n) determine the size of a shift register (w × m × n). You can cascade memory blocks to implement larger shift registers.
ROM	Yes	Yes	Use the memory blocks as ROM. • Initialize the ROM contents of the memory blocks using a **.mif** or **.hex**. • The address lines of the ROM are registered on M20K blocks but can be unregistered on MLABs. • The outputs can be registered or unregistered. • The output registers can be asynchronously or synchronously cleared. • The ROM read operation is identical to the read operation in the single-port RAM configuration.
FIFO	Yes	Yes	You can use the memory blocks as FIFO buffers. Use the SCFIFO and DCFIFO IP cores to implement single- and dual-clock asynchronous FIFO buffers in your design. For designs with many small and shallow FIFO buffers, the MLABs are ideal for the FIFO mode. However, the MLABs do not support mixed-width FIFO mode.

Caution: To avoid corrupting the memory contents, do not violate the setup time or hold time on any of the embedded memory block input registers during read and write operations. This limitation is applicable if you use the memory blocks in single-port RAM, simple dual-port RAM, true dual-port RAM, simple quad-port RAM, or ROM mode.

2.8 Stratix 10 Embedded Memory Clocking Modes

Each Stratix 10 embedded memory operation mode has supporting clocking modes.

Table 8. Memory Blocks Clocking Modes Supported for Each Memory Mode

Clocking Mode	Memory Mode					
	Single-Port	Simple Dual-Port	True Dual-Port	Simple Quad-Port	ROM	FIFO
Single clock mode	Yes	Yes	Yes	Yes	Yes	Yes
Read/write clock mode	–	Yes	–	–	–	Yes
Input/output clock mode	Yes	Yes	–[1]	–[1]	Yes	–

Note: The clock enable signals are supported for write address, byte enable, and data input registers on MLAB blocks.

1 Both input and output modes share the same clock.

2.8.1 Single Clock Mode

In the single clock mode, a single clock, together with a clock enable, controls all registers of the embedded memory block.

2.8.2 Read/Write Clock Mode

In the read/write clock mode, a separate clock is available for each read and write port.

- A read clock controls the data-output, read-address, and read-enable registers.
- A write clock controls the data-input, write-address, write-enable, and byte enable registers.

2.8.3 Input/Output Clock Mode

In input/output clock mode, a separate clock is available for each input and output port.

- An input clock controls all registers related to the data input to the embedded memory block including data, address, byte enables, read enables, and write enables.
- An output clock controls the data output registers.

2.8.4 Asynchronous/Synchronous Clears in Clocking Modes

In all clocking modes, asynchronous and synchronous clears are available only for output latches and output registers.

For the independent (read/write and input/output) clock modes, the asynchronous and synchronous clears are available on both ports.

2.8.5 Output Read Data in Simultaneous Read/Write

If you perform a simultaneous read/write to the same address location using the read/write clock mode, the output read data is unknown. If you require the output read data to be a known value, use single-clock or input/output clock mode and select the appropriate read-during-write behavior in the parameter editors of the RAM/ROM IP cores.

2.8.6 Independent Clock Enables in Clocking Modes

Independent clock enables are supported in the following clocking modes:

- Read/write clock mode—supported for both read and write clocks.
- Input/output clock mode—supported for the registers of both ports.

To save power, you can control the shutdown of a particular register using the clock enables.

2.9 Stratix 10 Embedded Memory Configurations

Table 9. Supported Embedded Memory Block Configurations

This table lists the maximum configurations supported for the Stratix 10 embedded memory blocks.

Embedded Memory Block	Depth (bits)	Programmable Width
MLAB	32	×16, ×18, or ×20
M20K	512	×32 or ×40 *Note:* For simple dual-port only.
	1024	×16 or ×20 *Note:* For simple dual-port and true dual-port.
	2048	×8 or ×10 *Note:* For simple dual-port, true dual-port, and simple quad-port.
eSRAM	2048	×72

Note: Unlike previous technologies, Stratix 10 devices do not support 1/32, 1/16, and 1/8 mixed-width port ratios.

2.9.1 Mixed-Width Port Configurations

The mixed-width port configuration is supported only in simple dual-port RAM memory operation modes.

Note: MLABs do not support mixed-width port configurations.

2.9.2 Mixed-Width Ratio Configurations

Table 10. Supported Mixed-width Ratio Configurations for Stratix 10

Operation Mode	Mixed-width Ratio	
	Without Byte Enable	With Byte Enable
Simple dual-port	1, 2, 4, 8, 16, and 32 *Note:* 8, 16, and 32 are emulated.	1, 2, and 4
True dual-port	1	1
Simple quad-port	1	1

2.10 Freeze Logic

The freeze logic feature specifies whether to implement clock-enable circuitry for use in a partial reconfiguration region.

You have the option to turn on **Implement clock-enable circuitry for use in a partial reconfiguration** to enable the freeze logic feature in the parameter editors of the RAM/ROM IP cores. This feature is applicable only to the RAM modes:

- Single-port RAM
- Dual-port RAM
- Quad-port RAM

2.11 Hardware Behavior

The Stratix 10 embedded memory blocks provide both corrupting and non-corrupting hardware behaviors using dual concurrent write operation on the same address. This feature is applicable if you use the memory blocks in true dual-port and single quad-port modes.

By default, the memory blocks will corrupt upon the dual concurrent write at the same address. To show a non-corrupting hardware behavior in the memory blocks, include the user-defined option “ENA_NON_CORRUPT=1” in the simulator setup script.

When the dual concurrent write occurs, the physical emulation uses a time-division multiplexing method to multiplex Port A and Port B together under the same data width. In this sequence, the value of Port B will be written first, followed by the value of Port A at the same address. This results the value of Port A being written to the memory.

3 Stratix 10 Embedded Memory Design Considerations

There are several considerations that require your attention to ensure the success of your Stratix 10 designs.

Note: Unless noted otherwise, these considerations apply to all variants of the Stratix 10 device family.

3.1 Consider the Memory Block Selection

The Quartus Prime software automatically partitions user-defined memory into the embedded memory blocks based on your design's speed and size constraints. For example, the Quartus Prime software may spread out the memory across multiple available memory blocks to increase the performance of your design.

To assign the memory to a specific block size manually, use the parameter editor of the On-Chip Memory IP cores.

For the MLABs, you can implement single-port SRAM through emulation using the Quartus Prime software. Emulation minimizes additional use of logic resources.

Because of the dual purpose architecture of the MLAB, the block has only data input registers, output registers, and write address registers. The MLABs gain read address registers from the ALMs.

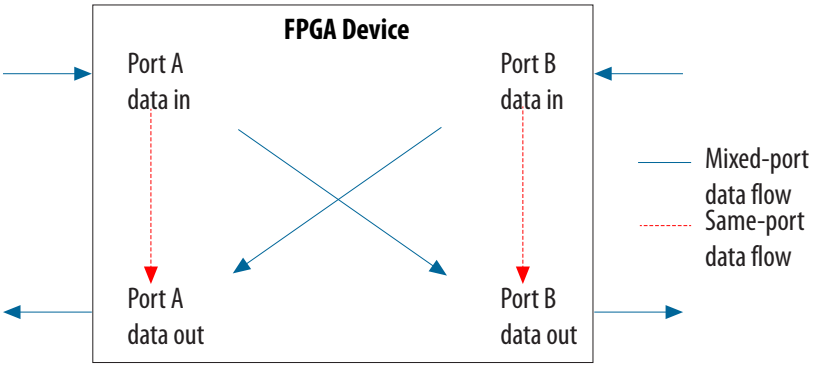
Note: For Stratix 10 devices, the Resource Property Editor and the TimeQuest Timing Analyzer report the location of the M20K block as *EC_X<number>_Y<number>_N<number>*, even though the assigned location allowed is *M20K_X<number>_Y<number>_N<number>*. Embedded Cell (EC) is the sub-location of the M20K block.

3.2 Customize Read-During-Write Behavior

Customize the read-during-write behavior of the memory blocks to suit your design requirements.

Figure 11. Read-During-Write Data Flow

This figure shows the difference between the two types of read-during-write operations available: same port and mixed port.



3.2.1 Same-Port Read-During-Write Mode

The same-port read-during-write mode applies to a single-port RAM or the same port of a true dual-port RAM.

Table 11. Output Modes for Embedded Memory Blocks in Same-Port Read-During-Write Mode

This table lists the available output modes if you select the embedded memory blocks in the same-port read-during-write mode.

Output Mode	Memory Type	Description
New Data	M20K	The new data is available on the rising edge of the same clock cycle on which the new data is written.
Don't Care	M20K, MLAB	The RAM produces *Don't Care* values for a read-during-write operation.

Figure 12. Same-Port Read-During-Write: New Data Mode

This figure shows sample functional waveforms of same-port read-during-write behavior in the *New Data* mode.

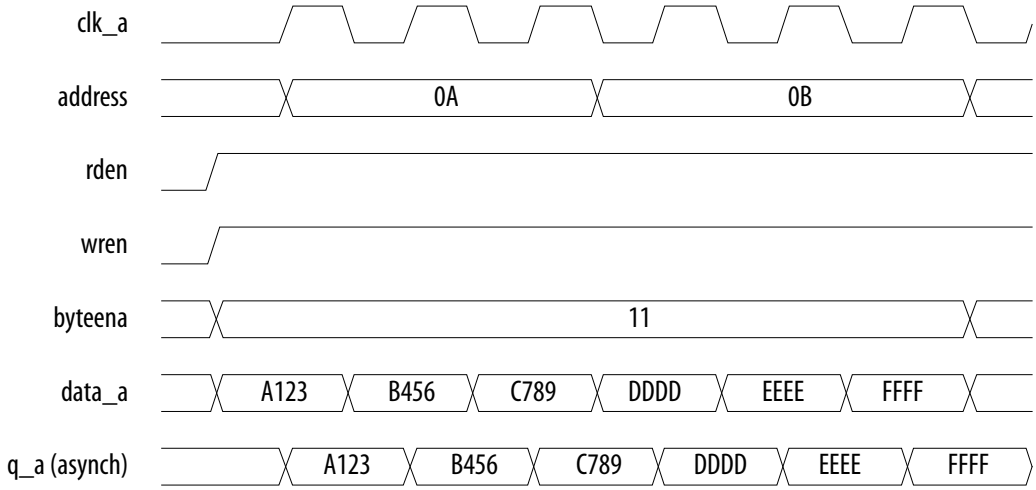
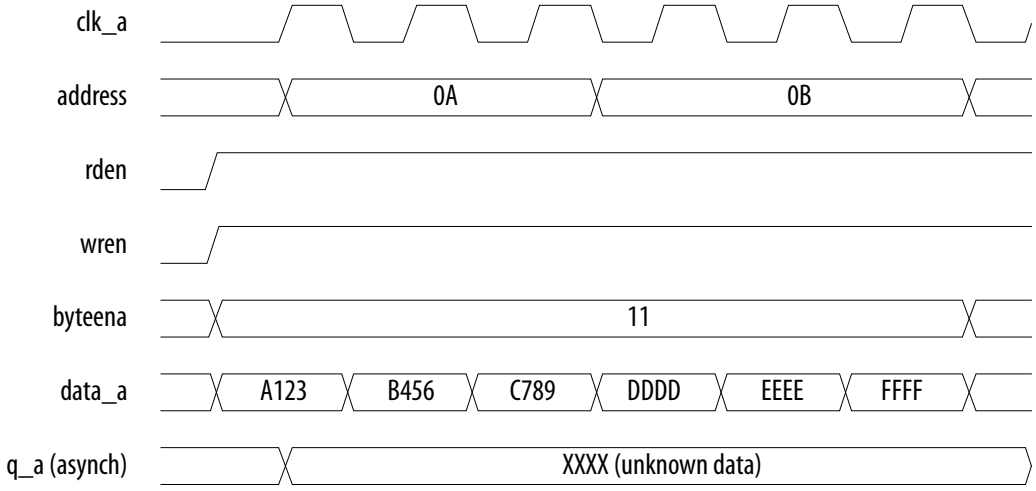


Figure 13. Same-Port Read-During-Write: Don't Care Mode

This figure shows sample functional waveforms of same-port read-during-write behavior in the *Don't Care* mode.



3.2.2 Mixed-Port Read-During-Write Mode

The mixed-port read-during-write mode applies to simple dual-port RAM mode.Two ports perform read and write operations on the same memory address using the same clock: one port reading from the address, and the other port writing to it.

Table 12. Output Modes for RAM in Mixed-Port Read-During-Write Mode

Output Mode	Memory Type	Description
New Data	MLAB	A read-during-write operation to different ports causes the MLAB registered output to reflect the *New Data* on the next rising edge after the data is written to the MLAB memory. This mode is available only if the output is registered.
Old Data	M20K, MLAB	A read-during-write operation to different ports causes the RAM output to reflect the *Old Data* value at that particular address. For MLAB, this mode is available only if the output is registered.
Don't Care	M20K, MLAB	The RAM produces *Don't Care* or *Unknown* value. • For M20K, the Quartus Prime software does not analyze the timing between write and read operations. • For MLAB, the Quartus Prime software does not analyze the timing between write and read operations by default. To enable this behavior: — Turn off the **Do not analyze the timing between write and read operation. Metastability issues are prevented by never writing and reading at the same address at the same time** option in the embedded memory IP core parameter editor. or — Turn on the **MLAB Add Timing Constraints For Mixed-Port Feed-Through Mode Setting Don't Care** option in the **Advanced Fitter Setting**.

Figure 14. Mixed-Port Read-During-Write: New Data Mode

This figure shows a sample functional waveform of mixed-port read-during-write behavior for the *New Data* mode.

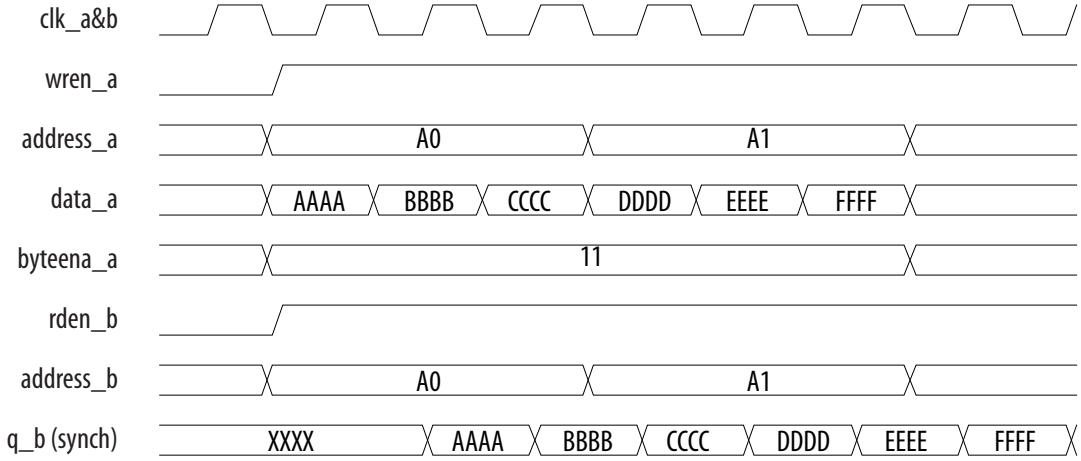


Figure 15. Mixed-Port Read-During-Write: Old Data Mode

This figure shows a sample functional waveform of mixed-port read-during-write behavior for the *Old Data* mode.

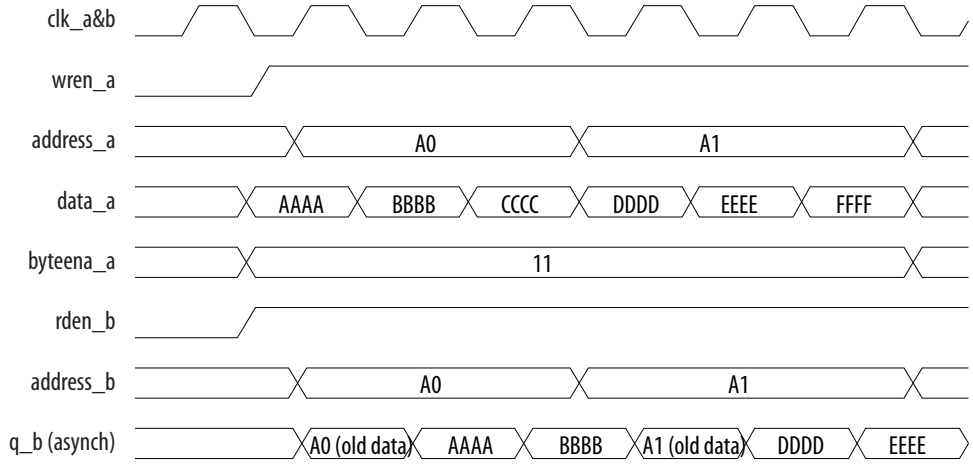
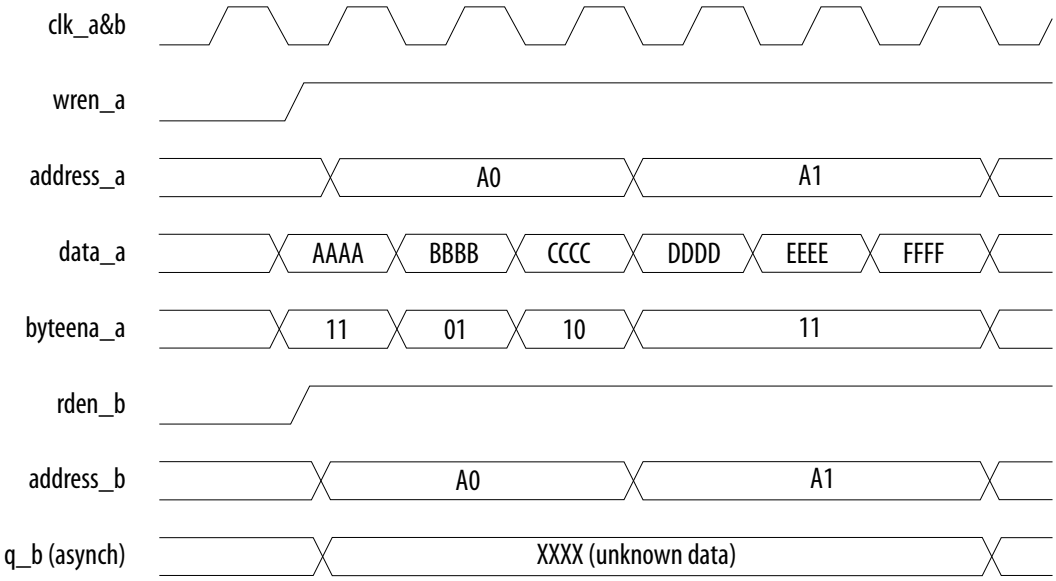


Figure 16. Mixed-Port Read-During-Write: Don't Care Mode

This figure shows a sample functional waveform of mixed-port read-during-write behavior for the *Don't Care* mode.



3.3 Consider Power-Up State and Memory Initialization

Consider the power-up state of the different types of memory blocks if your design logic evaluates the initial power-up values.

Table 13. Initial Power-Up Values of Embedded Memory Blocks

Memory Type	Output Registers	Power-Up Value
MLAB	Used	Zero (cleared)
	Bypassed	Read memory contents
M20K	Used	Zero (cleared)
	Bypassed	Zero (cleared)

By default, the Quartus Prime software initializes the embedded memory block in Stratix 10 devices to zero, unless you specify in the memory contents in a `.mif`.

All embedded memory blocks support initialization with a `.mif`. You can create `.mif` files in the Quartus Prime software and specify their use with the on-chip memory IP core when you instantiate a memory in your design. Even if a memory is pre-initialized (for example, using a `.mif`), the memory still powers up with its output cleared.

3.4 Reduce Power Consumption

Reduce alternating current (AC) power consumption of each memory block in your design.

- Use the Stratix 10 memory block clock enables to control the clocking of each embedded memory block.
- Use the read enable signal to ensure that read operations occur only when necessary. If your design does not require read-during-write, you can reduce power consumption by deasserting the read enable signal during write operations and when there are no memory operations.
- Use the Quartus Prime software to automatically place any unused embedded memory blocks in low-power mode to reduce static power.

4 Stratix 10 Embedded Memory IP Core References

You can access the features of the Stratix 10 Embedded Memory using the On-Chip Memory IP cores in the Quartus Prime software.

The On-Chip Memory IP cores include:

- RAM: 1-Port IP Core—instantiates the single-port RAM
- RAM: 2-Port IP Core—instantiates the dual-port and bidirectional-port RAM
- RAM: 4-Port IP Core—instantiates the quad-port RAM
- ROM: 1-Port IP Core—instantiates the single-port ROM
- ROM: 2-Port IP Core—instantiates the dual-port and bidirectional-port ROM
- Stratix 10 Embedded Synchronous Random Access Memory (eSRAM) IP Core—instantiates the eSRAM block

The information for each IP core parameter is described in the parameter editors in the Quartus Prime software.

Related Links

- Introduction to Intel IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- Creating Version-Independent IP and Qsys Simulation Scripts
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- Project Management Best Practices
  Guidelines for efficient management and portability of your project and IP files.

4.1 On-Chip Memory RAM and ROM IP Cores

Table 14.

On-Chip Memory IP Cores	Features
RAM: 1-PORT	• Non-simultaneous read and write operations from a single address. • Read enable port to specify the behavior of the RAM output ports during a write operation, to overwrite or retain existing value.
RAM: 2-PORT	Simple dual-port RAM • Simultaneous one read and one write operations to different locations. • Supports error correction code (ECC). • Emulates single-port RAM using DUAL_PORT configuration for block RAM.

continued...

On-Chip Memory IP Cores	Features
	True dual-port RAM • Simultaneous two reads. • Simultaneous two writes. • Simultaneous one read and one write at two different clock frequencies.
RAM: 4-PORT	• Simultaneous two reads and two writes to different locations.
ROM: 1-PORT	• One port for read-only operations. • Emulates single-port ROM using DUAL_PORT configuration for block RAM.
ROM: 2-PORT	• Two ports for read-only operations. • Emulates dual-port ROM using BIDIR_DUAL_PORT configuration for block RAM.

4.1.1 On-Chip Memory RAM: 1-Port IP Core Parameters

Table 15. RAM: 1-Port IP Core Parameters Description

Parameter	Legal Values	Description
Parameter Settings: Widths/Blk Type/Clks		
How wide should the 'q' output bus be?	—	Specifies the width of the 'q' output bus.
How many words of memory?	—	Specifies the number of bit words.
What should the memory block type be?	Auto, MLAB, M20K, LCs	Specifies the memory block type. The types of memory block that are available for selection depends on your target device.
Set the maximum block depth to	• MLAB: Auto, 32 • M20K: Auto, 512, 1024, 2048 • LCs: Auto	Specifies the maximum block depth in words.
How should the memory be implemented?	• Use default logic cell style • Use Stratix M512 emulation logic cell style	Specifies the logic cell implementation method. • Select default logic cell style if you prefer smaller and faster memory capacity. • Select Stratix M512 emulation logic cell style if you prefer the memory to be compatible to the Stratix M512 emulation style.
What clocking method would you like to use?	• Single clock • Dual clock: use separate 'input' and 'output' clocks	Specifies the clocking method to use. • **Single clock**—A single clock and a clock enable controls all registers of the memory block. • **Dual clock: use separate 'input' and 'output' clocks**—An input and an output clock controls all registers related to the data input and output to/from the memory block including data, address, byte enables, read enables, and write enables.
Parameter Settings: Regs/Clken/Byte Enable/Aclrs		
Which ports should be registered?	On/Off	Specifies whether to register the input and output ports.

continued...

Parameter		Legal Values	Description
The following options are available: • 'data' and 'wren' input ports • 'address' input port • 'q' output port			
Create one clock enable signal for each clock signal. Note: All registered ports are controlled by the enable signal(s)		On/Off	Specifies whether to turn on the option to create one clock enable signal for each clock signal.
More Options	Use clock enable for port A input registers	On/Off	Specifies whether to use clock enable for port A input registers.
	Use clock enable for port A output registers	On/Off	Specifies whether to use clock enable for port A output registers.
	Create an 'addressstall_a' input port.	On/Off	Specifies whether to create an addressstall_a input port. You can create this port to act as an extra active low clock enable input for the address registers.
Create byte enable for port A		On/Off	Specifies whether to create a byte enable for port A. Turn on this option if you want to mask the input data so that only specific bytes, nibbles, or bits of data are written. To enable byte enable for port A and port B, the data width ratio has to be 1 or 2 for the RAM: 1-PORT and RAM: 2-PORT IP cores.
What is the width of a byte for byte enables?		• MLAB: 5 or 10 • Other memory block types: 8 or 9 • M10K and M20K: 8, 9, or 10	Specifies the byte width of the byte enable port. The width of the data input port must be divisible by the byte size.
Create an 'aclr' asynchronous clear for the registered ports. • 'data' port • 'wren' port • 'address' port • 'q' port • 'byteena_a' port		On/Off	Turn on if you want the registered data, wren, address, q, and byteena_a ports to be affected by the asynchronous clear signal. The disabled ports are not affected by the asynchronous clear signal.
Create an 'sclr' synchronous clear for the registered port. 'q' port		On/Off	Turn on if you want the q port to be affected by the synchronous clear signal.
Create a 'rden' read enable signal		On/Off	Turn on if you want to create a read enable signal.
Parameter Settings: Read During Write Option			
What should the q output be when reading from a memory location being written to?		New Data, Old Data, Don't Care	Specifies the output behavior when read-during-write occurs. **New Data**—New data is available on the rising edge of the same clock cycle on which it was written. **Old Data**—The RAM outputs reflect the old data at that address before the write operation proceeds. **Don't Care**—The RAM outputs "don't care" or "unknown" values for read-during-write operation.

continued...

Parameter	Legal Values	Description
Get x's for write masked bytes instead of old data when byte enable is used	On/Off	Turn on this option to obtain 'X' on the masked byte. For M10K and M20K memory block, this option is not available if you specify **New Data** as the output behavior when RDW occurs.
Parameter Settings: Mem Init		
Do you want to specify the initial content of the memory?	• No, leave it blank • Yes, use this file for the memory content data	Specifies the initial content of the memory. To initialize the memory to zero, select **No, leave it blank**. To use a memory initialization file (`.mif`) or a hexadecimal (Intel-format) file (`.hex`), select **Yes, use this file for the memory content data.**
Initialize memory content data to XX.X on power-up in simulation	On/Off	
Implement clock-enable circuitry for use in a partial reconfiguration region	On/Off	Specifies whether to implement clock-enable circuitry for use in a partial reconfiguration region.
Allow In-System Memory Content Editor to capture and update content independently of the system clock	On/Off	Specifies whether to allow In-System Memory Content Editor to capture and update content independently of the system clock.
The 'Instance ID' of this RAM is	None	Specifies the RAM ID.
Parameter Settings: Performance Optimization		
Enable Force-to-Zero feature	On/Off	Specifies whether to set the output to zero when you deassert the read enable signal. Enabling this feature helps improve the glue logic performance when the selected memory depth is larger than a single memory block.

4.1.2 On-Chip Memory RAM: 2-Port IP Core Parameters

This table lists the parameters for the RAM: 2-Port IP Core

Table 16. RAM: 2-Port Parameter Settings

Parameter	Legal Values	Description
Parameter Settings: General		
How will you be using the dual port RAM?	Operation mode • With one read port and one write port • With two read /write ports	Specifies how you use the dual port RAM.
How do you want to specify the memory size?	Type • As a number of words • As a number of bits	Determines whether to specify the memory size in words or bits.
Parameter Settings: Widths/ Blk Type		
How many words of memory?	—	Specifies the number of words.

continued...

Parameter	Legal Values	Description
Use different data widths on different ports	On/Off	Specifies whether to use different data widths on different ports.
When you select **With one read port and one write port**, the following options are available: • How wide should the 'q_a' output bus be? • How wide should the 'data_a' input bus be? • How wide should the 'q_b' output bus be?	—	Specifies the width of the input and output ports.
When you select **With two read/ write ports**, the following options are available: • How wide should the 'q_a' output bus be? • How wide should the 'q_b' output bus be?		
Ram block type	Auto, MLAB, M20K, LCs	Specifies the memory block type. The types of memory block that are available for selection depends on your target device.
Set the maximum block depth to	• MLAB: Auto, 32 • M20K: Auto, 512, 1024, 2048 • LCs: Auto	Specifies the maximum block depth in words. • MLAB: Auto, 32 • M20K: Auto, 512, 1024, 2048 • LCs: Auto
How should the memory be implemented?	• Use default logic cell style • Use Stratix M512 emulation logic cell style	Specifies the logic cell implementation method. • Select default logic cell style if you prefer smaller and faster memory capacity. • Select Stratix M512 emulation logic cell style if you prefer the memory to be compatible to the Stratix M512 emulation style. This option is applicable only when you choose LCs memory type.
Parameter Settings: Clks/Rd, Byte En		
What clocking method would you like to use?	• Single clock • Dual clock: use separate 'input' and 'output' clocks • Dual clock: use separate 'read' and 'write' clocks • No clock (fully asynchronous) • Customize clocks for A and B ports	Specifies the clocking method to use.

continued...

Parameter	Legal Values	Description
		• **Single clock**—A single clock and a clock enable controls all registers of the memory block. • **Dual Clock: use separate 'input' and 'output' clocks**—An input and an output clock controls all registers related to the data input and output to/from the memory block including data, address, byte enables, read enables, and write enables. • **Dual clock: use separate 'read' and 'write' clock**—A write clock controls the data-input, write-address, and write-enable registers while the read clock controls the data-output, read-address, and read-enable registers. • **Dual clock: use separate clocks for A and B ports**—Clock A controls all registers on the port A side; clock B controls all registers on the port B side. Each port also supports independent clock enables for both port A and port B registers, respectively. • **No clock (fully asynchronous)**— • **Customize clocks for A and B ports**—
When you select **With one read port and one write port**, the following option is available: Create a 'rden' read enable signal	—	Specifies whether to create a read enable signal for port B.
When you select **With two read/ write ports**, the following option is available: Create a 'rden_a' and 'rden_b' read enable signals		Specifies whether to create a read enable signal for port A and B.
Create byte enable for port A	—	Specifies whether to create a byte enable for port A and B. Turn on these options if you want to mask the input data so that only specific bytes, nibbles, or bits of data are written. To enable byte enable for port A and port B, the data width ratio has to be 1 or 2 for the RAM: 1-PORT and RAM: 2-PORT IP cores. The option to create a byte enable for port B is only available when you select the **With two read/write ports** option.
Create byte enable for port B	—	
What is the width of a byte for byte enable		
Enable error checking and correcting (ECC) to check and correct single bit errors, double adjacent bit errors, and detect triple adjacent bit errors	On/Off	Specifies whether to enable the ECC feature that corrects single bit errors, double adjacent bit errors, and detects triple adjacent bit errors at the output of the memory.
Enable ECC pipeline registers before the output decoder to achieve that same performance as non-ECC mode at the expense of one cycle of latency	On/Off	Specifies whether to enable the ECC pipeline registers.

continued...

Parameter	Legal Values	Description
Enable ECC encoder bypass feature	On/Off	Specifies whether to enable the ECC encoder bypass feature that allows yu to selectively insert parity bits into the memory through eccencparity port.
Enable coherent read feature	On/Off	Specifies whether to enable the coherent read feature to present with coherent memory read. This feature allows you to read out current memory content, perform operation on top of the content, and write back to the same location in the same cycle.
Parameter Settings: Regs/Clkens/Aclrs		
Which ports should be registered? When you select **With one read port and one write port**, the following options are available: • All write input ports • raddress port • q_b port When you select **With two read/ write ports**, the following options are available: • All write input ports • raddress port • q_a port • q_b port	On/Off	Specifies whether to register the read or write input and output ports.
Clock Enables When you select **With one read port and one write port**, the following option is available: • Use different clock enables for registers • Use clock enable for write input registers • Use clock enable for read input registers • Use clock enable for output registers When you select **With two read / write ports**, the following options are available: • Use different clock enables for registers • Use clock enable for port A input registers • Use clock enable for port A output registers • Use clock enable for port B input registers • Use clock enable for port B output registers	On/Off	Specifies whether to create clock enables for read and write registers.

continued...

Parameter	Legal Values	Description
Addressstalls When you select **With one read port and one write port**, the following options are available: • Create a 'wr_addressstall' input port. • Create a 'rd_addressstall' input port. When you select **With two read / write ports**, the following options are available: • Create an 'addressstall_a' input port. • Create an 'addressstall_b' input port.	On/Off	Specifies whether to create clock enables for address registers. You can create these ports to act as an extra active low clock enable input for the address registers.
Aclr Options When you select **With one read port and one write port**, the following options are available: • rdaddress port • q_b port When you select **With two read / write ports**, the following options are available: • q_a port • q_b port	On/Off	Specifies whether to create an asynchronous clear port for the registered ports. Specifies whether the 'raddress', 'q_a', and 'q_b' ports are cleared by the aclr port.
Sclr Options When you select **With one read port and one write port**, the following options are available: • q_b port When you select **With two read / write ports**, the following options are available: • q_a port • q_b port	On/Off	Specifies whether to create a synchronous clear port for the registered ports. Specifies whether the 'q_a', and 'q_b' ports are cleared by the sclr port.
Parameter Settings: Output 1 (This tab is only available when you select one read port and one write ports)		
continued...		

Parameter	Legal Values	Description
How should the q_a and q_b outputs behave when reading a memory location that is being written from the other port?	• New Data • Old memory contents appear • I do not care (The outputs will be undefined)	Specifies the output behavior when read-during-write occurs. • **New Data**—New data is available on the rising edge of the same clock cycle on which it was written. • **Old memory contents appear**—The RAM outputs reflect the old data at that address before the write operation proceeds. • **I do not care**—This option functions differently when you turn it on depending on the following memory block type you select: — When you set the memory block type to **Auto**, **M144K**, **M512**, **M4K**, **M9K**, **M10K**, **M20K** or any other block RAM, the RAM outputs 'don't care' or "unknown" values for read-during-write operation without analyzing the timing path. — When you set the memory block type to **MLAB** (for LUTRAM), the RAM outputs 'don't care' or 'unknown' values for read-during-write operation but analyzes the timing path to prevent metastability.
Do not analyze the timing between write and read operation. Metastability issues are prevented by never writing and reading at the same address at the same time.	On/Off	Turn on this option when you want the RAM to output 'don't care' or unknown values for read-during-write operation without analyzing the timing path. This option is only available for LUTRAM and is enabled when you set memory block type to **MLAB.**
Parameter Settings: Output 2 (This tab is only available when you select two read/ write ports)		
What should the 'q_a' output be when reading from a memory location being written to?	• New data • Old Data	Specifies the output behavior when read-during-write occurs. • **New Data**—New data is available on the rising edge of the same clock cycle on which it was written. • **Old Data**—The RAM outputs reflect the old data at that address before the write operation proceeds.
What should the 'q_b' output be when reading from a memory location being written to?		
Get x's for write masked bytes instead of old data when byte enable is used	On/Off	Turn on this option to obtain 'X' on the masked byte.
Parameter Settings: Mem Init		
Do you want to specify the initial content of the memory?	• No, leave it blank • Yes, use this file for the memory content data	Specifies the initial content of the memory. To initialize the memory to zero, select **No, leave it blank.** To use a memory initialization file (**.mif**) or a hexadecimal (Intel-format) file (**.hex**), select **Yes, use this file for the memory content data**.
Initialize memory content data to XX.X on power-up in simulation	On/Off	

continued...

Parameter	Legal Values	Description
The initial content file should conform to which port's dimensions?	PORT_A, PORT_B	If you select to use the initial content file for memory content data, select the port the file should conform to.
Implement clock-enable circuitry for use in a partial reconfiguration region	On/Off	Specifies whether to implement clock-enable circuitry for use in a partial reconfiguration region.
Parameter Settings: Performance Optimization		
Enable Force-to-Zero feature	On/Off	Specifies whether to set the output to zero when you deassert the read enable signal. Enabling this feature helps improve the glue logic performance when the selected memory depth is larger than a single memory block.

4.1.3 On-Chip Memory RAM: 4-Port IP Core Parameters

This table lists the parameters for the RAM: 4-Port IP Core

Table 17. RAM: 4-Port Parameter Settings

Parameter	Legal Values	Description
Parameter Settings: Widths/ Blk Type		
How many words of memory?	—	Specifies the number of bit words.
How wide should the 'q_a' and 'q_b' output bus be?	—	Specifies the width of the input and output ports.
RAM block type	Auto, M20K	Specifies the memory block type. The types of memory block that are available for selection depends on your target device.
Set the maximum block depth to	M20K: Auto, 512, 1024, 2048	Specifies the maximum block depth in words.
Parameter Settings: Clks/Rd, Byte En		
What clocking method would you like to use?	Single clock	Specifies the clocking method to use. **Single clock**—A single clock and a clock enable controls all registers of the memory block.
Create 'rden_a' and 'rden_b' read enable signals	—	Specifies whether to create a read enable signal for ports A and B.
What is the width of a byte for byte enables?	M20K: 8, 9, 10	Specifies the byte width of the byte enable port. The width of the data input port must be divisible by the byte size.
Parameter Settings: Regs/Clkens/Aclrs		

continued...

Parameter	Legal Values	Description
Which ports should be registered? Input registers: • All write input ports • 'raddress' port Output registers: • 'q_a' port • 'q_b' port	On/Off	Specifies whether to register the read or write input and output ports.
Use clock enable for input and output registers.	On/Off	Specifies whether to turn on the option to create one clock enable signal for the input and output registers.
Create an 'aclr' asynchronous clear for the output ports. • 'q_a' port • 'q_b' port	On/Off	Specifies whether to create an asynchronous clear port for the output ports.
Create an 'sclr' synchronous clear for the output ports. • 'q_a' port • 'q_b' port	On/Off	Specifies whether to create a synchronous clear port for the output ports.
Parameter Settings: Output 1		
How should the 'q_a' and 'q_b' outputs behave when reading a memory location that is being written from the other port? The output of port A will be 'NEW' while the output of port B will be 'OLD'	On/Off	Specifies the output behavior when read-during-write occurs.
Parameter Settings: Output 2		
What should the 'q_a' output be when reading from a memory location being written to?	Don't Care	Specifies the output behavior when read-during-write occurs.
What should the 'q_b' output be when reading from a memory location being written to?		
Parameter Settings: Mem Init		
Do you want to specify the initial content of the memory?	• No, leave it blank • Yes, use this file for the memory content data	Specifies the initial content of the memory. To initialize the memory to zero, select **No, leave it blank.** To use a memory initialization file (**.mif**) or a hexadecimal (Intel-format) file (**.hex**), select **Yes, use this file for the memory content data**.
Initialize memory content data to XX.X on power-up simulation	On/Off	
The initial content file should conform to which port's dimensions?	PORT_A, PORT_B	If you select to use the initial content file for memory content data, select the port the file should conform to.

continued...

Parameter	Legal Values	Description
Implement clock-enable circuitry for use in a partial reconfiguration region	On/Off	Specifies whether to implement clock-enable circuitry for use in a partial reconfiguration region.
Parameter Settings: Performance Optimization		
Enable Force-to-Zero feature	On/Off	Specifies whether to set the output to zero when you deassert the read enable signal. Enabling this feature helps improve the glue logic performance when the selected memory depth is larger than a single memory block.

4.1.4 On-Chip Memory ROM: 1-PORT IP Core Parameters

This table lists the parameters for the ROM: 1-PORT IP Core.

Table 18. ROM: 1-PORT IP Core Parameters

Parameter	Legal Values	Description
Parameter Settings: General Page		
How wide should the 'q' output bus be?	—	Specifies the width of the 'q' output bus.
How many words of memory?	—	Specifies the number of words.
What should the memory block type be?	Auto, MLAB, M20K	Specifies the memory block type. The types of memory block that are available for selection depends on your target device.
Set the maximum block depth to	• MLAB: Auto, 32 • M20K: Auto, 512, 1024, 2048	Specifies the maximum block depth in words.
What clocking method would you like to use?	• Single clock • Dual clock: use separate 'input' and 'output' clocks	Specifies the clocking method to use. • **Single clock**—A single clock and a clock enable controls all registers of the memory block • **Dual clock (Input and Output clock)**—The input clock controls the address registers and the output clock controls the data-out registers. There are no write-enable, byte-enable, or data-in registers in ROM mode.
Parameter Settings: Regs/Clken/Aclrs		
Which ports should be registered?	On/Off	Specifies whether to register the input and output ports.

continued...

Parameter	Legal Values	Description
The following options are available: • 'address' input port • 'q' output port		
Use clock enable for port A input registers	On/Off	Specifies whether to use clock enable for port A input registers.
Use clock enable for port A output registers	On/Off	Specifies whether to use clock enable for port A output registers.
Create an 'addressstall_a' input port.	On/Off	Specifies whether to create an addressstall_a input port. You can create this port to act as an extra active low clock enable input for the address registers.
Create an 'aclr' asynchronous clear for the registered ports. The following options are available: • 'address' port • 'q' port	On/Off	Specifies whether the registered ports be affected by an asynchronous clear port.
Create a 'sclr' asynchronous clear for the registered ports. 'q' port	On/Off	Specifies whether the q port be affected by a synchronous clear port.
Create an 'rden' read enable signal	On/Off	Specifies whether to create a read enable signal.
Parameter Settings: Mem Init		
Do you want to specify the initial content of the memory?	• No, leave it blank • Yes, use this file for the memory content data	Specifies the initial content of the memory. In ROM mode, you must specify a memory initialization file (**.mif**) or a hexadecimal (Intel-format) file (**.hex**). The **Yes, use this file for the memory content data** option is turned on by default.
The initial content file should conform to which port's dimensions?	PORT_A	The initial content file for memory content data only conforms to port A.
Allow In-System Memory Content Editor to capture and update content independently of the system clock	On/Off	Specifies whether to allow In-System Memory Content Editor to capture and update content independently of the system clock
The 'Instance ID' of this ROM is	NONE	Specifies the ROM ID.
Parameter Settings: Performance Optimization		
Enable Force-to-Zero feature	On/Off	Specifies whether to set the output to zero when you deassert the read enable signal. Enabling this feature helps improve the glue logic performance when the selected memory depth is larger than a single memory block.

4.1.5 On-Chip Memory ROM: 2-PORT IP Core Parameters

This table lists the ROM: 2-PORT IP Core parameters.

Table 19. ROM: 2-PORT IP Core Parameters

Parameter	Legal Values	Description
Parameter Settings: Widths/Blk Type		
How do you want to specify the memory size?	• As a number of words • As a number of bits	Determines whether to specify the memory size in words or bits.
How many words of memory?	32, 64, 128, 256, 512, 1024, 2048, 4096, 8192, 16384, 32768, 65536	Specifies the number of words.
Use different data widths on different ports	On/Off	Specifies whether to use different data widths on different ports.
How wide should the 'q_a' output bus be?	—	Specifies the width of the 'q_a' and 'q_b' output ports.
How wide should the 'q_b' output bus be?		
RAM block type	Auto, M20K	Specifies the memory block type. The types of memory block that are available for selection depends on your target device
Set the maximum block depth to	M20K: Auto, 512, 1024, 2048	Specifies the maximum block depth in words. This option is enabled only when you choose **Auto** as the memory block type.
Parameter Settings: Clks/Rd, Byte En		
What clocking method would you like to use?	• Single clock • Dual clock: use separate 'input' and 'output' clocks • Customize clocks for A and B ports	Specifies the clocking method to use. • **Single clock**—A single clock and a clock enable controls all registers of the memory block • **Dual clock: use separate 'input' and 'output' clocks**—The input clock controls the address registers and the output clock controls the data-out registers. There are no write-enable, byte-enable, or data-in registers in ROM mode. • **Customize clocks for A and B ports**—Clock A controls all registers on the port A side; clock B controls all registers on the port B side. Each port also supports independent clock enables for both port A and port B registers, respectively.

continued...

Parameter	Legal Values	Description
Create a 'rden_a' and 'rden_b' read enable signals	On/Off	Specifies whether to create read enable signals.
Parameter Settings: Regs/Clkens/Aclrs		
Which ports should be registered? Read output port(s)	On/Off	Specifies whether to register the read output ports.
'q_a' port	On/Off	Specifies whether to register the 'q_a' output port.
'q_b' port	On/Off	Specifies whether to register the 'q_b' output port.
Use clock enable for port A input registers	On/Off	Specifies whether to use clock enable for port A input registers.
Use clock enable for port A output registers	On/Off	Specifies whether to use clock enable for port A output registers.
Use clock enable for port B input registers	On/Off	Specifies whether to use clock enable for port B input registers.
Use clock enable for port B output registers	On/Off	Specifies whether to use clock enable for port B output registers.
Create an 'addressstall_a' input port.	On/Off	Specifies whether to create addressstall_a and addressstall_b input ports. You can create these ports to act as an extra active low clock enable input for the address registers.
Create an 'addressstall_b' input port.	On/Off	Specifies whether to create an asynchronous clear port for the registered ports.
Aclr Options • 'q_a' port • 'q_b' port	On/Off	Specifies whether the registered ports should be cleared by the asynchronous clear port.
Sclr Options • 'q_a' port • 'q_b' port	On/Off	Specifies whether the registered ports should be cleared by the synchronous clear port.
Parameter Settings: Mem Init		
Do you want to specify the initial content of the memory?	• No, leave it blank • Yes, use this file for the memory content data	Specifies the initial content of the memory. In ROM mode, you must specify a memory initialization file (**.mif**) or a hexadecimal (Intel-format) file (**.hex**). The **Yes, use this file for the memory content data** option is turned on by default.

continued...

Parameter	Legal Values	Description
The initial content file should conform to which port's dimensions?	• PORT_A • PORT_B	Specifies whether the initial content file conforms to port A or port B.
Parameter Settings: Performance Optimization		
Enable Force-to-Zero feature	On/Off	Specifies whether to set the output to zero when you deassert the read enable signal. Enabling this feature helps improve the glue logic performance when the selected memory depth is larger than a single memory block.

4.1.6 On-Chip Memory RAM and ROM Interface Signals

Table 20. Interface Signals of the Stratix 10 On-Chip Memory RAM and ROM IP Cores

Signal	Direction	Required	Description
data_a	Input	Optional	Data input to port A of the memory. The data_a port is required for all RAM operation modes: • SINGLE_PORT • DUAL_PORT • BIDIR_DUAL_PORT • QUAD_PORT
address_a	Input	Yes	Address input to port A of the memory. The address_a signal is required for all operation modes.
wren_a	Input	Optional	Write enable input for address_a port. The wren_a signal is required all RAM operation modes: • SINGLE_PORT • DUAL_PORT • BIDIR_DUAL_PORT • QUAD_PORT
rden_a	Input	Optional	Read enable input for address_a port. The rden_a signal is supported depending on your selected memory mode and memory block.
byteena_a	Input	Optional	Byte enable input to mask the data_a port so that only specific bytes, nibbles, or bits of the data are written. The byteena_a port is not supported in the following conditions: • If implement_in_les parameter is set to ON • If operation_mode parameter is set to ROM
addressstall_a	Input	Optional	Address clock enable input to hold the previous address of address_a port for as long as the addressstall_a port is high.
q_a	Output	Yes	Data output from port A of the memory.

continued...

Signal	Direction	Required	Description
			The q_a port is required if the operation_mode parameter is set to any of the following values: • SINGLE_PORT • BIDIR_DUAL_PORT • QUAD_PORT • ROM The width of q_a port must be equal to the width of data_a port.
data_b	Input	Optional	Data input to port B of the memory. The data_b port is required if the operation_mode parameter is set to BIDIR_DUAL_PORT.
address_b	Input	Optional	Address input to port B of the memory. The address_b port is required if the operation_mode parameter is set to the following values: • DUAL_PORT • BIDIR_DUAL_PORT • QUAD_PORT
wren_b	Input	Yes	Write enable input for address_b port. The wren_b port is required if operation_mode is set to BIDIR_DUAL_PORT.
rden_b	Input	Optional	Read enable input for address_b port. The rden_b port is supported depending on your selected memory mode and memory block
byteena_b	Input	Optional	Byte enable input to mask the data_b port so that only specific bytes, nibbles, or bits of the data are written. The byteena_b port is not supported in the following conditions: • If implement_in_les parameter is set to ON • If operation_mode parameter is set to SINGLE_PORT, DUAL_PORT, or ROM
addressstall_b	Input	Optional	Address clock enable input to hold the previous address of address_b port for as long as the addressstall_b port is high.
q_b	Output	Yes	Data output from port B of the memory. The q_b port is required if the operation_mode is set to the following values: • DUAL_PORT • BIDIR_DUAL_PORT • QUAD_PORT The width of q_b port must be equal to the width of data_b port.
clock0	Input	Yes	The following describes which of your memory clock must be connected to the clock0 port, and port synchronization in different clocking modes:

continued...

Signal	Direction	Required	Description
			• Single clock: Connect your single source clock to `clock0` port. All registered ports are synchronized by the same source clock. • Read/Write: Connect your write clock to `clock0` port. All registered ports related to write operation, such as `data_a` port, `address_a` port, `wren_a` port, and `byteena_a` port are synchronized by the write clock. • Input Output: Connect your input clock to `clock0` port. All registered input ports are synchronized by the input clock. • Independent clock: Connect your port A clock to `clock0` port. All registered input and output ports of port A are synchronized by the port A clock.
`clock1`	Input	Optional	The following describes which of your memory clock must be connected to the `clock1` port, and port synchronization in different clocking modes: • Single clock: Not applicable. All registered ports are synchronized by `clock0` port. • Read/Write: Connect your read clock to `clock1` port. All registered ports related to read operation, such as `address_b` port, `rden_b` port, and `q_b` port are synchronized by the read clock. • Input Output: Connect your output clock to `clock1` port. All the registered output ports are synchronized by the output clock. • Independent clock: Connect your port B clock to `clock1` port. All registered input and output ports of port B are synchronized by the port B clock.
`clocken0`	Input	Optional	Clock enable input for `clock0` port.
`clocken1`	Input	Optional	Clock enable input for `clock1` port.
`clocken2`	Input	Optional	Clock enable input for `clock0` port.
`clocken3`	Input	Optional	Clock enable input for `clock1` port.
`aclr0` `aclr1`	Input	Optional	Asynchronously clear the registered input and output ports. The `aclr0` port affects the registered ports that are clocked by `clock0` clock, while the `aclr1` port affects the registered ports that are clocked by `clock1` clock. The asynchronous clear effect on the registered ports can be controlled through their corresponding asynchronous clear parameter, such as `outdata_aclr_a`,`address_aclr_a`, and so on.
`eccstatus`	Output	Optional	A 3-bit wide error correction status port. Indicate whether the data that is read from the memory has an error in single-bit with correction, fatal error with no correction, or no error bit occurs. In Stratix V devices, the M20K ECC status is communicated with two-bit wide error correction status port. The M20K ECC detects and fixes a single bit error event or a double adjacent error event, or detects three adjacent errors without fixing the errors. The `eccstatus` port is supported if all the following conditions are met: • `operation_mode` parameter is set to `DUAL_PORT` • `ram_block_type` parameter is set to `M144K` or `M20K` • `width_a` and `width_b` parameter have the same value • Byte enable is not used

continued...

Signal	Direction	Required	Description
eccencbypass		Optional	When active, this port allow user to inject parity bits through eccencparity ports. When inactive, parity bits will be generated using internal ecc encoder. This port can only be used when enable_ecc_encoder_bypass is set to "TRUE".
eccencparity		Optional	When eccencbypass is active, user can inject 8-bits parity through eccencparity port. This port can be used only when enable_ecc_encoder_bypass is set to "TRUE".
data	Input	Yes	Data input to the memory. The data port is required and the width must be equal to the width of the q port.
wraddress	Input	Yes	Write address input to the memory. The wraddress port is required and must be equal to the width of the raddress port.
wren	Input	Yes	Write enable input for wraddress port. The wren port is required.
rdaddress	Input	Yes	Read address input to the memory. The rdaddress port is required and must be equal to the width of wraddress port.
rden	Input	Optional	Read enable input for rdaddress port. The rden port is supported when the use_eab parameter is set to OFF. The rden port is not supported when the ram_block_type parameter is set to MLAB. Instantiate the ALTSYNCRAM IP core if you want to use read enable feature with other memory blocks.
byteena	Input	Optional	Byte enable input to mask the data port so that only specific bytes, nibbles, or bits of data are written. It is supported in Stratix 10 devices when you set the ram_block_type parameter to MLAB.
wraddressstall	Input	Optional	Write address clock enable input to hold the previous write address of wraddress port for as long as the wraddressstall port is high.
rdaddressstall	Input	Optional	Read address clock enable input to hold the previous read address of rdaddress port for as long as the wraddressstall port is high.
q	Output	Yes	Data output from the memory. The q port is required, and must be equal to the width data port.
inclock	Input	Yes	The following describes which of your memory clock must be connected to the inclock port, and port synchronization in different clocking modes: • Single clock: Connect your single source clock to inclock port and outclock port. All registered ports are synchronized by the same source clock. • Read/Write: Connect your write clock to inclock port. All registered ports related to write operation, such as data port, wraddress port, wren port, and byteena port are synchronized by the write clock. • Input/Output: Connect your input clock to inclock port. All registered input ports are synchronized by the input clock.
outclock	Input	Yes	The following describes which of your memory clock must be connected to the outclock port, and port synchronization in different clocking modes:

continued...

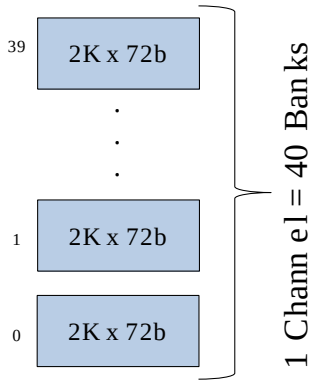
Signal	Direction	Required	Description
			• Single clock: Connect your single source clock to `inclock` port and `outclock` port. All registered ports are synchronized by the same source clock. • Read/Write: Connect your read clock to `outclock` port. All registered ports related to read operation, such as `rdaddress` port, `rdren` port, and `q` port are synchronized by the read clock. • Input/Output: Connect your output clock to `outclock` port. The registered `q` port is synchronized by the output clock.
`inclocken`	Input	Optional	Clock enable input for `inclock` port.
`outclocken`	Input	Optional	Clock enable input for `outclock` port.
`aclr`	Input	Optional	Asynchronously clear the registered input and output ports. The asynchronous clear effect on the registered ports can be controlled through their corresponding asynchronous clear parameter, such as `indata_aclr`, `wraddress_aclr`, and so on.

4.2 Stratix 10 eSRAM IP Core

The basic building block of the eSRAM IP core is a bank, which consists of an array of 2K x 72-bit SRAM blocks.

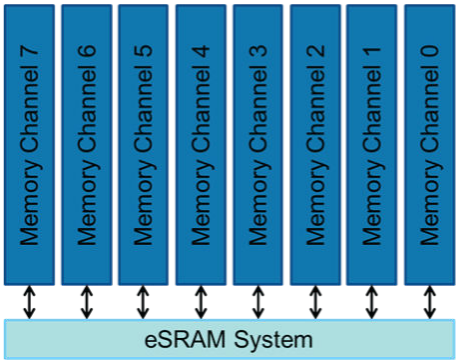
Forty eSRAM banks combine to form a channel.

Figure 17. eSRAM Channel



Eight memory channels combine to form an eSRAM system.

Figure 18. eSRAM System



A Revision History for Stratix 10 Embedded Memory User Guide

Date	Version	Changes
May 2017	2017.05.08	• Removed parity bit support for MLAB blocks under the Error Correction Code (ECC) support feature in the Stratix 10 Embedded Memory Features table. • Updated the descriptions for M20K and MLAB blocks under Error Correction code (ECC) support feature in the Stratix 10 Embedded Memory Features table. • Updated the Embedded Memory Capacity and Distribution in Stratix 10 Devices table to remove TX4500 and TX5500, which are no longer part of Stratix 10 TX variant. • Updated the Byte Enable Controls in ×10 Data Width (MLAB) table. • Removed parity bit support for MLAB blocks in the Parity Bit topic. • Added notes to the Supported Embedded Memory Block Configurations table in the Stratix 10 Embedded Memory Configurations topic. • Added Mixed-Width Ratio Configurations topic. • Added Freeze Logic topic. • Added the Implement clock-enable circuitry for use in a partial reconfiguration region option for the RAM: 1-PORT, RAM: 2-PORT, and RAM: 4-PORT IP cores. • Removed the Use different data widths on different ports option from RAM: 4-Port Parameter Settings table because this option is not available in RAM: 4-Port. • Added Hardware Behavior topic. • Added figures for the Coherent Read topic. • Updated the feature description for ROM: 1-PORT and ROM: 2-PORT in the table of the On-Chip Memory RAM and ROM IP Cores topic. • Added `ecc_enc_bypass` and `ecc_enc_parity` signals in the Interface Signals of the Stratix 10 On-Chip Memory RAM and ROM IP Cores table. • Added Stratix 10 eSRAM IP core topic. • Minor typographical corrections.
October 2016	2016.10.31	Initial release.