Intel® Stratix® 10 General Purpose I/O User Guide

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1 Intel® Stratix® 10 I/O Overview

The Intel® Stratix® 10 general purpose I/O (GPIO) system consists of the I/O elements (IOE) and the Intel FPGA GPIO IP core.

- The IOEs contain bidirectional I/O buffers and I/O registers located in LVDS I/O banks.
- The Intel FPGA GPIO IP core supports the GPIO components and features, including double data rate I/O (DDIO), delay chains, I/O buffers, control signals, and clocking.
- Two of the LVDS I/O banks are shared with the Secure Device Manager (SDM).
- For devices with Hard Processor System (HPS), three of the LVDS I/O banks are shared with the HPS SDRAM interface.
- The 3 V I/O banks do not feature I/O registers and DDIOs.

Related Links

- Secure Device Manager, Intel Stratix 10 Configuration User Guide
  Provides more information about the Secure Device Manager.
- Restrictions on I/O Bank Usage for Intel Stratix 10 EMIF with HPS, Intel Stratix 10 External Memory Interfaces User Guide
  Provides more information about the shared LVDS I/O banks that are used by the HPS SDRAM interface.
- Modular I/O Banks in Intel Stratix 10 Devices on page 8
- HyperFlex Core Architecture, Intel Stratix 10 Device Overview
  Provides more information about Hyper-Registers and the HyperFlex core architecture. Hyper-Registers are additional registers available in every interconnect routing segment throughout the core fabric, including the routing segments connected to the I/O buffer inputs and outputs.

1.1 Intel Stratix 10 I/O and Differential I/O Buffers

The general purpose I/Os (GPIOs) consist of LVDS I/O and 3 V I/O banks:

- LVDS I/O bank—supports differential and single-ended I/O standards up to 1.8 V. The LVDS I/O pins form pairs of true differential LVDS channels. Each pair supports a parallel input/output termination between the two pins. You can use each LVDS channel as transmitter only or receiver only. Each LVDS channel supports transmit SERDES and receive SERDES with DPA circuitry. For example, if you use 30 channels of the available 72 channels as transmitters, you can use the balance 42 channels as receivers.
- 3 V I/O bank—supports only single-ended I/O standards up to 3 V. Each adjacent I/O pair also supports Differential SSTL and Differential HSTL I/O standards. In Intel Stratix 10 devices, each 3 V I/O bank supports only two output enables (OE) for its eight single-ended I/Os. The single-ended output of the 3 V I/O supports all programmable I/O element (IOE) features except:
  - Programmable pre-emphasis
  - R_D on-chip termination (OCT)
  - Calibrated R_S and R_T OCT
  - Internal V_{REF} generation
  - Dynamic OCT

Note: The 3 V I/O banks in Intel Stratix 10 devices do not support the DDIO feature of the Intel FPGA GPIO IP core. Bypass the DDIO if you use an I/O standard supported only by 3 V I/O banks, such as 3.0 V LVCMOS. To bypass the DDIO feature, set the **Register mode** of the Intel FPGA GPIO IP core to **none**.

Note: The Intel Stratix 10 devices with E-Tile transceiver variant does not feature 3 V I/O banks.

Related Links

Programmable IOE Features in Intel Stratix 10 Devices on page 23

1.2 GPIO Buffers and LVDS Channels in Intel Stratix 10 Devices

1.2.1 FPGA I/O Resources in Intel Stratix 10 GX Packages

Table 1. GPIO Buffers and LVDS Channels in Intel Stratix 10 GX Devices—Preliminary

The LVDS channels counts include dedicated clock pins.

Product Line	Package		GPIO			LVDS Channels
	Code	Type	3 V I/O	LVDS I/O	Total	
GX 400	HF35	1,152-pin FBGA	8	384	392	192
GX 650	HF35	1,152-pin FBGA	8	384	392	192
	NF43	1,760-pin FBGA	16	384	400	192
GX 850	NF43	1,760-pin FBGA	16	672	688	336
	NF48	2,112-pin FBGA	16	720	736	360

continued...

Product Line	Package		GPIO			LVDS Channels
	Code	Type	3 V I/O	LVDS I/O	Total	
GX 1100	NF43	1,760-pin FBGA	16	672	688	336
	NF48	2,112-pin FBGA	16	720	736	360
GX 1650	NF43	1,760-pin FBGA	16	672	688	336
	UF50	2,397-pin FBGA	32	672	704	336
GX 2100	NF43	1,760-pin FBGA	16	672	688	336
	UF50	2,397-pin FBGA	32	672	704	336
GX 2500	NF43	1,760-pin FBGA	16	672	688	336
	UF50	2,397-pin FBGA	32	672	704	336
	HF55	2,912-pin FBGA	8	1152	1160	576
GX 2800	NF43	1,760-pin FBGA	16	672	688	336
	UF50	2,397-pin FBGA	32	672	704	336
	HF55	2,912-pin FBGA	8	1152	1160	576
GX 4500	HF55	2,912-pin FBGA	8	1632	1640	816
GX 5500	HF55	2,912-pin FBGA	8	1632	1640	816

Related Links

Modular I/O Banks in Intel Stratix 10 Devices on page 8

1.2.2 FPGA I/O Resources in Intel Stratix 10 TX Packages

Table 2. GPIO Buffers and LVDS Channels in Intel Stratix 10 TX Devices—Preliminary

The LVDS channels counts include dedicated clock pins.

Product Line	Package		GPIO			LVDS Channels
	Code	Type	3 V I/O	LVDS I/O	Total	
TX 1650	SF48	2,112-pin FBGA	16	528	544	264
	UF50	2,397-pin FBGA	8	432	440	216
TX 2100	SF48	2,112-pin FBGA	16	528	544	264
	UF50	2,397-pin FBGA	8	432	440	216
TX 2500	SF48	2,112-pin FBGA	16	528	544	264
	UF50	2,397-pin FBGA	8	432	440	216
	YF55	2,912-pin FBGA	8	288	296	144
TX 2800	SF48	2,112-pin FBGA	16	528	544	264
	UF50	2,397-pin FBGA	8	432	440	216
	YF55	2,912-pin FBGA	8	288	296	144

Related Links

Modular I/O Banks in Intel Stratix 10 Devices on page 8

1.2.3 FPGA I/O Resources in Intel Stratix 10 MX Packages

Table 3. GPIO Buffers and LVDS Channels in Intel Stratix 10 MX Devices—Preliminary

The LVDS channels counts include dedicated clock pins.

Product Line	Package		GPIO			LVDS Channels
	Code	Type	3 V I/O	LVDS I/O	Total	
MX 1100	NF43	1,760-pin FBGA	16	432	448	216
MX 1650	UF53	2,597-pin FBGA	32	624	656	312
	UF55	2,912-pin FBGA	8	576	584	288
MX 2100	UF53	2,597-pin FBGA	32	624	656	312
	NF53	2,597-pin FBGA	16	624	640	312
	UF55	2,912-pin FBGA	8	576	584	288

Related Links

Modular I/O Banks in Intel Stratix 10 Devices on page 8

1.2.4 FPGA I/O Resources in Intel Stratix 10 SX Packages

Table 4. GPIO Buffers and LVDS Channels in Intel Stratix 10 SX Devices—Preliminary

The LVDS channels counts include dedicated clock pins.

Product Line	Package		GPIO			LVDS Channels
	Code	Type	3 V I/O	LVDS I/O	Total	
SX 400	HF35	1,152-pin FBGA	8	384	392	192
SX 650	HF35	1,152-pin FBGA	8	384	392	192
	NF43	1,760-pin FBGA	16	384	400	192
SX 850	NF43	1,760-pin FBGA	16	672	688	336
	NF48	2,112-pin FBGA	16	720	736	360
SX 1100	NF43	1,760-pin FBGA	16	672	688	336
	NF48	2,112-pin FBGA	16	720	736	360
SX 1650	NF43	1,760-pin FBGA	16	672	688	336
	UF50	2,397-pin FBGA	32	672	704	336
SX 2100	NF43	1,760-pin FBGA	16	672	688	336
	UF50	2,397-pin FBGA	32	672	704	336
SX 2500	NF43	1,760-pin FBGA	16	672	688	336
	UF50	2,397-pin FBGA	32	672	704	336
	HF55	2,912-pin FBGA	8	1152	1160	576
SX 2800	NF43	1,760-pin FBGA	16	672	688	336
	UF50	2,397-pin FBGA	32	672	704	336

continued...

Product Line	Package		GPIO			LVDS Channels
	Code	Type	3 V I/O	LVDS I/O	Total	
	HF55	2,912-pin FBGA	8	1152	1160	576
SX 4500	HF55	2,912-pin FBGA	8	1632	1640	816
SX 5500	HF55	2,912-pin FBGA	8	1632	1640	816

Related Links

Modular I/O Banks in Intel Stratix 10 Devices on page 8

1.3 Modular I/O Banks in Intel Stratix 10 Devices

The I/O pins in Intel Stratix 10 devices are arranged in groups called modular I/O banks:

- The I/O banks are located in I/O columns.
- Each I/O bank contains its own I/O PLL, DPA block, SERDES, hard memory controller, and I/O sequencer circuitries.
- The I/O banks have independent supplies that allow each bank to support different I/O standards.
- Each modular I/O bank can support multiple I/O standards that use the same voltage.

1.3.1 I/O Banks Locations in Intel Stratix 10 Devices

These figures show the locations of the I/O banks in different Intel Stratix 10 devices. For the availability of each I/O bank in different packages, refer to the related information.

Figure 1. I/O Banks Locations for Intel Stratix 10 Devices with Two LVDS I/O Columns—Preliminary

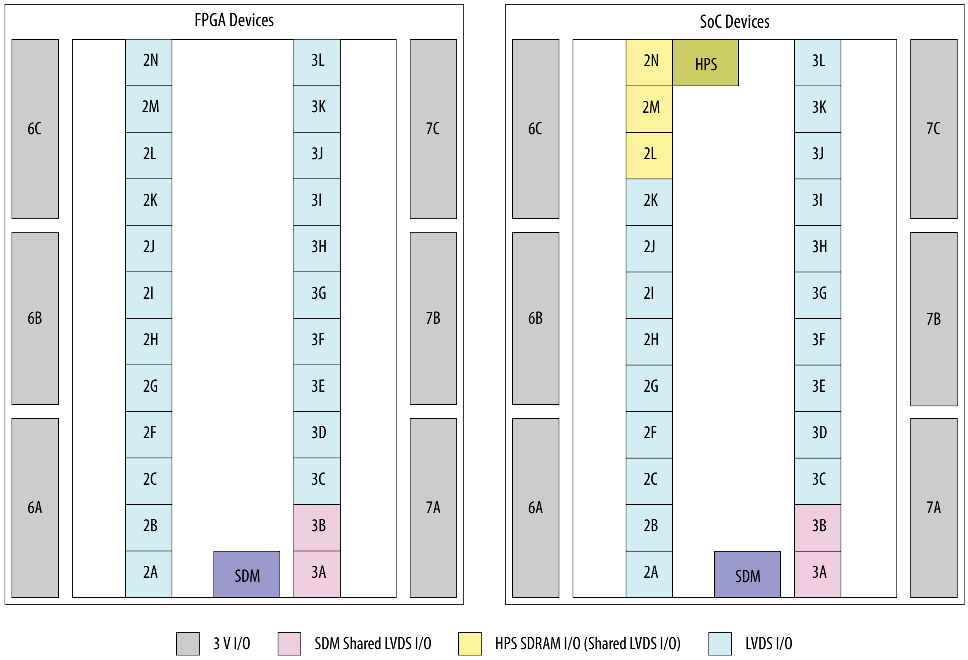


Figure 2. I/O Banks Locations for Intel Stratix 10 Devices with Three LVDS I/O Columns—Preliminary

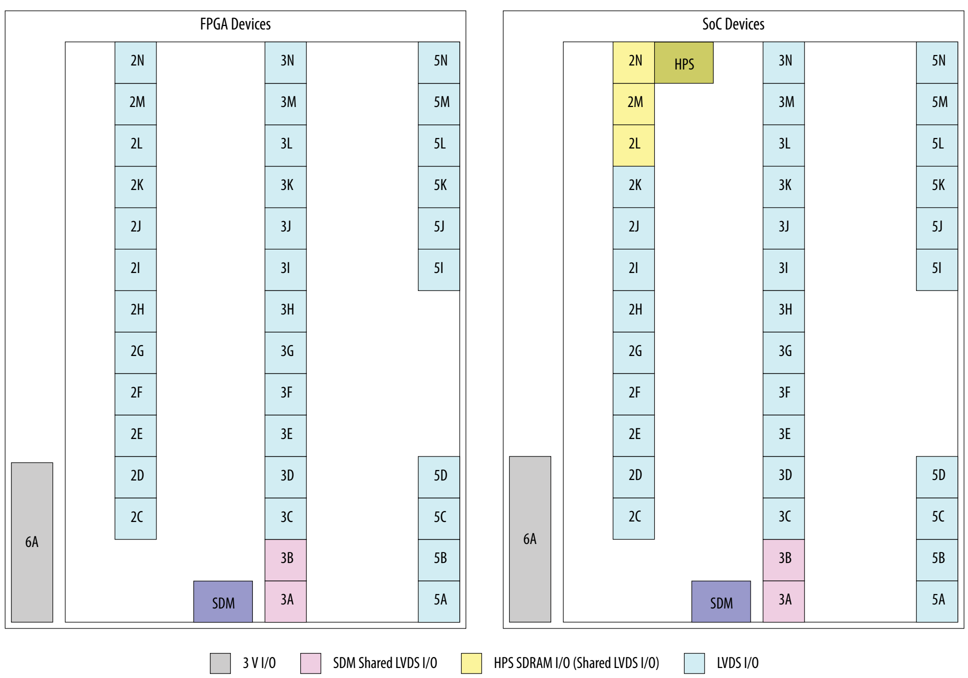


Table 5. Number of LVDS I/O Columns in Intel Stratix 10 Devices

LVDS I/O Columns Count	Intel Stratix 10 Device
Two	• GX 850 and SX 850 • GX 1100, MX 1100, and SX 1100 • GX 1650, TX 1650, MX 1650, and SX 1650 • GX 2100, TX 2100, MX 2100, and SX 2100 • GX 2500, TX 2500, and SX 2500 • GX 2800, TX 2800, SX 2800
Three	• GX 4500 and SX 4500 • GX 5500 and SX 5500

Related Links

- Secure Device Manager, Intel Stratix 10 Configuration User Guide
  Provides more information about the Secure Device Manager.
- Restrictions on I/O Bank Usage for Intel Stratix 10 EMIF with HPS, Intel Stratix 10 External Memory Interfaces User Guide
  Provides more information about the shared LVDS I/O banks that are used by the HPS SDRAM interface.
- Hard Processor System I/O Pin Multiplexing, Intel Stratix 10 Hard Processor System Technical Reference Manual
  Provides more information about the dedicated I/O pins in the HPS.
- SDM Pin Mapping, Intel Stratix 10 Configuration User Guide
  Provides more information about pins in the SDM-shared LVDS I/O banks that are used by the SDM.
- Secure Device Manager (SDM) Pins, Intel Stratix 10 GX, MX, and SX Device Family Pin Connection Guidelines
  Provides the descriptions and connection guidelines for the SDM pins.
- I/O Banks Availability and Pin Counts in Intel Stratix 10 Device Packages on page 10
  Lists the I/O banks and I/O pins available in different packages and product lines of the Intel Stratix 10 device family.

1.3.2 I/O Banks Availability and Pin Counts in Intel Stratix 10 Device Packages

These tables list the number of I/O pins in the FPGA I/O banks, including the shared LVDS I/O pins. For information about the SDM pin mapping and the dedicated I/O pins in the HPS, refer to the related information.

Table 6. I/O Pin Counts for HF35, NF43, NF48, and SF48 Packages—Preliminary

Bank		Device Package					
		HF35	NF43			NF48	SF48
Type	Name	GX 400 SX 400 GX 650 SX 650	GX 650 SX 650	GX 850 SX 850 GX 1100 SX 1100 GX 1650 SX 1650 GX 2100 SX 2100 GX 2500 SX 2500 GX 2800 SX 2800	MX 1100	GX 850 SX 850 GX 1100 SX 1100	TX 1650 TX 2100 TX 2500 TX 2800
3 V I/O	7C	—	—	—	TBD	—	—
	7B	—	—	—	TBD	—	—
	7A	—	8	—	TBD	—	—
	6C	—	—	8	TBD	8	8
	6B	—	—	—	TBD	—	—
	6A	8	8	8	TBD	8	8
LVDS I/O	3L	—	—	48	TBD	48	48
	3K	—	—	48	TBD	48	48
	3J	—	—	48	TBD	48	—
	3I	—	—	48	TBD	—	—
	3H	—	—	—	TBD	—	—
	3G	—	—	—	TBD	—	—
	3F	—	—	—	TBD	—	—
	3E	—	—	—	TBD	—	—
	3D	48	48	48	TBD	48	48
	3C	48	48	48	TBD	48	48
SDM Shared LVDS I/O	3B	48	48	48	TBD	48	48
	3A	48	48	48	TBD	48	48
HPS SDRAM I/O (Shared LVDS I/O) (1)	2N	48	48	48	TBD	48	48
	2M	48	48	48	TBD	48	48
	2L	48	48	48	TBD	48	48
LVDS I/O	2K	48	48	—	TBD	48	48
	2J	—	—		TBD	—	—
	2I	—	—		TBD	—	—

continued...

(1) In devices without HPS, these are normal LVDS I/Os.

Bank		Device Package					
		HF35	NF43			NF48	SF48
Type	Name	GX 400 SX 400 GX 650 SX 650	GX 650 SX 650	GX 850 SX 850 GX 1100 SX 1100 GX 1650 SX 1650 GX 2100 SX 2100 GX 2500 SX 2500 GX 2800 SX 2800	MX 1100	GX 850 SX 850 GX 1100 SX 1100	TX 1650 TX 2100 TX 2500 TX 2800
	2H	—	—		TBD	—	—
	2G	—	—		TBD	—	—
	2F	—	—		TBD	48	—
	2C	—	—	48	TBD	48	48
	2B	—	—	48	TBD	48	48
	2A	—	—	48	TBD	48	48
Total		392	400	688	448	736	544

Table 7. I/O Pin Counts for UF50, NF53, UF53, UF55, and YF55 Packages—Preliminary

Bank		Device Package					
		UF50		NF53	UF53	UF55	YF55
Type	Name	GX 1650 SX 1650 GX 2100 SX 2100 GX 2500 SX 2500 GX 2800 SX 2800	TX 1650 TX 2100 TX 2500 TX 2800	MX 1650 MX 2100	MX 1650 MX 2100	MX 1650 MX 2100	TX 2500 TX 2800
3 V I/O	7C	8	—	—	8	TBD	—
	7B	—	—	—	—	TBD	—
	7A	8	—	8	8	TBD	—
	6C	8	—	—	8	TBD	—
	6B	—	—	—	—	TBD	—
	6A	8	8	8	8	TBD	8
LVDS I/O	3L	48	—	48	48	TBD	—
	3K	48	—	48	48	TBD	—
	3J	48	—	48	48	TBD	—
	3I	48	—	—	—	TBD	—
	3H	—	—	—	—	TBD	—

continued...

Bank		Device Package					
		UF50		NF53	UF53	UF55	YF55
Type	Name	GX 1650 SX 1650 GX 2100 SX 2100 GX 2500 SX 2500 GX 2800 SX 2800	TX 1650 TX 2100 TX 2500 TX 2800	MX 1650 MX 2100	MX 1650 MX 2100	MX 1650 MX 2100	TX 2500 TX 2800
	3G	—	—	—	—	TBD	—
	3F	—	—	—	—	TBD	—
	3E	—	—	—	—	TBD	—
	3D	—	—	—	—	TBD	—
	3C	48	—	48	48	TBD	48
SDM Shared LVDS I/O	3B	48	48	48	48	TBD	48
	3A	48	48	48	48	TBD	48
HPS SDRAM I/O (Shared LVDS I/O) [(2)]	2N	48	48	48	48	TBD	48
	2M	48	48	48	48	TBD	48
	2L	48	48	48	48	TBD	48
LVDS I/O	2K	—	48	24	24	TBD	—
	2J	—	—	—	—	TBD	—
	2I	—	—	—	—	TBD	—
	2H	—	—	—	—	TBD	—
	2G	—	—	—	—	TBD	—
	2F	48	—	24	24	TBD	—
	2C	48	48	48	48	TBD	—
	2B	48	48	48	48	TBD	—
	2A	48	48	48	48	TBD	—
Total		704	440	400	688	584	296

(2) In devices without HPS, these are normal LVDS I/Os.

Table 8. I/O Pin Counts for HF55 Package—Preliminary

Bank		Device Package	
		HF55	
Type	Name	GX 2500 SX 2500 GX 2800 SX 2800	GX 4500 SX 4500 GX 5500 SX 5500
3 V I/O	6A	8	8
LVDS I/O	5N	—	48
	5M	—	48
	5L	—	48
	5K	—	48
	5J	—	48
	5I	—	48
	5H	—	—
	5G	—	—
	5F	—	—
	5E	—	—
	5D	—	48
	5C	—	48
	5B	—	48
	5A	—	48
	3N	—	—
	3M	—	—
	3L	48	48
	3K	48	48
	3J	48	48
	3I	48	48
	3H	48	48
	3G	48	48
	3F	48	48
	3E	48	48
	3D	48	48
	3C	48	48
SDM Shared LVDS I/O	3B	48	48
	3A	48	48
HPS SDRAM I/O (Shared LVDS I/O) (3)	2N	48	48
	2M	48	48

continued...

Bank		Device Package	
		HF55	
Type	Name	GX 2500 SX 2500 GX 2800 SX 2800	GX 4500 SX 4500 GX 5500 SX 5500
	2L	48	48
LVDS I/O	2K	48	48
	2J	48	48
	2I	48	48
	2H	48	48
	2G	48	48
	2F	48	48
	2E	—	48
	2D	—	48
	2C	48	48
	2B	48	—
	2A	48	—
Total		1160	1640

Related Links

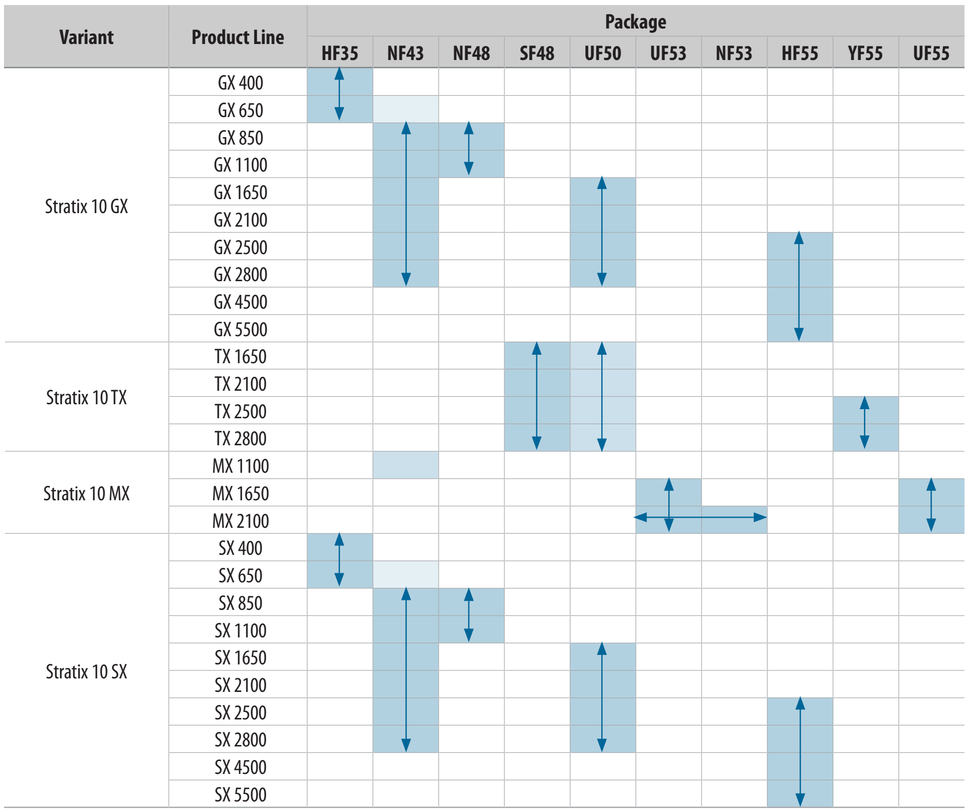
- Secure Device Manager, Intel Stratix 10 Configuration User Guide
  Provides more information about the Secure Device Manager.
- Restrictions on I/O Bank Usage for Intel Stratix 10 EMIF with HPS, Intel Stratix 10 External Memory Interfaces User Guide
  Provides more information about the shared LVDS I/O banks that are used by the HPS SDRAM interface.
- Hard Processor System I/O Pin Multiplexing, Intel Stratix 10 Hard Processor System Technical Reference Manual
  Provides more information about the dedicated I/O pins in the HPS.
- SDM Pin Mapping, Intel Stratix 10 Configuration User Guide
  Provides more information about pins in the SDM-shared LVDS I/O banks that are used by the SDM.
- Secure Device Manager (SDM) Pins, Intel Stratix 10 GX, MX, and SX Device Family Pin Connection Guidelines
  Provides the descriptions and connection guidelines for the SDM pins.
- I/O Banks Locations in Intel Stratix 10 Devices on page 8

(3) In devices without HPS, these are normal LVDS I/Os.

1.4 Intel Stratix 10 I/O Vertical Migration Support

Figure 3. Migration Capability Across Intel Stratix 10 Product Lines—Preliminary

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Devices with fewer resources in the same path have lighter shades.
- To achieve the full I/O migration across product lines in the same migration path, restrict I/Os and transceivers usage to match the product line with the lowest I/O and transceiver counts.
- You can migrate horizontally between the UF53 and NF53 packages of the Intel Stratix 10 MX 2100 product line. However, different ordering part number of the product line has different LE count or HBM features.



Note: To verify the pin migration compatibility, use the **Pin Migration View** window in the Intel Quartus® Prime software Pin Planner.

2 Intel Stratix 10 I/O Architecture and Features

The I/O system of Intel Stratix 10 devices support various I/O standards. In the Intel Stratix 10 devices, the I/O pins are located in I/O banks. The I/O pins and I/O buffers have several programmable features.

The Intel Stratix 10 I/Os support the following features:

- Single-ended, non-voltage-referenced, and voltage-referenced I/O standards
- Low-voltage differential signaling (LVDS), RSDS, mini-LVDS, HSTL, HSUL, SSTL, and POD I/O standards
- Serializer/deserializer (SERDES)
- Programmable output current strength
- Programmable slew rate
- Programmable bus-hold
- Programmable weak pull-up resistor
- Programmable pre-emphasis for DDR4 and the LVDS output buffer
- Programmable I/O delay
- Programmable differential output voltage (V_{OD})
- Programmable open-drain output
- On-chip series termination (R_S OCT) with and without calibration
- On-chip parallel termination (R_T OCT)
- On-chip differential termination (R_D OCT)
- HSTL and SSTL input buffer with dynamic power down
- Dynamic on-chip parallel termination for all I/O banks
- Internally generated V_{REF} with DDR4 calibration

Note: The information in this chapter is applicable to all Intel Stratix 10 variants, unless noted otherwise.

2.1 I/O Standards and Voltage Levels in Intel Stratix 10 Devices

The Intel Stratix 10 device family consists of FPGA and SoC devices. Apart from the FPGA I/O buffers, the Intel Stratix 10 SoC devices also have HPS I/O buffers with support for different I/O standards.

2.1.1 Intel Stratix 10 I/O Standards Support

Table 9. Intel Stratix 10 Devices I/O Standards Support for FPGA I/O—Preliminary

I/O Standard	I/O Buffer Type Support		Application	Standard Support
	LVDS I/O	3 V I/O(4)		
3.0 V LVTTL/3.0 V LVCMOS	No	Yes	General purpose	JESD8-B
2.5 V LVCMOS	No	Yes (5)	General purpose	JESD8-5
1.8 V LVCMOS	Yes	Yes (5)	General purpose	JESD8-7
1.5 V LVCMOS	Yes	Yes (5)	General purpose	JESD8-11
1.2 V LVCMOS	Yes	Yes (5)	General purpose	JESD8-12
SSTL-18 Class I and Class II	Yes	No	Flash interface	JESD8-15
SSTL-15 Class I and Class II	Yes	No	DDR3	—
SSTL-15	Yes	No	DDR3	JESD79-3D
SSTL-135	Yes	No	DDR3L	—
SSTL-125(6)	Yes	No	QDR-IV	—
SSTL-12	Yes	No	RLDRAM 3, QDR-IV	—
POD12	Yes	No	DDR4, QDR-IV	JESD8-24
1.8 V HSTL Class I and Class II	Yes	No	DDR II+, QDR II+, and RLDRAM 2	JESD8-6
1.5 V HSTL Class I and Class II	Yes	No	DDR II+, QDR II+, QDR II, and RLDRAM 2	JESD8-6
1.2 V HSTL Class I and Class II	Yes	No	QDR-IV, General purpose	JESD8-16A
HSUL-12	Yes	No	LPDDR2, LPDDR3	—
Differential SSTL-18 Class I and Class II	Yes	No	DDR2	JESD8-15
Differential SSTL-15 Class I and Class II	Yes	No	DDR3	—
Differential SSTL-15	Yes	No	DDR3	JESD79-3D
Differential SSTL-135	Yes	No	DDR3L	—
Differential SSTL-125(6)	Yes	No	General purpose	—
Differential SSTL-12	Yes	No	RLDRAM 3	—
Differential POD12	Yes	No	DDR4	JESD8-24
Differential 1.8 V HSTL Class I and Class II	Yes	No	DDR II+, QDR II+, and RLDRAM 2	JESD8-6

continued...

(4) Not supported in Intel Stratix 10 devices with E-Tile transceiver variant.

(5) You must set the USE_AS_3V_GPIO Intel Quartus Prime assignment to the pin.

(6) Even though the Intel Stratix 10 I/O buffers support various I/O standards for memory application, Intel validates and support only IPs for memory interfaces listed in Performance Support Summary, Intel Stratix 10 External Memory Interfaces User Guide.

I/O Standard	I/O Buffer Type Support		Application	Standard Support
	LVDS I/O	3 V I/O[4]		
Differential 1.5 V HSTL Class I and Class II	Yes	No	DDR II+, QDR II+, QDR II, and RLDRAM 2	JESD8-6
Differential 1.2 V HSTL Class I and Class II	Yes	No	General purpose	JESD8-16A
Differential HSUL-12	Yes	No	LPDDR2, LPDDR3	—
LVDS	Yes	No	SGMII, SFI, SPI	ANSI/TIA/EIA-644
Mini-LVDS	Yes	No	SGMII, SFI, SPI	—
RSDS	Yes	No	SGMII, SFI, SPI	—
LVPECL	Yes	No	SGMII, SFI, SPI	—

Note: To use the 1.2 V, 1.5 V, 1.8 V, or 2.5 V I/O standards in the 3 V I/O bank, you must set the **USE_AS_3V_GPIO** assignment to the I/O pin. In the Intel Quartus Prime Settings File (`.qsf`), specify the following assignment: `set_instance_assignment -name USE_AS_3V_GPIO ON -to` *<your pin name>*

Table 10. Intel Stratix 10 SX Devices I/O Standards Support for HPS I/O—Preliminary

I/O Standard	Application	Standard Support
1.8 V LVCMOS	General purpose	JESD8-7

2.1.2 Intel Stratix 10 I/O Standards Voltage Support

Table 11. Intel Stratix 10 Devices I/O Standards Voltage Levels

This table lists the typical power supplies for each supported I/O standards in Intel Stratix 10 devices.

I/O Standard	V_{CCIO}(V)		V_{CCPT}(V) (Pre-Driver Voltage)	V_{REF}(V) (Input Ref Voltage)	V_{TT}(V) (Board Termination Voltage)
	Input[7]	Output			
3.0 V LVTTL/3.0 V LVCMOS	3.0	3.0	1.8	—	—
2.5 V LVCMOS	3.0/2.5	2.5	1.8	—	—
1.8 V LVCMOS	1.8	1.8	1.8	—	—
1.5 V LVCMOS	1.5	1.5	1.8	—	—
1.2 V LVCMOS	1.2	1.2	1.8	—	—
SSTL-18 Class I and Class II	V_{CCPT}	1.8	1.8	0.9	0.9
SSTL-15 Class I and Class II	V_{CCPT}	1.5	1.8	0.75	0.75
SSTL-15	V_{CCPT}	1.5	1.8	0.75	0.75
SSTL-135	V_{CCPT}	1.35	1.8	0.675	0.675

continued...

(4) Not supported in Intel Stratix 10 devices with E-Tile transceiver variant.

(7) Input for the SSTL, HSTL, Differential SSTL, Differential HSTL, POD, Differential POD, LVDS, RSDS, Mini-LVDS, LVPECL, HSUL, and Differential HSUL are powered by V_{CCPT}

I/O Standard	V_{CCIO}(V)		V_{CCPT}(V) (Pre-Driver Voltage)	V_{REF}(V) (Input Ref Voltage)	V_{TT}(V) (Board Termination Voltage)
	Input[7]	Output			
SSTL-125	V_{CCPT}	1.25	1.8	0.625	0.625
SSTL-12	V_{CCPT}	1.2	1.8	0.6	0.6
POD12	V_{CCPT}	1.2	1.8	0.84	1.2
1.8 V HSTL Class I and Class II	V_{CCPT}	1.8	1.8	0.9	0.9
1.5 V HSTL Class I and Class II	V_{CCPT}	1.5	1.8	0.75	0.75
1.2 V HSTL Class I and Class II	V_{CCPT}	1.2	1.8	0.6	0.6
HSUL-12	V_{CCPT}	1.2	1.8	0.6	—
Differential SSTL-18 Class I and Class II	V_{CCPT}	1.8	1.8	—	0.9
Differential SSTL-15 Class I and Class II	V_{CCPT}	1.5	1.8	—	0.75
Differential SSTL-15	V_{CCPT}	1.5	1.8	—	0.75
Differential SSTL-135	V_{CCPT}	1.35	1.8	—	0.675
Differential SSTL-125	V_{CCPT}	1.25	1.8	—	0.625
Differential SSTL-12	V_{CCPT}	1.2	1.8	—	0.6
Differential POD12	V_{CCPT}	1.2	1.8	—	1.2
Differential 1.8 V HSTL Class I and Class II	V_{CCPT}	1.8	1.8	—	0.9
Differential 1.5 V HSTL Class I and Class II	V_{CCPT}	1.5	1.8	—	0.75
Differential 1.2 V HSTL Class I and Class II	V_{CCPT}	1.2	1.8	—	0.6
Differential HSUL-12	V_{CCPT}	1.2	1.8	—	—
LVDS	V_{CCPT}	1.8	1.8	—	—
Mini-LVDS	V_{CCPT}	1.8	1.8	—	—
RSDS	V_{CCPT}	1.8	1.8	—	—
LVPECL (Differential clock input only)	V_{CCPT}	—	1.8	—	—

(7) Input for the SSTL, HSTL, Differential SSTL, Differential HSTL, POD, Differential POD, LVDS, RSDS, Mini-LVDS, LVPECL, HSUL, and Differential HSUL are powered by V_{CCPT}

2.1.3 MultiVolt I/O Interface in Intel Stratix 10 Devices

The MultiVolt I/O interface feature allows Intel Stratix 10 devices in all packages to interface with systems of different supply voltages:

- Each I/O bank in Intel Stratix 10 devices has its own V_{CCIO} supply and can support only one V_{CCIO} voltage.
- The supported V_{CCIO} voltage is 1.2 V, 1.25 V, 1.35 V, 1.5 V, 1.8 V, 2.5 V, or 3.0 V.
- The 2.5 V and 3.0 V V_{CCIO} is supported only on the 3 V I/O buffer type.
- The I/O buffers are powered by V_{CC}, V_{CCPT} and V_{CCIO}.

2.2 I/O Element Structure in Intel Stratix 10 Devices

The I/O elements (IOEs) in Intel Stratix 10 devices contain a bidirectional I/O buffer and I/O registers to support a complete embedded bidirectional single data rate (SDR) or double data rate (DDR) transfer.

The IOEs are located in I/O columns within the core fabric of the Intel Stratix 10 device.

The Intel Stratix 10 SX devices also have IOEs for the HPS.

The GPIO IOE register consists of the DDR register, the half rate register, and the transmitter delay chains for input, output, and output enable (OE) paths:

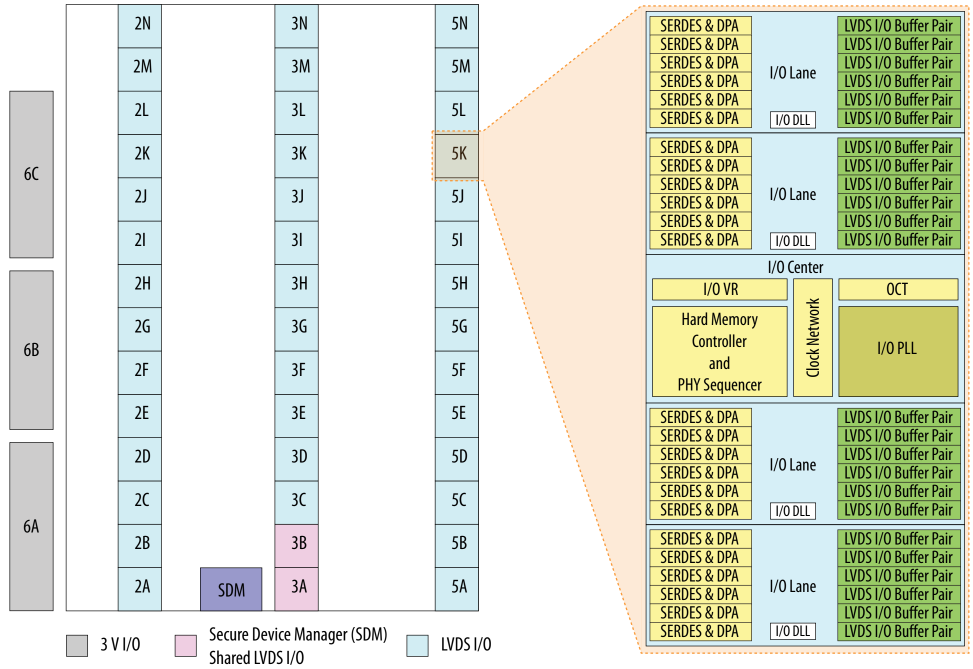
- You can take data from the combinatorial path or the registered path.
- Only the core clock clocks the data.
- The half rate clock routed from the core clocks the half rate register.
- The full rate clock from the core clocks the full rate register.

2.2.1 I/O Bank Architecture in Intel Stratix 10 Devices

In each LVDS I/O bank, there are four I/O lanes with 12 I/O pins in each lane. Other than the I/O lanes, each I/O bank also contains dedicated circuitries including the I/O PLL, DPA block, SERDES, hard memory controller, and I/O sequencer.

In each 3 V I/O bank, there are eight single-endded 3 V I/O buffers.

Figure 4. I/O Bank Structure



Related Links

- Secure Device Manager, Intel Stratix 10 Configuration User Guide
  Provides more information about the Secure Device Manager.
- Restrictions on I/O Bank Usage for Intel Stratix 10 EMIF with HPS, Intel Stratix 10 External Memory Interfaces User Guide
  Provides more information about the shared LVDS I/O banks that are used by the HPS SDRAM interface.

2.2.2 I/O Buffer and Registers in Intel Stratix 10 Devices

I/O registers are composed of the input path for handling data from the pin to the core, the output path for handling data from the core to the pin, and the output enable (OE) path for handling the OE signal to the output buffer. These registers allow faster source-synchronous register-to-register transfers and resynchronization.

The input and output paths contains the following blocks:

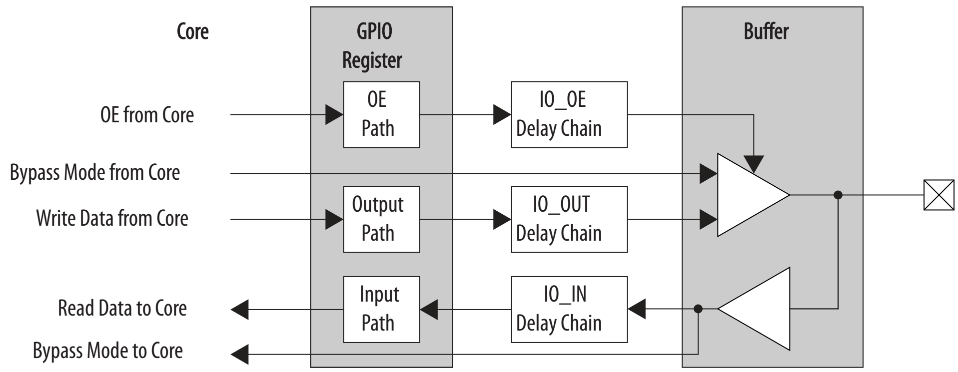
- Input registers—support half/full rate data transfer from peripheral to core, and support double or single data rate data capture from I/O buffer.
- Output registers—support half/full rate data transfer from core to peripheral, and support double or single data rate data transfer to I/O buffer.
- OE registers—support half or full rate data transfer from core to peripheral, and support single data rate data transfer to I/O buffer.

The input and output paths also support the following features:

- Clock enable.
- Asynchronous or synchronous reset.
- Bypass mode for input and output paths.
- Delays chains on input and output paths.

Figure 5. IOE Structure for Intel Stratix 10 Devices

This figure shows the Intel Stratix 10 FPGA IOE structure.



Note: The GPIOs in the 3 V I/O banks do not have I/O registers.

2.3 Programmable IOE Features in Intel Stratix 10 Devices

Table 12. Intel Stratix 10 Programmable IOE Features Settings and Assignment Name

Feature	Setting	Condition	Intel Quartus Prime Assignment Name
Slew Rate Control	0 (Slow), 1 (Fast). Default is 1.	Disabled if you use the R_S OCT feature.	SLEW_RATE
I/O Delay	Refer to the device datasheet	—	INPUT_DELAY_CHAIN OUTPUT_DELAY_CHAIN
Open-Drain Output	On, Off. Default is Off	—	AUTO_OPEN_DRAIN_PINS
Bus-Hold	On, Off. Default is Off.	Disabled if you use the weak pull-up resistor feature.	ENABLE_BUS_HOLD_CIRCUITRY
Weak Pull-up Resistor	On, Off. Default is Off.	Disabled if you use the bus-hold feature.	WEAK_PULL_UP_RESISTOR
Pre-Emphasis	0 (disabled), 1 (enabled). Default is 1.	—	PROGRAMMABLE_PREEMPHASIS
Differential Output Voltage	0 (low), 1 (medium low), 2 (medium high), 3 (high). Default is 2.	—	PROGRAMMABLE_VOD

Table 13. Intel Stratix 10 Programmable IOE Features I/O Buffer Types and I/O Standards Support

This table lists the I/O buffer types and I/O standards that support the programmable IOE features. For information about which I/O standards are available for each I/O buffer type, refer to the related information.

Feature	I/O Buffer Type Support			I/O Standards Support
	LVDS I/O	3 V I/O	HPS I/O (SoC Devices Only)	
Slew Rate Control	Yes	Yes	Yes	• 3.0 V LVTTL • 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.0 V LVCMOS • SSTL-18, SSTL-15, SSTL-135, SSTL-125, and SSTL-12 • 1.2 V, 1.5 V, and 1.8 V HSTL • HSUL-12 • POD12 • Differential SSTL-18, Differential SSTL-15, Differential SSTL-135, Differential SSTL-125, and Differential SSTL-12 • Differential 1.2 V, 1.5 V, and 1.8 V HSTL • Differential HSUL-12
I/O Delay	Yes	Yes	—	
Open-Drain Output	Yes	Yes	Yes	• 3.0 V LVTTL • 1.2 V, 1.5 V, 1.8 V, and 3.0 V LVCMOS
Bus-Hold	Yes	Yes	—	
Weak Pull-up Resistor	Yes	Yes	Yes	
Pre-Emphasis	Yes	—	—	• LVDS • RSDS • Mini-LVDS • LVPECL • Differential POD12
Differential Output Voltage	Yes	—	—	• LVDS • RSDS • Mini-LVDS • LVPECL

Related Links

- Intel Stratix 10 Device Datasheet
- Intel Stratix 10 I/O Standards Support on page 18
  Lists the I/O standards supported by the LVDS I/O, 3 V I/O, and HPS I/O buffers.

2.3.1 Programmable Output Slew Rate Control

You can specify the slew rate on a pin-by-pin basis because each I/O pin contains a slew rate control. The slew rate control affects both the rising and falling edges.

You can select between two slew rate settings, 1 and 0:

- Fast slew rate (1)—provides high-speed transitions for high-performance systems. This is the default setting. If you enable on-chip termination (OCT), this setting is always used.
- Slow slew rate (0)—reduces system noise and crosstalk but adds a nominal delay to the rising and falling edges.

Note: Intel recommends that you perform IBIS or SPICE simulations to determine the best slew rate setting for your specific application.

2.3.2 Programmable IOE Delay

You can activate the programmable IOE delays to ensure zero hold times, minimize setup times, or increase clock-to-output times. This feature helps read and write timing margins because it minimizes the uncertainties between signals in the bus.

Each pin can have a different input delay from pin-to-input register or a delay from output register-to-output pin values to ensure that the signals within a bus have the same delay going into or out of the device.

For more information about the programmable IOE delay specifications, refer to the device datasheet.

Related Links

Programmable IOE Delay, Intel Stratix 10 Device Datasheet

2.3.3 Programmable Open-Drain Output

An open-drain output provides a high-impedance state on output when logic-to-pin is high. If logic-to-pin is low, output is low.

You can attach several open-drain output to a wire. This connection type is like a logical OR function and is commonly called an active-low wired-OR circuit. If at least one of the outputs is in logic 0 state (active), the circuit sinks the current and brings the line to low voltage.

You can use open-drain output if you are connecting multiple devices to a bus. For example, you can use the open-drain output for system-level control signals that can be asserted by any device or as an interrupt.

You can enable the open-drain output assignment using one of these methods:

- Design the tristate buffer using OPNDRN primitive.
- Turn on the **Auto Open-Drain Pins** option in the Intel Quartus Prime software.

You can design open-drain output without enabling the option assignment. However, your design will not use the I/O buffer's open-drain output feature. The open-drain output feature of the I/O buffer provides you the best propagation delay from OE to output.

Related Links

Plan Stage Reports, Intel Quartus Prime Pro Edition Handbook Volume 1: Design and Compilation
Provides more information about the Fitter Plan Stage report that you can use to check the I/O pins settings.

2.3.4 Programmable Bus Hold

Each I/O pin provides an optional bus-hold feature that is active only after configuration. When the device enters user mode, the bus-hold circuit captures the value that is present on the pin by the end of the configuration.

The bus-hold circuitry uses a resistor with a nominal resistance (R_{BH}), approximately 7 kΩ, to weakly pull the signal level to the last-driven state of the pin. The bus-hold circuitry holds this pin state until the next input signal is present. Because of this, you do not require an external pull-up or pull-down resistor to hold a signal level when the bus is tri-stated.

For each I/O pin, you can individually specify that the bus-hold circuitry pulls non-driven pins away from the input threshold voltage—where noise can cause unintended high-frequency switching. To prevent over-driving signals, the bus-hold circuitry drives the voltage level of the I/O pin lower than the V_{CCIO} level.

If you enable the bus-hold feature, you cannot use the programmable pull-up option. To configure the I/O pin for differential signals, disable the bus-hold feature.

2.3.5 Programmable Pull-Up Resistor

Each I/O pin provides an optional programmable pull-up resistor during user mode. The pull-up resistor weakly holds the I/O to the V_{CCIO} level.

The Intel Stratix 10 device supports programmable weak pull-up resistors only on user I/O pins but not on dedicated configuration pins, dedicated clock pins, or JTAG pins .

If you enable the weak pull-up resistor, you cannot use the bus-hold feature.

2.3.6 Programmable Pre-Emphasis

The V_{OD} setting and the output impedance of the driver set the output current limit of a high-speed transmission signal. At a high frequency, the slew rate may not be fast enough to reach the full V_{OD} level before the next edge, producing pattern-dependent jitter. With pre-emphasis, the output current is boosted momentarily during switching to increase the output slew rate.

Pre-emphasis increases the amplitude of the high-frequency component of the output signal, and thus helps to compensate for the frequency-dependent attenuation along the transmission line. The overshoot introduced by the extra current happens only during a change of state switching to increase the output slew rate and does not ring, unlike the overshoot caused by signal reflection. The amount of pre-emphasis required depends on the attenuation of the high-frequency component along the transmission line.

Figure 6. Programmable Pre-Emphasis

This figure shows the LVDS output with pre-emphasis.

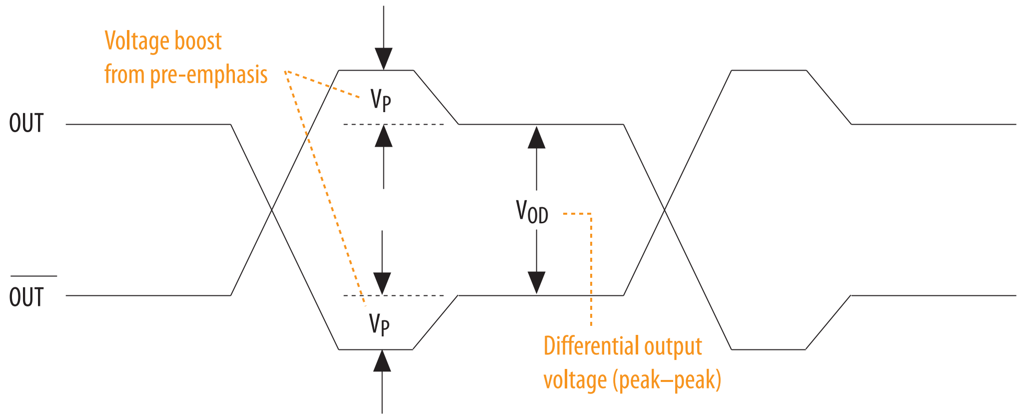


Table 14. Software Assignment Editor—Programmable Pre-Emphasis

This table lists the assignment name for programmable pre-emphasis and its possible values in the software Assignment Editor.

Field	Assignment
To	`tx_out`
Assignment name	Programmable Pre-emphasis
Allowed values	0 (disabled), 1 (enabled). Default is 1.

2.3.7 Programmable Differential Output Voltage

The programmable V_{OD} settings allow you to adjust the output eye opening to optimize the trace length and power consumption. A higher V_{OD} swing improves voltage margins at the receiver end, and a smaller V_{OD} swing reduces power consumption. You can statically adjust the V_{OD} of the differential signal by changing the V_{OD} settings in the software Assignment Editor.

Figure 7. Differential V_{OD}

This figure shows the V_{OD} of the differential LVDS output.

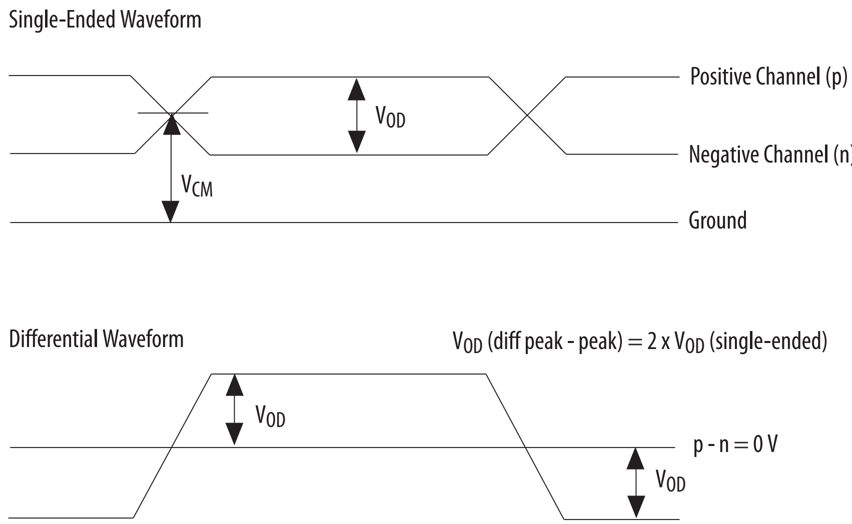


Table 15. Software Assignment Editor—Programmable V_{OD}

This table lists the assignment name for programmable V_{OD} and its possible values in the software Assignment Editor. Value "0" is available for the RSDS and mini-LVDS I/O standards only, and is not available for the LVDS I/O standard.

Field	Assignment
To	`tx_out`
Assignment name	Programmable Differential Output Voltage (V_{OD})
Allowed values	0 (low), 1 (medium low), 2 (medium high), 3 (high). Default is 2.

2.3.8 Programmable Current Strength

You can use the programmable current strength to mitigate the effects of high signal attenuation that is caused by a long transmission line or a legacy backplane.

Note: To use programmable current strength, you must specify the current strength assignment in the Intel Quartus Prime software. Without explicit assignments, the Intel Quartus Prime software uses these predefined default values:

- All HSTL and SSTL Class I, and all non-voltage-referenced I/O standards—50 Ω R_S OCT without calibration
- All HSTL and SSTL Class II I/O standards—25 Ω R_S OCT without calibration
- POD12 I/O standard—34 Ω R_S OCT without calibration

Table 16. Programmable Current Strength Settings for Intel Stratix 10 Devices

The output buffer for each Intel Stratix 10 device I/O pin has a programmable current strength control for the I/O standards listed in this table.

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA)			
	Supported in FPGA		Supported in HPS (8) (SoC Devices Only)	
	Available	Default	Available	Default
3.0 V LVTTL/3.0 V CMOS	16, 12, 8, 4	12	—	—
2.5 V LVCMOS	16, 12, 8, 4	12	—	—
1.8 V LVCMOS	16, 12, 10, 8, 6, 4, 2	12	12, 10, 8	12
1.5 V LVCMOS	12, 10, 8, 6, 4, 2	12	—	—
1.2 V LVCMOS	8, 6, 4, 2	8	—	—
SSTL-18 Class I	8, 6, 4	8	—	—
SSTL-18 Class II	8	8	—	—
SSTL-15 Class I	8, 6, 4	8	—	—
SSTL-15 Class II	8	8	—	—
SSTL-135	8, 6, 4	8	—	—
SSTL-125	8, 6, 4	8	—	—
SSTL-12	8, 6, 4	8	—	—
POD12	8, 6, 4	8	—	—
1.8 V HSTL Class I	12, 10, 8, 6, 4	8	—	—
1.8 V HSTL Class II	14	14	—	—
1.5 V HSTL Class I	12, 10, 8, 6, 4	8	—	—
1.5 V HSTL Class II	14	14	—	—
1.2 V HSTL Class I	8, 6, 4	8	—	—
Differential SSTL-135	12, 10, 8, 6, 4	8	—	—
Differential SSTL-125	12, 10, 8, 6, 4	8	—	—
Differential SSTL-12 Class I	12, 10, 8, 6, 4	8	—	—
Differential POD12	8, 6, 4	8	—	—
Differential 1.8 V HSTL Class I	12, 10, 8, 6, 4	8	—	—
Differential 1.8 V HSTL Class II	14	14	—	—

continued...

(8) The programmable current strength information for the HPS is preliminary.

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA)			
	Supported in FPGA		Supported in HPS [8] (SoC Devices Only)	
	Available	Default	Available	Default
Differential 1.5 V HSTL Class I	12, 10, 8, 6, 4	8	—	—
Differential 1.5 V HSTL Class II	14	14	—	—
Differential 1.2 V HSTL Class I	8, 6, 4	8	—	—

Note: Intel recommends that you perform IBIS or SPICE simulations to determine the best current strength setting for your specific application.

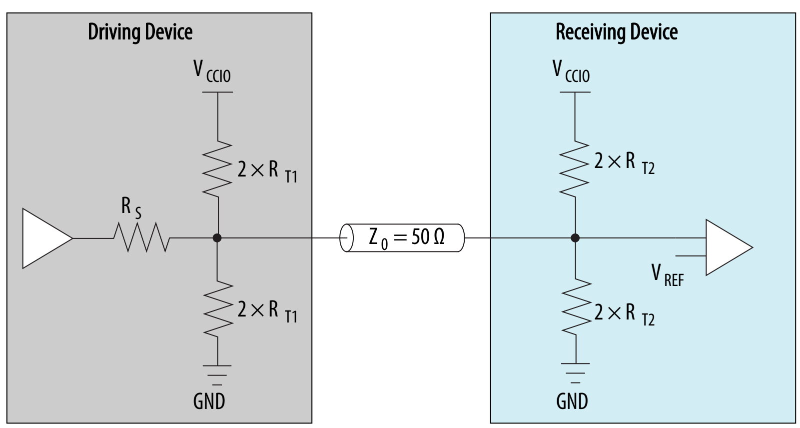
2.4 On-Chip I/O Termination in Intel Stratix 10 Devices

Serial (R_S) and parallel (R_T) OCT provides I/O impedance matching and termination capabilities. OCT maintains signal quality, saves board space, and reduces external component costs.

The Intel Stratix 10 devices support OCT in all FPGA I/O banks. For the 3 V I/Os, the I/Os support only OCT without calibration.

Figure 8. Single-ended Termination (R_S and R_T)

This figure shows the single-ended termination schemes supported in Intel Stratix 10 devices. R_{T1} and R_{T2} are dynamic parallel terminations and are enabled only if the device is receiving. In bidirectional applications, R_{T1} and R_{T2} are automatically switched on when the device is receiving and switched off when the device is driving.



(8) The programmable current strength information for the HPS is preliminary.

Table 17. OCT Schemes Supported in Intel Stratix 10 Devices

Direction	OCT Schemes	I/O Type Support	
		LVDS I/O	3 V I/O
Output	R_S OCT with calibration	Yes	—
	R_S OCT without calibration	Yes	—
Input	R_T OCT with calibration	Yes	—
	R_D OCT (LVDS I/O standard only)	Yes	—
Bidirectional	Dynamic R_S and R_T OCT	Yes	—

2.4.1 R_S OCT without Calibration in Intel Stratix 10 Devices

The Intel Stratix 10 devices support R_S OCT for single-ended and voltage-referenced I/O standards. R_S OCT without calibration is supported on output only.

Table 18. Selectable I/O Standards for R_S OCT Without Calibration

This table lists the output termination settings for uncalibrated OCT on different I/O standards.

I/O Standard	Uncalibrated OCT (Output)
	R_S (Ω)
3.0 V LVTTL/3.0 V LVCMOS	25, 50
2.5 V LVCMOS	25, 50
1.8 V LVCMOS	25, 50
1.5 V LVCMOS	25, 50
1.2 V LVCMOS	25, 50
SSTL-18 Class I	50
SSTL-18 Class II	25
SSTL-15 Class I	50
SSTL-15 Class II	25
SSTL-15	34, 40
SSTL-135	34, 40
SSTL-125	34, 40
SSTL-12	34, 40, 60, 120, 240
POD12	34, 40, 48, 60
1.8 V HSTL Class I	50
1.8 V HSTL Class II	25
1.5 V HSTL Class I	50
1.5 V HSTL Class II	25
1.2 V HSTL Class I	50
1.2 V HSTL Class II	25
HSUL-12	34, 40, 48, 60, 80

continued...

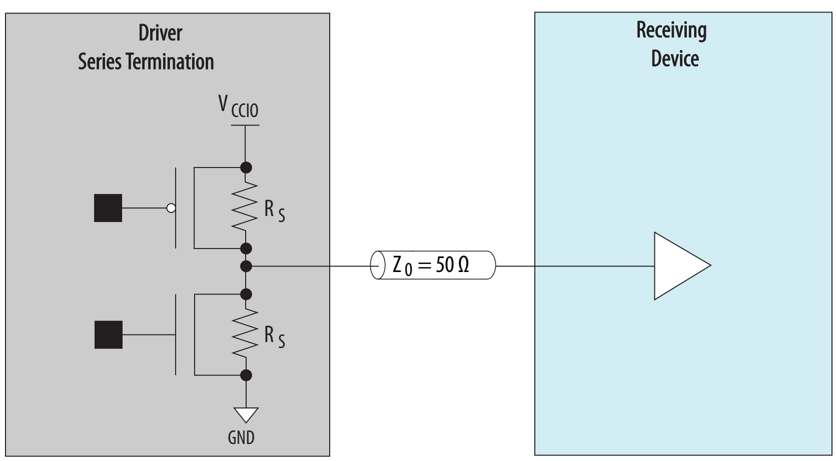
I/O Standard	Uncalibrated OCT (Output)
	R_S (Ω)
Differential SSTL-18 Class I	50
Differential SSTL-18 Class II	25
Differential SSTL-15 Class I	50
Differential SSTL-15 Class II	25
Differential SSTL-15	34, 40
Differential SSTL-135	34, 40
Differential SSTL-125	34, 40
Differential SSTL-12	34, 40, 60, 120, 240
Differential POD12	34, 40, 48, 60
Differential 1.8 V HSTL Class I	50
Differential 1.8 V HSTL Class II	25
Differential 1.5 V HSTL Class I	50
Differential 1.5 V HSTL Class II	25
Differential 1.2 V HSTL Class I	50
Differential 1.2 V HSTL Class II	25
Differential HSUL-12	34, 40, 48, 60, 80

Driver-impedance matching provides the I/O driver with controlled output impedance that closely matches the impedance of the transmission line. As a result, you can significantly reduce signal reflections on PCB traces.

If you use impedance matching, you cannot specify the current strength.

Figure 9. R_S OCT Without Calibration

This figure shows the R_S as the intrinsic impedance of the output transistors.



2.4.2 R_SOCT with Calibration in Intel Stratix 10 Devices

The Intel Stratix 10 devices support R_S OCT with calibration in all LVDS I/O banks.

Table 19. Selectable I/O Standards for R_SOCT With Calibration

This table lists the output termination settings for calibrated OCT on different I/O standards.

I/O Standard	Calibrated OCT (Output)	
	R_S (Ω)	RZQ (Ω)
1.8 V LVCMOS	25, 50	100
1.5 V LVCMOS	25, 50	100
1.2 V LVCMOS	25, 50	100
SSTL-18 Class I	50	100
SSTL-18 Class II	25	100
SSTL-15 Class I	50	100
SSTL-15 Class II	25	100
SSTL-15	34, 40	240
SSTL-135	34, 40	240
SSTL-125	34, 40	240
SSTL-12	34, 40, 60, 120, 240	240
POD12	34, 40, 48, 60	240
1.8 V HSTL Class I	50	100
1.8 V HSTL Class II	25	100
1.5 V HSTL Class I	50	100
1.5 V HSTL Class II	25	100
1.2 V HSTL Class I	50	100
1.2 V HSTL Class II	25	100
HSUL-12	34, 40, 48, 60, 80	240
Differential SSTL-18 Class I	50	100
Differential SSTL-18 Class II	25	100
Differential SSTL-15 Class I	50	100
Differential SSTL-15 Class II	25	100
Differential SSTL-15	34, 40	240
Differential SSTL-135	34, 40	240
Differential SSTL-125	34, 40	240
Differential SSTL-12	34, 40, 60, 120, 240	240
Differential POD12	34, 40, 48, 60	240
Differential 1.8 V HSTL Class I	50	100
Differential 1.8 V HSTL Class II	25	100
Differential 1.5 V HSTL Class I	50	100
Differential 1.5 V HSTL Class II	25	100

continued...

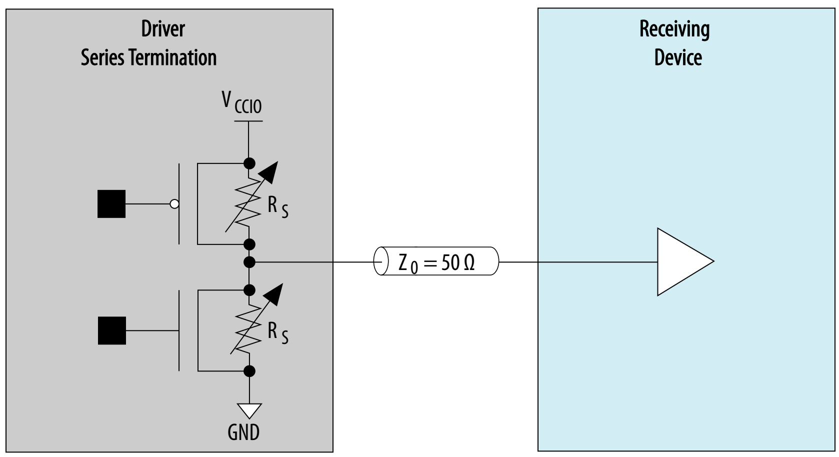
I/O Standard	Calibrated OCT (Output)	
	R_S (Ω)	RZQ (Ω)
Differential 1.2 V HSTL Class I	50	100
Differential 1.2 V HSTL Class II	25	100
Differential HSUL-12	34, 40, 48, 60, 80	240

The R_S OCT calibration circuit compares the total impedance of the I/O buffer to the external reference resistor connected to the RZQ pin and dynamically enables or disables the transistors until they match.

Calibration occurs at the end of device configuration. When the calibration circuit finds the correct impedance, the circuit powers down and stops changing the characteristics of the drivers.

Figure 10. R_S OCT with Calibration

This figure shows the R_S as the intrinsic impedance of the output transistors.



2.4.3 R_T OCT with Calibration in Intel Stratix 10 Devices

The Intel Stratix 10 devices support R_T OCT with calibration in all LVDS I/O banks but not in the 3 V I/O banks. R_T OCT with calibration is available only for configuration of input and bidirectional pins. Output pin configurations do not support R_T OCT with calibration. If you use R_T OCT, the V_{CCIO} of the bank must match the I/O standard of the pin where you enable the R_T OCT.

Table 20. Selectable I/O Standards for R_TOCT With Calibration

This table lists the input termination settings for calibrated OCT on different I/O standards.

I/O Standard	Calibrated OCT (Input)	
	R_T (Ω)	RZQ (Ω)
SSTL-18 Class I	50	100
SSTL-18 Class II	50	100
SSTL-15 Class I	50	100
SSTL-15 Class II	50	100

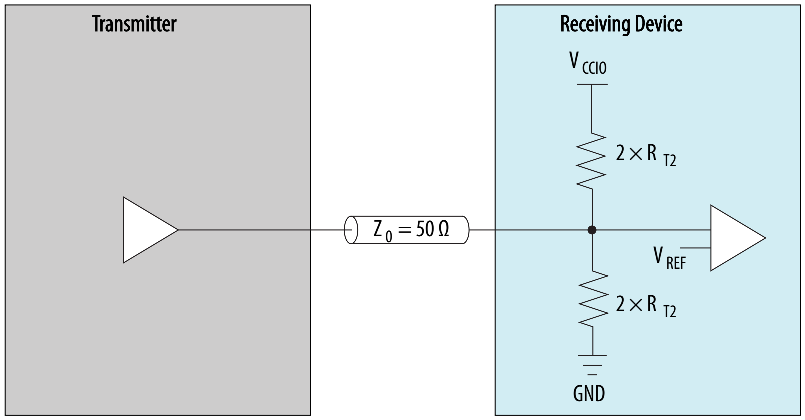
continued...

I/O Standard	Calibrated OCT (Input)	
	R_T (Ω)	RZQ (Ω)
SSTL-15	48, 50, 60,120	240
SSTL-135	48, 60, 120	240
SSTL-125	48, 60, 120	240
SSTL-12	60, 120	240
POD12	34, 40, 48, 60, 80, 120, 240	240
1.8 V HSTL Class I	50	100
1.8 V HSTL Class II	50	100
1.5 V HSTL Class I	50	100
1.5 V HSTL Class II	50	100
1.2 V HSTL Class I	50	100
1.2 V HSTL Class II	50	100
Differential SSTL-18 Class I	50	100
Differential SSTL-18 Class II	50	100
Differential SSTL-15 Class I	50	100
Differential SSTL-15 Class II	50	100
Differential SSTL-15	48, 50, 60,120	240
Differential SSTL-135	48, 60, 120	240
Differential SSTL-125	48, 60, 120	240
Differential SSTL-12	60, 120	240
Differential POD12	34, 40, 48, 60, 80, 120, 240	240
Differential 1.8 V HSTL Class I	50	100
Differential 1.8 V HSTL Class II	50	100
Differential 1.5 V HSTL Class I	50	100
Differential 1.5 V HSTL Class II	50	100
Differential 1.2 V HSTL Class I	50	100
Differential 1.2 V HSTL Class II	50	100

The R_T OCT calibration circuit compares the total impedance of the I/O buffer to the external resistor connected to the RZQ pin. The circuit dynamically enables or disables the transistors until the total impedance of the I/O buffer matches the external resistor.

Calibration occurs at the end of the device configuration. When the calibration circuit finds the correct impedance, the circuit powers down and stops changing the characteristics of the drivers.

Figure 11. R_T OCT with Calibration



2.4.4 Dynamic OCT

Dynamic OCT is useful for terminating a high-performance bidirectional path by optimizing the signal integrity depending on the direction of the data. Dynamic OCT also helps save power because device termination is internal—termination switches on only during input operation and thus draw less static power.

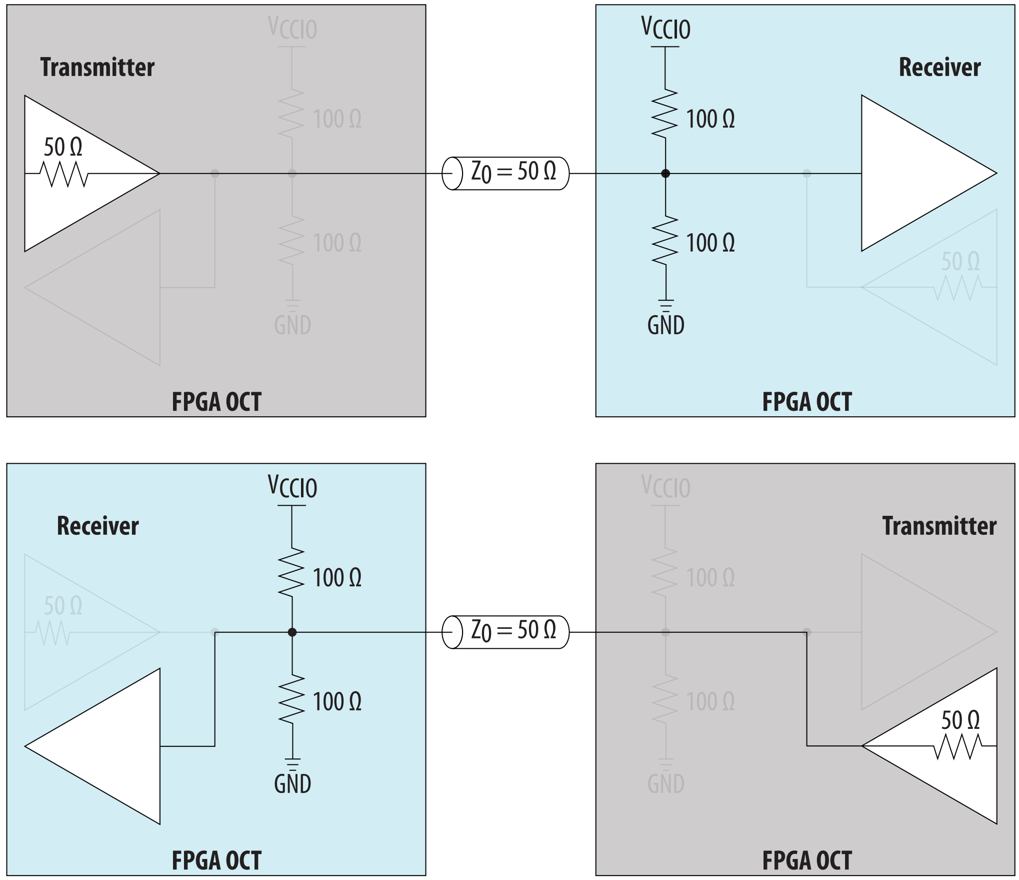
Note: If you use the SSTL-15, SSTL-135, and SSTL-125 I/O standards with the DDR3 memory interface, Intel recommends that you use OCT with these I/O standards to save board space and cost. OCT reduces the number of external termination resistors used.

Table 21. Dynamic OCT Based on Bidirectional I/O

Dynamic R_T OCT or R_S OCT is enabled or disabled based on whether the bidirectional I/O acts as a receiver or driver.

Dynamic OCT	Bidirectional I/O	State
Dynamic R_T OCT	Acts as a receiver	Enabled
	Acts as a driver	Disabled
Dynamic R_S OCT	Acts as a receiver	Disabled
	Acts as a driver	Enabled

Figure 12. Dynamic R_T OCT in Intel Stratix 10 Devices



2.4.5 Differential Input R_D OCT

All I/O pins and dedicated clock input pins in Intel Stratix 10 devices support on-chip differential termination, R_D OCT. The Intel Stratix 10 devices provide a 100 Ω, on-chip differential termination option on each differential receiver channel for LVDS standards.

You can enable on-chip termination in the Intel Quartus Prime software Assignment Editor.

Figure 13. On-Chip Differential I/O Termination

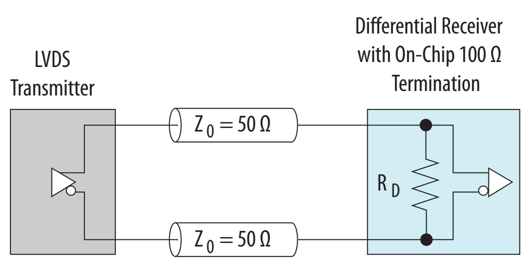


Table 22. Intel Quartus Prime Software Assignment Editor—On-Chip Differential Termination

This table lists the assignment name for on-chip differential termination in the Intel Quartus Prime software Assignment Editor.

Field	Assignment
To	`rx_in`
Assignment name	Input Termination
Value	Differential

2.4.6 OCT Calibration Block in Intel Stratix 10 Devices

You can calibrate the OCT using the OCT calibration block available in each I/O bank.

You can use R_S and R_T OCT in the same I/O bank for different I/O standards if the I/O standards use the same V_{CCIO} supply voltage. You cannot configure the R_S OCT and the programmable current strength for the same I/O buffer.

The OCT calibration process uses the RZQ pin that is available in every calibration block in a given I/O bank for series- and parallel-calibrated termination:

- Each OCT calibration block has an external 240 Ω reference resistor associated with it through the RZQ pin.
- Connect the RZQ pin to GND through an external 100 Ω or 240 Ω resistor (depending on the R_S or R_T OCT value).
- The RZQ pin shares the same V_{CCIO} supply voltage with the I/O bank where the pin is located.
- The RZQ pin is a dual-purpose I/O pin and functions as a general purpose I/O pin if you do not use the calibration circuit.

Intel Stratix 10 devices support calibrated R_S and calibrated R_T OCT on all LVDS I/O pins except for dedicated configuration pins.

2.5 External I/O Termination for Intel Stratix 10 Devices

Table 23. External Termination Schemes for Various I/O Standards

I/O Standard	External Termination Scheme
3.0 V LVTTL/3.0 V LVCMOS	No external termination required
2.5 V LVCMOS	
1.8 V LVCMOS	
1.5 V LVCMOS	
1.2 V LVCMOS	
SSTL-18 Class I and Class II	Single-Ended SSTL I/O Standard Termination
SSTL-15 Class I and Class II	
SSTL-15 (9)	No external termination required
SSTL-135 (9)	

continued...

I/O Standard	External Termination Scheme
SSTL-125 [9]	
SSTL-12	
POD12	Single-Ended POD I/O Standard Termination
1.8 V HSTL Class I and Class II	Single-Ended HSTL I/O Standard Termination
1.5 V HSTL Class I and Class II	
1.2 V HSTL Class I and Class II	
HSUL-12	No external termination required
Differential SSTL-18 Class I and Class II	Differential SSTL I/O Standard Termination
Differential SSTL-15 Class I and Class II	
Differential SSTL-15 [9]	No external termination required
Differential SSTL-135 [9]	
Differential SSTL-125 [9]	
Differential SSTL-12	
Differential POD12	Differential POD I/O Standard Termination
Differential 1.8 V HSTL Class I and Class II	Differential HSTL I/O Standard Termination
Differential 1.5 V HSTL Class I and Class II	
Differential 1.2 V HSTL Class I and Class II	
Differential HSUL-12	No external termination required
LVDS	LVDS I/O Standard Termination
RSDS	RSDS/mini-LVDS I/O Standard Termination
Mini-LVDS	
LVPECL	Differential LVPECL I/O Standard Termination

2.5.1 Single-Ended I/O Termination

Voltage-referenced I/O standards require an input V_{REF} and a termination voltage (V_{TT}). The reference voltage of the receiving device tracks the termination voltage of the transmitting device.

The supported I/O standards such as SSTL-12, SSTL-125, SSTL-135, and SSTL-15 typically do not require external board termination.

Intel recommends that you use OCT with these I/O standards to save board space and cost. OCT reduces the number of external termination resistors used.

Note: You cannot use R_S and R_T OCT simultaneously. For more information, refer to the related information.

(9) Intel recommends that you use OCT with these I/O standards to save board space and cost. OCT reduces the number of external termination resistors used.

Figure 14. SSTL I/O Standard Termination

This figure shows the details of SSTL I/O termination on Intel Stratix 10 devices.

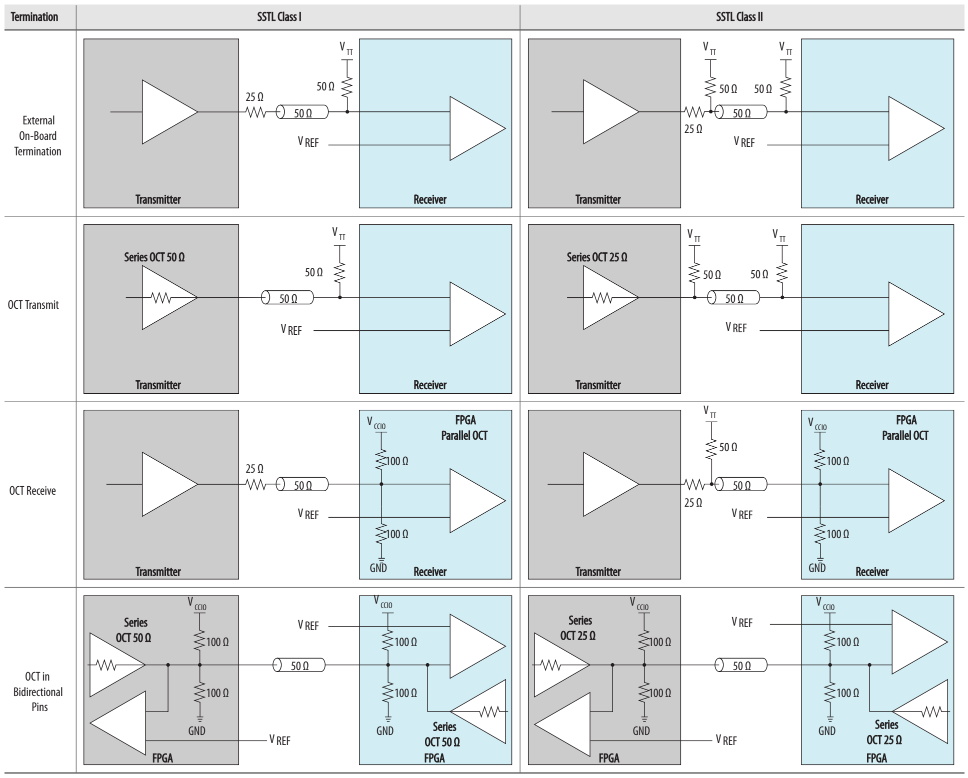


Figure 15. HSTL I/O Standard Termination

This figure shows the details of HSTL I/O termination on the Intel Stratix 10 devices.

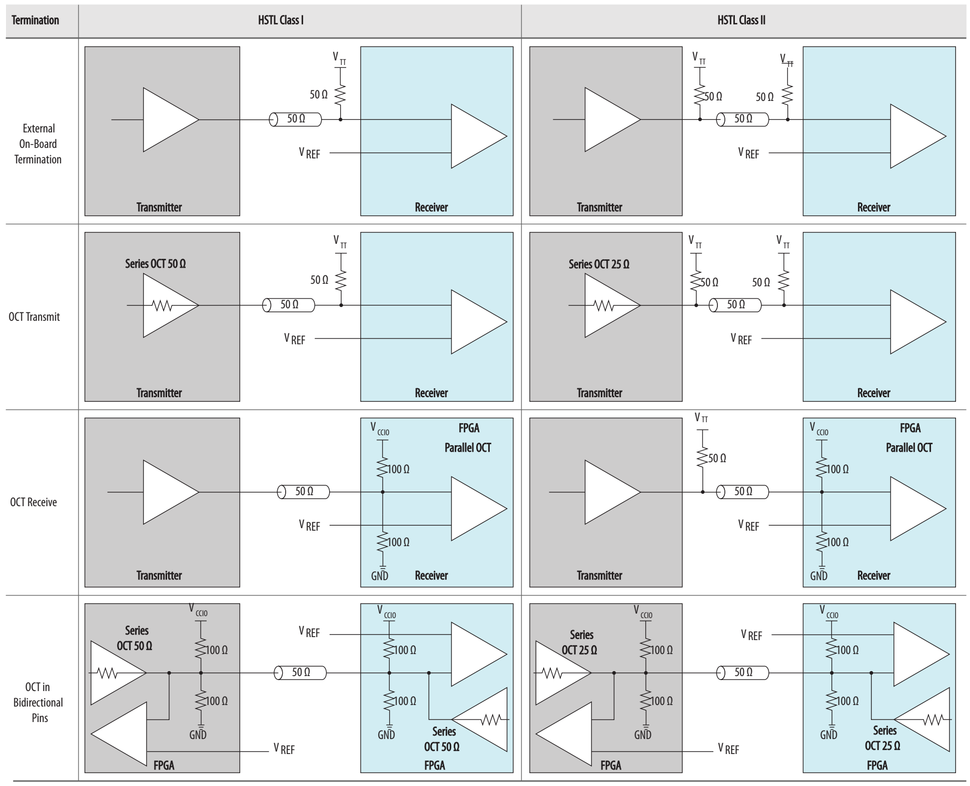
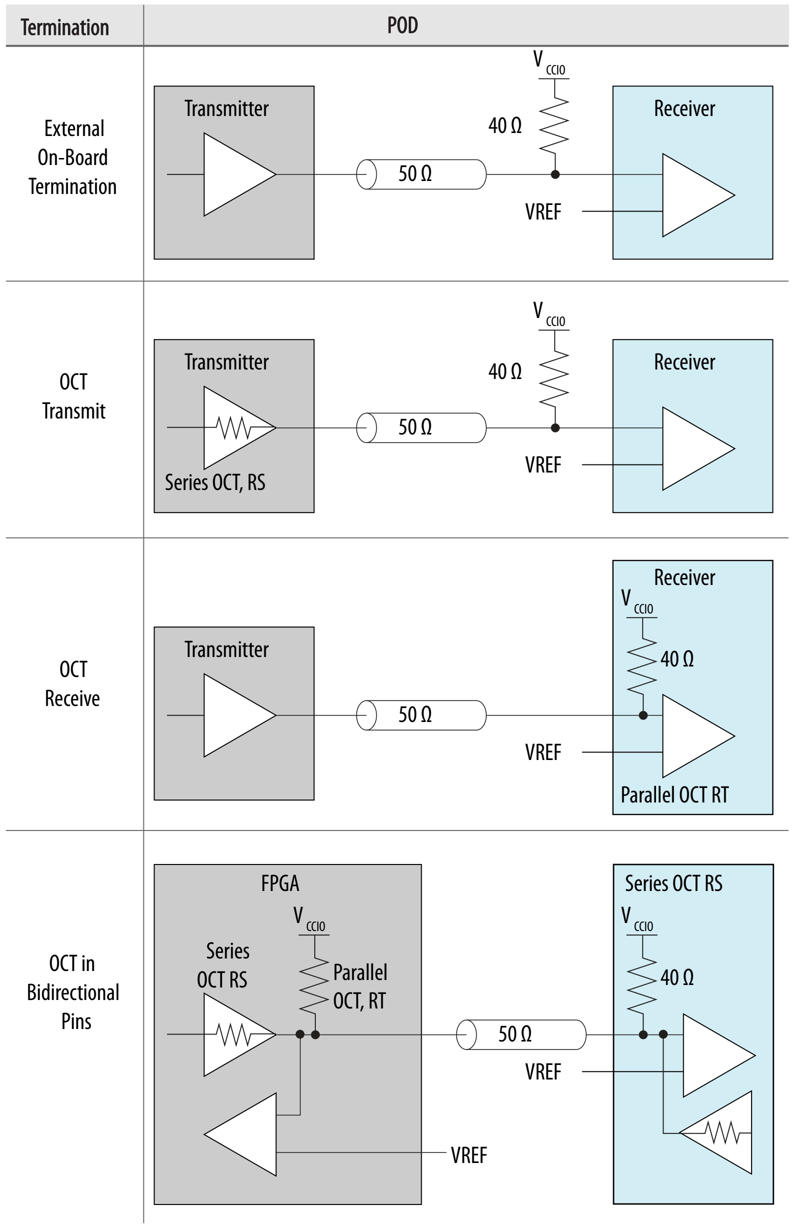


Figure 16. POD I/O Standard Termination

This figure shows the details of POD I/O termination on the Intel Stratix 10 devices.



Related Links

Dynamic OCT on page 36

2.5.2 Differential I/O Termination for Intel Stratix 10 Devices

The I/O pins are organized in pairs to support differential I/O standards. Each I/O pin pair can support differential input and output buffers.

The supported I/O standards such as Differential SSTL-12, Differential SSTL-15, Differential SSTL-125, and Differential SSTL-135 typically do not require external board termination.

Intel recommends that you use OCT with these I/O standards to save board space and cost. OCT reduces the number of external termination resistors used.

2.5.2.1 Differential HSTL, SSTL, HSUL, and POD Termination

Differential HSTL, SSTL, HSUL, and POD inputs use LVDS differential input buffers. However, R_D support is only available if the I/O standard is LVDS.

Differential HSTL, SSTL, HSUL, and POD outputs are not true differential outputs. These I/O standards use two single-ended outputs with the second output programmed as inverted.

Figure 17. Differential SSTL I/O Standard Termination

This figure shows the details of Differential SSTL I/O termination on Intel Stratix 10 devices.

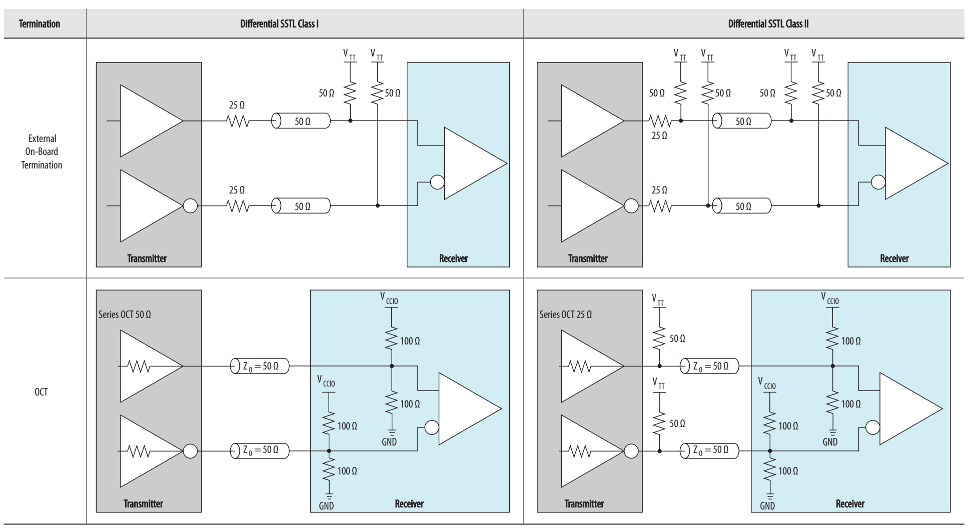


Figure 18. Differential HSTL I/O Standard Termination

This figure shows the details of Differential HSTL I/O standard termination on Intel Stratix 10 devices.

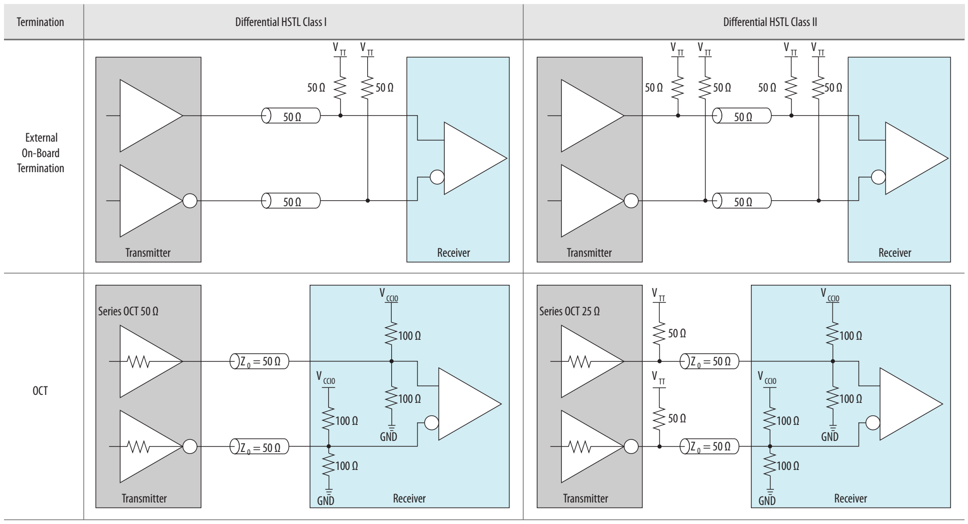
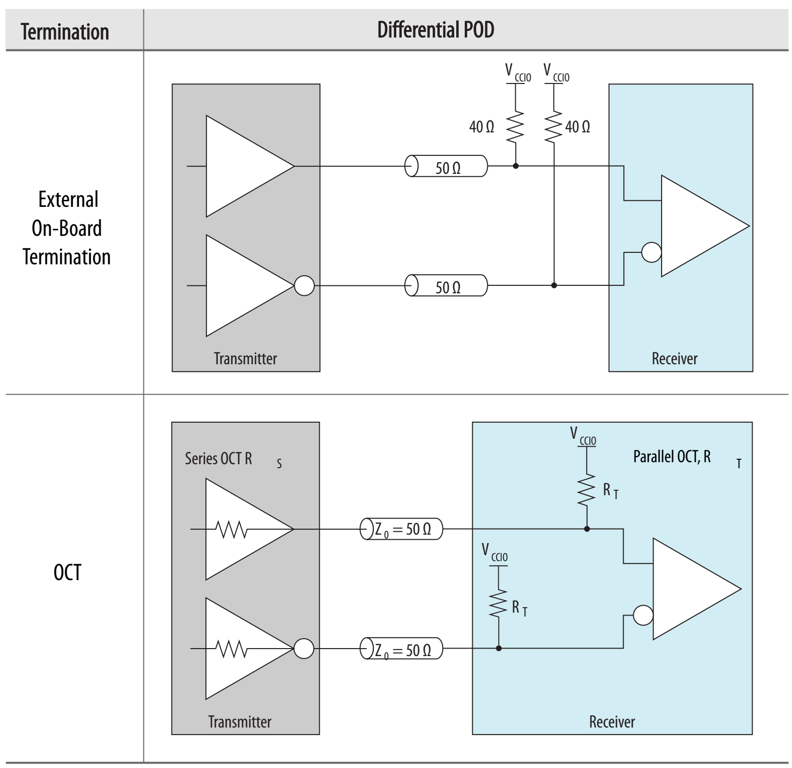


Figure 19. Differential POD I/O Standard Termination

This figure shows the details of Differential POD I/O termination on the Intel Stratix 10 devices.

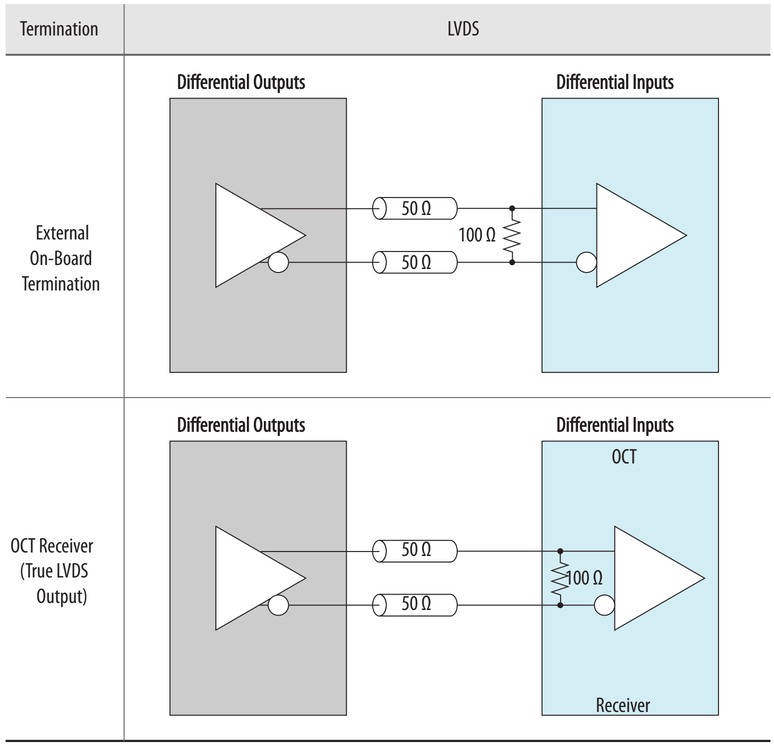


2.5.2.2 LVDS, RSDS, and Mini-LVDS Termination

All I/O banks have dedicated circuitry to support the true LVDS, RSDS, and mini-LVDS I/O standards by using true LVDS output buffers without resistor networks.

Figure 20. LVDS I/O Standard Termination

This figure shows the LVDS I/O standard termination. The on-chip differential resistor is available in all I/O banks.



2.5.2.3 LVPECL Termination

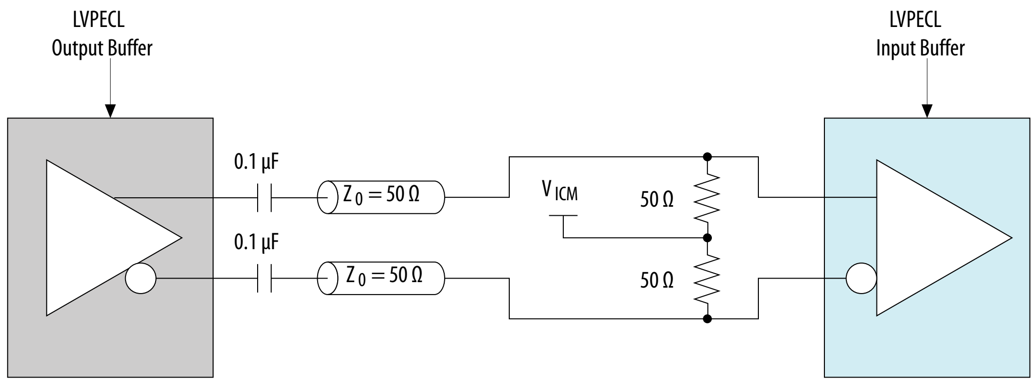
The Intel Stratix 10 devices support the LVPECL I/O standard on input clock pins only:

- LVPECL input operation is supported using LVDS input buffers.
- LVPECL output operation is not supported.

Use AC coupling if the LVPECL common-mode voltage of the output buffer does not match the LVPECL input common-mode voltage.

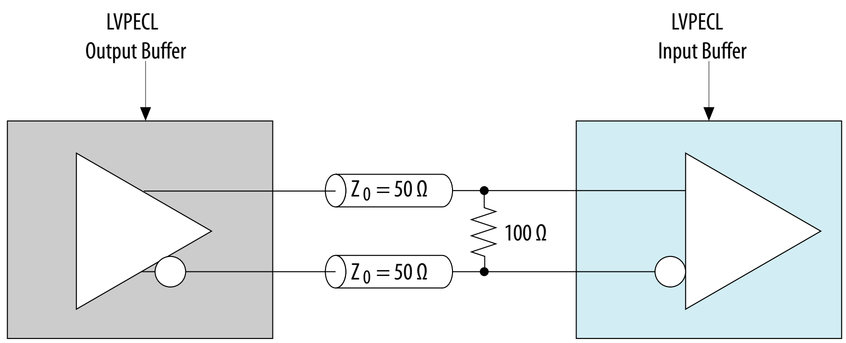
Note: Intel recommends that you use IBIS models to verify your LVPECL AC/DC-coupled termination.

Figure 21. LVPECL AC-Coupled Termination



Support for DC-coupled LVPECL is available if the LVPECL output common mode voltage is within the Intel Stratix 10 LVPECL input buffer specification.

Figure 22. LVPECL DC-Coupled Termination



For information about the V_{ICM} specification, refer to the device datasheet.

3 Intel Stratix 10 I/O Design Considerations

There are several considerations that require your attention to ensure the success of your designs. Unless noted otherwise, these design guidelines apply to all variants of this device family.

3.1 Guideline: V_{REF} Sources and VREF Pins

For Intel Stratix 10 devices, consider the following VREF pins guidelines:

- Intel Stratix 10 devices support internal and external V_{REF} sources.
  - There is an external VREF pin for every I/O bank, providing one external V_{REF} source for all I/Os in the same bank.
  - Each I/O lane in the bank also has its own internal V_{REF} generator. You can configure each I/O lane independently to use its internal V_{REF} or the I/O bank's external V_{REF} source. All I/O pins in the same I/O lane use the same V_{REF} source.
- You can use the internal V_{REF} with calibration to support DDR4 using the POD12 I/O standard.
- You can place any combination of input, output, or bidirectional pins near VREF pins. There is no VREF pin placement restriction.
- The VREF pins are dedicated for single-ended I/O standards. You cannot use the VREF pins as user I/Os.
- Connect unused VREF pins to VCCIO or GND.

For more information about pin capacitance of the VREF pins, refer to the device datasheet.

Related Links

- Intel Stratix 10 Device Datasheet
- Intel Stratix 10 Pin Connection Guidelines
- Pin-Out Files for Intel Stratix 10 Devices
  Provides the location of the V_{REF} and V_{CCIO} pins in different Intel Stratix 10 devices and packages.

3.2 Guideline: Observe Device Absolute Maximum Rating for 3.0 V Interfacing

To ensure device reliability and proper operation when you use the device for 3.0 V I/O interfacing, do not violate the absolute maximum ratings of the device. For more information about absolute maximum rating and maximum allowed overshoot during transitions, refer to the device datasheet.

Tip: Perform IBIS or SPICE simulations to make sure the overshoot and undershoot voltages are within the specifications.

Single-Ended Transmitter Application

If you use the Intel Stratix 10 device as a transmitter, use slow slew rate and series termination to limit the overshoot and undershoot at the I/O pins. Transmission line effects that cause large voltage deviations at the receiver are associated with an impedance mismatch between the driver and the transmission lines. By matching the impedance of the driver to the characteristic impedance of the transmission line, you can significantly reduce overshoot voltage. You can use a series termination resistor placed physically close to the driver to match the total driver impedance to the transmission line impedance.

Single-Ended Receiver Application

If you use the Intel Stratix 10 device as a receiver, use an external clamping diode to limit the overshoot and undershoot voltage at the I/O pins.

The 3.0 V I/O standard is supported using the bank supply voltage (V_{CCIO}) at 3.0 V and a V_{CCPT} voltage of 1.8 V. In this method, the clamping diode can sufficiently clamp overshoot voltage to within the DC and AC input voltage specifications. The clamped voltage is expressed as the sum of the V_{CCIO} and the diode forward voltage.

Related Links

- Intel FPGA IBIS Models
- SPICE Models for Intel FPGA Devices

3.3 Guideline: Voltage-Referenced and Non-Voltage Referenced I/O Standards

Each I/O bank can simultaneously support multiple I/O standards. Follow these guidelines if you use both non-voltage-referenced and voltage-referenced I/O standards in an I/O bank.

Non-Voltage-Referenced I/O Standards

An I/O bank can simultaneously support any number of input signals with different I/O standard assignments if the I/O standards support the V_{CCIO} level of the I/O bank.

For output signals, a single I/O bank supports non-voltage-referenced output signals that drive at the same voltage as V_{CCIO}. Because an I/O bank can only have one V_{CCIO} value, it can only drive out the value for non-voltage-referenced signals.

Voltage-Referenced I/O Standards

To accommodate voltage-referenced I/O standards:

- Each Intel Stratix 10 FPGA I/O bank contains a dedicated VREF pin.
- Each bank can have only a single V_{CCIO} voltage level and a single voltage reference (V_{REF}) level.

The voltage-referenced input buffer is powered by V_{CCPT}. Therefore, an I/O bank featuring single-ended or differential standards can support different voltage-referenced standards under the following conditions:

- The V_{REF} are the same levels.
- On-chip parallel termination (R_T OCT) is disabled.

If you enable R_T OCT, the voltage for the input standard and the V_{CCIO} of the bank must match.

This feature allows you to place voltage-referenced input signals in an I/O bank with a V_{CCIO} of 1.8 V or below. For example, you can place HSTL-15 input pins in an I/O bank with 1.8 V V_{CCIO}. However, the voltage-referenced input with R_T OCT enabled requires the V_{CCIO} of the I/O bank to match the voltage of the input standard. R_T OCT cannot be supported for the HSTL-15 I/O standard when V_{CCIO} is 1.8 V.

Voltage-referenced bidirectional and output signals must be the same as the V_{CCIO} voltage of the I/O bank. For example, you can place only SSTL-18 output pins in an I/O bank with a 1.8 V V_{CCIO}.

Mixing Voltage-Referenced and Non-Voltage Referenced I/O Standards

An I/O bank can support voltage-referenced and non-voltage-referenced pins by applying each of the rule sets individually.

Examples:

- An I/O bank can support SSTL-18 inputs and outputs, and 1.8 V inputs and outputs with a 1.8 V V_{CCIO} and a 0.9 V V_{REF}.
- An I/O bank can support 1.5 V standards, 1.8 V inputs (but not outputs), and 1.5 V HSTL I/O standards with a 1.5 V V_{CCIO} and 0.75 V V_{REF}.

3.4 Guideline: Do Not Drive I/O Pins During Power Sequencing

The Intel Stratix 10 I/O buffers are powered by V_{CC}, V_{CCPT}, and V_{CCIO}.

Because the Intel Stratix 10 devices do not support hot socketing, do not drive the I/O pins externally during power up and power down. This includes all I/O pins including FPGA and HPS I/Os. Adhere to this guideline to:

- Avoid excess I/O pin current:
  - Excess I/O pin current affects the device's lifetime and reliability.
  - Excess current on the 3 V I/O pins can damage the Intel Stratix 10 device.
- Achieve minimum current draw and avoid I/O glitch during power up or power down.
- Avoid permanent damage on the 3 V I/O buffers in 3 V operation.

Related Links

Power-Up and Power-Down Sequences, Intel Stratix 10 Power Management User Guide

3.5 Guideline: Maximum DC Current Restrictions

There are no restrictions on the maximum DC current of any 10 consecutive I/O pins for Intel Stratix 10 devices.

Intel Stratix 10 devices conform to the V_{CCIO} Electro-Migration (EM) rule and IR drop targets for all I/O standard drive strength settings—ensuring reliability over the lifetime of the devices.

4 Intel Stratix 10 I/O Implementation Guides

You can implement your I/O design in the Intel Quartus Prime software. The software contains tools for you to create and compile your design, and configure your device.

The Intel Quartus Prime software allows you to prepare for device migration, set pin assignments, define placement restrictions, setup timing constraints, and customize IP cores. For more information about using the software, refer to the related information.

Related Links

- Intel Quartus Prime Design Software
  Provides more information about using Intel Quartus Prime software.
- IP Migration to the Intel FPGA GPIO IP Core on page 64
- Introduction to Intel FPGA IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- Creating Version-Independent IP and Qsys Simulation Scripts
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- Project Management Best Practices
  Guidelines for efficient management and portability of your project and IP files.

4.1 Intel FPGA GPIO IP Core

The Intel FPGA GPIO IP core supports the GPIO components and features of the Intel Stratix 10 device family. You can use the Intel Quartus Prime parameter editor to configure the Intel FPGA GPIO IP core.

Components of the Intel FPGA GPIO IP core:

- Double data rate input/output (DDIO)—doubles or halves the data-rate of a communication channel
- Delay chains—configure the delay chains to perform specific delay and assist in I/O timing closure
- I/O buffers—connect the pads to the FPGA

Note: The 3 V I/O banks in Intel Stratix 10 devices do not support the DDIO feature of the Intel FPGA GPIO IP core. Bypass the DDIO if you use an I/O standard supported only by 3 V I/O banks, such as 3.0 V LVCMOS. To bypass the DDIO feature, set the **Register mode** of the Intel FPGA GPIO IP core to **none**.

4.1.1 Intel FPGA GPIO IP Core Data Paths

Figure 23. High-Level View of Single-Ended GPIO

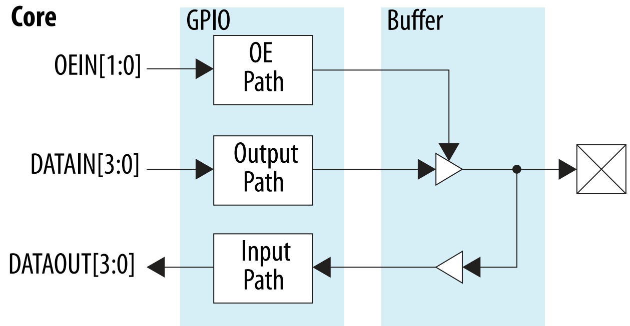


Table 24. Intel FPGA GPIO Data Path Modes

Data Path	Register Mode			
	Bypass	Simple Register	DDR I/O	
			Full-Rate	Half-Rate
Input	Data goes from the delay element to the core, bypassing all double data rate I/Os (DDIOs).	The full-rate DDIO operates as a simple register, bypassing half-rate DDIOs. The Fitter chooses whether to pack the register in the I/O or implement the register in the core, depending on the area and timing trade-offs.	The full-rate DDIO operates as a regular DDIO, bypassing the half-rate DDIOs.	The full-rate DDIO operates as a regular DDIO. The half-rate DDIOs convert full-rate data to half-rate data.
Output	Data goes from the core straight to the delay element, bypassing all DDIOs.	The full-rate DDIO operates as a simple register, bypassing half-rate DDIOs. The Fitter chooses whether to pack the register in the I/O or implement the register in the core, depending on the area and timing trade-offs.	The full-rate DDIO operates as a regular DDIO, bypassing the half-rate DDIOs.	The full-rate DDIO operates as a regular DDIO. The half-rate DDIOs convert full-rate data to half-rate data.
Bidirectional	The output buffer drives both an output pin and an input buffer.	The full-rate DDIO operates as a simple register. The output buffer drives both an output pin and an input buffer.	The full-rate DDIO operates as a regular DDIO. The output buffer drives both an output pin and an input buffer. The input buffer drives a set of three flip-flops.	The full-rate DDIO operates as a regular DDIO. The half-rate DDIOs convert full-rate data to half-rate. The output buffer drives both an output pin and an input buffer. The input buffer drives a set of three flip-flops.

If you use asynchronous clear and preset signals, all DDIOs share these same signals.

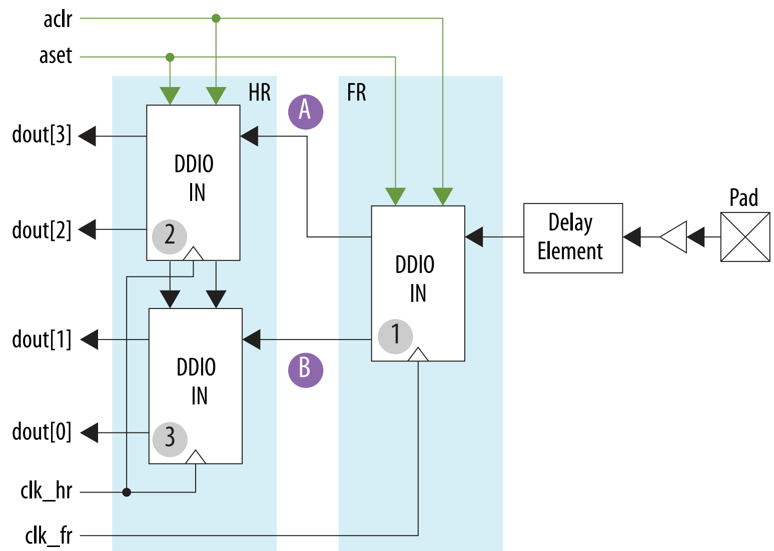
Half-rate and full-rate DDIOs connect to separate clocks. When you use half-rate and full-rate DDIOs, the full-rate clock must run at twice the half-rate frequency. You can use different phase relationships to meet timing requirements.

4.1.1.1 Input Path

The pad sends data to the input buffer, and the input buffer feeds the delay element. After the data goes to the output of the delay element, the programmable bypass multiplexers select the features and paths to use.Each LVDS I/O input path contains two stages of DDIOs, which are full-rate and half-rate.

The 3 V I/Os do not support DDIOs.

Figure 24. Simplified View of Single-Ended GPIO Input Path

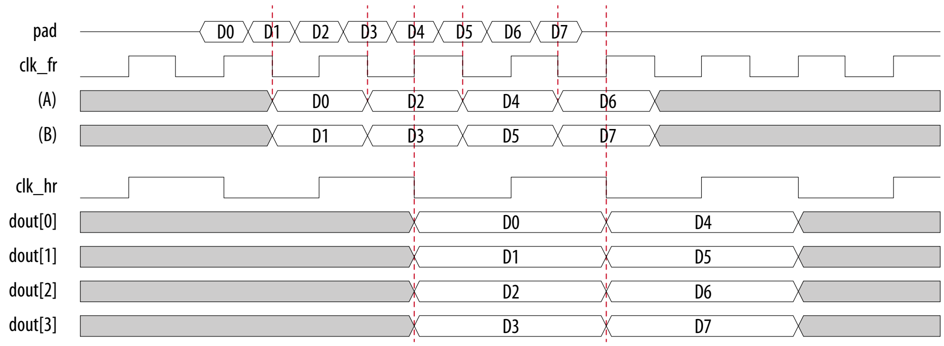


1. The pad receives data.
2. DDIO IN (1) captures data on the rising and falling edges of `clk_fr` and sends the data, signals (A) and (B) in the following waveform figure, at single data rate.
3. DDIO IN (2) and DDIO IN (3) halve the data rate.
4. `dout[3:0]` presents the data as a half-rate bus.

Figure 25. Input Path Waveform in DDIO Mode with Half-Rate Conversion

In this figure, the data goes from full-rate clock at double data rate to half-rate clock at single data rate. The data rate is divided by four and the bus size is increased by the same ratio. The overall throughput through the Intel FPGA GPIO IP core remains unchanged.

The actual timing relationship between different signals may vary depending on the specific design, delays, and phases that you choose for the full-rate and half-rate clocks.



Note: The Intel FPGA GPIO IP core does not support dynamic calibration of the input path. For applications that require dynamic calibration of the input path, refer to the related information.

Related Links

Intel FPGA PHYLite for Parallel Interfaces IP Core User Guide
Provides more information for applications that require dynamic calibration of the input path.

4.1.1.2 Output and Output Enable Paths

The output delay element sends data to the pad through the output buffer.

Each LVDS I/O output path contains two stages of DDIOs, which are half-rate and full-rate.

The 3 V I/Os do not support DDIOs.

Figure 26. Simplified View of Single-Ended GPIO Output Path

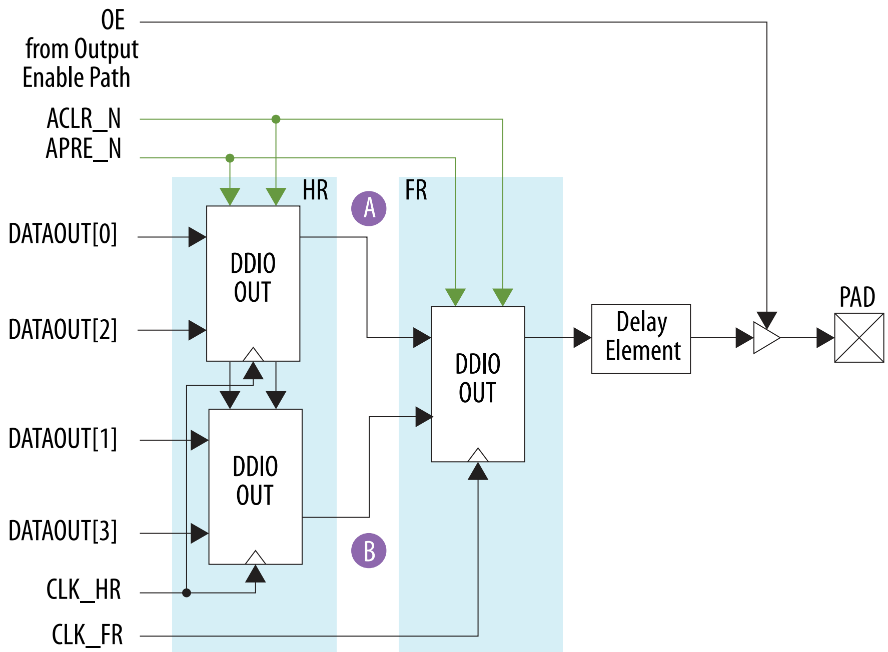


Figure 27. Output Path Waveform in DDIO Mode with Half-Rate Conversion

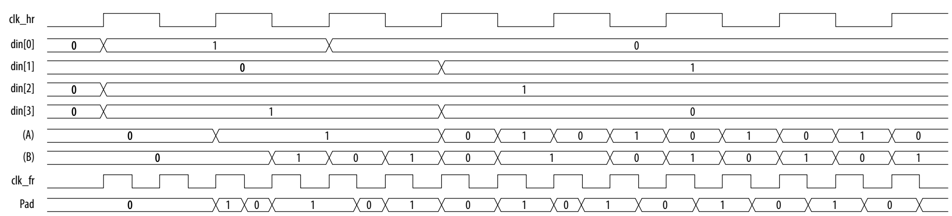
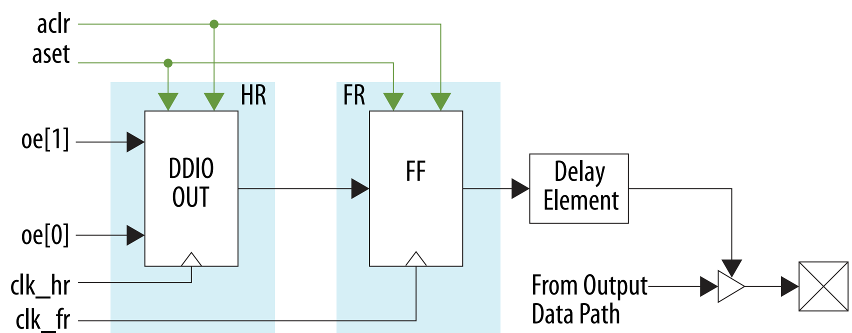


Figure 28. Simplified View of Output Enable Path



The difference between the output path and output enable (OE) path is that the OE path does not contain full-rate DDIO. To support packed-register implementations in the OE path, a simple register operates as full-rate DDIO. For the same reason, only one half-rate DDIO is present.

The OE path operates in the following three fundamental modes:

- Bypass—the core sends data directly to the delay element, bypassing all DDIOs.
- Packed Register—bypasses half-rate DDIO.
- SDR output at half-rate—half-rate DDIOs convert data from full-rate to half-rate.

In Intel Stratix 10 devices, each 3 V I/O bank supports only two output enables (OE) for its eight single-ended I/Os.

Note: The Intel FPGA GPIO IP core does not support dynamic calibration of the output path. For applications that require dynamic calibration of the output path, refer to related information.

Related Links

- Intel FPGA PHYLite for Parallel Interfaces IP Core User Guide
  Provides more information for applications that require dynamic calibration of the output path.
- Input Path on page 53

4.1.2 Register Packing

The Intel FPGA GPIO IP core allows you to pack register into the periphery to save area and resource utilization.

You can configure the full-rate DDIO on the input and output path as a flip flop. To do so, add the `.qsf` assignments listed in this table.

Table 25. Register Packing QSF Assignments

Path	QSF Assignment
Input register packing	`set_instance_assignment -name FAST_INPUT_REGISTER ON -to` *<path to register>*
Output register packing	`set_instance_assignment -name FAST_OUTPUT_REGISTER ON -to` *<path to register>*
Output enable register packing	`set_instance_assignment -name FAST_OUTPUT_ENABLE_REGISTER ON -to` *<path to register>*

Note: These assignments do not guarantee register packing. However, these assignments enable the Fitter to find a legal placement. Otherwise, the Fitter will keep the flip flop in the core.

4.2 Verifying Resource Utilization and Design Performance

You can refer to the Intel Quartus Prime compilation reports to get details about the resource usage and performance of your design.

1. On the menu, click **Processing ➤ Start Compilation** to run a full compilation.
2. After compiling the design, click **Processing ➤ Compilation Report**.
3. Using the **Table of Contents**, navigate to **Fitter ➤ Resource Section**.
   a. To view the resource usage information, select **Resource Usage Summary**.

b. To view the resource utilization information, select **Resource Utilization by Entity**.

4.3 Intel FPGA GPIO Timing

The performance of the Intel FPGA GPIO IP core depends on the I/O constraints and clock phases. To validate the timing for your Intel FPGA GPIO configuration, Intel recommends that you use the Timing Analyzer.

Related Links

The Intel Quartus Prime Timing Analyzer

4.3.1 Timing Components

The Intel FPGA GPIO IP core timing components consist of three paths.

- I/O interface paths—from the FPGA to external receiving devices and from external transmitting devices to the FPGA.
- Core interface paths of data and clock—from the I/O to the core and from the core to I/O.
- Transfer paths—from half-rate to full-rate DDIO, and from full-rate to half-rate DDIO.

Note: The Timing Analyzer treats the path inside the DDIO_IN and DDIO_OUT blocks as black boxes.

Figure 29. Input Path Timing Components

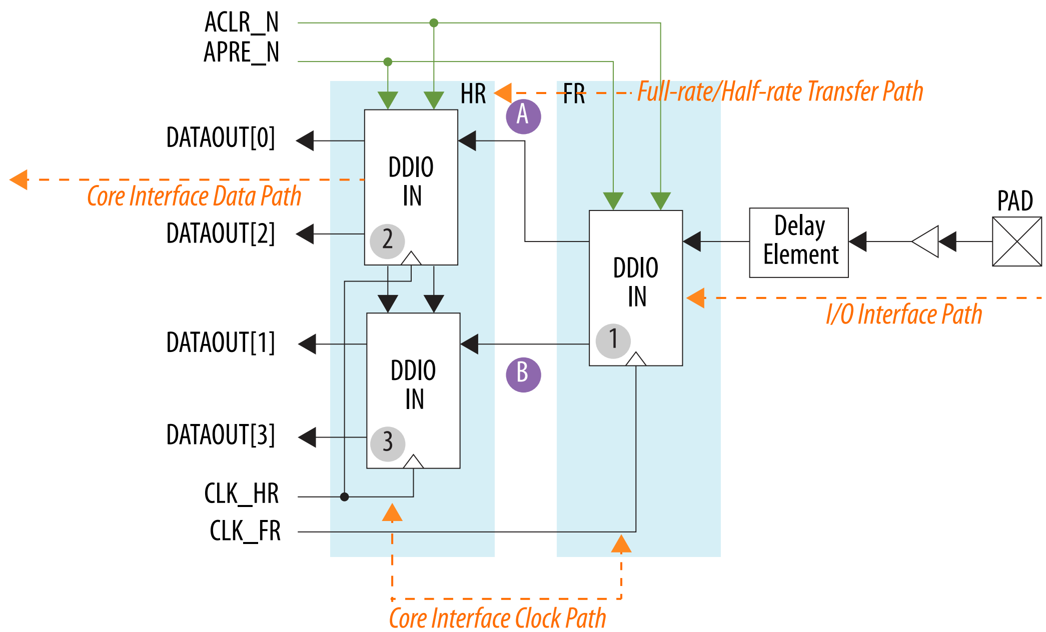


Figure 30. Output Path Timing Components

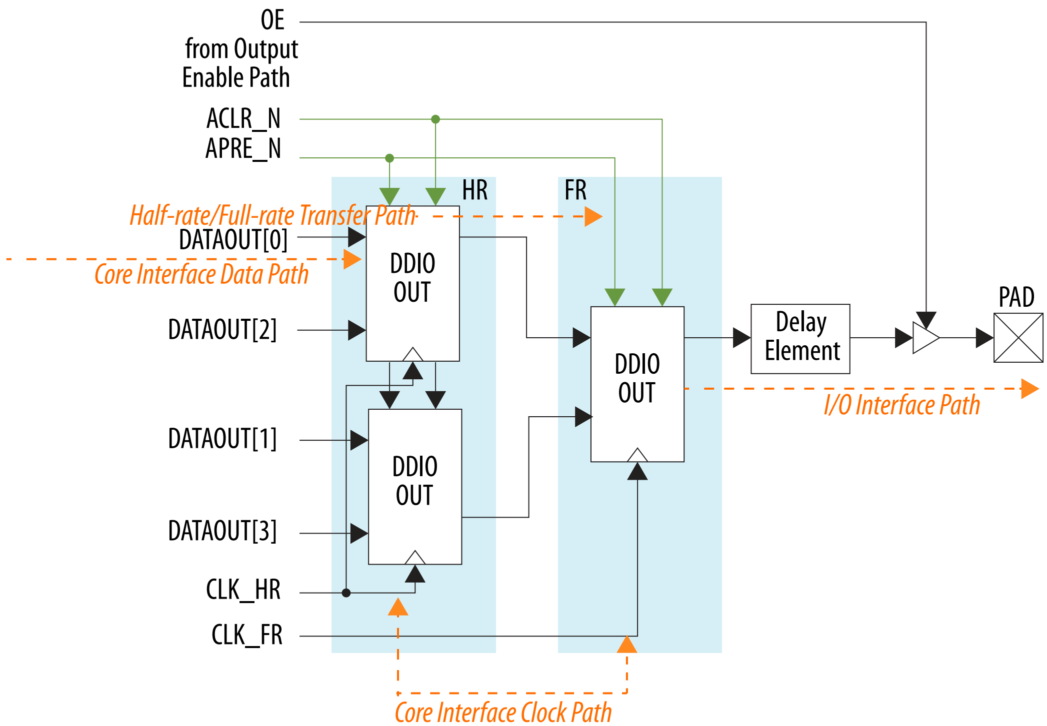
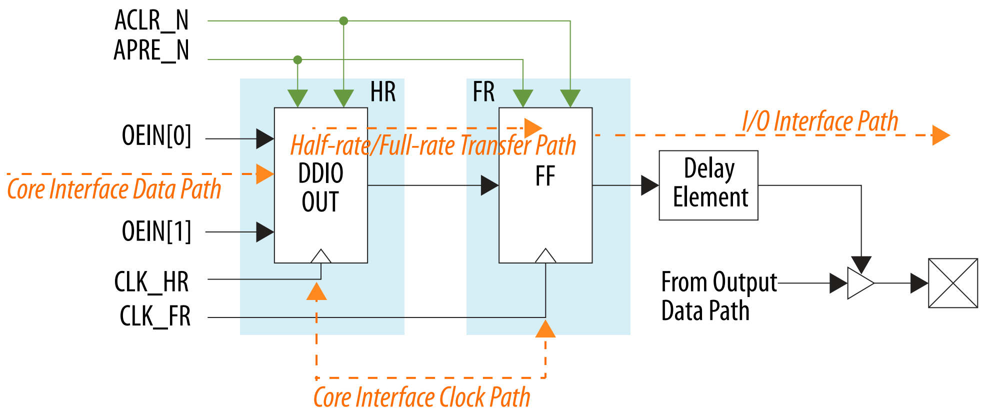


Figure 31. Output Enable Path Timing Components



4.3.2 Delay Elements

The Intel Quartus Prime software does not automatically set delay elements to maximize slack in the I/O timing analysis. To close the timing or maximize slack, set the delay elements manually in the Intel Quartus Prime settings file (.qsf).

Table 26. Delay Elements .qsf Assignments

Specify these assignments in the .qsf to access the delay elements.

Delay Element	.qsf Assignment
Input Delay Element	set_intance_assignment -to <PIN> -name INPUT_DELAY_CHAIN <0..63>
Output Delay Element	set_intance_assignment -to <PIN> -name OUTPUT_DELAY_CHAIN <0..15>
Output Enable Delay Element	set_intance_assignment -to <PIN> -name OE_DELAY_CHAIN <0..15>

4.3.3 Timing Analysis

The Intel Quartus Prime software does not automatically generate the SDC timing constraints for the Intel FPGA GPIO IP core. You must manually enter the timing constraints.

Follow the timing guidelines and examples to ensure that the Timing Analyzer analyzes the I/O timing correctly.

- To perform proper timing analysis for the I/O interface paths, specify the system level constraints of the data pins against the system clock pin in the .sdc file.
- To perform proper timing analysis for the core interface paths, define these clock settings in the .sdc file:
  - — Clock to the core registers
  - — Clock to the I/O registers for the simple register and DDIO modes

Related Links

AN 433: Constraining and Analyzing Source-Synchronous Interfaces
Describes techniques for constraining and analyzing source-synchronous interfaces.

4.3.3.1 Single Data Rate Input Register

Figure 32. Single Data Rate Input Register

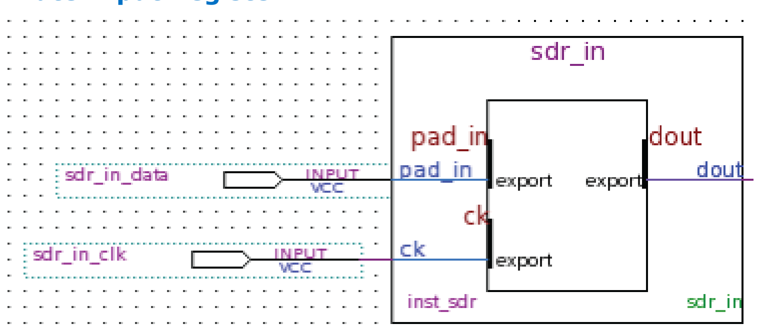


Table 27. Single Data Rate Input Register .sdc Command Examples

Command	Command Example	Description
create_clock	create_clock -name sdr_in_clk -period "100 MHz" sdr_in_clk	Creates clock setting for the input clock.
set_input_delay	set_input_delay -clock sdr_in_clk 0.15 sdr_in_data	Instructs the Timing Analyzer to analyze the timing of the input I/O with a 0.15 ns input delay.

4.3.3.2 Full-Rate or Half-Rate DDIO Input Register

The input side of the full-rate and half-rate DDIO input registers are the same. You can properly constrain the system by using a virtual clock to model the off-chip transmitter to the FPGA.

Figure 33. Full-Rate or Half-Rate DDIO Input Register

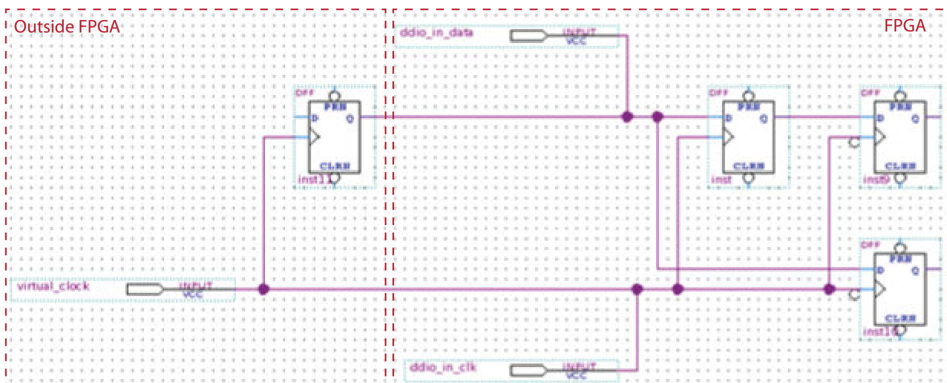


Table 28. Full-Rate or Half-Rate DDIO Input Register .sdc Command Examples

Command	Command Example	Description
create_clock	create_clock -name virtual_clock -period "200 MHz" create_clock -name ddio_in_clk -period "200 MHz" ddio_in_clk	Create clock setting for the virtual clock and the DDIO clock.
set_input_delay	set_input_delay -clock virtual_clock 0.25 ddio_in_data set_input_delay -add_delay -clock_fall -clock virtual_clock 0.25 ddio_in_data	Instruct the Timing Analyzer to analyze the positive clock edge and the negative clock edge of the transfer. Note the -add_delay in the second set_input_delay command.
set_false_path	set_false_path -fall_from virtual_clock -rise_to ddio_in_clk set_false_path -rise_from virtual_clock -fall_to ddio_in_clk	Instruct the Timing Analyzer to ignore the positive clock edge to the negative edge triggered register, and the negative clock edge to the positive edge triggered register. *Note:* The CLK_HR frequency must be half the CLK_FR frequency. If the I/O PLL drives the clocks, you can consider using the derive_pll_clocks .sdc command.

4.3.3.3 Single Data Rate Output Register

Figure 34. Single Data Rate Output Register

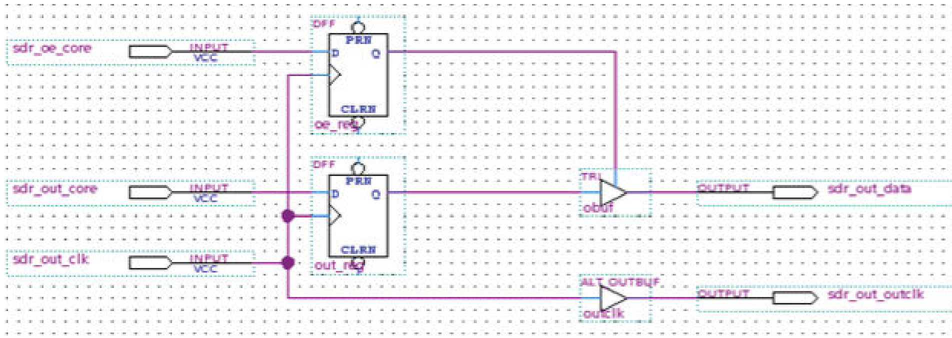


Table 29. Single Data Rate Output Register .sdc Command Examples

Command	Command Example	Description
create_clock and create_generated_clock	create_clock -name sdr_out_clk -period "100 MHz" sdr_out_clk create_generated_clock -source sdr_out_clk -name sdr_out_outclk sdr_out_outclk	Generate the source clock and the output clock to transmit.
set_output_delay	set_output_delay -clock sdr_out_clk 0.45 sdr_out_data	Instructs the Timing Analyzer to analyze the output data to transmit against the output clock to transmit.

4.3.3.4 Full-Rate or Half-Rate DDIO Output Register

The output side of the full-rate and half-rate DDIO output registers are the same.

Table 30. DDIO Output Register .sdc Command Examples

Command	Command Example	Description
create_clock and create_generated_clock	create_clock -name ddio_out_fr_clk -period "200 MHz" ddio_out_fr_clk create_generated_clock -source ddio_out_fr_clk -name ddio_out_fr_outclk ddio_out_fr_outclk	Generate the clocks to the DDIO and the clock to transmit.
set_output_delay	set_output_delay -clock ddio_out_fr_outclk 0.55 ddio_out_fr_data set_output_delay -add_delay -clock_fall -clock ddio_out_fr_outclk 0.55 ddio_out_fr_data	Instruct the Timing Analyzer to analyze the positive and negative data against the output clock.
set_false_path	set_false_path -rise_from ddio_out_fr_clk -fall_to ddio_out_fr_outclk set_false_path -fall_from ddio_out_fr_clk -rise_to ddio_out_fr_outclk	Instruct the Timing Analyzer to ignore the rising edge of the source clock against the falling edge of the output clock, and the falling edge of source clock against rising edge of output clock

4.3.4 Timing Closure Guidelines

For the Intel FPGA GPIO input registers, the input I/O transfer is likely to fail the hold time if you do not set the input delay chain. This failure is caused by the clock delay being larger than the data delay.

To meet the hold time, add delay to the input data path using the input delay chain. In general, the input delay chain is around 30 ps per step at the –1 speed grade. To get an approximate input delay chain setting to pass the timing, divide the negative hold slack by 60 ps.

However, if the I/O PLL drives the clocks of the GPIO input registers (simple register or DDIO mode), you can set the compensation mode to source synchronous mode. The Fitter will attempt to configure the I/O PLL for a better setup and hold slack for the input I/O timing analysis.

For the Intel FPGA GPIO output and output enable registers, you can add delay to the output data and clock using the output and output enable delay chains.

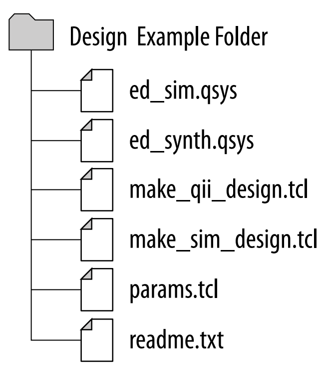
- If you observe setup time violation, you can increase the output clock delay chain setting.
- If you observe hold time violation, you can increase the output data delay chain setting.

4.4 Intel FPGA GPIO IP Core Design Examples

The Intel FPGA GPIO IP core can generate design examples that match your IP configuration in the parameter editor. You can use these design examples as references for instantiating the IP core and the expected behavior in simulations.

You can generate the design examples from the Intel FPGA GPIO IP core parameter editor. After you have set the parameters that you want, click **Generate Example Design**. The IP core generates the design example source files in the directory you specify.

Figure 35. Source Files in the Generated Design Example Directory



Note: The `.qsys` files are for internal use during design example generation only. You cannot edit these `.qsys` files.

4.4.1 Intel FPGA GPIO Synthesizable Intel Quartus Prime Design Example

The synthesizable design example is a compilation-ready Platform Designer system that you can include in an Intel Quartus Prime project.

Generating and Using the Design Example

To generate the synthesizable Intel Quartus Prime design example from the source files, run the following command in the design example directory:

```
quartus_sh -t make_qii_design.tcl
```

To specify an exact device to use, run the following command:

```
quartus_sh -t make_qii_design.tcl [device_name]
```

The TCL script creates a `qii` directory that contains the `ed_synth.qpf` project file. You can open and compile this project in the Intel Quartus Prime software.

4.4.2 Intel FPGA GPIO IP Core Simulation Design Example

The simulation design example uses your Intel FPGA GPIO IP core parameter settings to build the IP instance connected to a simulation driver. The driver generates random traffic and internally checks the legality of the out going data.

Using the design example, you can run a simulation using a single command, depending on the simulator that you use. The simulation demonstrates how you can use the Intel FPGA GPIO IP core.

Generating and Using the Design Example

To generate the simulation design example from the source files for a Verilog simulator, run the following command in the design example directory:

```
quartus_sh -t make_sim_design.tcl
```

To generate the simulation design example from the source files for a VHDL simulator, run the following command in the design example directory:

```
quartus_sh -t make_sim_design.tcl VHDL
```

The TCL script creates a `sim` directory that contains subdirectories—one for each supported simulation tool. You can find the scripts for each simulation tool in the corresponding directories.

4.5 Verifying Pin Migration Compatibility

You can use the **Pin Migration View** window in the Intel Quartus Prime software Pin Planner to assist you in verifying whether your pin assignments migrate to a different device successfully. You can vertically migrate to a device with a different density while using the same device package, or migrate between packages with different densities and ball counts.

1. Open **Assignments ➤ Pin Planner** and create pin assignments.
2. If necessary, perform one of the following options to populate the Pin Planner with the node names in the design:

- — Analysis & Elaboration
- — Analysis & Synthesis
- — Fully compile the design

3. Then, on the menu, click **View ➤ Pin Migration View**.
4. To select or change migration devices:
   a. Click **Device** to open the **Device** dialog box.
   b. Under **Migration compatibility** click **Migration Devices**.
5. To show more information about the pins:
   a. Right-click anywhere in the **Pin Migration View** window and select **Show Columns**.
   b. Then, click the pin feature you want to display.
6. If you want to view only the pins, in at least one migration device, that have a different feature than the corresponding pin in the migration result, turn on **Show migration differences**.
7. Click **Pin Finder** to open the **Pin Finder** dialog box to find and highlight pins with specific functionality.

   If you want to view only the pins highlighted by the most recent query in the **Pin Finder** dialog box, turn on **Show only highlighted pins**.
8. To export the pin migration information to a Comma-Separated Value file (**.csv**), click **Export**.

Related Links

Intel Quartus Prime Design Software
Provides more information about using Intel Quartus Prime software.

4.6 IP Migration to the Intel FPGA GPIO IP Core

The Intel FPGA GPIO IP core can migrate your GPIO IPs from previous devices to work in Intel Stratix 10 designs.

Depending on the mode you use in your previous IP, the IP migration tool can automatically configure the new Intel FPGA GPIO IP core based on settings in your previous IP. For unsupported modes, you can use the Intel FPGA GPIO IP core parameter editor to manually configure the migrated IP core.

4.6.1 Migrating Your ALTDDIO_IN, ALTDDIO_OUT, ALTDDIO_BIDIR, and ALTIOBUF IP Cores

To migrate your ALTDDIO_IN, ALTDDIO_OUT, ALTDDIO_BIDIR, and ALTIOBUF IP cores to the Intel FPGA GPIO IP core, follow these steps:

1. Open your ALTDDIO_IN, ALTDDIO_OUT, ALTDDIO_BIDIR, or ALTIOBUF IP core in the IP Parameter Editor.
2. In the **Currently selected device family**, select **Stratix 10**.
3. Click **Finish** to open the Intel FPGA GPIO IP Parameter Editor.

The IP Parameter Editor configures the Intel FPGA GPIO IP core settings similar to the ALTDDIO_IN, ALTDDIO_OUT, ALTDDIO_BIDIR, or ALTIOBUF IP core settings.

4. If there are any incompatible settings between the two, select **new supported settings**.
5. Click **Finish** to regenerate the IP core.
6. Replace your ALTDDIO_IN, ALTDDIO_OUT, ALTDDIO_BIDIR, or ALTIOBUF IP core instantiation in RTL with the Intel FPGA GPIO IP core.

Note: The Intel FPGA GPIO IP core port names may not match the ALTDDIO_IN, ALTDDIO_OUT, ALTDDIO_BIDIR, or ALTIOBUF IP core port names. Therefore, simply changing the IP core name in the instantiation may not be sufficient.

4.6.2 Guideline: Swap `datain_h` and `datain_l` Ports in Migrated IP

When you migrate your GPIO IP to the Intel FPGA GPIO IP core, you can turn on **Use legacy top-level port names** option in the Intel FPGA GPIO IP core parameter editor. However, the behavior of these ports in the Intel FPGA GPIO IP core is different than in the IP cores used for the Stratix V, Arria V, and Cyclone V devices.

The Intel FPGA GPIO IP core drives these ports to the output registers on these clock edges:

- `datain_h`—on the falling edge of `outclock`
- `datain_l`—on the rising edge of `outclock`

If you migrated your GPIO IP from Stratix V, Arria V, and Cyclone V devices, swap the `datain_h` and `datain_l` ports when you instantiate the IP generated by the Intel FPGA GPIO IP core.

5 Intel FPGA GPIO IP Core Reference

You can set various parameter settings for the Intel FPGA GPIO IP core to customize its behaviors, ports, and signals.

The Intel Quartus Prime software generates your customized Intel FPGA GPIO IP core according to the parameter options that you set in the parameter editor.

5.1 Intel FPGA GPIO Parameter Settings

You can set the parameter settings for the Intel FPGA GPIO IP core in the Intel Quartus Prime software. There are three groups of options: **General**, **Buffer**, and **Registers**.

Table 31. Intel FPGA GPIO Parameters - General

Parameter	Condition	Allowed Values	Description
Data Direction	—	• Input • Output • Bidir	Specifies the data direction for the GPIO.
Data width	—	1 to 128	Specifies the data width.
Use legacy top-level port names	—	• On • Off	Use same port names as in Stratix V, Arria V, and Cyclone V devices. For example, `dout` becomes `dataout_h` and `dataout_l`, and `din` becomes `datain_h` and `datain_l`. *Note:* The behavior of these ports are different than in the Stratix V, Arria V, and Cyclone V devices. For the migration guideline, refer to the related information.

Table 32. Intel FPGA GPIO Parameters - Buffer

Parameter	Condition	Allowed Values	Description
Use differential buffer	—	• On • Off	If turned on, enables differential I/O buffers.
Use pseudo differential buffer	• Data Direction = Output • Use differential buffer = On	• On • Off	If turned on in output mode, enables pseudo differential output buffers. This option is automatically turned on for bidirectional mode if you turn on **Use differential buffer**.
Use bus-hold circuitry	• Data Direction = Input or Bidir • Use differential buffer = Off	• On • Off	If turned on, the bus hold circuitry can weakly hold the signal on an I/O pin at its last-driven state where the output buffer state will be 1 or 0 but not high-impedance.

continued...

Parameter	Condition	Allowed Values	Description
Use open drain output	• Data Direction = Output or Bidir • Use differential buffer = Off	• On • Off	If turned on, the open drain output enables the device to provide system-level control signals such as interrupt and write enable signals that can be asserted by multiple devices in your system.
Enable output enable port	Data Direction = Output	• On • Off	If turned on, enables user input to the OE port. This option is automatically turned on for bidirectional mode. In Intel Stratix 10 devices, each 3 V I/O bank supports only two output enables (OE) for its eight single-ended I/Os.
Enable seriestermination / paralleltermination ports	—	• On • Off	If turned on, enables the `seriesterminationcontrol` and `parallelterminationcontrol` ports of the output buffer.

Table 33. Intel FPGA GPIO Parameters - Registers

Parameter	Condition	Allowed Values	Description
Register mode	—	• None • Simple register • DDIO	Specifies the register mode for the Intel FPGA GPIO IP core: • **None**—specifies a simple wire connection from/to the buffer. • **Simple register**—specifies that the DDIO is used as a simple register in single data-rate mode (SDR). The Fitter may pack this register in the I/O. • **DDIO**— specifies that the IP core uses the DDIO. If you use an I/O standard supported only by the 3 V I/O banks, select **None**.
Enable synchronous clear / preset port	• Register mode = DDIO	• None • Clear • Preset	Specifies how to implement synchronous reset port. • **None**—Disables synchronous reset port. • **Clear**—Enables the SCLR port for synchronous clears. • **Preset**—Enables the SSET port for synchronous preset.
Enable asynchronous clear / preset port	• Register mode = DDIO	• None • Clear • Preset	Specifies how to implement asynchronous reset port. • **None**—Disables asynchronous reset port. • **Clear**—Enables the ACLR port for asynchronous clears. • **Preset**—Enables the ASET port for asynchronous preset. ACLR and ASET signals are active high.

continued...

Parameter	Condition	Allowed Values	Description
Enable clock enable ports	Register mode = DDIO	• On • Off	• **On**—exposes the clock enable (CKE) port to allow you to control when data is clocked in or out. This signal prevents data from being passed through without your control. • **Off**—clock enable port is not exposed and data always pass through the register automatically.
Half Rate logic	Register mode = DDIO	• On • Off	If turned on, enables half-rate DDIO.
Separate input / output Clocks	• Data Direction = Bidir • Register mode = Simple register or DDIO	• On • Off	If turned on, enables separate clocks (CK_IN and CK_OUT) for the input and output paths in bidirectional mode.

Related Links

Guideline: Swap datain_h and datain_l Ports in Migrated IP on page 65

5.2 Intel FPGA GPIO Interface Signals

Depending on parameter settings you specify, different interface signals are available for the Intel FPGA GPIO IP core.

Figure 36. Intel FPGA GPIO IP Core Interfaces

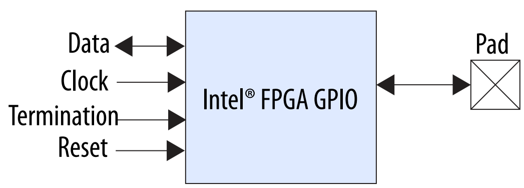


Figure 37. Intel FPGA GPIO Interface Signals

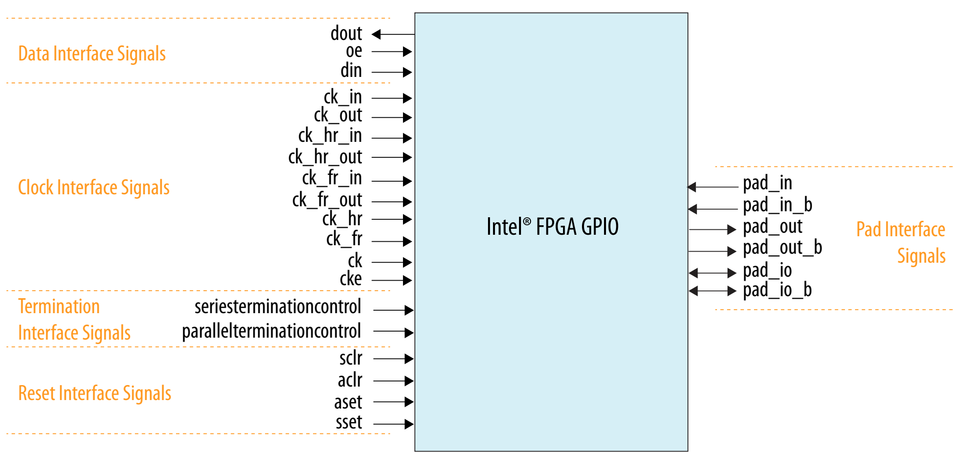


Table 34. Pad Interface Signals

The pad interface is the physical connection from the Intel FPGA GPIO IP core to the pad. This interface can be an input, output or bidirectional interface, depending on the IP core configuration. In this table, *SIZE* is the data width specified in the IP core parameter editor.

Signal Name	Direction	Description
`pad_in[`*SIZE*`-1:0]`	Input	Input signal from the pad.
`pad_in_b[`*SIZE*`-1:0]`	Input	Negative node of the differential input signal from the pad. This port is available if you turn on the **Use differential buffer** option.
`pad_out[`*SIZE*`-1:0]`	Output	Output signal to the pad.
`pad_out_b[`*SIZE*`-1:0]`	Output	Negative node of the differential output signal to the pad. This port is available if you turn on the **Use differential buffer** option.
`pad_io[`*SIZE*`-1:0]`	Bidirectional	Bidirectional signal connection with the pad.
`pad_io_b[`*SIZE*`-1:0]`	Bidirectional	Negative node of the differential bidirectional signal connection with the pad. This port is available if you turn on the **Use differential buffer** option.

Table 35. Data Interface Signals

The data interface is an input or output interface from the Intel FPGA GPIO IP core to the FPGA core. In this table, *SIZE* is the data width specified in the IP core parameter editor.

Signal Name	Direction	Description
`din[`*DATA_SIZE*`-1:0]`	Input	Data input from the FPGA core in output or bidirectional mode. *DATA_SIZE* depends on the register mode: • Bypass or simple register—*DATA_SIZE* = *SIZE* • DDIO without half-rate logic—*DATA_SIZE* = 2 × *SIZE* • DDIO with half-rate logic—*DATA_SIZE* = 4 × *SIZE*
`dout[`*DATA_SIZE*`-1:0]`	Output	Data output to the FPGA core in input or bidirectional mode, *DATA_SIZE* depends on the register mode: • Bypass or simple register—*DATA_SIZE* = *SIZE* • DDIO without half-rate logic—*DATA_SIZE* = 2 × *SIZE* • DDIO with half-rate logic—*DATA_SIZE* = 4 × *SIZE*
`oe[`*OE_SIZE*`-1:0]`	Input	OE input from the FPGA core in output mode with **Enable output enable port** turned on, or bidirectional mode. OE is active high. When transmitting data, set this signal to 1. When receiving data, set this signal to 0. *OE_SIZE* depends on the register mode: • Bypass or simple register—*DATA_SIZE* = *SIZE* • DDIO without half-rate logic—*DATA_SIZE* = *SIZE* • DDIO with half-rate logic—*DATA_SIZE* = 2 × *SIZE*

Table 36. Clock Interface Signals

The clock interface is an input clock interface. It consists of different signals, depending on the configuration. The Intel FPGA GPIO IP core can have zero, one, two, or four clock inputs. Clock ports appear differently in different configurations to reflect the actual function performed by the clock signal.

Signal Name	Direction	Description
`ck`	Input	In input and output paths, this clock feeds a packed register or DDIO if you turn off the **Half Rate logic** parameter. In bidirectional mode, this clock is the unique clock for the input and output paths if you turn off the **Separate input/output Clocks** parameter.
`ck_fr`	Input	In input and output paths, these clocks feed the full-rate and half-rate DDIOs if your turn on the **Half Rate logic** parameter.
`ck_hr`		

continued...

Signal Name	Direction	Description
		In bidirectional mode, the input and output paths use these clocks if you turn off the **Separate input/output Clocks** parameter.
ck_in ck_out	Input	In bidirectional mode, these clocks feed a packed register or DDIO in the input and output paths if you specify both these settings: • Turn off the **Half Rate logic** parameter. • Turn on the **Separate input/output Clocks** parameter.
ck_fr_in ck_fr_out ck_hr_in ck_hr_out	Input	In bidirectional mode, these clocks feed a full-rate and half-rate DDIOS in the input and output paths if you specify both these settings • Turn on the **Half Rate logic** parameter. • Turn on the **Separate input/output Clocks** parameter. For example, ck_fr_out feeds the full-rate DDIO in the output path.
cke	Input	Clock enable.

Table 37. Termination Interface Signals

The termination interface connects the Intel FPGA GPIO IP core to the I/O buffers.

Signal Name	Direction	Description
seriesterminationcontrol	Input	Input from the termination control block (OCT) to the buffers. It sets the buffer series impedance value.
parallelterminationcontrol	Input	Input from the termination control block (OCT) to the buffers. It sets the buffer parallel impedance value.

Table 38. Reset Interface Signals

The reset interface connects the Intel FPGA GPIO IP core to the DDIOs.

Signal Name	Direction	Description
sclr	Input	Synchronous clear.
aclr	Input	Asynchronous clear. Active high.
aset	Input	Asynchronous set. Active high.
sset	Input	Synchronous set.

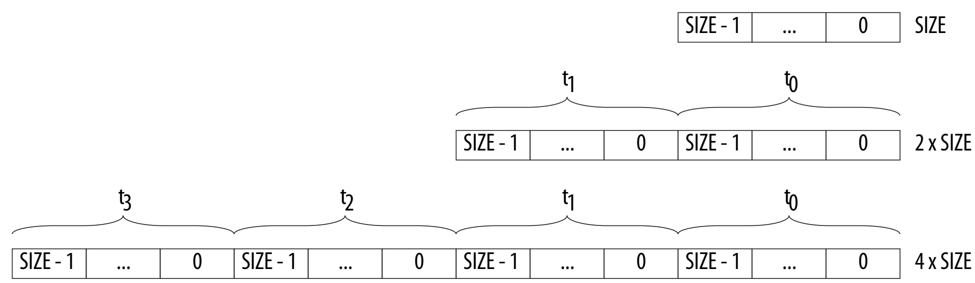
5.2.1 Shared Signals

- The input, output, and OE paths share the same clear and preset signals.
- The output and OE path shares the same clock signals.

5.2.2 Data Bit-Order for Data Interface

Figure 38. Data Bit-Order Convention

This figure shows the bit-order convention for the din, dout and oe data signals.



- If the data bus size value is SIZE, the LSB is at the right-most position.
- If the data bus size value is 2 × SIZE, the bus is made of two words of SIZE .
- If the data bus size value 4 × SIZE, the bus is made of four words of SIZE.
- The LSB is in the right-most position of each word.
- The right-most word specifies the first word going out for output buses and the first word coming in for input buses.

Related Links

Input Path on page 53

5.2.3 Data Interface Signals and Corresponding Clocks

Table 39. Data Interface Signals and Corresponding Clocks

Signal Name	Parameter Configuration			Clock
	Register Mode	Half Rate	Separate Clocks	
din	• Simple Register • DDIO	Off	Off	ck
	DDIO	On	Off	ck_hr
	• Simple Register • DDIO	Off	On	ck_in
	DDIO	On	On	ck_hr_in
• dout • oe	• Simple Register • DDIO	Off	Off	ck
	DDIO	On	Off	ck_hr
	• Simple Register • DDIO	Off	On	ck_out
	DDIO	On	On	ck_hr_out

continued...

Signal Name	Parameter Configuration			Clock
	Register Mode	Half Rate	Separate Clocks	
• sclr • sset • All pad signals	• Simple Register • DDIO	Off	Off	ck
	DDIO	On	Off	ck_fr
	• Simple Register • DDIO	Off	On	• Input path: ck_in • Output path: ck_out
	DDIO	On	On	• Input path: ck_fr_in • Output path: ck_fr_out

6 Document Revision History for Intel Stratix 10 General Purpose I/O User Guide

Date	Version	Changes
November 2017	2017.11.06	• Clarified that each 3 V I/O bank supports only two OEs for its eight single-ended I/Os. • Removed Intel Stratix 10 TX 4500 and TX 5500 devices. • Added package SF48 to Intel Stratix 10 TX 1650 and TX 2100 devices. • Added Intel Stratix 10 MX devices. • Specified that 3 V I/Os are not available for Intel Stratix 10 devices with E-Tile transceiver variants. • Updated descriptions of the table that lists the GPIO buffers and LVDS channels in Intel Stratix 10 GX devices to specify that the LVDS channels counts include dedicated clock pins. • Removed the HF50 package from all Intel Stratix 10 devices. • Restructured the topics and tables that list the I/O banks locations and pin counts. • Added support for 2.5 V LVCMOS I/O standard. • Added 3 V I/O bank support for the 1.8 V LVCMOS, 1.5 V LVCMOS, and 1.2 V LVCMOS I/O standards. • Removed all instances of "DDR3U". Intel validates and support only IPs for memory interfaces listed in Performance Support Summary, Intel Stratix 10 External Memory Interfaces User Guide. • Added a note to specify that to use the 1.2 V, 1.5 V, 1.8 V, and 2.5 V I/O standards on the 3 V I/O bank, you need to set the USE_AS_3V_GPIO assignment. • Updated the tables that lists the programmable IOE features supported by the I/O buffer types and I/O standards. • Removed the table that lists the I/O standards and current strengths that support programmable slew rate control. • Added information about the default slew rate setting. • Updated the topic about programmable IOE delay to remove the input and output delay information. The I/O delay numbers are pending characterization. • Added information about the default predefined current strength if you do not specifically assign a current strength in the Intel Quartus Prime software.

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Date	Version	Changes
		• Updated the table listing the programmable current strength settings. — Added current strength settings for these I/O standards: • 2.5 V LVCMOS • SSTL-135 and Differential SSTL-135 • SSTL-125 and Differential SSTL-125 • SSTL-12 and Differential SSTL-12 Class I • POD12 and Differential POD12 • Differential 1.8 V HSTL Class I and Class II • Differential 1.5 V HSTL Class I and Class II • Differential 1.2 V HSTL Class I — Removed 6 mA, 4 mA, and 2 mA HPS current strength settings for the 1.8 V LVCMOS I/O standard — Removed all HPS current strength settings except for the 1.8 V LVCMOS I/O standard — Removed 12 mA and 10 mA current strength settings from the following I/O standards: • 1.2 V LVCMOS • SSTL-18 Class I • SSTL-15 Class I • 1.2 V HSTL Class I — Removed 16 mA current strength settings from the SSTL-18 Class II and SSTL-15 Class II I/O standards — Updated the current strength setting from 16 mA to 14 mA for the 1.8 V HSTL Class II and 1.5 V HSTL Class II I/O standards — Removed programmable current strength for the 1.2 V HSTL Class II I/O standard • Removed OCT support for 3 V I/O. • Updated the tables listing the R_S and R_T OCT support to update I/O standards and available OCT settings. • Updated the tables listing the external termination schemes to add 2.5 V LVCMOS. • Updated the signal names in figures to match the signal names in the Intel FPGA GPIO IP core. • Added the output path waveform. • Renamed "Altera GPIO IP core" to "Intel FPGA GPIO IP core". • Clarified that the ASET and ACLR signals are active high.
September 2017	2017.09.04	• Added 8 mA to SSTL-2 Class II, SSTL-18 Class II, and SSTL-15 Class II, and removed 12 mA from SSTL-18 Class II in the list of current strength settings that support programmable output slew rate control. • Added 8 mA current strength settings to SSTL-18 Class II and SSTL-15 Class II. • Added these I/O standards to the table listing the selectable I/O standards for R_S OCT without calibration: — Differential SSTL-15 — Differential SSTL-135 — Differential SSTL-125 — Differential SSTL-12 — Differential HSUL-12 • Added 16 mA current strength setting to 1.8 V LVCMOS I/O standard. • Added 12 mA and 10 mA current strength settings to 1.2 V LVCMOS I/O standard. • Removed 25 Ω and 50 Ω R_S OCT settings from Differential SSTL-15 in the table that lists the selectable I/O standards for R_S OCT with calibration. • Updated the table listing the Intel FPGA GPIO buffer parameters to specify the conditions for the **Use bus-hold circuitry** parameter option.

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Date	Version	Changes
February 2017	2017.02.13	• Removed the SF48 package from the Intel Stratix 10 TX 1650 and TX 2100 devices. • Updated topics to clarify that the 3 V I/O banks do not have I/O registers and DDIOs, and do not support all features of the Intel FPGA GPIO IP core.
December 2016	2016.12.05	Corrected the number of I/Os in I/O bank 3L for the HF55 package of the GX 4500 and SX 5500 devices.
October 2016	2016.10.31	Initial release.