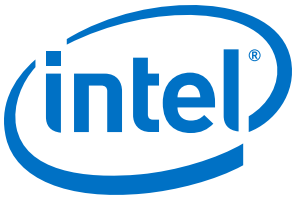


# Intel® Stratix® 10 Analog to Digital Converter User Guide

Updated for Intel® Quartus® Prime Design Suite: **17.1**



**UG-S10ADC | 2017.11.06**
Latest document on the web: **PDF** | **HTML**

# Contents

# 1 Intel® Stratix® 10 ADC Overview

The analog-to-digital converters (ADCs) in Intel® Stratix® 10 devices provide built-in capability for converting external analog voltage signals and monitoring on-die temperature.

Intel Stratix 10 devices contain two types of on-die sensors:

- Voltage sensor—provides digital voltage readings.
  - — You can use the voltage sensor to perform live monitoring of critical on-chip supply voltages and external analog signals.
  - — You can access the voltage readout using the Intel FPGA S10 Voltage Sensor IP core.
- Temperature sensor—provides on-die temperature readings.
  - — The internal digital temperature sensor consists of internal temperature sensing diodes (TSD) and built-in ADC.
  - — You can monitor the on-die temperature through the internal digital temperature sensor in the Intel Stratix 10 core fabric and transceiver tiles.
  - — You can use the Intel FPGA S10 Temperature Sensor IP core to read the digital temperature in Celcius.
  - — You can also access on-die TSDs using external third-party temperature sensors.
  - — If you want temperature reading correlation, you can use both internal and external temperature sensors simultaneously.

### Related Links

- Secure Device Manager
- Stratix 10 Device Datasheet
- Stratix 10 Power Management User Guide

# 2 Intel Stratix 10 ADC Architecture and Features

In Intel Stratix 10 devices, the SDM contains the voltage sensor and internal temperature sensor. To access the voltage or temperature readouts, use the Intel FPGA S10 Voltage Sensor or Intel FPGA S10 Temperature Sensor IP core.

## 2.1 Intel Stratix 10 Voltage Sensor

The on-chip voltage sensor in Intel Stratix 10 is an 8-bit full differential ADC.

The voltage sensor monitors two external differential inputs and five internal power supplies. To read the voltage values through the SDM, use the Intel FPGA S10 Voltage Sensor IP core.

**Figure 1. Intel Stratix 10 Voltage Sensor**

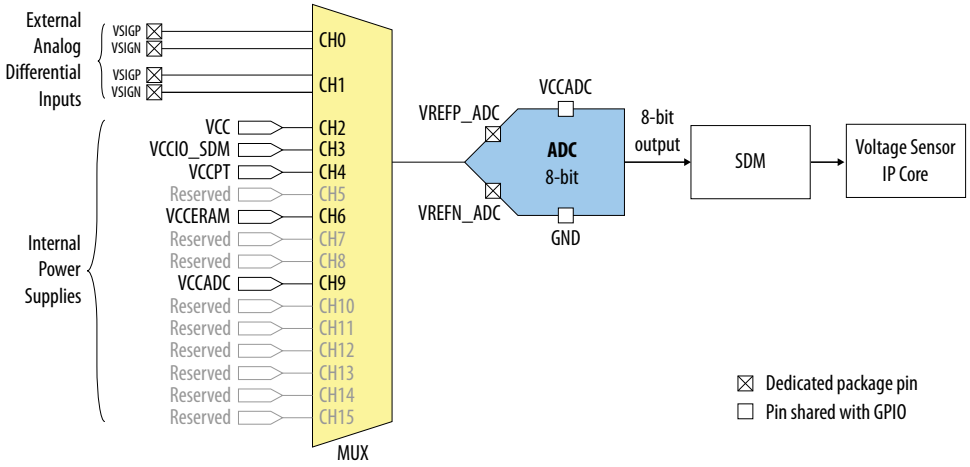
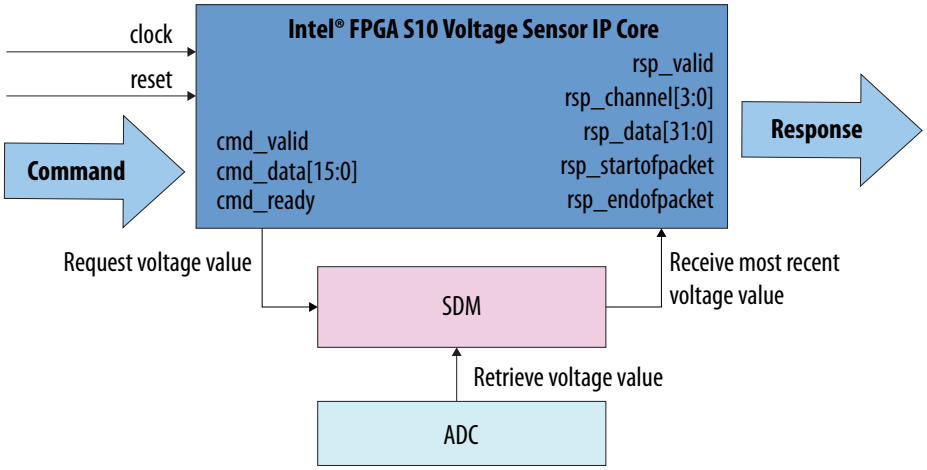


**Figure 2. Intel FPGA S10 Voltage Sensor IP Core Block Diagram**




The SDM samples the voltage at regular intervals. When the Intel FPGA S10 Voltage Sensor IP core sends voltage sampling request to the SDM, the SDM returns the most recently read voltage value. The IP core then returns the observed voltage value as an unsigned 32-bit fixed point binary number.

The maximum value of the external analog signal (differential scale) is 1.25 V.

**Related Links**

- Sampling the ADC Voltage Sensor Channels on page 11
  Provides the steps to read the voltage values and the timing diagram.
- Intel FPGA S10 Voltage Sensor IP Core Digital Signals on page 14
  Provides more information about the command and response signals of the Intel FPGA S10 Voltage Sensor IP core.
- Guidelines: Connecting External Voltage Reference to the Intel Stratix 10 ADC Voltage Reference Pins on page 10

### 2.1.1 Voltage Conversion

The Intel FPGA S10 Voltage Sensor IP core returns the sampled voltage in unsigned 32-bit fixed point binary format, with 16 bits below binary point.

For example, if the returned value is `0x0000C000`, the voltage value is 0.75 V.

## 2.2 Intel Stratix 10 Temperature Sensing Diodes

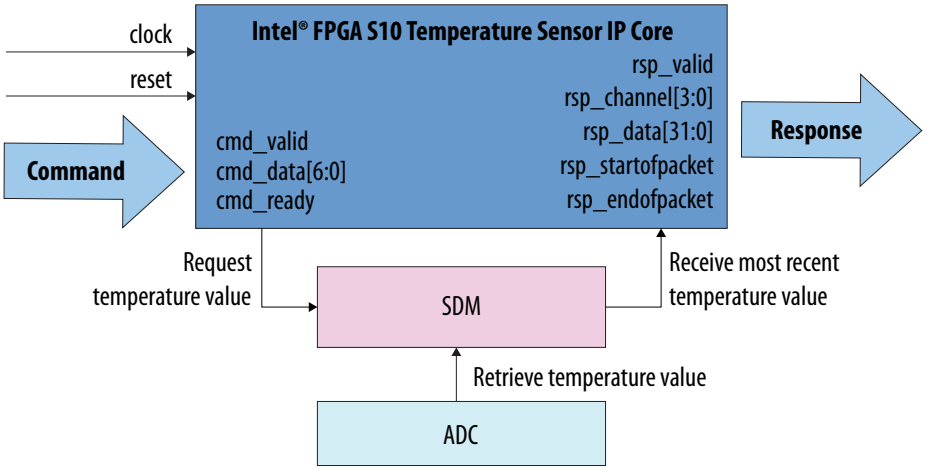
For system-level power supply management, the Intel Stratix 10 device provides internal and external TSDs. You can use both internal and external TSDs simultaneously.

- The internal TSDs allow you to monitor the device's on-die temperature using the on-chip digital temperature sensing circuitry.
- The external TSDs allow you to monitor the device's on-die temperature using external temperature sensors.

### 2.2.1 Internal Temperature Sensor

The internal temperature sensor in the SDM reads the temperature value from the internal TSDs in the core fabric and transceiver tiles. To sample the on-die temperature value through the SDM, use the Intel FPGA S10 Temperature Sensor IP core.

**Figure 3. Intel FPGA S10 Temperature Sensor IP Core Block Diagram**




The SDM samples the temperature at a regular interval. When the Intel FPGA S10 Temperature Sensor IP core sends temperature sampling request to the SDM, the SDM returns the most recently read temperature value. The IP core then returns the observed temperature value in Celsius as a signed 32-bit fixed point binary number.

*Note:* You can use any clock source or speed to clock the Intel FPGA S10 Temperature Sensor IP core. However, you must always ensure that your design closes timing.

**Related Links**

- Intel FPGA S10 Temperature Sensor IP Core Digital Signals on page 15
  Provides more information about the command and response signals of the Intel FPGA S10 Temperature Sensor IP core.
- Using the Intel Stratix 10 ADC Temperature Sensor on page 12
  Provides the steps to read the temperature values and the timing diagram.

#### 2.2.1.1 Temperature Calculation for the Internal Temperature Sensor

The Intel FPGA S10 Temperature Sensor IP core returns the Celsius temperature value in signed 32-bit fixed point binary format, with eight bits below binary point.

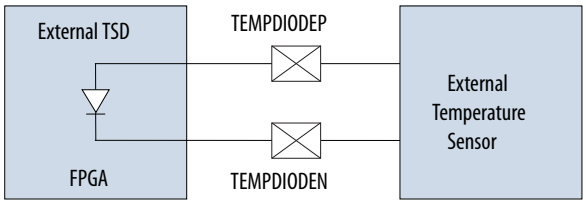
To convert the returned value into decimal, use two's complement operation on the signed integer portion. Then, add the decimal number to the unsigned 8-bit fraction (bit value × $2^{-1}$+ bit value × $2^{-2}$+...+ bit value × $2^{-8}$). For example, if the returned value is `0xFFFFE1C0`, the temperature value is -30.25°C.

### 2.2.2 External Temperature Sensor

You can monitor the Intel Stratix 10 device's die temperature by connecting an external temperature sensor to the Intel Stratix 10 external TSD.

The external TSD requires two pins for voltage reference. If you do not use the external TSD pins, leave the pins unconnected.

**Figure 4. External Temperature Sensor Connection to Intel Stratix 10 External TSD**




**Related Links**

Guidelines: Using External Temperature Sensors on page 9

## 2.2.3 Temperature Sensor Channels and Locations

The Intel Stratix 10 internal and external TSDs are located in the core fabric and transceiver tiles.

- To read the internal TSDs, specify which channels to sample in the Intel FPGA S10 Temperature Sensor IP core.
- To read the external TSDs, connect external temperature sensors to the designated TEMPDIODE pin.

**Figure 5. Locations and Channel Numbers of Intel Stratix 10 TSDs**

In this diagram, the tranceiver tiles are labeled using the 3 V I/O bank number. Each transceiver tile contains one 3 V I/O bank and several transceiver banks.

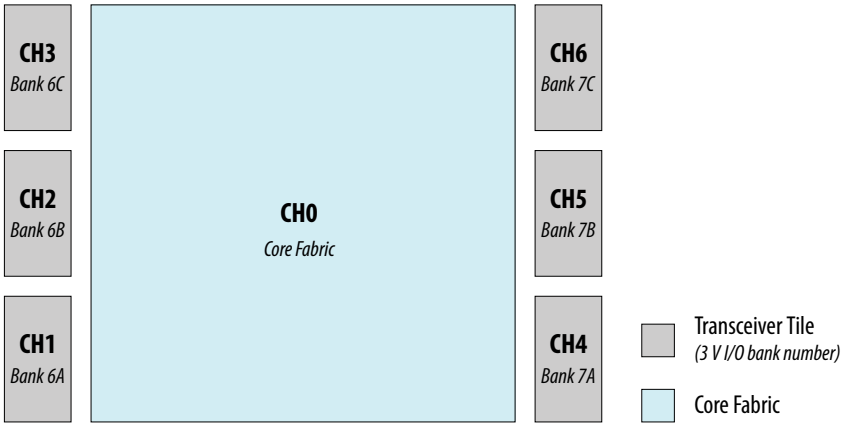



**Table 1. External TSD Designated Pins**

| Channel | Designated Pin | Device and Package Support |
|---|---|---|
| CH0 | TEMPDIODEp[0]<br>TEMPDIODEn[0] | All Intel Stratix 10 devices and packages. |
| CH1 | TEMPDIODEp[1]<br>TEMPDIODEn[1] | All Intel Stratix 10 devices and packages. |

*continued...*

| Channel | Designated Pin | Device and Package Support |
|---|---|---|
| CH2 | TEMPDIODEp[2]<br>TEMPDIODEn[2] | Support of these channels depends on availability of the transceiver tile.<br>However, regardless of transceiver tile availability, these channels are not supported in the NF43, UF50, and HF55 packages of the following devices:<br>• GX 850 and SX 850<br>• GX 1100 and SX 1100<br>• GX 1650 and SX 1650<br>• GX 2100 and SX 2100<br>• GX 2500 and SX 2500<br>• GX 2800 and SX 2800<br>• GX 4500 and SX 4500<br>• GX 5500 and SX 5500 |
| CH3 | TEMPDIODEp[3]<br>TEMPDIODEn[3] | |
| CH4 | TEMPDIODEp[4]<br>TEMPDIODEn[4] | |
| CH5 | TEMPDIODEp[5]<br>TEMPDIODEn[5] | |
| CH6 | TEMPDIODEp[6]<br>TEMPDIODEn[6] | |

*Note:* The availability of each transceiver tile varies among Intel Stratix 10 devices. You can identify the location of the transceiver tile by referring to the 3 V I/O bank number in the Intel Quartus® Prime Chip Planner.

### Related Links

Intel FPGA S10 Temperature Sensor IP Core Digital Signals on page 15

# 3 Intel Stratix 10 ADC Design Considerations

There are several considerations that require your attention to ensure the success of your designs. Unless noted otherwise, these design guidelines apply to all variants of this device family.

## 3.1 Guidelines: Using External Temperature Sensors

Noise coupled from board traces or from within the Intel Stratix 10 device package can influence the sensitive TSD circuit. The signal from the device to the external temperature sensor is based on millivolts (mV) of difference at the external TSD pins. Switching the I/O near the external TSD pins can affect the temperature reading.

Intel recommends that you sample the temperature when the device is inactive or use the internal temperature sensor with the internal TSD.

You can use both internal and external temperature sensors simultaneously.

### Board Connection Guidelines for the Traces to the External TSD Pins

- Keep the trace lengths to the $\texttt{TEMPDIODE}_P$ or $\texttt{TEMPDIODE}_N$ pins less than eight inches.
- Route both traces in parallel and place them close to each other with grounded guard tracks on each side.
- Intel recommends a 10-mils width and space for both traces.
- Route both traces through the most minimum number of vias and crossunders possible to minimize the thermocouple effects.
- Ensure that the number of vias for both traces are the same.
- Ensure that both traces are approximately the same length.
- To avoid coupling, insert a GND plane between the external TSD pins traces and high-frequency toggling signals, such as clocks and I/O signals.
- To filter high-frequency noise, place an external capacitor between the traces close to the external sensors. For Maxim* temperature sensors, use an external capacitor between 2200 pF and 3300 pF.
- Place a 0.1 uF bypass capacitor close to the external temperature sensor.
- If you use only the internal TSD, you can leave the $\texttt{TEMPDIODE}_P$ and $\texttt{TEMPDIODE}_N$ pins unconnected.

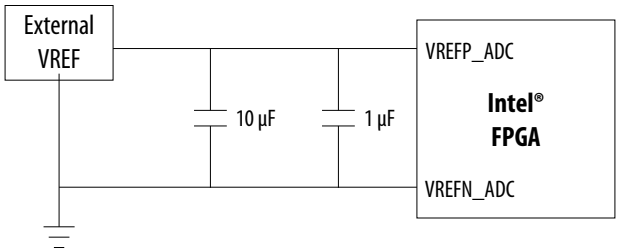
For details about device specifications and connection guidelines, refer to the external temperature sensor manufacturer's datasheet.

## 3.2 Guidelines: Connecting External Voltage Reference to the Intel Stratix 10 ADC Voltage Reference Pins

The Intel Stratix 10 ADC voltage sensor has two dedicated voltage reference pins, VREFP_ADC and VREFN_ADC. Follow these guidelines when you connect an external voltage reference to the VREFP_ADC and VREFN_ADC pins.

- To minimize noise coupling to the power rail, Intel recommends that you keep the external $V_{REF}$ source as close as possible to the VREFP_ADC and VREFN_ADC pins.
- Route the reference traces as a tightly-coupled differential pair to the package ball with ground shielding.
- You must place a 10 µF and a 1 µF board capacitors to decouple the VREFP_ADC and VREFN_ADC pins.
- Place the 1 µF board capacitor as close as possible to the package balls.

**Figure 6. Board Capacitors to Decouple VREFP_ADC and VREFN_ADC Pins**



# 4 Intel Stratix 10 ADC Implementation Guides

The Intel FPGA S10 Voltage Sensor and Intel FPGA S10 Temperature Sensor IP cores are soft controllers for the ADC hard IP blocks. With these IP cores, you can read sampling values from the different ADC channels through the SDM.

- To sample external or internal voltages, use the Intel FPGA S10 Voltage Sensor IP core.
- To sample the on-die temperature using the internal TSDs, use the Intel FPGA S10 Temperature Sensor IP core.

The command and response interfaces of the Intel FPGA S10 Voltage Sensor and Intel FPGA S10 Temperature Sensor IP cores are Avalon® Streaming (Avalon-ST) interfaces with ready latency of 0.

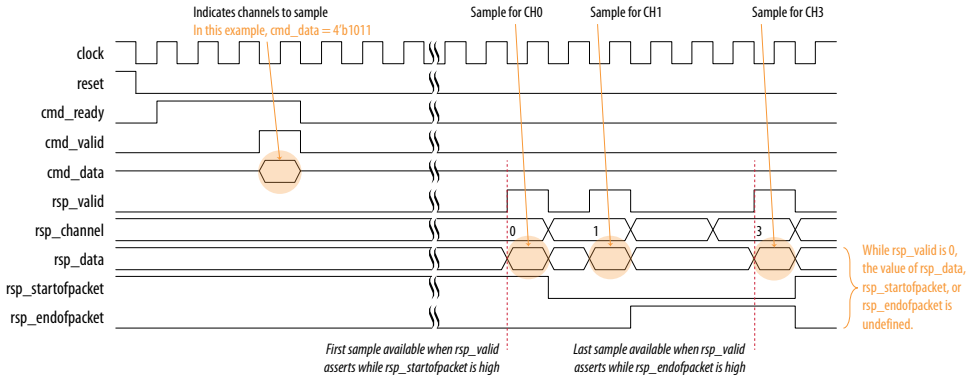
**Related Links**

Secure Device Manager

## 4.1 Sampling the ADC Voltage Sensor Channels

To sample a single ADC channel or multiple ADC channels, specify which channels to sample in the Intel FPGA S10 Voltage Sensor IP core.

**Figure 7. Waveform Example: Sampling Voltage Values from Channels 0, 1, and 3**




*Note:* Set only valid bits in the `cmd_data` word. Otherwise, the response from the voltage sensor is undefined.

1. Simultaneously, assert a logic high to the `cmd_valid` signal and send the `cmd_data` value. To perform continuous sampling, assert `cmd_valid` continuously.

   The `cmd_data` signal is a 16-bit bitmask that specifies from which channel to sample the voltage. The SDM samples the voltages approximately every 1 ms (1).

When you assert `cmd_valid` while `cmd_ready` is high, the IP core requests from the SDM the most recent voltage values of the channels you specify in `cmd_data`. After sending the request, the IP core drives `cmd_ready` low and waits for response from the SDM.

2. Each time the `rsp_valid` signal goes high, indicating that the voltage value is ready, read the `rsp_data` and `rsp_channel` response signals.

   The `rsp_valid` signal goes high once for each bit in the `cmd_data` word. The first valid data in the cycle is available when `rsp_valid` asserts while the `rsp_startofpacket` signal is high. The last valid data in the cycle is available when `rsp_valid` asserts while the `rsp_endofpacket` signal is high. In each valid response, the `rsp_data` signal provides the voltage value while the `rsp_channel` signal indicates from which channel the voltage was sampled.

The value in `rsp_data` is an unsigned 32-bit fixed point binary number, with 16 bits below the binary point.

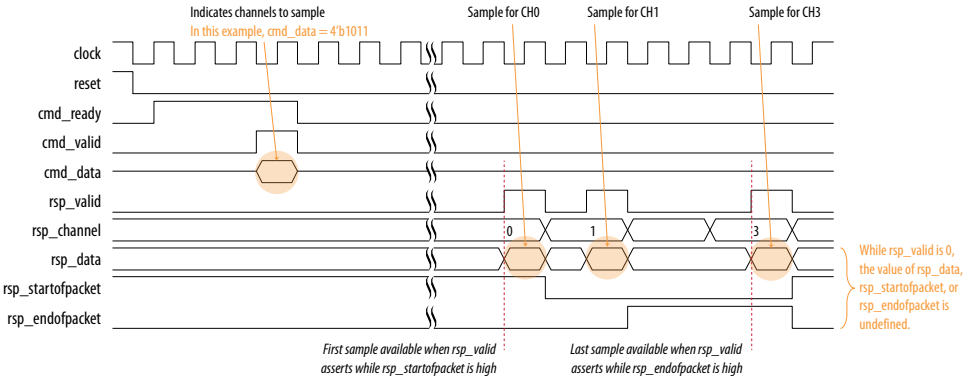
### Related Links

- Voltage Conversion on page 5
- Intel FPGA S10 Voltage Sensor IP Core Digital Signals on page 14
  Provides the list of voltage sensor signals and descriptions.
- Intel Stratix 10 Voltage Sensor on page 4

## 4.2 Using the Intel Stratix 10 ADC Temperature Sensor

To sample the Intel Stratix 10 die temperature using the internal TSDs, use the Intel FPGA S10 Temperature Sensor IP core.

**Figure 8. Waveform Example: Sampling Temperature from Channels 0, 1, and 3**




*Note:* Set only valid bits in the `cmd_data` word. Otherwise, the response from the temperature sensor is undefined.

1. Simultaneously, assert a logic high to the `cmd_valid` signal and send the `cmd_data` value. To perform continuous sampling, assert `cmd_valid` continuously.

(1) If the SDM processor is busy, the response time may be longer.

The `cmd_data` signal is a 7-bit bitmask that specifies from which channel to sample the temperature.

When you assert `cmd_valid` while `cmd_ready` is high, the IP core requests from the SDM the most recent temperature values of the channels you specify in `cmd_data`. After sending the request, the IP core drives `cmd_ready` low and waits for response from the SDM.

2. Each time the `rsp_valid` signal goes high, indicating that the temperature value is ready, read the `rsp_data` and `rsp_channel` response signals.

   The `rsp_valid` signal goes high once for each bit in the `cmd_data` word. The first valid data in the cycle is available when `rsp_valid` asserts while the `rsp_startofpacket` signal is high. The last valid data in the cycle is available when `rsp_valid` asserts while the `rsp_endofpacket` signal is high. For each valid response, the `rsp_data` signal provides the temperature value while the `rsp_channel` signal indicates from which channel the temperature was sampled.

The value in `rsp_data` is a signed 32-bit fixed point binary number, with 8 bits below the binary point.

### Related Links

- Temperature Calculation for the Internal Temperature Sensor on page 6
- Intel FPGA S10 Temperature Sensor IP Core Digital Signals on page 15
  Provides the list of temperature sensor signals and descriptions.
- Internal Temperature Sensor on page 6

# 5 Stratix 10 ADC IP Core References

The Intel FPGA S10 Voltage Sensor and Intel FPGA S10 Temperature Sensor IP cores are soft controllers for the ADC hard IP blocks. Use these IP cores to read sampling values from different ADC channels.

The Intel Quartus Prime software generates your Intel FPGA S10 Voltage Sensor or Intel FPGA S10 Temperature Sensor IP core according to the parameter options that you specify in the parameter editor.

## 5.1 Intel FPGA S10 Voltage Sensor IP Core Digital Signals

These signals are the operational signals of the Intel FPGA S10 Voltage Sensor IP core. The command and response interfaces are Avalon Streaming (Avalon-ST) interfaces with ready latency of 0.

**Figure 9. Intel FPGA S10 Voltage Sensor IP Core**

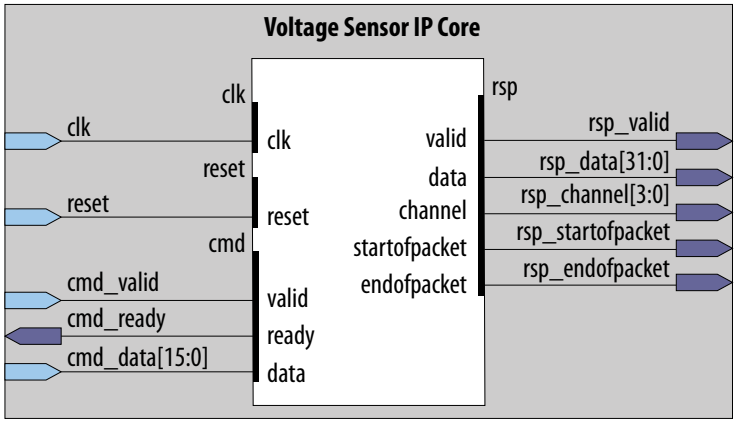



**Table 2. Clock and Reset Signals**

| Signal | Width (Bit) | Type | Description |
|---|---|---|---|
| clk | 1 | Input | All signals in the IP core is synchronous to this clock. The maximum frequency supported for this clock is 250 MHz. |
| reset | 1 | Input | Active high reset. Deassert this signal synchronous to the clock. |

**Table 3. Command Signals**

| Signal | Width (Bit) | Type | Description |
|---|---|---|---|
| `cmd_valid` | 1 | Input | Assert this signal high to send voltage sampling request to the IP core. |
| `cmd_ready` | 1 | Output | The IP core drives this signal high to indicate that the IP core is ready to receive command. |
| `cmd_data` | 16 | Input | Bitmask to indicate from which channel to return the voltage value. Send this data signal together with the `cmd_valid` signal.<br>• Bit 0 to 1—sample the external voltage values from the specified analog input channels.<br>• Bits 2 to 15—sample the internal voltage values from the specified channels.<br>For example, `0000001000010001` signals the IP core to sample the voltage values from channels 0, 4, and 9.<br>Set only valid bits in the `cmd_data` word. Otherwise, the response from the voltage sensor is undefined. |

**Table 4. Response Signals**

| Signal | Width (Bit) | Type | Description |
|---|---|---|---|
| `rsp_valid` | 1 | Output | Indication from the IP core that the voltage value is ready. |
| `rsp_channel` | 4 | Output | Indicates the channel of the voltage value sampled from the analog inputs or internal supplies. |
| `rsp_data` | 32 | Output | The voltage value in a signed 32-bit fixed-point binary format, with 16 bits below the binary point. |
| `rsp_startofpacket` | 1 | Output | Indicates that the current transfer is the start of packet. |
| `rsp_endofpacket` | 1 | Output | Indicates that the current transfer is the end of packet. |

**Related Links**

- Voltage Conversion on page 5
- Sampling the ADC Voltage Sensor Channels on page 11
  Provides the steps to read the voltage values and the timing diagram.
- Intel Stratix 10 Voltage Sensor on page 4
  Provides a list of channel numbers and the supply voltages the ADC monitors.

## 5.2 Intel FPGA S10 Temperature Sensor IP Core Digital Signals

These signals are the operational signals of the Intel FPGA S10 Temperature Sensor IP core. The command and response interfaces are Avalon Streaming (Avalon-ST) interfaces with ready latency of 0.

**Figure 10. Intel FPGA S10 Temperature Sensor IP Core**

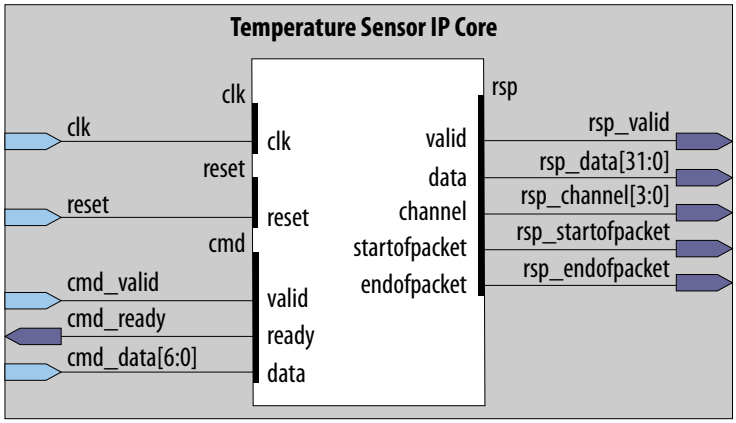



**Table 5. Clock and Reset Signals**

| Signal | Width (Bit) | Type | Description |
|---|---|---|---|
| `clk` | 1 | Input | All signals in the IP core is synchronous to this clock. The maximum frequency supported for this clock is 250 MHz. |
| `reset` | 1 | Input | Active high reset. Deassert this signal synchronous to the clock. |

**Table 6. Command Signals**

| Signal | Width (Bit) | Type | Description |
|---|---|---|---|
| `cmd_valid` | 1 | Input | Assert this signal high to send temperature sampling request to the IP core. |
| `cmd_ready` | 1 | Output | The IP core drives this signal high to indicate that the IP core is ready to receive command. |
| `cmd_data` | 7 | Input | Bitmask to indicate from which channel to return the temperature. Send this data signal together with the `cmd_valid` signal.<br>• Bit 0—sample the temperature value from the internal TSD in the core fabric.<br>• Bits 1 to 6—sample the temperature values from internal TSDs in the transceiver tiles.<br>For example, `0000101` signals the IP core to sample the temperature values from channels 0 and 2.<br>For the designated temperature sensor channel number of each transceiver tile, refer to the related information.<br>Set only valid bits in the `cmd_data` word. Otherwise, the response from the temperature sensor is undefined.<br>*Note:* The availability of the internal TSD channels varies among Intel Stratix 10 devices and packages. |

### Table 7. Response Signals

| Signal | Width (Bit) | Type | Description |
|---|---|---|---|
| `rsp_valid` | 1 | Output | Indication from the IP core that the temperature value is ready. |
| `rsp_channel` | 4 | Output | Indicates the channel of the temperature value sampled from the core fabric or transceiver tile. |
| `rsp_data` | 32 | Output | The temperature value in a signed 32-bit fixed-point binary format, with 8 bits below the binary point. |
| `rsp_startofpacket` | 1 | Output | Indicates that the current transfer is the start of packet. |
| `rsp_endofpacket` | 1 | Output | Indicates that the current transfer is the end of packet. |

### Related Links

- Temperature Calculation for the Internal Temperature Sensor on page 6
- Using the Intel Stratix 10 ADC Temperature Sensor on page 12
  Provides the steps to read the temperature values and the timing diagram.
- Temperature Sensor Channels and Locations on page 7

# 6 Document Revision History for Intel Stratix 10 Analog to Digital Converter User Guide

| Date | Version | Changes |
|---|---|---|
| November 2017 | 2017.11.06 | • Added support for external temperature sensors.<br>• Restructured the document, updated content, and added topics to support the external temperature sensors feature.<br>• Added board design guidelines for connecting external voltage reference sources to the ADC $V_{REF}$ pins.<br>• Updated the waveform examples to improve clarity. |
| May 2017 | 2017.05.08 | • Updated the topic about the voltage sensor to specify that the voltage sensor monitors two external voltages and only five internal power supplies.<br>• Updated the timing diagrams and descriptions in the topics about sampling the voltage and temperature sensors to improve clarity.<br>• Updated `cmd_data` width in the Intel FPGA S10 Temperature Sensor IP core block diagram from 6 bits to 7 bits.<br>• Updated the description of `cmd_data` to specify that invalid bits cause undefined response data from the sensors.<br>• Updated the temperature sensor channels location figure with 3 V I/O bank numbers to identify in which transceiver tile the sensor is located. |
| February 2017 | 2017.02.13 | • Updated the Intel FPGA S10 Voltage Sensor and Intel FPGA S10 Temperature Sensor IP cores block diagrams to improve clarity.<br>• Updated the topic about temperature calculation to clarify about the values returned by the temperature sensors in the tranceiver tiles.<br>• Updated the topics about sampling the voltage sensor and temperature sensor channels to improve clarity.<br>• Updated the temperature sensor `cmd_data` bitmask signal from 6 bits to 7 bits.<br>• Updated the maximum supported frequency of the Intel FPGA S10 Temperature Sensor and Intel FPGA S10 Voltage SensorIP cores clock input to be equivalent to the system clock.<br>• Added a topic showing the temperature sensor locations and channel numbers.<br>• Updated the topics listing the Intel FPGA S10 Voltage Sensor and Intel FPGA S10 Temperature Sensor IP core signals. |
| December 2016 | 2016.12.05 | Updated the tables listing the clock and reset signals for the Intel FPGA S10 Voltage Sensor and Intel FPGA S10 Temperature Sensor IP cores. |
| October 2016 | 2016.10.31 | Initial release. |