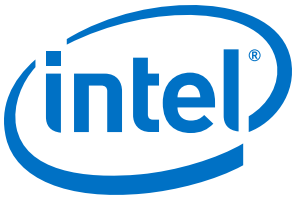

Differences Among Intel SoC Device Families

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Contents

UF-1005 | 2018.08.22

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Differences Among Intel SoC Device Families

This document lists the differences among hard processor systems (HPSs) in Intel's SoC device families.

There are several families of Intel® SoC devices:

- Altera® Cyclone® V SoC
- Altera Arria® V SoC
- Intel Arria 10 SoC
- Intel Stratix® 10 SoC

This document briefly lists the differences among these device families. For complete descriptions and explanations of device family features, refer to the handbook for each device family.

Note: The information in this document regarding the Stratix 10 SoC devices is preliminary and subject to change.

Related Information

- Cyclone V Device Handbook, Volume 3
  Detailed descriptions of features in the Cyclone V SoC device family
- Arria V Device Handbook, Volume 3
  Detailed descriptions of features in the Arria V SoC device family
- Arria 10 Hard Processor System Technical Reference Manual
  Detailed descriptions of features in the Arria 10 SoC device family
- Stratix 10 Hard Processor System Technical Reference Manual
  Detailed descriptions of features in the Stratix 10 SoC device family

Overview of HPS Modules

Table 1. Summary: Differences Among HPS Modules

HPS Module	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Microprocessor Unit Subsystem (MPU)	Single / Dual Cortex®-A9	Dual Cortex-A9	Dual Cortex-A9	Quad Cortex-A53
Cache Coherency Controller	Accelerator coherency port (ACP)	ACP	ACP	Cache Coherency Unit (CCU)
System Memory Management Unit	No	No	No	Yes
On-Chip RAM	64 KB	64 KB	256 KB	256 KB
Error Correction Code (ECC) Controller	No	No	Yes	Yes

continued...

HPS Module	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
DMA Controller	Yes	Yes	Yes	Yes
Clock Manager	Yes	Yes	Yes	Yes
Reset Manager	Yes	Yes	Yes	Yes
FPGA Manager	Yes	Yes	Yes	No
System Manager	Yes	Yes	Yes	Yes
Scan Manager	Yes	Yes	No	No
Security Manager	No	No	Yes	No (SDM)
System Interconnect	Yes	Yes	Yes	Yes
HPS-FPGA Bridges	Yes	Yes	Yes	Yes
General Purpose I/O (GPIO)	Yes	Yes	Yes	Yes
Available dedicated I/Os	10	10	17	48
Available shared I/Os	Up to 67	94	48	0
SDRAM Controller	Inside HPS	Inside HPS	Outside of HPS	Outside of HPS
NAND Flash Controller	Yes	Yes	Yes	Yes
Secure digital/multimedia card (SD/MMC) Controller	Yes	Yes	Yes	Yes
Quad SPI (QSPI) Flash Controller	Yes	Yes	Yes	No(1)
USB 2.0 On-the-Go (OTG)	2	2	2	2
Ethernet Media Access Control (MAC)	2	2	3	3
SPI Master Controller	2	2	2	2
SPI Slave Controller	2	2	2	2
Inter-Integrated Circuit (I^2C) Controller	2	2	5	5
UART Controller	2	2	2	2
Controller Area Network (CAN) Controller	2	0	0	0
Timer	4	4	4	4
Watchdog Timer	2	2	2	4
CoreSight Debug and Trace	Yes	Yes	Yes	Yes
Secure Device Manager (SDM) Interface	No	No	No	Yes

HPS MPU Subsystem Differences

MPU Subsystem Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
CPU	Single/Dual Cortex-A9	Dual Cortex-A9	Dual Cortex-A9	Quad Cortex-A53
Maximum frequency (MHz)	925	1050	1500	1500
Core revision	r3p0	r3p0	r4p1-00rel0	r0p4-51rel0

continued...

(1) The SDM supports QSPI

MPU Subsystem Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
L1 instruction cache	32 KB	32 KB	32 KB	32 KB
L1 data cache	32 KB	32 KB	32 KB	32 KB
L2 cache	512 KB	512 KB	512 KB	1 MB
ACP enabled	Yes	Yes	Yes	No (2)
L1 data cache error checking	Parity (3)	Parity(3)	Parity(3)	ECC (4)
L1 instruction cache error checking	Parity(3)	Parity(3)	Parity(3)	Parity(3) on data and tag bits
L2 cache error checking	ECC(5) ; ECC interrupts; optional parity(3) for tag bits	ECC(5); ECC interrupts; optional parity (3) for tag bits	ECC(5); ECC interrupts; optional parity (3) for tag bits	ECC(5) on data and tag bits; ECC interrupts
Translation lookaside buffer (TLB) error checking	Parity(3)	Parity(3)	Parity(3)	Parity(3)

Related Information

Cache Coherency Unit chapter of the *Stratix 10 Hard Processor System Technical Reference Manual*
Detailed information about the CCU in the Stratix 10 SoC device family

Stratix 10 HPS Interface to SDM

Secure Device Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Secure device manager implemented	No	No	No	Yes

The SDM is a hard subsystem in the FPGA portion of the Stratix 10 device that is responsible for:

- Configuring the FPGA
- Bootstrapping the HPS
- Providing device-wide security features

The SDM is responsible for copying the HPS bootloader(6) from its flash storage device to the on-chip RAM inside the HPS. Since the SDM is also used for configuration, the HPS can request that the SDM configure or reconfigure the FPGA. The SDM and HPS communicate with one another through the SDM interface, which is a bridge that exposes the address map of each subsystem to the other.

(2) System level cache coherency is provided by the CCU. For details, please refer to the *Cache Coherency Unit* chapter of the *Stratix 10 Hard Processor System Technical Reference Manual*.

(3) Single-bit error detection (SED)

(4) Data: single-bit error correction, double-bit error detection (SECDED). Control bits: parity (SED)

(5) SECDED with single-event upset (SEU) protection

(6) typically U-Boot or Unified Extensible Firmware Interface (UEFI)

Booting and Configuration Differences

Table 2. FPGA Configuration Method Differences

FPGA Configuration Method	Cyclone V	Arria V	Arria 10	Stratix 10
NAND	HPS FPGA Manager	HPS FPGA Manager	HPS FPGA Manager	N/A
SD/MMC, Embedded Multimedia Card (eMMC)	HPS FPGA Manager	HPS FPGA Manager	HPS FPGA Manager	SDM
Active serial (AS)	FPGA configuration block (CB)	FPGA CB	FPGA configuration subsystem (CSS)	SDM
Passive serial (PS)	FPGA CB	FPGA CB	FPGA CSS	N/A
Fast passive parallel (FPP)	FPGA CB, HPS FPGA Manager	FPGA CB, HPS FPGA Manager	FPGA CSS, HPS FPGA Manager	SDM (7)
Configuration via protocol (CvP)	FPGA CB	FPGA CB	FPGA CSS	SDM
JTAG	FPGA CB	FPGA CB	FPGA CSS	SDM
Supports early I/O release	N/A	N/A	Yes	Yes

Table 3. Booting Differences

HPS Boot Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Initial HPS Image Loader	HPS Boot ROM	HPS Boot ROM	HPS Boot ROM	SDM
HPS Boot from SD/eMMC	Yes	Yes	Yes	Yes (8)
HPS Boot from NAND	Yes	Yes	Yes	Yes (8)
HPS Boot from Quad SPI (QSPI)	Yes	Yes	Yes	Yes (8)
HPS Boot from CvP	No	No	No	No
HPS Boot from Avalon Streaming (Avalon-ST) interface	No	No	No	Yes (8)
HPS Boot from FPGA	Yes	Yes	Yes	No (9)
HPS boots first, then HPS configures FPGA	Yes	Yes	Yes	Yes
HPS Boot Image Compression	No	No	No	Yes (8)
HPS Boot Image Security	No	No	Yes	Yes

Related Information

HPS Security Feature Differences on page 11

(7) FPP support based on Avalon®-ST

(8) The initial Stratix 10 HPS bootloader is loaded by the SDM, supporting the same features and image sources as for FPGA configuration.

(9) Because the Stratix 10 HPS bootloader is loaded by the SDM from the same source as the FPGA configuration image, the HPS does not have to boot from the FPGA image. This saves FPGA resources.

HPS Cache Coherency Controller Differences

Cache Coherency Controller Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
System level cache coherency	Implemented by ACP in MPCore and ACP ID mapper block	Implemented by ACP in MPCore and ACP ID mapper block	Implemented by ACP in MPCore and level 3 (L3) interconnect	Implemented by cache coherency unit (CCU)

Cyclone V, Arria V, and Arria10 SoC devices implement system level cache coherency by exposing the MPU accelerator coherency port (ACP) to masters in the system including the FPGA fabric connected to the FPGA-to-HPS bridge. The Cyclone V and Arria V SoCs require these masters to access the ACP ID mapper while Arria 10 SoC only requires the masters to perform cacheable accesses to the MPU cache subsystem.

The Stratix 10 HPS includes a cache coherency unit that resides between the MPU and the rest of the system, allowing cacheable accesses from masters in the system, including soft IP in the FPGA fabric connected to the FPGA-to-HPS bridge. The Stratix 10 HPS CCU also performs routing functionality between the MPU, FPGA-to-HPS bridge, L3 interconnect, and SDRAM scheduler.

HPS System Memory Management Differences

System Memory Management Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
SMMU implementation	None	None	None	ARM MMU-500 r2p0

The Stratix 10 HPS includes a system memory management unit (SMMU) which is responsible for translating virtual addresses to physical addresses. Distributed translation buffer units (TBUs), located between system masters and the L3 interconnect, communicate with the central translation control unit (TCU). The TBUs for the following components accelerate mapping by caching translations:

- USB
- Ethernet media access controller (EMAC)
- NAND controller
- SD/MMC
- Embedded trace router (ETR)
- DMA
- FPGA-to-HPS bridge

The SMMU allows drivers executing in the MPU to pass virtual addresses directly to peripherals that master memory. This capability reduces driver overhead and complexity, compared to performing virtual-to-physical address translation in software.

HPS On-Chip RAM Differences

On-Chip RAM Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
On-Chip RAM Size	64 KB	64 KB	256 KB	256 KB
ECC protection	Basic	Basic	Enhanced	Enhanced
ECC errors can be directly injected from the ECC controller	N/A	N/A	Yes	Yes

HPS Error Correction Differences

Table 4. HPS Error Correction Differences in Peripheral RAM

Error Correction Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
USB 2.0 OTG Error correction code (ECC) support	Basic (10)	Basic	Enhanced (10)	Enhanced
SD/MMC ECC support	Basic	Basic	Enhanced	Enhanced
EMAC ECC support	Basic	Basic	Enhanced	Enhanced
DMA ECC support	Basic	Basic	Enhanced	Enhanced
NAND ECC support	Basic	Basic	Enhanced	Enhanced
QSPI ECC support	Basic	Basic	Enhanced	N/A
SDRAM ECC support	Basic	Basic	Enhanced	Enhanced
ECC error injection	System manager	System manager	ECC controller	ECC controller
On-Chip RAM Read-Modify-Write Available with ECC Enabled	No	No	No	Yes
Note: The L1 and L2 caches have their own dedicated parity checking and ECC support. The SDRAM controller also has its own dedicated ECC support. For more information about cache and SDRAM ECC features for a specific device family, refer to that family's *Hard Processor Technical Reference Manual*.				

Table 5. Basic and Enhanced ECC Features

Feature	Basic (Arria V, Cyclone V)	Enhanced (Arria 10, Stratix 10)
Single-bit error detection and correction	Yes	Yes
Double-bit error detection	Yes	Yes
Indirect memory access; for RAM testing and double-bit error correction	No	Yes
Logs most recent error memory address	No	Yes
Memory initialization block implements memory initialization	No	Yes
Single-bit error counter with programmable counter-match interrupt	No	Yes

Related Information

- Cyclone V Device Handbook, Volume 3
  Detailed descriptions of features in the Cyclone V SoC device family

(10) See the "Basic and Enhanced ECC Features" table for the differences between basic and enhanced ECC.

- Arria V Device Handbook, Volume 3
  Detailed descriptions of features in the Arria V SoC device family
- Arria 10 Hard Processor System Technical Reference Manual
  Detailed descriptions of features in the Arria 10 SoC device family
- Stratix 10 Hard Processor System Technical Reference Manual
  Detailed descriptions of features in the Stratix 10 SoC device family

HPS DMA Controller Differences

DMA Controller Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Number of peripheral request interfaces	31	31	32	32
Peripheral request interface for FPGA manager	No	No	Yes	N/A
ECC protection for internal memory	Basic	Basic	Enhanced	Enhanced
ECC errors can be directly injected from the ECC controller	N/A	N/A	Yes	Yes

HPS Clock Manager Differences

Clock Manager Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Number of phase-locked loop (PLL) blocks	3	3	2	2
HPS I/O clock inputs	HPS_CLK1, HPS_CLK2	HPS_CLK1, HPS_CLK2	HPS_CLK1	HPS_OSC_CLK
HPS I/O clock input location	Fixed pin locations in HPS I/O	Fixed pin locations in HPS I/O	Fixed pin locations in HPS dedicated I/O	Can be assigned to any of the 48 dedicated I/Os
HPS I/O clock signaling	1.8 V, 2.5 V, or 3.0 V LVCMOS	1.8 V, 2.5 V, or 3.0 V LVCMOS	1.8 V, 2.5 V, or 3.0 V LVCMOS	1.8 V LVCMOS
HPS I/O functional test clock outputs	No	No	No	Yes (11)

(11) Internal HPS PLL counter outputs on HPS dedicated I/O:
- Two main counter clock outputs
- Two peripheral counter clock outputs
- One output for additional debug (such as PLL lock status)

Software can configure all test outputs through the MUX control registers.

HPS Reset Manager Differences

Reset Manager Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Cold Reset Sources	• POR [12] monitor • nPOR pin • FPGA fabric • FPGA CB [13] and scan manager • Software cold reset request	• POR monitor • nPOR pin • FPGA fabric • FPGA CB and scan manager • Software cold reset request	• Security manager • nPOR pin • FPGA fabric • FPGA CB • Software cold reset request	• SDM • HPS cold reset pin [14] • HPS software cold reset request
Warm reset sources	• nRST pin • FPGA fabric • Software warm reset request • MPU watchdogs • System watchdogs	• nRST pin • FPGA fabric • Software warm reset request • MPU watchdogs • System watchdogs	• nRST pin • FPGA fabric • Software warm reset request • MPU watchdogs • System watchdogs	• SDM • FSBL [15] or software warm reset request • System watchdogs
Debug reset resources	• DAP [16] reset • FPGA fabric	• DAP reset • FPGA fabric	• DAP reset • FPGA fabric	DAP reset
RAM-clearing reset	No	No	Yes	Handled by SDM
Anti-tamper reset	No	No	Yes	Handled by SDM

HPS FPGA Manager Differences

FPGA Manager Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
FPGA Manager present	Yes	Yes	Yes	No – all configuration is handled by the SDM
Full configuration of FPGA	Yes	Yes	Yes	N/A
Partial reconfiguration of FPGA	Yes	Yes	Yes	N/A
CRC Error Message data registers (EMR)	No	No	Yes	N/A
General Purpose 32-bit Input/Output from HPS to FPGA	Yes	Yes	Yes	N/A

(12) Power-on reset

(13) Control block

(14) One of the dedicated SDM I/Os can be configured to work as an HPS cold reset pin

(15) First-stage boot loader

(16) Debug access port

HPS System Manager Differences

System Manager Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Injects errors to ECC-protected peripherals	Yes	Yes	No (17)	No (17)

HPS Scan Manager Differences

Scan Manager Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Scan Manager Present	Yes	Yes	No	No

The HPS scan manager is supported only in the Cyclone V SoC and Arria V SoC device families. The HPS I/O pins are configured through a series of scan chains in the Cyclone V and Arria V SoCs.

In contrast, in the Arria 10 SoC and Stratix 10 SoC, the HPS I/O pins are configured in the FPGA bitstream. There is no separate block to configure HPS I/O in Arria 10 SoC and Stratix 10 SoC.

HPS Security Feature Differences

The Cyclone V and Arria V families offer basic security functionality with ARM TrustZone® and Advanced Encryption Standard (AES) encryption.

The Arria 10 family improves on Cyclone V and Arrive V security with the following features:

- Recognition of secure fuse configuration
- Secure state control and status check of security features
- Secure boot options
- Varying levels of debug visibility
- Anti-tamper support

The Stratix 10 family includes the Secure Device Manager (SDM). The SDM implements the following functions:

- Device configuration
- Security features
- Booting the HPS

(17) In the Arria 10 and Stratix 10 device families, the ECC controller performs this function.

The SDM provides a robust, secure, and fully authenticated configuration scheme, allowing you to customize device configuration. Advantages of the SDM, compared to security features in earlier Intel SoC device families, include:

- Improved configuration time
- Improved response to single-event upset
- Reactive zeroization of data as a response to security breaches
- Key management and update
- Field upgrade support

This combination of features and flexibility enables you to create secure designs that protect sensitive intellectual property (IP) and data in both FPGA and SoC devices.

The following table summarizes the differences in the security features among the various SoC families.

Table 6. HPS Security Location Differences

Security Feature Location	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Security Fuses	N/A	N/A	Security Manager	SDM
AES Decryption	N/A	N/A	Security Manager	SDM
Authentication	N/A	N/A	Security Manager	SDM
HPS Boot Reset	Reset Manager	Reset Manager	Security Manager	SDM
Anti-tamper RAM Scramble	N/A	N/A	Security Manager	SDM
Control of Secure Boot	N/A	N/A	Security Manager	SDM

HPS Interconnect Differences

Interconnect Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Interconnect Implementation	ARM® CoreLink™ Network Interconnect (NIC-301)	ARM CoreLink Network Interconnect (NIC-301)	Arteris FlexNOC™ Network-on-Chip Interconnect	Arteris FlexNOC Network-on-Chip Interconnect
Firewall and Security Support	No	No	Yes	Yes
SDRAM scheduling implementation	Multi-port front end (MPFE) in hard memory controller (HMC)	MPFE in HMC	SDRAM scheduler in interconnect	SDRAM scheduler in interconnect
On-chip Debug and Trace Capabilities	No	No	Yes	Yes

HPS-FPGA Bridge Differences

HPS-FPGA Bridge Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
HPS-to-FPGA	32-, 64-, or 128-bit	32-, 64-, or 128-bit	32-, 64-, or 128-bit	32-, 64-, or 128-bit
Lightweight HPS-to-FPGA	32-bit	32-bit	32-bit	32-bit
FPGA-to-HPS	32-, 64-, or 128-bit	32-, 64-, or 128-bit	32-, 64-, or 128-bit	128-bit
Protocol Support	AMBA AXI-3	AMBA AXI-3	AMBA AXI-3	AMBA AXI-4 + AMBA4 ACE-Lite
Ready latency support for improved timing	No	No	Yes	Yes

Although the HPS and the FPGA logic can operate independently, they are tightly coupled through a high bandwidth system interconnect built from high-performance ARM Advanced Microcontroller Bus Architecture (AMBA®) Advanced eXtensible Interface (AXI™) bus bridges.

Bus masters on soft logic cores in the FPGA fabric have access to HPS bus slaves through the FPGA-to-HPS bridge. Similarly, HPS bus masters have access to bus slaves in the FPGA through the HPS-to-FPGA bridge.

On Cyclone V, Arria V, and Arria 10 devices, the bridges are AMBA AXI-3 compliant and support simultaneous read and write transactions. Up to three masters in the FPGA fabric can share the HPS SDRAM controller with the processor.

On Stratix 10 devices, the FPGA-to-HPS bridge implements the AXI Coherency Extension (ACE) protocol, and passes through the CCU block.

The processor can be used to configure the core fabric under program control through a dedicated 32-bit configuration port.

HPS General Purpose I/O Interface Differences

GPIO Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Synopsys IP Version	2.08b	2.08b	2.09d	2.10a
Programmable I/O Delays	No	No	No	Yes

HPS I/O Configuration Differences

The available I/Os on SoC devices are divided into the following categories:

- Dedicated function – Each I/O has only one function and cannot be used for other purposes.
- Dedicated I/O with loaner capability – The I/Os are primarily used by the HPS, but individual I/Os can be used by the FPGA if the HPS is not using them.
- Dedicated I/O – The I/Os can be used only by the HPS. The pins are not accessible to logic in the FPGA.
- Shared I/O – The I/Os can be used by either the HPS or the FPGA. These pins are used by HPS peripheral signals, particularly high-speed HPS peripherals such as EMAC and USB. Pins can be assigned to either the HPS or the FPGA in blocks of 12.
- FPGA I/O – These I/Os can only be used by the FPGA. Slow-speed HPS peripheral signals can be routed through the FPGA fabric and assigned to FPGA I/O.

Table 7. Types and Numbers of HPS I/O Pins

Type	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Reset pins	3 dedicated function	3 dedicated function	2 dedicated function	SDM controls HPS resets(18)
Clock pins	2 dedicated function	2 dedicated function	1 dedicated function	Choose one of the 48 dedicated I/Os
JTAG pins	5 dedicated pins JTAG interface is independent of FPGA JTAG interfaces	5 dedicated pins JTAG interface is independent of FPGA JTAG interfaces	Chained internally into FPGA JTAG interface	4 optional dedicated Independent or chained internally into FPGA JTAG interface
Peripherals pins	Up to 67 dedicated I/Os with loaner capability	94 dedicated I/Os with loaner capability	14 dedicated I/Os 48 shared I/Os	48 total dedicated I/Os (including pins used for clock and JTAG)
Supported voltages	3.3 V 3.0 V 2.5 V 1.8 V 1.5 V	3.3 V 3.0 V 2.5 V 1.8 V 1.5 V	3.0 V 2.5 V 1.8 V	1.8 V

HPS SDRAM Controller Subsystem Differences

SDRAM Controller Subsystem Features	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
HPS SDRAM bandwidth	8, 16, or 32 bits, up to 400 MHz	8, 16, or 32 bits, up to 533 MHz	16, 32, or 64 bits, up to 1200 MHz	16, 32, or 64 bits, up to 1066 MHz
Supported SDRAM standards	Double data rate 3 (DDR3)	DDR3 DDR2	DDR4 DDR3	DDR4 DDR3

continued...

(18) The SDM controls the HPS resets, including POR, warm, cold, and debug resets. You can assign HPS_COLD_RESET to an available SDM I/O pin. This pin serves both as an input to reset the HPS and as an output to assert reset to the system when the HPS is in reset.

SDRAM Controller Subsystem Features	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
	DDR2 Low power DDR2 (LPDDR2)	LPDDR2		
FPGA-to-SDRAM available port sizes	32 bits 64 bits 128 bits	32 bits 64 bits 128 bits	32 bits 64 bits 128 bits	32 bits 64 bits 128 bits
FPGA-to-SDRAM maximum total interface width	256 bits	256 bits	256 bits	384 bits
Controller implementation	Dedicated controller in the HPS	Dedicated controller in the HPS	Uses the hard memory controller (HMC) in the FPGA I/O column, bank 2K	Uses the HMC in the FPGA I/O column, bank 2M
External SDRAM interface I/O pin locations	Fixed locations in the HPS I/O	Fixed locations in the HPS I/O	Uses DDR I/O in the FPGA I/O column See table below for bank assignments	Uses DDR I/O in the FPGA I/O column See table below for bank assignments
Shared access management	Multi port front end (MPFE) in the HPS SDRAM controller subsystem	MPFE in the HPS SDRAM controller subsystem	Arteris FlexNoC scheduler in the HPS SDRAM L3 Interconnect	Arteris FlexNoC scheduler in the HPS SDRAM L3 Interconnect
Device and package support for x64/72 external SDRAM interfaces (64 data bits, 8 ECC bits)	N/A	N/A	KF40 package only	All device and package combinations
Supports HPS and core external memory interface (EMIF) instances in the same I/O column	N/A	N/A	No	Yes

Mem I/O	Bank	
	Arria 10 SoC	Stratix 10 Soc
Data[63:32]	2I	2L
Data[31:0]	2J	2N
Address, Command and ECC	2K	2M

HPS NAND Flash Controller Differences

NAND Flash Controller Feature		Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Cadence IP version		R5	R5	R5 with enhancements	R5 with enhancements
ECC protection for internal memory		Basic	Basic	Enhanced	Enhanced
ECC errors can be directly injected from the ECC controller		N/A	N/A	Yes	Yes
Maximum NAND flash width	HPS dedicated I/O	8	8	8	16
	HPS shared I/O	N/A	N/A	16	N/A
	FPGA I/O	N/A	N/A	16	16

HPS SD/MMC Controller Differences

SD/MMC Controller Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Synopsys IP Version	2.40a	2.40a	2.70a	2.80a
Embedded Multimedia card (eMMC) version	4.41	4.41	4.5	4.51 and 5.0
ECC protection for internal memory	Basic	Basic	Enhanced	Enhanced
ECC errors can be directly injected from the ECC controller	N/A	N/A	Yes	Yes

HPS Quad SPI Flash Controller Differences

Quad SPI Flash Controller Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Cadence IP Version	r1p01	r1p01	r1p01	N/A
ECC protection for internal memory	Basic	Basic	Basic	N/A
ECC errors can be directly injected from the ECC controller	N/A	N/A	N/A	N/A

There is no Quad SPI flash controller in the Stratix 10 SoC. The HPS can boot from Quad SPI flash memory attached to the SDM.

HPS USB 2.0 OTG Controller Differences

USB 2.0 OTG Controller Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
ECC protection for internal memory	Included	Included	Enhanced	Enhanced
ECC errors can be directly injected from the ECC controller	N/A	N/A	Yes	Yes
Synopsys IP Version	2.93a	2.93a	3.20a	3.30
MAC-PHY connection	HPS I/O	HPS I/O	Shared I/O	Dedicated I/O
PHY I/O support	3.3V, 3.0V, 2.5V, 1.8V, 1.5V	3.3V, 3.0V, 2.5V, 1.8V, 1.5V	3.0V, 2.5V, 1.8V	1.8V

HPS EMAC Differences

EMAC Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Synopsys IP version	3.70a	3.70a	3.72a	3.73a
Number of controllers supported	2	2	3	3
Reduced Media Independent Interface (RMII) for 10/100	No	No	Yes	Yes
Reduced Gigabit Media Independent Interface (RGMII)	Yes	Yes	Yes	Yes
Serial timestamp interface	Yes	Yes	Yes	Yes
ECC protection for internal memory	Included	Included	Enhanced	Enhanced

continued...

EMAC Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
ECC errors can be directly injected from the ECC controller	N/A	N/A	Yes	Yes
FIFO size	Rx: 4 KB Tx: 4 KB	Rx: 4 KB Tx: 4 KB	Rx: 16 KB Tx: 4 KB	Rx: 16 KB Tx: 16 KB
HPS PHY interface I/O bank location	HPS I/O	HPS I/O	HPS shared I/O bank	HPS dedicated I/O bank
HPS I/O PHY RGMII-ID support	No	No	Facilitated with delay elements in I/O element	Enhanced support with delay elements in pin MUX(19)

HPS SPI Controller Differences

SPI Controller Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Synopsys IP Version	3.20a	3.20a	3.22a	4.00a
Number of SPI master cores	2	2	2	2
Number of SPI slave cores	2	2	2	2
Maximum master clock rate	60 MHz	60 MHz	60 MHz	60 MHz
Maximum slave clock rate	50 MHz	50 MHz	50 MHz	33.33 MHz
Programmable data frame size	4 to 16 bits	4 to 16 bits	4 to 16 bits	4 to 32 bits
SPI master bit rate clock ratio	$F_{spi\_m\_clk} \geq 2 \times \max(F_{sclk\_out})$			
SPI slave bit rate clock ratio	$F_{l4\_main\_clk} \geq 8 \times \max(F_{sclk\_in})$			$F_{l4\_main\_clk} \geq 12 \times \max(F_{sclk\_in})$
Toggle slave select signal between frames when in SPI mode and SCPH=0?	Yes	Yes	Yes	No (slave select signal stays low during data frames transfer)

HPS I²C Controller Differences

I²C Controller Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Synopsys IP Version	1.20a	1.20a	1.21a-lp02	2.00a
Number of controller instances	4	4	5	5
Controllers available to support Ethernet communication	2	2	3	3

Some of the inter-integrated circuit (I^2C) controllers can be used either for the EMAC or for general I^2C communication, as listed in the table above. Using an I^2C controller for Ethernet provides flexibility for the EMACs to use Management Data Input/Output (MDIO) or I^2C for PHY communication. The remaining I^2C controllers are available for general I^2C communication.

(19) Delay elements are more accurate than in the Arria 10 family. The skew range is larger and more consistent.

HPS UART Controller Differences

The HPS includes two 16550-compatible UART controllers to provide asynchronous serial communications. The UARTs support 16750-compatible automatic flow control.

UART Controller Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Synopsys IP Version	3.11a	3.11a	3.14b	3.15a
16550-compatible	Yes	Yes	Yes	Yes
Real-time clock flow trigger control	No	No	Yes	Yes

The UART controller uses two separate trigger levels for a DMA request and handshake signal to maximize throughput on the interface.

HPS CAN Controller Differences

The HPS Controller Area Network (CAN) controller is supported only in the Cyclone V SoC family.

EMAC Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Bosch D-CAN IP version	1.1.1	N/A	N/A	N/A

HPS Timer Differences

Timer Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Synopsys IP Version	2.05a	2.05a	2.08a	2.09a

HPS Watchdog Timer Differences

Watchdog Timer Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Number of watchdog timers	2	2	2	4
Synopsys IP Version	1.06a	1.06a	1.07c	1.08a

HPS CoreSight Debug and Trace Differences

CoreSight Debug and Trace Feature	Cyclone V SoC	Arria V SoC	Arria 10 SoC	Stratix 10 SoC
Supports Level 3 (L3) Cross Trigger Interface (CTI)	No	No	Yes	Yes
Trace width to HPS I/O	8	8	4 bits	16 bits
Trace width to FPGA I/O	32	32	16 bits	32 bits

Document Revision History

Table 8. Revision History for Differences Among Intel SoC Device Families

Date	Version	Changes
August 2018	2018.08.22	Corrections in *Booting and Configuration Differences*:

continued...

Date	Version	Changes
		• NAND configuration not supported by Intel Stratix 10 SoC • FPP configuration in Intel Stratix 10 SoC based on Avalon-ST
April 2018	2018.04.11	Correction in "HPS SDRAM Controller Subsystem Differences": LPDDR3 not supported in the Intel Stratix 10 SoC
May 2017	2017.05.06	Additional detail about: • MPU ACP support • MPU cache error correction • Clock implementation • Stratix 10 security features • HPS-FPGA bridge latency support • Supported NAND flash memory widths • USB 2.0 OTG PHY connections • Corrected EMAC IP version number • EMAC FIFO sizes • EMAC I/O bank usage • EMAC RGMII-ID support • Details about SPI controller frame sizes, clocks, bit rates, and slave select • UART compatibility features
November 2016	2016.11.11	• Added Stratix 10 SoC information • Reorganized for easier reference • Added IP version numbers for some third-party components • Added details about I/O configuration differences • Added booting and configuration differences
August 2014	2014.08.18	Updated Arria 10 SoC information
January 2014	2014.01.15	Initial release.