4. Stratix GX Board Design Guidelines

Introduction

Digital board design has become more complicated over the years. Devices have 0.13-μm gate lengths and are powered by 1.5-V power supplies. While the trend toward miniaturization continues, device speeds are increasing. FPGAs now have embedded transceivers that can support serial data transmission at 3.125 Gigabits per second (Gbps). The low-voltage supply results in decreased noise margin; therefore, small voltage noise on the board can cause a bit to flip. Similarly, voltage noise directly increases the clock jitter, which reduces the timing margin. If the jitter is large enough, the bit transition boundaries can become fuzzy, and the current data bit could be confused for the past or future bit. To reduce voltage and timing noise and ensure error-free data transmission, good design techniques are essential.

The following things are critical when designing a successful high-speed digital board:

- Clean power supply design (see “Power Circuitry” on page 4–6)
- Decoupling capacitor selection (see “Decoupling Circuitry Design” on page 4–13)
- Analog ground and power isolation (see “Ground Plane & Island Design” on page 4–30)
- Transmission line termination (see “Transmission Line Termination” on page 4–52)
- Crosstalk minimization (see “Crosstalk” on page 4–72)
- Impedance discontinuity minimization (see “Transmission Line Routing” on page 4–58)
- Proper differential signal routing (see “Transmission Line Routing” on page 4–58)

This document explains high-speed board design concepts and techniques as applied to Stratix® GX devices and explains the major aspects of successful high-speed board design. The Stratix GX device and the Stratix GX development board are used as the platforms for the tests and measurements described in this document. Topics covered include clock circuitry design, power circuitry design, power supply decoupling, transmission line topologies, length matching, AC versus DC coupling, termination techniques, time domain reflectometer (TDR) usage, and S-parameters.
Board Design Overview

A typical high-speed board design begins with a product requirements document, a concept review, and a functional specification. After the specification is finalized, actual system design begins with the selection of key components. At this point, timing analysis for all the interfaces and power analysis—to determine the power requirements—is performed. Based on the power analysis, power supply modules and regulators are chosen, and a decoupling scheme is specified. Based on the timing analysis, length-matching criteria for the buses is established. Upon completion of these tasks, as well as completion of the system design and selection of remaining components, the schematics are created. These are typically reviewed among engineers who make any necessary changes, after which they are given to the layout designer. A layout guidelines document, which specifies how to place components on the board and how to route the traces, is created and given to the layout designer as well.

A pre-layout simulation is performed to determine the ideal stackup, trace widths, spacing, and other routing requirements. Any changes to the schematic, based on the simulation results, are incorporated in the schematic and provided to the layout designer. When the layout is complete, a post-layout simulation is performed on the critical sections of the board to ensure that there are no major signal integrity problems. Based on the results of the post-layout simulation, any changes required are incorporated into the layout, and finally the layout is released to the fabrication house for board manufacturing.

Figure 4–1 shows a typical board design process.
Support Circuitry Design

Support circuitry includes clocks, power, and decoupling. This section contains detailed guidelines for designing these parts of a high-speed board.
Support Circuitry Design

Clock Circuitry

Clocks serve as references for digital signals and must be designed very carefully. Any noise on the clock signal reduces the timing margin for digital signals. Typically, on-board clocks are derived from crystal-based oscillators. For the Stratix GX development board, Altera use the standard 3.3-V SM7745DV series CMOS crystals from Pletronics for high-frequency applications. This crystal has ±50 ppm stability and less than 1 ps RMS jitter from 12 kHz to 20 MHz from the carrier. For low-frequency applications Altera uses the standard 3.3 V SM7745HV series CMOS crystals from Pletronics. The stability of this crystal is ±50 ppm, but the jitter is not specified. Altera recommends these or equivalent crystals.

For maximum noise immunity, the crystal oscillator’s CMOS output typically needs to be converted to a differential standard like LVDS before it is fed to the Stratix GX device. An ICS8545 CMOS to LVDS buffer from Integrated Circuit Systems, Inc. achieves this conversion. A side benefit of using a clock buffer like this one is that it provides multiple outputs. This feature is very helpful because clock lines need to have one source and one destination for best signal integrity.

Other things to remember for optimal clock performance are:

- Place the crystal oscillator close to the driver circuitry for best jitter performance.
- Route the differential clock lines tightly coupled to each other.
- The oscillators and the drivers need clean power supplies.
- Place series termination at the clock output if the trace is too long.
- Place parallel differential termination close to the receiver pins.

Whether a particular trace is too long depends on the edge rate of the clock and on the speed at which the signal propagates on the board. If the electrical length of the trace is small (1/10 or 10%)\(^1\) compared to the rise time, then no termination is needed. Otherwise, use series termination. The propagation speed for microstrip and stripline, two of the commonly used transmission line topologies, is shown in the following equations\(^2\):

\[
Speed(Microstrip) = \frac{1}{85 \sqrt{0.475\varepsilon_r + 0.67}} \text{ inches / ps}
\]

\(^1\)Some designers use 1/6 or 16% as the cut-off point. The important thing to remember is that the length needs to be small.

\(^2\)Refer to High-Speed Digital Design: A Handbook of Black Magic by Johnson and Graham, pp186-188.
Using \( \varepsilon_r \) of 4.5 for typical FR-4 material, the propagation speed for microstrip and stripline traces works out to be 0.007021 inches/ps and 0.005546 inches/ps, respectively. Expressed another way, the signals travel 142 ps/inch in microstrip traces and 180 ps/inch in stripline traces.

**Case Study:** As a case study, the microstrip trace length from the output of the 156.25 MHz crystal to the driver (see Figure 4–2) is about 0.28 in on the Stratix GX development board. The signal takes 142 * 0.28 = 39.76 ps to traverse this distance. The rise time of the crystal output is 1.0 ns (see the Pletronics SM7745HV data sheet). The signal transit time is less than 4% of the signal rise time, so no termination is needed. When the clock is being brought to the board through an SMA connector (J104), the trace length from the SMA to the clock driver is about four times the crystal transit time calculated earlier, in addition to the SMA cable length. In this case, a termination is definitely needed. Use R176 for termination, as shown in Figure 4–2.

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**Figure 4–2. Layout Example for Clock Distribution**

The specifications for some I/O standards always require termination regardless of the trace length. These include PCML, LVDS, LVPECL, SSTL-II, and HSTL-II.
Isolated Power & Ground Plane Design

Isolated power and ground planes are created by using ferrite beads. A ferrite bead acts as a DC short but presents an impedance to the passage of high-frequency noise. It can be beneficial in systems that have lots of switching noise. Sources of switching noise include switching power supplies and simultaneous switching outputs. For Stratix GX devices, Altera recommends isolating the high-speed ground (GND_GXB) from the digital ground (GND), so that the noise from the digital ground does not reach the high-speed circuitry. In the Stratix GX development board, there are three ground planes: GND, GND_PLL, and GND_GXB, for characterization purposes. For most high-density designs, Altera recommends only two ground planes: GND and GND_GXB. If the board does not have lots of switching circuitry and is otherwise cleanly designed, one ground plane is acceptable.

Currently, the benefits of split power planes for the transceiver quads are under evaluation. Preliminary tests suggest that for most cases the benefits of isolating power for the quads are minimal. See “Power Plane & Island Design” and “Ground Plane & Island Design” for more information.

Power Circuitry

As gate lengths shrink, the power supply voltages of transistors also decrease. As a result, the noise margin also decreases. The reduced noise margin makes the transistors even more sensitive to noise on the power supply. The features of the board must be understood before the power supply can be designed. Some key characteristics of a high-density board with one or more FPGAs include:

- Hundreds of I/O pins with varying voltage standards switching at several frequencies.
- The core LE use is highly unpredictable and depends on the actual design loaded. The user could load a design that uses close to 100% of the LEs, embedded memory, and hard logic (like transceivers), and run everything at full speed.
- Analog and digital signals on the board. For example, TTL switching is digital while Stratix GX transceiver outputs are analog signals.
- The potential for noise to couple between different power and ground planes.

Regulator Selection

Altera recommends selecting linear regulators as much as possible, because they are easy to design and their performance is less critical to layout. You must sometimes select switching regulators, because linear
regulators cannot supply the desired amount of power efficiently. In those cases, you must design and layout the switching regulators very carefully. All major switching components and traces must be closely contained on the same layer.

The Stratix GX development board uses Fairchild FAN5066 switching regulators (U36 and U37) for 3.3-V and 1.5-V digital supplies. Refer to “Switching Regulator Layout Example” on page 4–8 for details on the layout of these regulators on the Stratix GX development board.

To support a board with the characteristics listed earlier, the power circuitry must be able to do the following:

- Supply large amounts of current to the core and I/O voltages.
- Supply clean power and ground to sensitive analog components such as PLLs and transceivers.
- Maintain good efficiency to prevent excess heat dissipation on the regulators.

Voltage regulators come in two forms: linear and switching. Linear regulators are easy to design and provide very clean output voltage, but often they cannot provide large amounts of current without getting very hot. Switching regulators can provide large amounts of currents (over 10 A) with good efficiency, so there is no need for a heat sink. Switching regulators require very good design and layout practices to achieve good noise performance.

Use a switching regulator for the core supply, because current draw on the core can be high, and linear regulators cannot supply the necessary current without requiring a large heat sink. For example, if the core current needs to be 5 A, and the input and output voltages of the linear regulator are 3.3/1.5 volts, the heat dissipation would be approximately 5 * (3.3 – 1.5) = 9 Watts. This much heat requires a large heat sink on the linear regulator, which may not be possible to use on the board because of form factors, costs, or aesthetics.

For sensitive circuitry such as phase-locked loops (PLLs), transceivers, and double-data rate (DDR) memory, linear regulators are preferred. Choose the linear regulator based on the current requirements. Sometimes a small heat sink is required, depending on the current being drawn from the regulator and the voltage drop from the input to the output. Refer to AN 185: Thermal Management Using Heat Sinks for more details on regulator and heat sink selection.

If there are hundreds of LVTTL signals on the I/O, all of which can potentially switch at the same time, a switching regulator may be necessary, because the current requirement can be several Amperes.
Switching Regulator Layout Example

Linear regulators are relatively easy to design and lay out. Switching regulators, on the other hand, require a great deal of care. Typically schematics for both the linear and switching regulators can be taken directly from the vendor data sheet or the application note. Some of the linear regulators Altera recommends include Micrel MIC29502BU, National LMS1585 and National LP2995M. Similarly, Altera has used Fairchild FAN5066 for switching regulators with good results.

With switching regulators, component layout is extremely important. To explain this point further, consider an actual example. Figure 4–3 shows a capture plot of the FAN5066 circuit from the Stratix GX development board.

This switching regulator runs from a 5.0-V supply and can generate an output voltage that equals the voltage reference. Set the reference voltage on the board by applying the required voltage on the CNTRL pin (pin 16). The 12.0-V supply is used only for biasing and draws very little current. The overall circuitry consists of the FAN5066 switching controller, external FETs (Q3 and Q4) to boost the current output capability, and the associated resistors, diodes, inductors, and capacitors as recommended by the manufacturer.

The switching regulator is essentially a feedback loop consisting of a pulse width modulator (PWM). The feedback loop compares the actual output voltage to the desired voltage (reference voltage). If the actual output is less than desired, then the high drive (HIDRV) output is asserted, which turns the upper field effect transistor (FET) on and charges the output capacitor (C73). The end result is that the output voltage climbs. If the actual output is more than desired, the low drive (LODRV) output is asserted, which turns the lower FET on and discharges the output capacitor (C73). The end result is that the output voltage drops. In steady state the output voltage equals the input reference voltage. Figure 4–4 shows the schematic of the switching regulator used in the SGX development board.
Figure 4–3. Switching Regulator Schematic

Make This Trace as Short as Possible

Clean Output (Vout)
Figures 4–5 through 4–7 show the waveforms at the gates of the upper and the lower FET. While the lower FET switches from about 0 V to 5 V, the upper FET switches from approximately 0 V to 10 V. These are large magnitudes on a board with 3.3-, 2.5-, or 1.5-volt logic signals. Routing fast switching signals close to sensitive analog and digital signals and across multiple layers can cause the switching signals to radiate energy to other critical traces. Consequently, it is very important to contain the large switching signals compactly on the same layer.
Figure 4–5. Switching Waveforms at the Output of the FET

Figure 4–6. Switching Waveforms at the Gate of the Upper FET
Altera has compared the performance improvement of the output ripple when using a good layout versus a poor layout. The results of excessive ripple at the output of a switching regulator because of poor board layout, are shown in Figure 4–8. The output ripple is almost 1.5 V peak to peak. This example may be an extreme case, but the board in this example was designed with an intentionally poor layout. The layout was later improved by reducing the length of the HIDRV and LODRV signals and minimizing via count to determine how much improvement would result. With the improved layout, the noise decreased to about 71 mV peak to peak.
Altera recommends that you follow the switching regulator layout of the Stratix GX development board and review the Fairchild Semiconductor FAN5066 data sheet in detail. The guidelines are summarized here:

- Place all components on the same layer, if possible.
- Minimize the trace lengths for the gate drives (HIDRV and LODRV).
- Place all the 0.1 \( \mu \text{F} \) decoupling capacitors close to the pins.
- Place the HIDRV, LODRV, VCCQP and the FET output traces far away from the analog sections of the chip, including VCNTRL (pin 16), VFB, and IFB (feedback pins 4 and 5), and C\text{EXT} (pin 1). Do all routing for the switching signals (VCCQP, HIDRV, LODRV, and FET output) on the component layer to avoid radiation to multiple layers through the vias.
- Surround the capacitor connected to pin 1 (C\text{EXT}) with a ground guard trace and place a ground plane beneath it.

**Decoupling Circuitry Design**

You can divide decoupling capacitor circuitry into two categories: bulk decoupling and local decoupling. Bulk decoupling uses large decoupling capacitors (often tens to hundreds of microfarads), usually placed close to the regulators and designed to work for low frequencies. Local decoupling involves smaller capacitors (typically 2.2 \( \mu \text{F} \), 0.1 \( \mu \text{F} \), or 0.01 \( \mu \text{F} \)) that are placed close to the chips and are designed to decouple high frequency noise from the power supply.
Determining the number of decoupling capacitors depends on the expected current draw from the power supply, the rate of current change, and the desired impedance between the power plane and the ground plane at the frequency of interest. For switching (or sometimes even linear) regulators, the manufacturers specify a certain minimum bulk decoupling at the output of the regulator for stability and for ensuring a clean output.

**Bulk Decoupling**

The amount of bulk decoupling needed depends on the number of outputs switching, the load capacitance, the slew rate, and the inductance of the planes and routing traces and vias.

Estimate the amount of bulk decoupling needed as follows:

1. Determine the worst case current draw on the power net. This draw depends on how many gates can switch at the same time and how much load they need to drive.

   For example, assume there are 100 3.3-V LVTTL I/O pins switching, each with 11.5 pF loads, and the switch is completed in 1 ns. (These values are fairly typical for Stratix and Stratix GX devices.) The total worst case current required is:

   \[ \Delta I = NC \frac{\delta V}{\delta t} = 100 \times 11.5 \text{ pF} \times \frac{3.3V}{1\text{ ns}} = 3.8\text{Amps} \]

2. Determine the maximum noise margin degradation allowed in the logic circuit. This value depends on the standard being used. For LVTTL, the threshold is shown in Table 4–1.

   The noise margin between \( V_{OH} \) and \( V_{IH} \) is \( 2.4 - 1.7 = 0.7 \text{ V} \). The margin between \( V_{OL} \) and \( V_{IL} \) is \( 0.7 - 0.45 = 0.25 \text{ V} \). Therefore, the worst case noise margin is 0.25 V, the absolute maximum value of noise allowed on the power supply while still guaranteeing successful data transfer. A good design allows for safety margin, so this example specifies 0.1 V as the maximum value of noise permitted. Call this parameter \( \Delta V \).

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{CCIO} )</td>
<td>Output supply voltage</td>
<td></td>
<td>3.0</td>
<td>3.6</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IH} )</td>
<td>High-level input voltage</td>
<td></td>
<td>1.7</td>
<td>4.1</td>
<td>V</td>
</tr>
</tbody>
</table>

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Support Circuitry Design
3. Using $\Delta V$ from step 2 and $\Delta I$ from step 1, determine the maximum impedance allowed on the power supply plane. In the example, it equals $Z_{\text{max}} = \Delta V / \Delta I = 0.1 / 3.8 = 26.3 \text{ mW}$.

4. Next, determine the power supply wiring inductance. This inductance depends on the actual routing path of the power supply to the plane and the device pin. This path includes the vias, inductance of the balls to the actual connection on the die, inductance of the regulator output pin, and inductance of the actual routing from the regulator to the via. Approximate the inductance of the via with the following formula:

$$L_{\text{via}} = 5.08h[\ln\left(\frac{4h}{d}\right) + 1]$$

Assume that the height ($h$) of the via is 63 mils and that the diameter is 10 mils. Using these values in the above formula, the via inductance is 1.4 nH. These values are typical for vias on the Stratix GX development board for a signal traversing about 2/3 of the board thickness. Divide the via inductance by the number of vias that are in parallel. For 10 vias, the total via inductance is 0.14 nH. Other factors that add to this result are the ball-to-die connection and the inductance of the traces, which are harder to estimate and depend on the exact layout. Inductance of the plane is very small (less than 1 nH) if the physical dimensions are at least 1” by 1.” You can lump all these inductances into a single approximation of 5 nH ($L_{\text{total}} = 5 \text{ nH}$), which represents the worst case inductance on a typical system, assuming wide traces for power distribution.

Given the value for the power supply inductance, you can now estimate the frequency above which decoupling is required. Use this equation:

$$F_{\text{critical}} = \frac{Z_{\text{max}}}{2\pi L_{\text{total}}} = \frac{26.3 \times 10^{-3}}{2\pi 5 \times 10^{-9}} = 838 \text{ kHz}$$

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Minimum</th>
<th>Maximum</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IL}$</td>
<td>Low-level input voltage</td>
<td></td>
<td>−0.5</td>
<td>0.7</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>High-level output voltage</td>
<td>$I_{OH} = -4 \text{ to } -24 \text{ mA}$</td>
<td>2.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low-level output voltage</td>
<td>$I_{OH} = 4 \text{ to } 24 \text{ mA}$</td>
<td></td>
<td>0.45</td>
<td>V</td>
</tr>
</tbody>
</table>
5. Finally, use this equation to calculate the value of the decoupling capacitor:

\[
C_{\text{bypass}} = \frac{1}{2\pi f^2_{\text{critical}} Z_{\text{max}}} = \frac{1}{2\pi \times 838 \times 10^3 \times 26.3 \times 10^{-3}} = 7.25 \mu F
\]

Consider the example on the Stratix GX development board. There are about 350 LVTTL signals on the Stratix device (on banks 1, 2, 3, 4, 7, and 8). The calculation above was for 100 LVTTL signals. For 350 signals, the required value of bulk decoupling increases by a factor of \((3.5)^2\), or 12.25. Therefore, bulk decoupling equals 7.25 * 12.25 = 89 \mu F. The development board uses a 100 \mu F capacitor on the 3.3-V power supply net (3.3V_S_IO) for bulk decoupling for the Stratix device. This is in addition to the bulk decoupling required by the switching regulators and the associated filters at the output. With this level of decoupling, there is good performance.

**Local Decoupling**

Local decoupling is designed to work at high frequencies. Unfortunately, at high frequencies, discrete capacitors are rarely effective by themselves. There must be a combination of discrete capacitors and plane capacitance. The analysis is quite involved and its accuracy is not easy to verify. So, experimental data is more helpful for creating design guidelines. Altera has conducted several experiments on this topic. Based on these experiments, Altera recommends about one decoupling capacitor per power pin. The results of simulations using Agilent design system (ADS) software determined the values of capacitors required.

The amount of local decoupling is more difficult to determine, because high frequency effects are more pronounced for local decoupling. Altera recommends using one capacitor per power pin. More detailed guidelines for specific situations will be available in the near future. You should not mix values of capacitors, because doing so can create resonant peaks of impedances. In most cases it is best to choose the highest value of the capacitance available in the package required by the designer.

**Simulating Decoupling Circuits**

The efficacy of a decoupling scheme is indicated by the impedance between the power plane and the ground plane across the frequency of interest. The goal of a power supply decoupling scheme is to achieve the lowest possible impedance across the frequency of interest. If the impedance is low, then the noise on the power rail is shunted to the ground, whereas if the impedance is high, the noise stays on the power rail and can cause the circuitry to malfunction.
In this simulation, Altera placed 25 decoupling capacitors of different values in parallel and measured the impedance from 1 MHz to 10 GHz. The frequency of interest can be different for each application, so focus on the frequency band of interest for your application. Using 25 decoupling capacitors gives a realistic number of capacitors used in a typical decoupling scheme. The behavior of vias, pads, and traces were captured using the multilayer transmission line models of ADS, which considers the dielectric material and its dissipative losses.

Eight different cases, summarized in Table 4–2, were simulated to get a wide range of capacitor ratios.

<table>
<thead>
<tr>
<th>Table 4–2. Simulation Cases</th>
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<tbody>
<tr>
<td>Case</td>
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<tr>
<td>1</td>
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<tr>
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<td>3</td>
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<tr>
<td>4</td>
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<tr>
<td>5</td>
</tr>
<tr>
<td>6</td>
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<tr>
<td>7</td>
</tr>
<tr>
<td>8</td>
</tr>
</tbody>
</table>

*Figure 4–9* shows the simulation setup with only one capacitor (only one capacitor is shown for clarity), including the parasitics, pads, routing trace to the vias, and the vias themselves. For the cases shown in Table 4–2, the model of the capacitor shown in Figure 4–9 was applied repeatedly in parallel.

Each capacitor is modeled as a series RLC circuit. The parasitic resistance (R) and the parasitic inductance (L) were obtained from the data sheet published by the manufacturer of the capacitor. The capacitor pads on the board were modeled as 42-mil by 32-mil square pads. The vias were modeled as circular vias with pad diameters of 20 mils and hole diameters of 10 mils. The routing distance from the capacitor pad to the via was modeled as a trace, 50 mils long and 25 mils wide, equal to the total distance for routing on both sides of the capacitor. These are typical values and were extracted from the Stratix GX development board layout design.
Table 4–3 shows the extracted models of 470 pF, 1000 pF, 0.01 μF, 0.1 μF, and 2.2 μF capacitors from the vendor datasheets (Panasonic and AVX).

<table>
<thead>
<tr>
<th>Capacitor Value</th>
<th>Part Number</th>
<th>Vendor</th>
<th>Parasitic L (nH)</th>
<th>Parasitic R (Ω)</th>
<th>SRF (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.1 μF</td>
<td>ECJ1VB1C104K</td>
<td>Panasonic</td>
<td>1.50</td>
<td>0.07</td>
<td>13</td>
</tr>
<tr>
<td>0.01 μF</td>
<td>ECJ1VB1C103K</td>
<td>Panasonic</td>
<td>0.83</td>
<td>0.10</td>
<td>55</td>
</tr>
<tr>
<td>2.2 μF</td>
<td>08056D225KAT2A</td>
<td>AVX/Kyocera</td>
<td>1.00</td>
<td>0.02</td>
<td>3.4</td>
</tr>
<tr>
<td>470 pF</td>
<td>ECJ-0EB1E471K</td>
<td>Panasonic</td>
<td>0.86</td>
<td>0.10</td>
<td>250</td>
</tr>
<tr>
<td>0.001 μF</td>
<td>ECJ-1VB1H102K</td>
<td>Panasonic</td>
<td>1.13</td>
<td>0.05</td>
<td>150</td>
</tr>
</tbody>
</table>

Figure 4–10 shows the simulated impedance profile for the eight cases listed in Table 4–2.
The following observations were made:

- Decoupling at very high frequencies cannot be achieved by discrete capacitors. It must be done with a sandwiched power and ground plane.

- Traditionally, the number of capacitors is doubled for every lower decade in value. For example, beginning with one 0.1 μF capacitor, you would use two 0.01 μF capacitors. Case 1 in Table 4–2 on page 4–17 approximates this behavior. However, this approach often performs worse than when using equal numbers of capacitors of equal values, or even reversing the ratio (number of capacitors halved for each decade lower in value).

- Using a very large number of values can cause resonance spikes at multiple frequencies, so use as few values as possible to contain the magnitude of the resonance spike.
Using all 2.2 µF capacitors gives the lowest impedance profile without any resonance spikes. Although 1000 pF capacitors (when used in conjunction with 2.2 µF caps) do give the low impedance dip at higher frequencies, they also result in the corresponding resonance spike.

To study how the ratio of 2.2 µF versus 1000 pF capacitors affects the impedance profile, Altera performed further simulations. Figure 4–11 shows the impedance profiles when using all 24 2.2-µF caps versus using a mix of 2.2 µF and 1000 pF. Only 24 capacitors were used in this simulation as opposed to 25, allowing for easy ratios. This difference is not significant. The lower red graph in Figure 4–11 shows the case when all 24 capacitors are 2.2 µF. It has the smoothest impedance profile and is lower in impedance than other cases, except for a dip at 129 MHz. If a particular board has significant noise at the frequency of the dip (approximately 129 MHz), a 1000 pF capacitor is helpful. However, you must ensure that there is negligible noise at the resonant peaks. The resonant peaks occur at 54 MHz, 75 MHz, 92 MHz, 106 MHz, and 118 MHz, depending on the ratio of 1000 pF caps to 2.2 µF caps.

Figure 4–11. Impedance Profile With a Combination of 2.2 µF & 0.001 µF Capacitors
Based on the simulation results, it is important to select the highest value possible in a particular package, because these capacitors have the lowest impedance for the largest band of frequency. Examples include 2.2 µF, 1.0 µF, and 0.1 µF. Do not go lower than that unless there is a compelling reason to do so, such as the presence of a strong noise spike at the exact frequency where the lower value capacitor resonates. Also, do not mix capacitor values (for example using 10 of 0.1 µF and 10 of 0.001 µF). This mixing can create undesired resonances.

The Stratix GX development board uses many mixed capacitor values for decoupling, not because it is the best approach but because it allows the flexibility to test several approaches and values.

**Plane Capacitance**

For very high frequencies (above 300 MHz), decoupling using discrete capacitors is less effective. Use power plane capacitance for decoupling noise at these frequencies.

You can understand the concept of plane capacitance by studying the classic parallel plate capacitor, shown in Figure 4–12.

*Figure 4–12. Parallel Plane Capacitance*

An electric field is created when there is a power plane next to a ground plane. The upper area in Figure 4–12 shows the power island or plane, the lower area shows the ground plane, and the arrows represent the electric field lines. This electric field gives rise to a capacitance, the magnitude of which is shown by:

\[ C = \frac{\varepsilon_0 \varepsilon_r A}{h} \]
where

\[ \varepsilon_0 = \text{permittivity of free space} \]

\[ \varepsilon_r = \text{relative permittivity of the dielectric used} \]

\[ A = \text{area of overlap} \]

\[ h = \text{separation of the planes.} \]

If there are ground planes on both sides of the power island, then the capacitance needs to be calculated for each side and added to determine the total capacitance.

Plane capacitance is the primary way of decoupling at high frequencies, so it must be an integral part of any high speed design. At high frequencies (above 300 MHz), the discrete capacitors are not very effective.

As an example, consider the following.

**Example:** Determine the parallel plate capacitance for 1 square inch of area overlap in an FR-4 dielectric \((\varepsilon_r = 4.5)\) and a separation of 4 mils.

**Solution:**

\[ h = 4 \text{ mils} = 1.016 \times 10^{-4} \text{ m} \]

\[ \varepsilon_0 = \text{permittivity of free space} = 8.85 \times 10^{-12} \text{ F/m} \]

\[ A = 1 \text{ sq inch} = 6.4516 \times 10^{-4} \text{ m}^2 \]

\[ \varepsilon_r = 4.5 \]

Applying these numbers to the equation on page 4–21 yields \( C = 253 \text{ pF} \). Therefore, there is about 253 pF per square inch of area overlap on a typical FR-4 board with 4 mils of separation. The value scales inverse linearly with separation and linearly with area.

Altera has successfully used plane capacitance in several of its boards.

**Case Study:** Altera designed two boards with the Stratix GX test chip. On the first board, the separation between the ground and the 1.5-V transceiver power plane was about 16 mils. On the second board, ground
islands were added (with approximate areas of 0.13 square inches) next to the 1.5 V transceiver plane. The islands were on the next layer and the separation was 4 mils. Figure 4–13 shows the islands as they appear on the board layout.

**Figure 4–13. Ground Island Used With the 1.5V_XCVR Plane to Increase Decoupling at High Frequencies**

Figures 4–14 and 4–15 show the reduction in noise after adding the islands. The addition of the islands reduced the noise from 70 mV p-p to less than 50 mV p-p under the same experimental conditions.
When using split ground planes, it is best to pair the correct ground plane with the correct power plane. For example, 1.5V_XCVR and GND_GXB planes and islands should be used rather than 1.5V_XCVR and GND.

**Plane & Island Design**

The following sections discuss various issues related to the design of power planes, ground planes, and power and ground islands.
Power Plane & Island Design

Stratix GX devices have many power and ground pins, and it is important to know how to connect them on the board. Table 4–4 shows the list of power and ground pins and how they connect on the Stratix GX development board. For the actual pin numbers, refer to the pin tables at www.altera.com.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Description</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCCP_B[17..13]</td>
<td>Digital power for Stratix GX transceiver quads (banks) 13 through 17</td>
<td>1.5 V (linear)</td>
</tr>
<tr>
<td>VCCT_B[17..13]</td>
<td>Transmitter power for Stratix GX transceiver quads (banks) 13 through 17</td>
<td>1.5 V (linear)</td>
</tr>
<tr>
<td>VCCR_B[17..13]</td>
<td>Receiver power for Stratix GX transceiver quads (banks) 13 through 17</td>
<td>1.5 V (linear)</td>
</tr>
<tr>
<td>VCCG_B[17..13]</td>
<td>Power for Stratix GX transceiver quads (banks) 13 through 17 guard rings.</td>
<td>1.5 V (linear)</td>
</tr>
<tr>
<td>VCCA_B[17..13]</td>
<td>Analog power for Stratix GX transceiver quads (banks) 13 through 17</td>
<td>3.3 V (linear)</td>
</tr>
<tr>
<td>VCCG_PLL[12,11,8,6,5,2,1]</td>
<td>Power supply for the guard ring of PLLs</td>
<td>1.5 V (linear)</td>
</tr>
<tr>
<td>VCCA_PLL[12,11,8,6,5,2,1]</td>
<td>Analog power supply for PLLs</td>
<td>1.5 V (linear)</td>
</tr>
<tr>
<td>VCC_PLL5_OUTA</td>
<td>PLL output buffer supply for PLL5 outputs [1..0]</td>
<td>3.3 V, 2.5 V or 1.5 V (1) (linear)</td>
</tr>
<tr>
<td>VCC_PLL5_OUTB</td>
<td>PLL output buffer supply for PLL5 outputs [3..2]</td>
<td>3.3 V, 2.5 V or 1.5 V (1) (linear)</td>
</tr>
<tr>
<td>VCC_PLL6_OUTA</td>
<td>PLL output buffer supply for PLL6 outputs [1..0]</td>
<td>3.3 V, 2.5 V or 1.5 V (1) (linear)</td>
</tr>
<tr>
<td>VCC_PLL6_OUTB</td>
<td>PLL output buffer supply for PLL6 outputs [3..2]</td>
<td>3.3 V, 2.5 V or 1.5 V (1) (linear)</td>
</tr>
<tr>
<td>VCCINT</td>
<td>Digital power supply for device internal power</td>
<td>1.5 V (linear or switching)</td>
</tr>
<tr>
<td>VCCIO[8..7, 4..1]</td>
<td>Power supply for I/Os in the banks 8, 7, 4..1</td>
<td>Variable (2) (linear or switching)</td>
</tr>
</tbody>
</table>
Support Circuitry Design

Table 4–4. Stratix GX Power & Ground Pins (Part 2 of 2)

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>Description</th>
<th>Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>GNDG_PLL[12,11,8,5,2,1]</td>
<td>Ground for the guard rings of PLLs 1, 2, 5, 6, 8, 11, and 12</td>
<td>0 V</td>
</tr>
<tr>
<td>GNDA_PLL[12,11,8,6,5,2,1]</td>
<td>Analog ground for PLLs 1, 2, 5, 6, 8, 11, and 12</td>
<td>0 V</td>
</tr>
<tr>
<td>GND_GXB</td>
<td>Ground for the high-speed circuitry in the 3.125 Gbps transceivers</td>
<td>0 V</td>
</tr>
<tr>
<td>GND</td>
<td>General-purpose ground</td>
<td>0 V</td>
</tr>
</tbody>
</table>

Notes for Table 4–4:
(1) Connect this pin to the desired voltage depending on the I/O standard for the PLL outputs chosen. For example, in the Stratix GX development board, VCC_PLL6_OUTA and VCC_PLL6_OUTB connect to 2.5 V to allow an SSTL-II clock (2.5 V I/O) on the PLL6 output for the double data rate (DDR) memory application.
(2) Connect this pin to the I/O standard of the signals on the bank. This value is 3.3 V for LVTTL, 2.5 V for SSTL-II, and so on. On the Stratix GX development board, VCCIO7 connects to 2.5 V because the board uses the SSTL-II I/O standard on that bank. On other banks, it connects to 3.3 V.

Table 4–5 also shows the recommended regulator (linear or switching). The circuitry pertaining to PLLs and transceivers should be connected to voltages generated from linear power supplies. General purpose I/O and core supplies can be switching or linear. It is always better to use linear if possible, but for some I/Os and cores, the current draw might be too large.

The transceivers have many types of power supply pins. Altera recommends that you isolate the receive (VCCR_B[17..13]) and transmit (V CCT_B[17..13]) power supplies of each quad with a ferrite bead. The reason behind the isolation is to prevent noise from one quad leaking to the other quads. The digital power supply (V CCP_B[17..13]) can be shared among all the quads because it is less sensitive to noise. The guard power supply VCCG_B[17..13] can also be shared among quads. Use the islands shown in Table 4–5:

Table 4–5. Islands Used for Stratix GX Transceiver Quads (Part 1 of 2)

<table>
<thead>
<tr>
<th>Islands</th>
<th>Quads</th>
</tr>
</thead>
<tbody>
<tr>
<td>Island 1</td>
<td>Use for quad 1 VCCT and VCCR pins (VCCT_B13 and VCCR_B13)</td>
</tr>
<tr>
<td>Island 2</td>
<td>Use for quad 2 VCCT and VCCR pins (VCCT_B14 and VCCR_B14)</td>
</tr>
<tr>
<td>Island 3</td>
<td>Use for quad 3 VCCT and VCCR pins (VCCT_B15 and VCCR_B15)</td>
</tr>
</tbody>
</table>
Table 4–5. Islands Used for Stratix GX Transceiver Quads (Part 2 of 2)

<table>
<thead>
<tr>
<th>Islands</th>
<th>Quads</th>
</tr>
</thead>
<tbody>
<tr>
<td>Island 4</td>
<td>Use for quad 4 VCCT and VCCR pins (VCCT_B16 and VCCR_B16)</td>
</tr>
<tr>
<td>Island 5</td>
<td>Use for quad 5 VCCT and VCCR pins (VCCT_B17 and VCCR_B17)</td>
</tr>
<tr>
<td>Island 6</td>
<td>Use for VCCP_B[17..13], for example, digital supply for all quads</td>
</tr>
<tr>
<td>Island 7</td>
<td>Use for VCCG_B[17..13], for example, guard supply for all quads</td>
</tr>
</tbody>
</table>

Note to Table 4–5:
(1) Island 5 is required only for the 5-quad devices.

Figure 4–16 shows a block diagram of the islands.
Figure 4–16. Block Diagram Representation for Quad Isolation

Note to Figure 4–16:
(1) Island 5 is required only for the 5-quad devices.

Altera has successfully used the island approach to powering the Stratix GX transceivers on the Stratix GX development board. Figure 4–17 shows the section of the schematic that shows the islands. The net named 1.5V_XCVR is the output of a linear regulator that is split into seven islands, namely: 1.5V_XCVR1, 1.5V_XCVR2, 1.5V_XCVR3, 1.5V_XCVR4, 1.5V_XCVR5, 1.5V_VCCP, and 1.5V_VCCG.

Altera is currently evaluating the degree to which the islands help in reducing jitter.
Figure 4–18 shows the layout of six of the islands. The 1.5V_VCCG (guard) island is on a different layer because of layout constraints.
Ground Plane & Island Design

The Stratix GX development board has three types of ground pins: GND, GND_GXB and GND_PLL. GND_GXB is used for 3.125 Gbps transceiver ground, GND_PLL is used for PLL ground, and GND is used for general purpose ground on the board. In the die, GND_GXB and GND are separate planes, but they are connected by a trace at the package level. GND_PLL does not have a separate plane and is connected to the GND plane at the package level.
When designing your board you must decide whether to connect all the ground pins to a single ground plane on the board or create separate ground planes for GND\_GXB, GND, and GND\_PLL and connect them by using ferrite beads. This is a difficult trade-off, and there are two schools of thought in the industry regarding splitting ground planes.

Proponents of isolating ground planes say that it is good for systems that can generate a lot of noise because of switching I/Os or power supplies. The idea is that the ferrite beads attenuate the noise leaking from the system ground (which can be noisy) to the clean ground. Noise-sensitive analog subsystems like the transceivers require clean power and ground, and the isolation provides better performance. The ferrite beads must be carefully selected to allow for plenty of current handling, low DC voltage loss, and high AC impedance. See “Resistors, Capacitors, Inductors & Ferrite Beads” on page 4–77 for more details.

Supporters of the solid ground plane approach claim that there is no benefit to isolating ground planes, because noise cannot simply disappear from the ground plane and reaches the analog circuitry by some path or other. The layout is also complicated by having isolated ground planes because more layers might be needed. If the same plane is split into two, instead of adding a new layer, the layout designer must ensure that no critical signals cross over the split, because the split causes impedance discontinuity.

There is no one answer on this topic that applies to all systems. If the system is relatively simple without too many fast switching I/Os, and if there are no switching regulators, a solid ground plane is unlikely to cause problems. However, if the system has many fast, high-amplitude digital signals switching and noisy external components such as switching regulators, Altera recommends isolating ground planes.

The Stratix GX development board uses an isolated ground approach. There are three distinct ground nets: GND, GND\_PLL, and GND\_GXB, separated by several ferrite beads. Figure 4–19 shows a section of the Stratix GX development board schematic highlighting the isolation of the ground planes. Many ferrite beads were used in parallel to facilitate testing with several possible combinations.

Altera tested the performance of this system with the ferrite beads intact, as shown in Figure 4–19, and with them shorted to a wire. The Stratix GX EP1SGX40 device had about 72% of its LEs used with a design that had Gray code counters. The Stratix GX device had a DDR interface running at 200 MHz and 17 channels of SPI-4.2 data running at 1 Gbps per channel. The LE usage was about 46%. The Stratix GX device also had 19 channels of transceivers running at PRBS$^5$ - 1 data at 3.125 Gbps in an external loopback. The transmitter output of the 20th channel was sent to
an oscilloscope to observe the jitter and the eye diagram. This setup should result in a fairly heavy load for the devices and should generate a good deal of noise on the power planes. The test setup was identical for both tests, except for the shorted ferrite beads.

The tests showed a jitter improvement of approximately 10% when isolating the ground planes. If the devices are loaded even more fully, the improvement is even greater. If the devices are lightly loaded, the improvement is less.

Figure 4-19. Isolation of GND, GND_GXB & GND_PLL

Based on the test results and the benefit of isolating ground planes for noisy boards, Altera® recommends isolating the GND_GXB and GND planes with ferrite beads. To determine how many ferrite beads to use,
consider the following. The power consumption per quad is about 450 mW, so the current draw is about 450 mW / 1.5 = 300 mA. Therefore, the total expected current draw is about 1.5 Amps. Each ferrite bead has 25 mW of DC resistance. So, if there is one ferrite bead, the voltage drop is 37.5 mV, which is 2.5% of the 1.5-V supply. To reduce this drop, use multiple ferrite beads in parallel. On the Stratix GX development board, there are five beads in parallel, so that the voltage drop is reduced to 0.5% of the supply voltage.

For the GND_PLL plane, it is not crucial to use a separate ground plane. At the device package level, this plane shares the ground plane with the general-purpose logic ground. There is a separate plane on the development board for GND_PLL for testing flexibility.

Altera recommends two ground planes, GND and GND_GXB, isolated by ferrite beads. These planes are especially important for complex boards with many noisy signals and switching regulators. If the board does not have switching regulators or switching signals, and it is otherwise very cleanly designed, one ground plane is acceptable. Altera recommends connecting the PLL ground pins directly to the system GND.

**Transmission Lines**

This section discusses transmission line designs for high-speed digital boards.

**Transmission Line Topologies**

This section provides a brief overview of the main transmission line topologies commonly used in high-speed digital boards. Refer to any transmission line design book, such as Brian Wadell’s *Transmission Line Design Handbook*, for impedance equations and design techniques.

**Striplines**

The following sections detail the variations on stripline design topologies.

**Simple Stripline**

Simple stripline is a planar type transmission line well suited for multilayer PCB design. *Figure 4–20* shows the basic structure of this transmission line. A thin, centered conductive strip with width W placed between two conductive planes separated by a dielectric with thickness B is the most basic stripline structure.
Figures 4–21 and 4–22 show the frequency domain simulation setup and results for a 50 Ω simple stripline, respectively.
Offset Stripline

The offset stripline configuration is shown in Figure 4–23. The only difference between the structure of the offset stripline and the normal stripline is that the conductor strip is not placed at the center (B/2 distance from any of the planes). The relative position of the conductor strip is S from B/2. This transmission line is useful for single-ended signals routed between a ground plane and a power plane. The strip is placed closer to the ground plane, which is less noisy than the power plane. In this way there is less noise power coupled to the signal and an improved S/N ratio without the need for an extra ground plane. You must use this structure when the dielectric between the planes is constructed of three layers of dielectrics (two cores, one prepeg, or vice versa). In the Stratix GX development board there are two cores and one prepeg. This arrangement of dielectrics produces better results because the cores have lower permittivity and thickness tolerances than prepegs.
Figures 4–24 and 4–25 show the frequency domain simulation setup and results for a 50 \( \Omega \) offset stripline, respectively.
Figure 4–25. Simulation Results for an Offset Stripline

Edge-Coupled Differential Stripline

The edge-coupled differential stripline is shown in Figure 4–26. Altera recommends using differential transmission lines in noisy environments where the common mode noise is suppressed in the receiver. This type of transmission line requires some degree of coupling between the two conductive strips. The coupling is directly proportional to the distance S. The differential transmission lines have two operation modes. Even mode, in which both traces are excited with equal amplitude and phase, and odd mode, in which the traces are excited with equal amplitude but one is 180° out of phase. This structure must be analyzed as one unit and with the proper excitation. For differential signaling, the odd mode is the desired operation mode for canceling common mode noise.

Figure 4–26. Edge-Coupled Differential Stripline
Figures 4–27 and 4–28 show the frequency domain simulation setup and results for a 100-Ω edge-coupled differential stripline, respectively.

The differential impedance is:

\[ Z_{\text{DIFF}} = 2 \times (Zo) \]

If you excite one port and terminate all others (three) with its characteristic impedance \( Zo \) (50 Ω) the input impedance is:

\[ Zo = \sqrt{Z_{\text{oe}} \times Zo} \]

where:

- \( Z_{\text{oe}} \) is the even mode characteristic impedance
- \( Zo \) is the odd mode characteristic impedance
- \( Z_{\text{DIFF}} \) is the differential characteristic impedance
- \( Zo \) is the characteristic impedance

**Figure 4–27. Simulation Setup for an Edge-Coupled Differential Stripline**
Edge-Coupled Differential Offset Stripline

The edge-coupled differential offset stripline topology, shown in Figure 4–29, is used when an odd number of dielectric layers exists between the planes. The signals in this dielectric arrangement are routed closer to one of the planes. This transmission line offers all the advantages of the differential transmission lines, plus the flexibility to use wider traces without the penalty on the total board thickness.

Figures 4–30 and 4–31 show the frequency domain simulation setup and results for a 100-Ω edge-coupled differential offset stripline, respectively. The Stratix GX development board contains many edge-coupled
differential striplines. Examples from the board are discussed in “Crosstalk” on page 4–72. This topology is also known as dual stripline, because there are two signal layers between the two power planes.

Figure 4–30. Simulation Setup for an Edge-Coupled Differential Offset Stripline

Figure 4–31. Simulation Results for an Edge-Coupled Differential Offset Stripline

Broadside-Coupled Differential Stripline
Broadside-coupled differential stripline, shown in Figure 4–32, has some advantages over the edge-coupled differential stripline, including higher coupling and easier routing. The disadvantages are the possibility of the
traces becoming too narrow for the manufacturability of the board and the board becoming too thick to compensate for the trace-width thickness ratio.

This configuration is helpful when differential high-speed lines reside in the inner rows of the BGA, and it is impossible to route two lines (one differential pair) between vias or pads.

**Figure 4–32. Broadside-Coupled Differential Stripline**

Figures 4–33 and 4–34 show the frequency domain simulation setup and results for a 100-Ω broadside-coupled differential stripline, respectively.

**Figure 4–33. Simulation Setup for a Broadside-Coupled Differential Stripline**

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**Figure 4–34. Simulation Results for a Broadside-Coupled Differential Stripline**
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**Figure 4–34. Simulation Results for a Broadside-Coupled Differential Stripline**

The broadside-coupled differential offset stripline structure, shown in Figure 4–35, has the advantages of the broadside-coupled differential stripline with the added flexibility that allows you to adjust the differential impedance by offsetting the two conductor strips. The differential impedance increases as the offset dimension $W_0$ increases.

**Figure 4–35. Broadside-Coupled Differential Offset Stripline**

**Figure 4–36 and 4–37** show the frequency domain simulation setup and results for a 100-Ω broadside-coupled differential offset stripline, respectively.
The Stratix GX development board uses edge coupling instead of broadside coupling, with loose coupling between the positive and negative traces. Although tight coupling provides greater noise immunity, it is necessary to loosen the coupling because of the mechanical placement requirements of SMA connectors. With loose coupling, if the routing is broadside coupled, the thickness of the board increases. With loose coupling, edge-coupled routing is preferred unless there is the flexibility to increase board thickness.

Figure 4–36. Simulation Setup for a Broadside-Coupled Differential Offset Stripline

![Diagram of simulation setup](image)

Figure 4–37. Simulation Results for a Broadside-Coupled Differential Offset Stripline

![Graphs of input reflection coefficient and forward transmission](image)
Microstrips

Microstrip topologies can be either simple or differential. Microstrips are the most popular planar transmission lines because of their low cost and easy integration with other passive and active components on PCBs.

Simple Microstrip

Figure 4–38 shows the simple microstrip topology. A microstrip is a conductive strip of width W and thickness t, placed on top of a dielectric material backed with a ground plane.

Figure 4–38. Simple Microstrip

Figures 4–39 and 4–40 show the frequency domain simulation setup and results for a 50-W simple microstrip, respectively.

Figure 4–39. Simulation Setup for a Simple Microstrip
Differential Microstrip

The differential microstrip topology, shown in Figure 4–41, has the advantages of the simple microstrip, but also provides common mode noise cancellation. The main problem with differential microstrips is that the coupling between the positive and negative traces is low.

Figures 4–42 and 4–43 show two variants of the differential microstrip extracted from the Stratix GX development board.
Figures 4–44 and 4–45 show the frequency domain simulation setup and results for a 100-Ω tightly coupled differential microstrip, respectively.
Coplanar Wave Guides

There are three types of coplanar wave guides: simple, grounded, and grounded differential.

Simple Coplanar Wave Guide
The simple coplanar wave guide, shown in Figure 4–46, is used primarily in microwave systems. This structure does not require vias, and you can easily mount passive or active devices in the signal path, resulting in a
Transmission Lines

low-loss, high-speed transmission line. The simple coplanar wave guide requires that the substrate thickness (H) be “infinite,” so that the fields remain outside the dielectric.

You cannot use this structure on multilayer boards because it cannot have a second layer.

**Figure 4–46. Simple Coplanar Wave Guide**

Grounded Coplanar Wave Guide
The grounded coplanar wave guide is used extensively in communications systems that integrate different technologies such as surface mount technology, multichip modules, and multilayer boards. The dielectric thickness (H) must be at least five times the spacing (S) to be considered a grounded coplanar wave guide; otherwise, it is considered a microstrip with a ground shield. **Figure 4–47** shows the grounded coplanar wave guide topology.

**Figure 4–47. Grounded Coplanar Wave Guide**

Figures 4–48 and 4–49 show the frequency domain simulation setup and results for a 50-Ω grounded coplanar wave guide, respectively.
Figure 4–48. Simulation Setup for a Grounded Coplanar Wave Guide

Figure 4–49. Simulation Results for a Grounded Coplanar Wave Guide

Figure 4–50 shows the Stratix GX development board’s grounded coplanar wave guide and its edge-coupled differential offset stripline layout capture plot. This particular differential pair was used for the 1.0-Gbps source synchronous lines.
Grounded Differential Coplanar Wave Guide

The grounded differential coplanar wave guide is the differential version of the grounded coplanar wave guide and is used in high-speed digital systems that require maximum noise immunity. Figure 4–51 shows the topology. The same limitations for S and G apply in this topology as for the grounded coplanar wave guide.

This topology does not appear on the Stratix GX development board because of the loose coupling requirements. See “Broadside-Coupled Differential Offset Stripline” on page 4–42 for more information.
Figures 4–52 and 4–53 show the frequency domain simulation setup and results for a 100-Ω grounded differential coplanar wave guide, respectively.
Transmission Line Termination

High-speed signals require termination at the beginning, end, or both sides of the transmission line to prevent the reflected signal from the ends from corrupting the original signal. This section briefly describes several termination techniques. For more details about each technique, refer to AN315: Guidelines for Designing High-Speed FPGA PCBs. Figure 4–54 shows the different termination techniques.
**Series Termination**

With series termination, you place the termination resistor in series with the transmission line at the source end of the transmission line. The value of the resistor $(R_t)$ and the value of the output impedance of the buffer must add up to 50 Ω for optimal performance. This is not always possible in cases when the buffer output impedance depends on the current setting or the voltage swing. In most cases, using a 22-Ω resistor in series works well for typical CMOS buffers such as those in Stratix GX devices. Series termination minimizes the DC power dissipation, but perfect impedance matching is not always possible, because the buffer output impedance varies.
Parallel Termination

With parallel termination, you place a resistor whose value is equal to the impedance of the trace at the end of the line on the receiver side. Ideally, the resistor should be directly on the pin. Parallel termination is better than series termination when the output impedance of the buffer is unknown. With parallel termination, you get an almost perfect impedance match between the transmission line and the termination resistor. The disadvantage with parallel termination is that it increases the DC power dissipation because of the DC path to ground.

Thévenin Termination

Thévenin termination is identical to parallel termination, except that you use two resistors to achieve the impedance match. The two resistors can also provide a DC level. Two criteria determine the value of the resistors. First, the two resistors in parallel must equal the line impedance. Second, the resistors must form a voltage divider so that the restored DC voltage equals the desired DC level. With parallel termination, you can achieve an almost perfect impedance match between the transmission line and the termination resistors. You can also restore DC voltage to AC-coupled signals. The main disadvantages to thévenin termination are the DC power dissipation and the added elements.

AC Termination

AC termination is identical to parallel termination except that the termination impedance consists of a resistor and a capacitor. The capacitor acts as a DC block, reducing static power dissipation. The capacitor must be chosen so that the RC time constant is about one rise time of the signal. Perform simulations to choose the best value of the capacitor. AC termination provides the advantages of parallel termination without the DC power dissipation. The main disadvantages are the rise and fall time degradation and the added elements.

Differential Parallel Termination

With differential parallel termination, you place the termination resistor between the positive and negative signals, close to the receiver pins. This type of termination is a subset of parallel termination.

Specific I/O standards, for example, SSTL-II for the DDR interface, sometimes require both series and parallel termination. Figure 4–55 shows the termination shown in this particular standard.
Fly-By Termination

Fly-by termination is not precisely a termination technique, but a placement technique for termination resistors. To understand fly-by, consider the parallel (non fly-by) termination shown in Figure 4–56. Layout constraints might prevent the termination resistor, $R_t$, from being placed close to the receiver pin (the load). If the pin is in the middle of the device and there is only an inch of trace length between the termination point and the receiver pin, the setup degrades the signal quality, because the extra stub length acts as a capacitive load.

To prevent this degradation, place the termination resistor after the load, as shown in Figure 4–57. Even if the resistor is a couple of inches away, the termination occurs at the end of the transmission line, and there are no significant reflections. The trace from the transmission line to the receiver pin can be kept small.
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Figure 4–57. Fly-By Termination Resistor Placement Technique

The simulation setup for fly-by termination is shown in Figure 4–58. The upper circuit in this diagram is for fly-by termination resistor placement, and the lower is for normal placement. Figure 4–59 shows some simulation results that show how the fly-by termination technique helps improve signal integrity.

Figure 4–58. ADS Simulation Setup for Normal Versus Fly-By Termination

The simulation setup for fly-by termination is shown in Figure 4–58. The upper circuit in this diagram is for fly-by termination resistor placement, and the lower is for normal placement. Figure 4–59 shows some simulation results that show how the fly-by termination technique helps improve signal integrity.
The simulation results are shown in Figure 4–59. The signal quality remains the same regardless of how far away the resistor is, provided that it is placed in fly-by mode.

For the non fly-by case, the signal has an overshoot, which worsens when you place the resistor farther away.

![Figure 4–59. Signal Quality at the Receiver Device Pins](image)

Altera uses the fly-by resistor placement technique extensively on the Stratix GX development board. Figure 4–60 shows an example capture plot.
Transmission Line Routing

This section describes the things to keep in mind when designing transmission line routing for your high-speed board.

General Guidelines

This section provides a summary of routing guidelines.

- Use tight coupling for differential traces as much as possible. If it is not possible to maintain tight coupling throughout the trace length, then you must use loose coupling for the entire trace. Figure 4–61 shows 3.125-Gbps differential transceiver traces, which are loosely coupled on layer 15 and the top layer of the Stratix GX development board. Tight coupling is not possible on the top layer because of the minimum separation required (because of the mechanical constraints of the SMA connectors). If you used tight coupling on layer 15, the signal would need to transition from tight to loose coupling, which would introduce impedance discontinuities.
Microstrip and stripline transmission lines are both fine for routing. Stripline tends to have more loss than microstrip, but it also shields the signals from possible noise from other sources. The constraints during layout design often dictate on which layer to do the routing.

Use rounded corners while routing. Do not use 90° bends, which introduce impedance discontinuities. A 45° bend provides a compromise, but rounded corners offer the best performance.

Both broadside and edge coupling are fine. Generally, broadside coupling makes it easy to route out of the BGA, but requires more layers. Edge coupling makes it harder to route out of the BGA, but requires fewer layers. Both provide acceptable signal integrity performance.

Do not allow high-speed signals to cross over plane splits. A crossover causes signals to see a longer return path, which increases trace inductance. The increased inductance changes the impedance of the line, causing signal integrity problems.

Remove all unused via pads during the manufacturing process. Some fabrication houses refer to unused via pads as “nonfunctional via pads.” Unused via pads add additional capacitance on the signal path. Figure 4–62 shows examples of unused via pads.
If the signal must be routed through a via, route it so that the via stub length is minimized. The option shown in Figure 4–64 minimizes the via stub length and is preferred over the option shown in Figure 4–65. Altera used this technique in the Stratix GX development board. The high-speed traces were taken to layer 16 from the top layer through the vias to use as much of the via length as possible and to minimize the stubs.

For dual stripline traces (Power 1 – Signal 1 – Signal 2 - Power 2 configuration), ensure that the signals on the Signal 1 layer are orthogonal to the signals on the Signal 2 layer if they cross each other. If they do not cross each other, ensure that they are at least 4W away, where W is the width of the traces.

If a connector has a section that does not have controlled impedance, try to minimize the length of the connector. For example, for SMA connectors, reduce the center conductor length as much as you can (less than 20 mils if possible). This way the parasitic inductance is reduced.

Use “teardropping” to reduce impedance discontinuity when going from a wide pin and trace to a narrow pin or trace. For example, when you interface an SMA connector to a trace, use teardropping. Figure 4–63 shows the dimensions of an SMA connector and a screen capture of how Altera used teardropping on the Stratix GX development board. The SMA connector has a 50-mil diameter center pin, but the board traces might be 5-mils wide. Teardropping helps minimize the impedance discontinuity.
Avoid routing a high-speed signal over many layers, because this type of routing introduces via discontinuities.

Use reference ground vias wherever signal vias are necessary. The reference ground vias should be placed close to the signal vias. Figure 4–61 on page 4–59 shows an example of using ground reference vias near the signal vias where a high-speed trace changes layers. This example is from the edge-launch SMA connectors of the 3.125-Gbps transceivers on the Stratix GX development board.

Avoid having long stubs on the via, using most of the via length for routing. For example, if you have a signal that originates on the top layer and you have to use an internal layer for routing, use the one closest to the bottom layer. This approach avoids excess via length. The option shown in Figure 4–64 on page 4–63 is preferred over the option shown in Figure 4–65 on page 4–63.

Avoid reference plane changes for high-speed signals. Reference plane changes occur when you reference part of the trace to a ground plane and the other part to another ground plane or a power plane.

Avoid using power planes for references.

**Length Matching**

Source-synchronous interfaces require length matching, except when using dynamic phase alignment. You must ensure that this requirement is clearly stated in the layout guidelines. How closely the lengths must be matched depends on the data rate and the available timing margin. For example, consider a source synchronous link at 840 Mbps where the bit unit interval equals 1.19 ns. In this example, assume that you allocate a length mismatch of 2% for the maximum timing margin loss. At 1.19 ns
unit intervals, this value equals approximately 24 ps. Using the microstrip equation on page 4–4, for a microstrip line with FR-4 dielectric, the signal travels 1 inch in 142 ps. In 24 ps the signal can travel $\frac{24}{142} = 0.17$ inches, or 170 mils. Therefore, you must match the lengths of all the signals (including data, clocks, addresses, and any controls signals) to within ± 85 mils.

Examples of source-synchronous interfaces include the 840-Mbps interface available on Stratix and Stratix GX devices, the SSTL interface for DDR memory, and the HSTL interface for Quad Data Rate (QDR) interface.

A notable exception to the length matching requirement is the source-synchronous interface with DPA available in Stratix GX devices, which allows 1-Gbps data transfer without requiring length matching. The data and clock lines can literally be inches longer or shorter than each other and the interface still operates robustly.

You must account for the length of every via a signal traverses through and include the accumulated value in the length report (a file generated by the layout tool). Do not include the entire length of the via, just the portion the signal traverses (ignore the stub length). For example, Figures 4–64 and 4–65 show two possibilities for signal routing on a board with 12 signal layers. For both options, the signal originates at point A and ends at point B on the top layer. In Figure 4–65, the signal is routed on layer 3; in Figure 4–64, the signal is routed on the bottom layer. The total length the signal travels, for the respective options, is:

$$L_{routing,\text{option}1} = (z^* + y + z) = (2z^* + y)$$

$$L_{routing,\text{option}2} = (z + y + z) = (2z + y)$$
In Figure 4–65, W represents the extra stub that you need to consider in length calculations only if you use layer 16 for routing.

In the equations on page 4–62, the total difference in via lengths between these two routing options is $2z'-2z = 2w$. This distance can be over 100 mils for thick boards.

Because this kind of calculation can quickly become intractable, it is best to use as few vias as possible on the board and to tighten the length-matching specification. For instance, in the example above, you can tighten the specification from ±85 mils to ±50 mils.
For differential traces, it is important to match the length of the positive and negative signals. A mismatch in lengths causes duty cycle distortion, which can decrease the timing margin. Altera recommends that the lengths be matched to ± 50 mils. If the signal goes through a turn and the outer trace is longer than the inner trace, you can use a second turn in the opposite direction as an offset. Figure 4–66 shows an example of high-speed transceiver routing to achieve length matching on the Stratix GX development board.

Figure 4–66. Transceiver Signal Routing for Length Matching

Other Transmission Line Issues

This section describes transmission line issues other than routing.

Stackup

The stackup design is an iterative process in which the relative permittivity ($\varepsilon_r$), trace width, layer count, and transmission line structures are set by engineers to achieve the best system performance at the minimum cost. These parameters are selected based on the
engineering team’s knowledge of the system, the fabrication house, and the simulations. Table 4–6 shows the stackup for the Stratix GX development board.

Table 4–6. Stratix GX Stack-Up

<table>
<thead>
<tr>
<th>Layer Number</th>
<th>Type</th>
<th>Cu Weight (oz)</th>
<th>Foil Thickness (in.)</th>
<th>Dielectric Thickness (in.)</th>
<th>Construction</th>
<th>ε_r</th>
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<td>1</td>
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<td>0.0007</td>
<td>0.0036</td>
<td>$1 \times 1080$</td>
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<tr>
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<td>0.0014</td>
<td>0.0040</td>
<td>$1080 + 2113$</td>
<td>4.00</td>
</tr>
<tr>
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<td>0.0007</td>
<td>0.0061</td>
<td>2116</td>
<td>3.86</td>
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<tr>
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<td>0.0007</td>
<td>0.0040</td>
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<tr>
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<td>0.0014</td>
<td>0.0045</td>
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<td>3.86</td>
</tr>
<tr>
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<td>0.005</td>
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<td>0.0007</td>
<td>0.0045</td>
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</tr>
<tr>
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</tr>
<tr>
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<td>$1080 + 2113$</td>
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<td>4.00</td>
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<tr>
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<td>0.0014</td>
<td>0.0045</td>
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<tr>
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<td>2116</td>
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<td>$1080 + 2113$</td>
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<td>0.0007</td>
<td>0.0061</td>
<td>2116</td>
<td>3.86</td>
</tr>
</tbody>
</table>

The development board material is NELCO FR-4 4000-6, which is an enhanced multifunctional, high temperature resin system that shows a relative permittivity of ~3.86 and tan δ of 0.022. The stackup consists of 6 solid planes and 12 signal layers arranged symmetrically from the center.
For transmission line topologies, Altera uses differential microstrip, grounded coplanar wave guide, and differential dual stripline (offset edge-coupled differential stripline). The impedance is 50 Ω for single-ended traces and 100 Ω (differential) for differential traces.

In the stackup design process, the fabrication house has considerable influence during the fine-tuning stage. Typically, the engineer provides a preliminary stackup, and the fabrication house responds with a modified stackup based on their process tolerances. They typically guarantee the impedance required on the traces. Typical tolerances are ±10%, although ±5% is fairly common for high-speed boards. Altera uses ±5% for better system performance.

**Discontinuities**

You can characterize discontinuities in the transmission path using either a frequency domain tool or a time domain tool. In the frequency domain, you can use a network analyzer for characterization. A commonly used time domain tool is the time domain reflectometer (TDR). For digital systems that are commonly described in time domain, the TDR is often easier and more intuitive to use. This section summarizes the principles of a TDR and how to interpret the results.

A TDR is an oscilloscope with the capability of sending a very fast signal pulse. The pulse travels down the transmission line and is reflected wherever it sees a discontinuity. Figure 4–67 shows a conceptual diagram of a TDR. The reflected wave takes $2T$ time units to be displayed in the scope, because it takes $T$ time units for the pulse to reach the discontinuity and another $T$ time units for it to return to the scope.

**Figure 4–67. Conceptual Diagram of a TDR System**

![Conceptual Diagram of a TDR System](image-url)
Using a TDR, resistive discontinuities show a staircase profile, capacitive discontinuities cause a dip, and inductive discontinuities cause a bump. The reason for this is that initially the capacitor acts as a short-circuit for a high-frequency pulse, and the inductor acts like an open circuit. Based on the location of the impedance discontinuity on a TDR plot, you can trace it to the exact board location.

Figure 4–68 shows the different types of terminations and the associated TDR responses.
Figure 4–68. TDR Responses to Different Terminations & Discontinuities

A. Open Circuit

\[ Z_T = 0 \text{ Ohm} \]

B. Short Circuit

\[ Z_T = 0 \text{ Ohm} \]

C. Matched Termination

\[ Z_T = Z_O \]

\[ Z_T = Z_O \]

D. Over Termination

\[ Z_T > Z_O \]

\[ Z_T = Z_O \]

E. Capacitive Load

\[ Z_T = Z_O \]

F. Inductive Load

\[ Z_T = Z_O \]
To determine the value of the resistive discontinuity, look at the size of the step in the staircase waveform. To determine the value of the capacitive or inductive discontinuity, look at the rise time of the associated response. Then use the following formulas:

\[ R = Z_0 \frac{1 + \Gamma}{1 - \Gamma} \]

**Resistive Termination**

where \( \Gamma \) is the reflection coefficient. For a 1-V initial signal, \( \Gamma \) equals the step of the staircase. For a different initial step, you need to scale \( \Gamma \) linearly.

**Capacitive Termination**

\[ \tau = 2.2 t_r = R C \]

for first order R-C circuits.

**Inductive Termination**

\[ \tau = 2.2 t_r = L / R \]

for first order L-R circuits.

In the previous equations, \( R \) is the effective resistance and impedance in the circuit. The rise time \( (t_r) \) is determined from the TDR response. The only variables remaining are \( L \) and \( C \), either of which can be computed.

**Example:** Find the value of the inductance on the 0.1-in pitch header pin connector from the TDR response shown in Figure 4–69.
**Solution:** From the plot of the header discontinuity, the signal fall time is about 180 ps, and the cable’s impedance is 50 Ω. Therefore, 
\[ L = 2.2 \times t_r \times R = 2.2 \times 180 \times 50 = 19,800 \text{ pH} = 19.8 \text{ nH}. \]

Real-world TDR responses are often complicated and hard to interpret because of multiple reflections and a combination of discontinuities (capacitive, inductive, and resistive) that could be present on the board. One approach is to isolate each part and measure the TDR by soldering the part at the end of an SMA cable so that each part can be characterized separately.

As a real-world example of a TDR response, consider the following measurements, which were taken to characterize SMA connectors being evaluated during the design of the Stratix GX development board. The SMA connectors are shown in Figure 4–70, and the results are shown in Figure 4–71.

The first measurement Figure 4–71 shows the TDR response of the SMA cable used. The second shows the response of the SMA cable with the connector connected at the end. You can see quite a bit of ringing, signifying the presence of parasitics. The third shows the response of the SMA cable and connector assembly, with the connector’s center conductor stripped down to about 10 mils in length. This response is almost identical to the response of the SMA cable only, except for the
presence of a fixed delay. Comparing these plots shows that the center conductor of the SMA connector adds quite a few unwanted parasitics, but stripping down the conductor greatly reduces the parasitics.

**Figure 4–70. Top & Side Views of Original & Modified SMA**

![Original SMA (Long Center Conductor)](image1)

![Modified SMA (Trimmed Center Conductor)](image2)
Crosstalk

If two traces are close to each other, the signal switching on one trace can excite a voltage on the other, resulting in crosstalk. Crosstalk control must be a key objective of any board design. With high-speed designs it is especially important because of the reduced noise margins.

The following crosstalk case studies are simulations that vary the spacing between the aggressor net and the victim net. Both simulations used differential traces.

Crosstalk Case Study 1 – Loosely Coupled Microstrip Traces
This case study used two pairs of 1-inch long microstrip differential traces. The width (W) of all the traces is 5 mils. The spacing between the positive and negative loosely coupled traces is 15 mils. The aggressor trace had the same configuration, but was placed at varying distances to
see the effect of spacing on crosstalk. This test setup is based on the microstrip lines routed on the top layer of the Stratix GX development board. The simulation setup is shown in Figure 4–72.

Figure 4–72. ADS Test Setup for Loosely Coupled Microstrip Crosstalk Simulation

The simulation results are shown in Figure 4–73. The input waveform is at the top left. Crosstalk on the near and far victim lines for $S = 3W$ appears in the top right. The bottom left shows crosstalk for $S = 4W$, and the bottom right shows crosstalk for $S = 5W$. 
When the aggressor trace is $S = 3W$ away, the crosstalk on the nearest victim line is approximately 13.5 mV, and the crosstalk on the farthest victim line is approximately 0.9 mV. When the spacing is increased to $S = 4W$, the crosstalk on the nearest victim line decreases to 2.5 mV, and the crosstalk on the farthest victim line decreases to 0.6 mV. The decreases on the farthest line are not significant because the lines are loosely coupled: increasing the spacing by 1W does not significantly increase the overall distance to the farthest line. When the spacing is increased to $S = 5W$, the crosstalk on the nearest victim line decreases to 1.5 mV and the crosstalk on the farthest victim line decreases to 0.6 mV. These three situations allow you to determine what level of noise you can tolerate on your victim lines. Altera recommends maintaining a minimum $S = 4W$, which is the guideline followed for the Stratix GX development board.

**Crosstalk Case Study 2 – Tightly Coupled Stripline Traces**

This case study used two pairs of 1-inch-long tightly coupled stripline traces. This setup replicates the tightly coupled stripline traces of the Stratix GX development board. The width of all traces is 3.7 mils, and the spacing between positive and negative traces is 5.3 mils. The aggressor trace used the same configuration but was placed at varying distances to see the effect of spacing on crosstalk. Figure 4–74 shows the simulation setup, and Figure 4–75 shows the results. In Figure 4–75, the input waveform is on the top left. Crosstalk on the near and far victim lines for $S = 3W$ is shown in the top right. The bottom left shows crosstalk for $S = 4W$, and the bottom right shows crosstalk for $S = 5W$. 
Figure 4–74. ADS Test Setup for Tightly Coupled Stripline Crosstalk Simulation
When the aggressor trace is $S = 3\text{W}$ away, the crosstalk on the nearest victim line is approximately $13.5 \text{ mV}$, and the crosstalk on the farthest victim line is approximately $1.35 \text{ mV}$. When the spacing is increased to $S = 4\text{W}$, the crosstalk on the nearest victim line decreases to $5.5 \text{ mV}$, and the crosstalk on the farthest victim line decreases to $0.55 \text{ mV}$. The decreases on the farthest line are not significant because the lines are tightly coupled: increasing the spacing by $1\text{W}$ does not significantly increase the overall distance to the farthest line. When the spacing is increased to $S = 5\text{W}$, the crosstalk on the nearest victim line decreases to $2.5 \text{ mV}$, and the crosstalk on the farthest victim line decreases to $0.25 \text{ mV}$. These three situations allow you to determine what level of noise you can tolerate on your victim lines. Altera recommends maintaining a minimum $S = 4\text{W}$, which is the guideline it follows for the Stratix GX development board.

**Miscellaneous**

This section describes miscellaneous topics, including component selection, S-parameters, the Smith Chart, AC and DC coupling, unused pin connections, and power trace thickness.

**Component Selection for High-Speed Design**

Deciding which components to use is an important part of board design. This section provides information and guidelines for selecting discrete components for the PCB.
Resistors, Capacitors, Inductors & Ferrite Beads

You should choose the smallest footprint available when selecting discrete components such as resistors and capacitors. The small footprint means that the pad on the board can be small and that the parasitic capacitance and inductance will also be small. Altera typically uses 40 mil × 20 mil (0402) package components for the high-speed signals.

Inductors typically require bigger footprints because they are often used for power supply filtering and must be bigger to support high currents without saturating.

The three parameters of interest when choosing ferrite beads are:

- DC resistance
- AC impedance
- Current handling capability

A good ferrite bead has low DC resistance, high AC impedance, and high current handling capability. However, as the current handling capability increases, the AC impedance tends to drop; consequently there is a trade-off involved. The impedance versus frequency plot of a typical ferrite bead is shown in Figure 4–76.

Figure 4–76. Typical Impedance Profile of a Ferrite Bead
In Figure 4–76, the impedance at 2 GHz is more than 100 Ω. The ratio between that impedance and the power supply impedance, which is often lower than 1 Ω, is more than 100. As a result, most of the noise is blocked by the ferrite bead and is shunted to ground instead.

Altera recommends Steward MI0805M221R-00 ferrite beads for transceiver power and ground planes. The DC resistance for this part is lower than 50 mΩ and it can handle 2.5 A of current. The impedance is over 200 Ω at 1 GHz. Altera also recommends the Murata BLM31PG500SN1 ferrite bead. It has 25 mΩ of DC resistance, 3 A of current, and has 75 Ω of AC impedance at 1 GHz. Two Steward ferrite beads connected in parallel can provide 5 A of current capability with 25 mΩ of DC resistance and over 100 Ω of AC impedance. This performance level is adequate for most applications.

**SMA Connectors**

SMA connectors are typically used for high-speed signals because of their controlled impedance, mechanical robustness, and good signal integrity. These connectors come in the form of edge launch or vertical launch. For edge launch, the connector is connected to the board edge, the central conductor stays flush with the board, and the board is sandwiched between the ground conductors.

The vertical launch type is through-hole or surface mount. For the through-hole type, all the legs and the center conductor go through the board. For a surface mount type, the center conductor barely touches the top layer of the board.

The type of launch technique does not affect the signal quality very much. However, a long center conductor adds inductance to the transmission path and degrades the signal.

With vertical launch surface mount, you can often strip the center conductor down to below 20 mils. This stripping might be slightly harder to achieve in edge launch configuration, but the choice is dependent on the capability of the SMA manufacturers. Altera has stripped the center conductor down to less than 20 mils short in its designs. Altera recommends using Lighthorse Technologies and Northrop Grumman for SMA connector requirements.

**SMA Cables**

SMA cables have 18-GHz bandwidth or more, which is sufficient for 3.125-Gbps applications. However, be careful that the cable is crimped securely at both ends to avoid unpredictable behavior.
**Probes**

Use a good differential probe with short tips for differential signals. Differential probes make the measurement immune to common mode noise and pickup on the probes.

**S-Parameters**

It is difficult to define voltages or currents in transmission lines and to measure them at microwave frequencies, because direct measurements usually involve the magnitude (inferred from power) and phase of a wave traveling in a given direction, or the standing wave. Thus, equivalent voltages and currents, and the related impedance and admittance matrices, become somewhat of an abstraction when dealing with high-frequency networks.

A representation more consistent with direct measurements, and with the ideas of incident, reflected, and transmitted waves, is provided by the scattering matrix (S-parameters). S-parameters are often used to quantify the impedance, total losses, input return loss, insertion loss, and isolation and crosstalk for the different transmission lines structures. These concepts are most useful at those frequencies where you must consider distributed rather than lumped parameters.

To understand S-parameters, consider the two-port network shown in Figure 4–77. The network can contain a transmission line or any linear time invariant component. The incident voltages at port 1 and 2 are $E_{i1}$ and $E_{i2}$; and the reflected voltages are $E_{r1}$ and $E_{r2}$. $Z_o$ is the characteristic impedance of the transmission line. $Z_S$ and $Z_L$ are the source and the load impedances.

![Figure 4–77. S-Parameters](image)

Taking the incident and reflected voltage waves on each side of the two-port network and dividing them by the square root of the characteristic impedance, $Z_o$, results in new variables ($a_1$, $a_2$, $b_1$ and $b_2$), which are the normalized voltage wave amplitudes at each port.
The square of the magnitude of $a_1$ (|$a_1$|^2) represents the incident power in port 1, and (|$b_1$|^2) represents the reflected power from this port. The same relations apply to port 2.

\[ a_1 = \frac{E_{ll}}{\sqrt{Z_0}} \quad a_2 = \frac{E_{l2}}{\sqrt{Z_0}} \]

\[ b_1 = \frac{E_{r1}}{\sqrt{Z_0}} \quad b_2 = \frac{E_{r2}}{\sqrt{Z_0}} \]

The resulting parameters relate the scattered wave (reflected wave) from the network to the incidents waves. These parameters are called S-parameters and are defined by:

\[ b_1 = S_{11}a_1 + S_{12}a_2 \]

\[ b_2 = S_{21}a_1 + S_{22}a_2 \]

where $S_{11}$ is the input reflection coefficient, $S_{21}$ is the forward transmission through the network, $S_{12}$ is the reverse transmission through the network, and $S_{22}$ is the output reflection coefficient.

The measurement setup for S-parameters is shown in Figure 4–78 and Figure 4–79. Apply the following conditions for these measurements:

\[ S_{11} = \left. \frac{a_1}{b_1} \right|_{a_2=0} \]

\[ S_{21} = \left. \frac{b_2}{a_1} \right|_{a_2=0} \]

\[ S_{12} = \left. \frac{b_1}{a_2} \right|_{a_1=0} \]

\[ S_{22} = \left. \frac{b_2}{a_2} \right|_{a_1=0} \]
For example, to measure $S_{11}$, you have to ensure that $a_2 = 0$. The way to do so is by making sure that there is no reflection from the load (in other words, set $Z_L = Z_0$).

S-parameters are typically measured using network analyzers.

**Smith Chart**

The Smith Chart is a graphical representation of the impedances in a complex plane. You can use this tool to analyze transmission line impedance matching networks and capacitive or inductive behavior of loads. A typical Smith Chart is shown in Figure 4–80. If the impedance is capacitive, it shows up in the top half of the circle; if it is inductive, it shows up in the bottom half. The far-right point in the middle represents an open circuit; the far left represents a short circuit. The middle point (label 1.0) represents a perfect load match to the characteristic impedance of the line.
**AC Versus DC Coupling**

AC coupling refers to the use of a series capacitor on a signal to block the DC signals from going through. DC coupling refers to the case where this capacitor is not present and the signal passes through without any interruption. In AC coupling, a DC restore circuit is generally required after the capacitor to ensure that the common mode voltage requirements of the receiver are met. Sometimes, as in the Stratix GX transceiver inputs, the DC restore circuitry is built into the device. In that case, external DC restore circuitry is not necessary. DC coupling works only in cases where the output common mode voltage of the transmitter is in the required range of the input common mode voltage of the receiver.
The advantage of AC coupling is that it allows chips with different common mode voltages to interface with each other. The disadvantage is that it requires an extra capacitor, which can add some jitter or other degradation if not properly selected.

If you are certain that the common mode voltage requirements of the receiver are a subset of the common mode voltage output of the transmitter, use DC coupling. If you are in a borderline case, or if the requirements are not satisfied, then use AC coupling.

In choosing the value of the coupling capacitor, consider what happens if the capacitor is too big or too small. If the capacitor is too big, it can significantly slow the signal down and also respond poorly to fast changing input signals due to the long charge and discharge times. If the capacitor is too small, it presents a fair deal of impedance and can increase attenuation and change the characteristic impedance of the path. A good balance between these two conflicting requirements is a 0.01 \( \mu \)F capacitor, which Altera uses for its 3.125 Gbps transceiver designs.

When selecting components, use the smallest size possible, because smaller size components have smaller size pads, which reduce the discontinuity. Altera has used 0402 components (40 mils by 20 mils) in its designs.

You can design the DC restore circuitry in a variety of ways. Altera typically uses a simple resistive voltage divider (see Figure 4–81). Be sure to use precision resistors (0.1% or 1%) for differential signals, so that the restored DC levels on the positive and negative signals are very closely matched. In Figure 4–81, the DC restore circuitry restores the DC level to \( \frac{3.3 \times 78.7}{140 + 78.7} = 1.1875 \) Volts.
Stratix GX devices have DC biasing on the high-speed transceivers inputs and reference clock inputs (REFCLKB[17..13]n and REFCLKB[17..13]p) designed for the 1.5-V PCML standard, so AC coupling is not required. This saves components and board space. If you are using other I/O standards such as LVPECL or LVDS, then you need to AC-couple them, because their common mode voltage is different from the 1.5-V PCML common mode voltage. External biasing networks are not needed, because the common mode is generated internally in the device. Altera used external biasing network on the Stratix GX development board for evaluation purpose only.

Unused Pin Connections

The unused I/O pins should be driven to ground. The unused clock inputs should be grounded as well, but they can be left floating. Similarly, the VCC/GND pins for unused PLLs should be tied to their respective supplies and grounds. Refer to the pin tables of the particular devices for more details.

Power Trace Thickness

Power traces must be carefully specified to ensure that they can deliver the required currents to the destination with minimal voltage drop and minimal temperature rise. This requires the traces to have a certain thickness. Calculators are available to calculate the required trace width to support a certain amount of current at a specified temperature rise. You can find one such calculator at...
http://www.geocities.com/CapeCanaveral/Lab/9643/TraceWidth.htm. A good layout designer should also have charts and calculators for this purpose.