This chapter describes how to serialize the parallel data for transmission and convert received data into parallel data. Data transmission and reception is performed by pseudo current mode logic (PCML) buffers. These transceiver buffers support programmable pre-emphasis, equalization, and programmable $V_{OD}$ settings in I/O buffers.

The programmable pre-emphasis setting is available on transmit buffers to maximize the eye opening on the far-end receiver by boosting the high-frequency component of the data signal. Similarly, programmable equalization is available for receive buffers to reduce the high-frequency losses and inter-symbol interference. These features are useful in lossy transmission lines. Transceivers also support flexible reference clock generation capabilities, including a dedicated transmitter phase-locked loop (PLL) and four receiver PLLs per transceiver block.

The clock recovery unit (CRU) is the main part of each receive analog section; it recovers the clock from the serial data stream (refer to Figure 2–1).

You can set the CRU to automatically or manually alter the receiver PLL phase and frequency to match the bit transition on the incoming data stream. This is to eliminate any clock-to-data skew or to keep the receiver PLL locked to the reference clock (lock-to-data or lock-to-reference mode).

During the clock recovery phase, the receiver PLL initially locks to the reference clock and then attempts to lock on to the incoming data by first recovering the clock from the incoming serial data.
Transmitter Analog

This section describes the transmitter buffer, the transmitter PLL, and the serializer. Figure 2–2 shows the transmitter analog components.

Transmitter Buffer

The Stratix® GX transceiver buffers support the 1.5-V PCML standard at speeds up to 3.1875 gigabits per second (Gbps) and are capable of driving 40 inches of FR4 trace across two connectors. In addition, the buffer contains programmable output voltage, programmable pre-emphasis circuitry, and internal termination circuitry.
Programmable Voltage Output Differential ($V_{OD}$)

Stratix GX transceivers let you customize the differential output voltage ($V_{OD}$) to handle different length, backplane, and receiver requirements (refer to Figure 2–3). You can select the $V_{OD}$ (differential) from a range of 400 to 1,600 mV, as shown in Table 2–1.

Figure 2–3. $V_{OD}$ (Differential) Signal Level

Table 2–1 shows the differential output voltage ($V_{OD}$) setting per current level for each of the on-chip transmitter programmable termination values.

Table 2–1. Programmable $V_{OD}$ (Differential)

<table>
<thead>
<tr>
<th>100 $\Omega$ (mV)</th>
<th>120 $\Omega$ (mV)</th>
<th>150 $\Omega$ (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>400</td>
<td>480</td>
<td>600</td>
</tr>
<tr>
<td>800</td>
<td>960</td>
<td>1,200</td>
</tr>
<tr>
<td>1,000</td>
<td>1,200</td>
<td>1,500</td>
</tr>
<tr>
<td>1,200</td>
<td>1,440</td>
<td></td>
</tr>
<tr>
<td>1,400</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1,600</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
You can set the differential $V_{OD}$ values statically during configuration or dynamically adjust them in user mode. You select the static $V_{OD}$ value through a list in the altgxb MegaWizard® Plug-In Manager, which sets the appropriate $V_{OD}$ setting in the configuration file. The disadvantage of the static mode setting is that the $V_{OD}$ is set on a per transceiver block basis and cannot be changed unless you regenerate another programming file.

Alternatively, if you enable dynamic adjustment in the altgxb MegaWizard Plug-In Manager, you can dynamically configure the $V_{OD}$ setting by the device during user mode. This configuration is done by asserting encoded values on the tx_vodctrl bus, which is instantiated in the altgxb module when you select the dynamic adjustment option. This option lets you make quick performance evaluations of the various settings without having to recompile and regenerate multiple configuration files. Another advantage of this option is that it allows the $V_{OD}$ of each channel to be configured independently. Refer to the section “MegaWizard Plug-In Manager Analog Features” on page 2–20 for further details.

**Programmable Pre-Emphasis**

The programmable pre-emphasis module in each transmit buffer boosts the high frequencies in the transmit data signal, which may be attenuated in the transmission media. This maximizes the data eye opening at the far-end receiver. Pre-emphasis is particularly useful in lossy transmission mediums.

The transfer function of a transmission line can be represented in the frequency domain as a low-pass filter. Any frequency components below the –3 dB frequency pass through with minimal losses. Frequency components that are greater than the –3-dB frequency are attenuated. This variation in frequency response yields data-dependant jitter and other ISI effects. By applying pre-emphasis, the high frequency components are boosted, or in other words, pre-emphasized. This pre-emphasis equalizes the frequency response as seen at the receiver so that the delta between the low-frequency and high-frequency components is reduced, which in return minimizes the ISI effects from the transmission medium.

In Stratix GX transceivers, the programmable pre-emphasis settings can have one of six values (0 to 5). You should experiment with the pre-emphasis values to determine the optimal setting based on your system variables.
As with the $V_{OD}$ settings, you can set the pre-emphasis settings statically during configuration or adjust them dynamically in user mode. You can set the static pre-emphasis value through a drop-down menu in the altgxb MegaWizard Plug-In Manager, which sets the appropriate pre-emphasis setting in the configuration file. The disadvantage of the static mode setting is that the pre-emphasis is set on a per-transceiver-block basis and cannot be changed without regenerating another programming file.

On the other hand, if you select dynamic adjustment in the altgxb MegaWizard Plug-In Manager, the pre-emphasis setting can be configured dynamically by the device during user mode. This configuration is done by asserting encoded values on the $tx\_preemphasis\_ctrl$ bus, which is instantiated in the altgxb module when you select the dynamic adjustment option. This option lets you make quick performance evaluations of the various settings without having to recompile and regenerate multiple configuration files. Another advantage of this option is that it allows the pre-emphasis of each channel to be configured independently. For further details, refer to “MegaWizard Plug-In Manager Analog Features” on page 2–20.

Avoid pre-emphasis and $V_{OD}$ settings that yield a value greater than 1,600 mV. Settings beyond this value do not damage the buffer, but they prevent accurate device operation. Verify that the combination of $V_{OD}$ and pre-emphasis settings do not exceed the 1,600-mV limit.

**Programmable Transmitter Termination**

The Stratix GX transmitter buffer includes a 100-, 120-, or 150-$\Omega$ programmable on-chip differential termination resistor. The Stratix GX transmitter buffers are current-mode drivers, so the resultant $V_{OD}$ is a function of the transmitter termination value. For more information on resultant $V_{OD}$ values, refer to “Programmable Voltage Output Differential ($V_{OD}$)” on page 2–3.

**Transmitter PLL**

Each transceiver block contains a transmitter PLL and a slow-speed reference clock. The transmitter PLL receives the reference clock and generates the high-speed serial clock used by the serializer. The slow-speed reference clock is used for the transceiver logic. Figure 2–4 shows the transmitter PLL’s block diagram. The $pll\_locked$ signal indicates when the transmitter PLL is locked to the reference clock. A high signal indicates that the PLL is locked to the reference clock; a low signal indicates that the PLL is not locked to the reference clock.
Table 2–2 lists some of the transmitter PLL specifications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specifications</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input reference frequency range</td>
<td>25 MHz to 650 MHz</td>
</tr>
<tr>
<td>Data rate support</td>
<td>500 Mbps to 3.1875 Gbps</td>
</tr>
<tr>
<td>Multiplication factor (W)</td>
<td>2, 4, 5, 8, 10, 16, or 20 (1)</td>
</tr>
</tbody>
</table>

Note to Table 2–2:
(1) Multiplication factors 2 and 5 can only be achieved with the use of the pre-divider on the REFCLKB.

Clock Synthesis

The maximum input frequency of the phase frequency detector (PFD) is 325 MHz. To achieve reference clock frequency above this limitation, the /2 pre-divider on the dedicated local REFCLKB path can be enabled automatically by the Quartus® II software. The /2 pre-divider divides the reference clock frequency by a factor of 2 and then the /m factor compensates the frequency difference. An example would be a data rate of 2,488 Mbps with a 622-MHz reference clock. In this scenario, the reference clock must be assigned to the REFCLKB port where the 622-MHz reference clock is divided by 2, yielding a 311-MHz clock at the PFD. This 311-MHz reference clock is then multiplied by a factor of 8 to achieve the 2,488-MHz clock at the VCO.
If the reference clock exceeds 325 MHz, the clock must be fed by the dedicated local reference clock pin, REFCLKB. By default, the Quartus II software assigns pins to be LVTTL, so you must assign the 1.5-V PCML I/O standard to the I/O pins to select the REFCLKB port as the reference source. The Quartus II software prompts a fitter error if the reference clock exceeds 325 MHz and the reference clock source is not on the REFCLKB port.

You can also use the pre-divider on the REFCLKB path to support additional multiplication factors. The block diagram in Figure 2–4 shows that /m can only support multiplication factors of 4, 8, 10, 16, and 20, but Table 2–3 shows that the additional multiplication factors of 2 and 5 are also achievable. You can achieve these multiplication factors by using the pre-divider. A multiplication factor of 2 is achieved by pre-dividing the reference clock by 2 and then multiplying the resultant frequency by 4, which yields a multiplication factor of 2. A multiplication factor of 5 is achieved in the same manner by pre-dividing the reference clock by 2 and then multiplying the resultant frequency by 10, which yields a multiplication factor of 5.

Table 2–3 lists the possible multiplication values as a function of the source to the transmitter PLL. Table 2–3 assumes that the reference clock is directly fed from the source listed and does not factor any pre-clock synthesis (that is, the Stratix GX PLL driving a global clock that is used for the transmitter PLL reference clock source).

<table>
<thead>
<tr>
<th>Transmitter PLL Reference Clock Source</th>
<th>Multiplication Factors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Global clock, I/O bus, general routing</td>
<td>4, 8, 10, 16, 20</td>
</tr>
<tr>
<td>Inter-transceiver routing</td>
<td>2, 4, 5, 8, 10, 16, 20</td>
</tr>
<tr>
<td>Dedicated local REFCLKB</td>
<td>2, 4, 5, 8, 10, 16, 20</td>
</tr>
</tbody>
</table>

You must specify the data rate of the channel and input clock period of the reference clock. The data rate divided by the input clock period must equal one of the multiplication factors listed in Table 2–3.

**Transmitter PLL Bandwidth Setting**

The Stratix GX transmitter PLL in the transceiver block offers a programmable bandwidth setting. The PLL bandwidth is the measure of its ability to track the input clock and jitter. The bandwidth is determined by the –3-dB frequency of the closed-loop gain of the PLL.
A high-bandwidth setting provides a faster lock time and tracks more jitter on the input clock source which passes it through the PLL. This helps reject noise from the VCO and power supplies. A low-bandwidth setting, on the other hand, filters out more high frequency input clock jitter, but increases lock time.

You can set the bandwidth for Stratix GX devices to either low or high. The –3-dB frequencies for these settings can vary due to the non-linear nature and frequency dependencies of the circuit. As a result, you can vary the bandwidth to customize the performance on specific systems.

**Serializer (Parallel-to-Serial Converter)**

The serializer converts parallel data to serial data at the transmitter output buffer. The serializer can support 8- or 10-bit words when used with the transmitter multiplexer. The 8-bit serializer drives the serial data to the output buffer, as shown in Figure 2–5. The serializer can drive the serial bit-stream at a data rate range of 500 Mbps to 3.1875 Gbps. The serializer outputs the least significant bit (LSB) of the word first.

**Figure 2–5. Example of 8-Bit Serialization**

![Diagram of 8-Bit Serialization]

Figure 2–6 shows the serial bit order of the serializer output. In this example, a constant 8’h56 (01010110) value is serialized. The serial data is transmitted from LSB to most significant bit (MSB).
This section describes the receiver input buffer, the receiver PLL, the clock recovery unit, and the deserializer. Figure 2–7 shows the receiver analog components.

**Receiver Input Buffer**

The receiver input buffer contains internal termination and internal equalization. Figure 2–8 shows the structure of the input buffer. The input buffer has programmable equalization that you can apply to increase the signal integrity of the transmission line. The internal termination in the receiver buffer can support AC and DC coupling with programmable differential termination settings of 100, 120, or 150 Ω.
Programmable Receiver Termination

The Stratix GX receiver buffer includes programmable on-chip differential termination of 100, 120, or 150 Ω.

This assignment must be made per pin through the Assignment Editor in the Quartus II software. Select Assignment Organizer > Options for Individual Nodes Only > Stratix GX Termination Value (Assignments menu).

The proper termination settings should be selected and verified accordingly before compilation.

The transmitter PLL input signal (inclk) drives the termination resistance calibration circuit. The Quartus II software allows receiver-only configurations in Stratix GX devices. However, if you use the Quartus II software to remove the transmitter PLL in a receiver-only configuration, you will see an incorrect value or unpredictable behavior with the receiver input pin termination. If the rx_cruclk signal is globally routed, the Quartus II software handles this automatically. If the rx_cruclk signal is not globally routed or routed using the inter-quadrant line (IQ2), the Quartus II software returns a no-fit. In this situation, you must add a transmitter PLL to your design.

If the pll_areset (analog reset) signal goes high, the RX_Vcm value is less than the 1.1 V. This value varies unpredictably because the circuit is tristated. RX_Vcm is referenced from the Stratix GX receiver analog power supply.
If external termination is used, the receiver must be externally terminated and biased to 1.1 V. Figure 2–9 shows an example of an external termination and biasing circuit.

**Figure 2–9. External Termination & Biasing Circuit**

Enable Stratix GX-to-Stratix GX Receiver DC Coupling

You can configure the Stratix GX receiver buffers so that DC-coupled Stratix GX-to-Stratix GX communication is possible. The Stratix GX transmitter’s common-mode is typically around 750 mV, while the receiver common mode by default is approximately 1.1 V. However, by enabling DC coupling, the receiver common mode is biased to allow interoperability with the Stratix GX transmitter.

Equalizer Mode

Stratix GX transceivers offer an equalization circuit in each receiver channel to increase noise margins and help reduce the effects of high frequency losses. The programmable equalizer compensates for inter-symbol interference (ISI) and high frequency losses that distort the signal and reduce the noise margin of the transmission medium by equalizing the frequency response.

The transfer function of a transmission line can be represented in the frequency domain as a low-pass filter. Any frequency components below the –3-dB frequency pass through with minimal losses. Frequency components that are greater than the –3-dB frequency are attenuated.
This variation in frequency response yields data-dependant jitter and other ISI effects. By applying equalization, the low frequency components are attenuated. This equalizes the frequency response so that the delta between the low frequency and high frequency components are reduced, which minimizes the ISI effects from the transmission medium.

In Stratix GX transceivers, the programmable equalizer settings can have one of five values (0 through four). You should experiment with the equalization values to determine the optimal setting based on your system variables.

As with the VOD settings, you can set the equalization settings statically during configuration or adjust them dynamically in user mode. You can select the static equalization value through a drop-down menu in the altgxb MegaWizard Plug-In Manager. This action sets the appropriate equalization setting in the configuration file. The disadvantage of this mode is that the equalization is set on a per-transceiver block basis and cannot be changed without regenerating another programming file.

On the other hand, if you select the dynamic adjustment in the altgxb MegaWizard Plug-In Manager, the equalization setting can be configured dynamically by the device during user mode. This configuration is accomplished by asserting encoded values on the rx_equalizerctrl signal, which is instantiated in the altgxb module when this option is selected. This feature lets you make quick performance evaluations of the various settings without having to recompile and regenerate multiple configuration files. Another advantage is that this option allows the equalization of each channel to be configured independently. Refer to “MegaWizard Plug-In Manager Analog Features” on page 2–20 for more details.

**Receiver PLL**

Each transceiver block contains four receiver PLLs and a slow-speed reference clock. The receiver PLLs receive the reference clock and generate the high-speed serial clock used by the CR. The slow-speed reference clock is used for the transceiver logic. Figure 2–10 shows the block diagram for the lock-to-reference portion of the receiver PLL.

This section focuses on the receiver PLL in Lock-to-Reference mode. The lock-to-data circuit has been omitted. Refer to “Lock-to-Reference Mode & Lock-to-Data Mode” on page 2–16 for more information on the operation between the two modes.
The receiver PLL contains an optional loss-of-lock indicator signal (rx_locked) that indicates when the receiver PLL is not locked to the reference clock. The rx_locked signal is active low. A low signal indicates that the PLL is locked to a reference clock; a high signal indicates that the PLL is not locked to the reference clock.

Figure 2–10. Receiver PLL Block Diagram

Note to Figure 2–10:
(1) \( m = 8, 10, 16, \) or 20.

Table 2–4 lists some of the clock recovery unit specifications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input reference frequency range</td>
<td>25 MHz to 650 MHz</td>
</tr>
<tr>
<td>Data rate support</td>
<td>500 Mbps to 3.1875 Gbps</td>
</tr>
<tr>
<td>Multiplication factor ( (W) )</td>
<td>2, 4, 5, 8, 10, 16, or 20 ( (1) )</td>
</tr>
</tbody>
</table>

Note to Table 2–4:
(1) Multiplication factors 2, 4, and 5 can only be achieved with the use of the pre-divider on the REFCLKB port or if the CRU is trained with the low speed clock from the transmitter PLL.

Clock Synthesis

The maximum input frequency of the PFD of the receiver PLL is 325 MHz. To achieve reference clock frequency above this limit, the Quartus II software enables the divide by 2 pre-divider on the dedicated local REFCLKB path. This divides the reference clock frequency by a factor of 2 and then the /m factor compensates the frequency difference. For example, given a data rate of 2,488 Mbps with a reference clock of 622 MHz, the reference clock must be assigned to the REFCLKB port,
where the reference clock signal is divided by 2, yielding a 311 MHz clock at the PFD. This 311-MHz reference clock is then multiplied by a factor of 8 to achieve the 2,488-MHz clock at the VCO.

If the reference clock (\texttt{RX\_CRUCLK}) exceeds 325 MHz, the clock must be fed by the dedicated local reference clock pin, \texttt{REFCLKB}. By default, the Quartus II software assigns pins to be LVTTL, so a 1.5-V PCML I/O standard assignment is required to select the \texttt{REFCLKB} port as the reference source. The Quartus II software prompts a fitter error if the reference clock exceeds 325 MHz and the reference clock source is not on the \texttt{REFCLKB} port.

The pre-divider on the \texttt{REFCLKB} path is also used to support additional multiplication factors. The block diagram in Figure 2–10 on page 2–13 shows that /m supports only multiplication factors of 8, 10, 16, and 20, but Table 2–4 states that the additional multiplication factors of 2, 4, and 5 can also be achieved.

Without using the transmitter PLL, the pre-divider achieves the multiplication factors of 4 and 5. A multiplication factor of 4 is achieved by pre-dividing the reference clock by 2 and then multiplying the resulting frequency by 8, which yields a multiplication factor of 4. A multiplication factor of 5 is achieved in the same manner by pre-dividing the reference clock by 2 and then multiplying the resulting frequency by 10, which yields a multiplication factor of 5.

The MegaWizard Plug-In Manager \texttt{altgxb} option enables the transmitter PLL in receiver mode. There is also an option to train the receiver CRU with the output of the low-speed transmitter PLL clock. If you select this option, all the multiplication factors that are supported in the transmitter PLL are also supported in the receiver CRU PLL, including the multiplication factor of 2. This option selects the low-speed transmitter PLL clock as the reference source. The low speed transmitter PLL clock is either divided by a SERDES factor of 8 or 10. The receiver PLL then multiplies this reference clock by a factor of 8 or 10 to achieve the same multiplication factor as the transmitter PLL.

For example, a multiplication factor of 2 is achieved on the transmitter PLL by pre-dividing the reference clock by 2 and then multiplying the resultant frequency by 4, which yields a multiplication factor of 2. However, on the low-speed clock output, this frequency is divided by a factor of 8 or 10, depending on the deserialization factor. The low-speed clock feeds the reference of the receiver PLL where the clock is multiplied back up by a factor of 8 or 10, which results in total multiplication factor of 2.
Table 2–5 lists the possible multiplication values as a function of the reference clock source to the receiver PLL. Table 2–5 assumes that the reference clock (RX.CRUCCLK) is directly fed from the source listed and does not factor any pre-clock synthesis (that is, a Stratix GX PLL driving a global clock used for the receiver PLL reference clock source).

<table>
<thead>
<tr>
<th>Receiver PLL Reference Clock Source</th>
<th>Multiplication Factors</th>
</tr>
</thead>
<tbody>
<tr>
<td>Global clock, IO bus, general routing</td>
<td>8, 10, 16, 20</td>
</tr>
<tr>
<td>Inter-transceiver routing</td>
<td>4, 5, 8, 10, 16, 20</td>
</tr>
<tr>
<td>Dedicated local REFCLKB</td>
<td>4, 5, 8, 10, 16, 20</td>
</tr>
<tr>
<td>Low-speed transmitter PLL clock</td>
<td>2, 4, 5, 8, 10, 16, 20</td>
</tr>
</tbody>
</table>

You specify the data rate of the channel and receiver CRU clock period of the receiver reference clock. The data rate divided by the input clock period must equal one of the multiplication factors listed in Table 2–5.

**PPM Frequency Threshold Detector**

The PPM frequency threshold detector senses whether the incoming reference clock to the CRU and the PLL VCO of the CRU are within a prescribed PPM tolerance range. Valid parameters are 125, 250, 500, or 1,000 PPM. The default parameter, if no assignments are made, is 1,000 PPM. The output of the PPM frequency threshold detector is one of the variables that asserts the rx_freqlocked signal. Refer to “Clock Recovery Unit” on page 2–16 for more detail regarding the rx_freqlocked signal.

**Receiver Bandwidth Type**

The Stratix GX receiver PLL in the CRU offers a programmable bandwidth setting. The bandwidth of a data recovery PLL is the measure of its ability to track the input data and jitter. The bandwidth is determined by the –3-dB frequency of the closed-loop gain of the PLL.

A higher bandwidth setting provides a faster lock time and tracks greater jitter on the input data source, rx_in[], which passes it through the PLL. This helps reject noise from the VCO and power supplies. A low-bandwidth setting, on the other hand, filters out more high-frequency data input jitter, but increases lock time.
Valid receiver bandwidth settings are low, medium, and high. The –3-dB frequencies for these settings vary due to the non-linear nature and data dependencies of the circuit. You vary the bandwidth to customize the performance on specific systems.

Clock Recovery Unit

The CRU in each Stratix GX receiver channel recovers the clock from the serial data stream on RX_IN. You can set the CRU to automatically or manually alter the receiver PLL phase and frequency to match the bit transition on the incoming data stream. This is to eliminate any clock-to-data skew or to keep the receiver PLL locked to the reference clock (lock-to-data or lock-to-reference mode). The CRU generates two clocks, a high-speed RCVD_CLK to feed the deserializer and a low-speed RCVD_CLK to feed transceiver logic. You can set the CRU to optionally detect run-length violations in the incoming data stream and generate an error whenever the preset run length is exceeded (run-length violation detection circuit).

Lock-to-Reference Mode & Lock-to-Data Mode

The Stratix GX device offers both automatic and manual locking options, as described in the following sections.

Automatic Lock Mode

By default, the CRU initially locks to the CRU reference clock RX_CRUCLK (lock-to-reference mode) until conditions warrant the switchover to the incoming data (lock-to-data mode). The device switches to the lock-to-data mode when the rx_freqlocked signal goes high. After switching to lock-to-data mode, the CRU requires more time to lock to the incoming serial data.

For information about the CRU to serial data lock time, which includes frequency lock (during lock-to-reference mode) and phase lock (during lock-to-data mode), refer to the Stratix GX Device Family Data Sheet section of the Stratix GX Device Handbook, Volume 1. Also refer to the Reset Control & Power Down chapter for the recommendations on resets.

To automatically transition from the lock-to-reference mode to the lock-to-data mode, the following conditions must be met:

- The CRU PLL is within the prescribed PPM frequency threshold setting (125, 250, 500, or 1,000 PPM) of the CRU reference clock.
- Reference clock and CRU PLL output are phase matched (phases are within 0.08 UI).
During the lock-to-reference mode, the frequency detector determines whether the reference clock to the receiver PLL and the VCO output are within the prescribed PPM setting.

The phase lock happens when the phase-frequency detector up/down transitions are relatively few and, the pulse widths are sufficiently narrow. These conditions show that the PLL is close to absolute phase lock to the reference clock. This ensures that when actual data signals are sampled, the receiver PLL locks to the fundamental REFCLK frequency and does not drift off to any sub-harmonic.

In lock-to-data mode, the PLL uses a phase detector to keep the recovered clock aligned properly with the data. If the PLL does not stay locked to data because of problems such as frequency drift or severe amplitude attenuation, the receiver PLL locks back to the reference clock of the CRU to train the VCO. When the device is in lock-to-data mode, the CRU tries to align itself with incoming data and there is no phase relationship with the reference clock.

In lock-to-data mode, the `rx_freqlocked` signal is asserted, and the `rx_locked` signal looses its significance. The `rx_locked` signal signifies that the CRU has locked to the reference clock. When the CRU is in lock-to-data mode, the `rx_locked` signal behavior is not predictable.

In automatic lock mode, CRU is forced out of lock-to-data mode if the CRU PLL is not within the recommended PPM frequency threshold setting (125 PPM, 250 PPM, 500 PPM, 1000 PPM) of the CRU reference clock.

When the CRU goes out of lock-to-data mode, the `rx_freqlocked` signal goes low. The `rx_freqlocked` signal also goes low when either the `rxanalogreset` or `pll_areset` signal goes high. The `rxanalogreset` signal powers down the receiver and the `pll_areset` signal powers down the entire transceiver block (four channels).

**Manual Lock Options**

Two optional input pins, `rx_locktorefclk[]` and `rx_locktodata[]`, are available that let you control whether the CRU PLL automatically or manually switches between lock-to-reference clock and lock-to-data modes. This lets you bypass the default automatic switchover circuitry if either the `rx_locktorefclk[]` or `rx_locktodata[]` signal is instantiated.

When the `rx_locktorefclk[]` signal is asserted, it forces the CRU PLL to lock to the reference clock (RX_CUCLK). Asserting the `rx_locktodata[]` signal forces the CRU PLL to lock to data, whether
or not the CRU is ready. When both signals are asserted, the
rx_locktodata[] signal takes precedence over the
rx_locktorefclk[] signal.

You might want to have control over both rx_locktorefclk[] and
rx_locktodata[] signals to potentially reduce the CRU lock times.
The PPM threshold frequency detector and phase relationship detector
require additional latencies to ensure that the CRU is ready to lock to
data. These extra latencies are potentially reduced by manually
controlling the CRU train signals. You assert the rx_locktorefclk[]
signal to initially train the CRU and, after some delta time, assert the
rx_locktodata[] signal.

You configure the controller that controls the signals based on your
system. You do this by experimenting because many variables must be
considered, such as temperature, transition densities, and data rates.
However, by doing so, you are not subjected to the CRU lock times
required to verify if the two conditions to switch from lock-to-reference
mode to lock-to-data mode in the defaulted automatic mode are met.
When the rx_locktorefclk goes high, the rx_freqlocked signal is
ignored and does not toggle. The rx_freqlocked signal always goes
high if lock-to-data mode is asserted. If you want to transition from
lock-to-data mode to automatic mode, the transition should be followed
by rxanalogreset to send the rx_freqlocked signal low. The CRU
does not often transition from manual mode to automatic mode during
system operation.

The rxanalogreset signal functions like a power down signal
as opposed to a digital reset. For more information on various
reset signals, refer to the Reset Control & Power Down chapter of

Run Length Violation Detection Circuit

The programmable run length violation (RLV) circuit is in the CRU and
detects consecutive ones or zeros in the data. If the data stream exceeds
the preset maximum number of consecutive ones or zeros, the violation
is signified by the assertion of the rx_rlv signal.

The rx_rlv signal is not synchronized to the parallel data, and as a result
appears in the logic array earlier than the run-length violation data. To
ensure that the FPGA latches this signal in systems where there are
frequency variations between the recovered clock and the PLD logic
array clock, the rx_rlv signal is asserted for more than two clock cycles
in 8- or 10-bit data modes and three clock cycles in 16- or 20-bit data
modes.
If the data width is 8 or 16, set the legal run length threshold values within the range of 4 to 128 UI in multiples of four. If the data width is 10 or 20, or if using 8b10b, set the legal run length threshold values within the range of 5 to 160 UI in multiples of five.

Refer to the *Stratix GX Device Family Data Sheet* section of the *Stratix GX Device Handbook, Volume 1* to verify the guaranteed maximum run length.

**Deserializer (Serial-to-Parallel Converter)**

The deserializer converts incoming high-speed serial data streams to either 8- or 10-bit-wide parallel data synchronized to the recovered clock of the CRU. The deserializer drives the parallel data to the pattern detector and word aligner, as shown in Figure 2–11. The data rate of the deserializer output bus is the input data rate divided by the width of the output data bus. For example, for a 10-bit bus and a serial input data rate of 2.5 Gbps, the parallel data rate is 2500/10 or 250 MHz. The first bit into the deserializer is the LSB of the data bus out of the deserializer.

**Figure 2–11. Deserializer Block Diagram**

![Deserializer Block Diagram](image)

*Figure 2–12 shows the serial bit order of the deserializer input and the parallel data out of the deserializer.*

The serial data is received LSB to MSB.
This section describes the analog options for the instantiation of the 
\texttt{altgxb} megafunction in the Quartus II MegaWizard® Plug-In Manager. 
Altera® recommends that the Stratix GX transceiver block be instantiated 
and parameterized through the MegaWizard Plug-In Manager. The 
MegaWizard Plug-In Manager offers a graphical user interface (GUI) that 
organizes the \texttt{altgxb} options in easy-to-use sections. The wizard also 
sets the proper ports and parameters automatically, based on the options 
and parameters you select. Invalid settings are automatically flagged to 
avoid illegal configurations.

Although you can instantiate the Stratix GX block directly by calling out 
the \texttt{altgxb} megafunction, Altera recommends using the MegaWizard 
Plug-In Manager to instantiate your \texttt{altgxb} megafunction, reducing the 
likelihood of invalid settings.

\textbf{MegaWizard Plug-In Manager Analog Feature Considerations}

Each \texttt{altgxb} MegaWizard Plug-In Manager instantiation uses one or 
more transceiver blocks based on the number of channels you select. 
There are four channels per transceiver block. If a MegaWizard Plug-In 
Manager instantiation uses fewer than four channels, the remaining 
channels in that transceiver block are not available for use.

Each MegaWizard Plug-In Manager instantiation must have similar 
functionality and data rates. If you want transceiver blocks that differ in 
functionality and data rates, create a separate MegaWizard Plug-In 
Manager instantiation for each transceiver block.

As mentioned in the clocking section, the MegaWizard Plug-In Manager 
also displays the configuration of the \texttt{altgxb} megafunction. 
Figures 2–13 through 2–19 change dynamically based on the selected 
mode, options, and clocking schemes.

\textbf{Figure 2–13} shows the analog options on page 3 of the \texttt{altgxb} 
MegaWizard Plug-In Manager.
Table 2–6 describes the available options on page 3 of the MegaWizard Plug-In Manager for your altgxb custom megafunction variation.

<table>
<thead>
<tr>
<th>altgxb Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instantiate Transmitter PLL</td>
<td>This option is available in receiver-only mode. It supports use of the transmitter PLL even when the transmit channel is disabled. Provides a non-recovered clock output for the logic array.</td>
</tr>
<tr>
<td>Train Receiver PLL CRU clock from Transmitter PLL</td>
<td>This option enables the transmitter PLL to train the receiver PLL. Use this option to support additional multiplication factors for the receiver PLL. This option also supports the separation of receiver and transmitter reference clocks. An additional input receiver reference clock (rx_cruclk) is available when this option is turned off. The first option that is enabled is needed for non-encoded 16-bit modes with a line rate of 2,600 Mbps or greater. For more details about this feature, refer to &quot;Clock Synthesis&quot; on page 2–6.</td>
</tr>
</tbody>
</table>
Table 2–6. MegaWizard Plug-In Manager Options (Page 3 for Analog) (Part 2 of 2)

<table>
<thead>
<tr>
<th>altgxb Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Select the bandwidth type on the Transmitter PLL</td>
<td>High bandwidth supports faster lock times. It also tracks higher frequency jitter (based on the –3-db frequency of the PLL gain plot) on the input clock. Low bandwidth has a smaller pass band to filter out more high-frequency jitter, but has a slower lock time.</td>
</tr>
<tr>
<td>Select the acceptable PPM threshold between the Receiver PLL VCO and the CRU clock</td>
<td>Selectable PPM difference tolerance {125, 250, 500, 1000} between the Receiver PLL VCO and the CRU clock. This is one of three parameters that affect the rx_freqlocked signal. If an out-of-tolerance event occurs, rx_freqlocked goes low.</td>
</tr>
<tr>
<td>rxanalogreset (send reset signal to the analog portion of the receiver)</td>
<td>The rxanalogreset port resets the receiver's analog circuits, including the receiver PLL. Each active receiver channel has its own analog reset.</td>
</tr>
<tr>
<td>pll_aredset (send reset signal to the Quad)</td>
<td>The pll_aredset port resets the entire transceiver block (all receiver and transmitter digital and analog circuits, including receiver and transmitter PLLs).</td>
</tr>
<tr>
<td>pllenable (send enable signal to the Quad)</td>
<td>The pllenable port enables the entire transceiver block; if deasserted, the entire transceiver block is held in the reset condition.</td>
</tr>
<tr>
<td>pll_locked (indicates Transmitter PLL is in lock with the reference input clock)</td>
<td>For more information, refer to the Ports &amp; Parameters chapter in volume 2 of the Stratix GX Device Handbook.</td>
</tr>
</tbody>
</table>

Figure 2–14 shows the analog options on page 4 of the altgxb MegaWizard Plug-In Manager.
Figure 2–15 shows the analog options on page 5 of the altgxb MegaWizard Plug-In Manager.
Table 2–7 describes the available options on page 5 of the MegaWizard Plug-In Manager for your altgxb custom megafunction variation.

**Table 2–7. MegaWizard Plug-In Manager Options (Page 5 for Analog)**

<table>
<thead>
<tr>
<th>altgxb Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable run-length violation checking</td>
<td>Enable run-length violation circuit. If enabled, the optional output pin rx_rlv is available and pulses high when the specified run length is violated. In 8- or 16-bit mode, set the run length threshold from 4 to 124 in steps of 4. In 10 and 20-bit mode, or if using 8B/10B, set the run-length threshold from 5 to 160 in steps of 5.</td>
</tr>
</tbody>
</table>

Figure 2–16 shows the analog options on page 6 of the altgxb MegaWizard Plug-In Manager.
Table 2–8 describes the available options on page 6 of the MegaWizard Plug-In Manager for your altgxb custom megafunction variation.

<table>
<thead>
<tr>
<th>altgxb Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Enable Stratix GX to Stratix GX DC coupling</td>
<td>Stratix GX to Stratix GX DC coupling only. Lets the receiver accept a 1.5-V PCML signal from a Stratix GX transmitter buffer.</td>
</tr>
<tr>
<td>Force signal detection</td>
<td>This option forces rx_signaldetect to be set HIGH. This option is always enabled in the current version of the software.</td>
</tr>
<tr>
<td>Use equalizer control signal</td>
<td>The Use equalizer control signal option enables dynamic equalization via the optional rx_equalizerctrl input port.</td>
</tr>
<tr>
<td>Select the equalizer control setting</td>
<td>If this control signal is not used, you can set equalization in the MegaWizard Plug-In Manager via the Select the equalizer control setting. The valid values are 0 through 4, with 0 being off and 4 being the largest gain setting.</td>
</tr>
</tbody>
</table>
Table 2–8. MegaWizard Plug-In Manager Options (Page 6 for Analog) (Part 2 of 2)

<table>
<thead>
<tr>
<th>altgxb Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Select the signal loss threshold</td>
<td>This option is unavailable in the current version of the software. Receiver signal detection is always forced.</td>
</tr>
<tr>
<td>Select the bandwidth type on the Receiver</td>
<td>Available settings are High, Medium, and Low. High bandwidth allows for faster lock times and tracks higher frequency jitter (based on the -3 db frequency of the PLL gain plot) on the input clock. Low bandwidth contains a smaller pass band to filter out more high-frequency jitter, but has slower lock times.</td>
</tr>
</tbody>
</table>

Figure 2–17 shows the analog options on page 7 of the altgxb MegaWizard Plug-In Manager.
Table 2–9 describes the available options on page 7 of the MegaWizard Plug-In Manager for your altgxb custom megafunction variation.

Table 2–9. MegaWizard Plug-In Manager Options (Page 7 for Analog)

<table>
<thead>
<tr>
<th>altgxb Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>rx_locktorefclk (control signal for Receiver PLL to lock to the reference clock)</td>
<td>Optional input signal that forces the CRU to lock to the reference clock. This disables the auto switch-over mode that switches the CRU to lock-to-data mode. If both rx_locktorefclk and rx_locktodata are asserted, then rx_locktodata takes precedence.</td>
</tr>
<tr>
<td>rx_locktodata (control signal for Receiver PLL to lock to the received data)</td>
<td>Optional input signal that forces the CRU to lock to the incoming data. If both rx_locktorefclk and rx_locktodata are asserted, rx_locktodata takes precedence.</td>
</tr>
<tr>
<td>rx_clkout (receiver input clock)</td>
<td>Refer to the Ports &amp; Parameters chapter in volume 2 of the Stratix GX Device Handbook.</td>
</tr>
<tr>
<td>rx_locked (indicates that the Receiver PLL is locked to the reference clock (active low))</td>
<td>Refer to the Ports &amp; Parameters chapter in volume 2 of the Stratix GX Device Handbook.</td>
</tr>
</tbody>
</table>
| rx_freqlocked (indicates that the Receiver PLL is locked to the input data) | Optional output signal that indicates when the CRU is locked to the incoming data stream. The lock indication is based on the following conditions:  
  ● The CRU PLL is within the prescribed PPM frequency threshold setting (125 PPM, 250 PPM, 500 PPM, 1,000 PPM) of the CRU reference clock.  
  ● The reference clock and CRU PLL output are phase matched (~ phases are within 0.08 UI). |
| rx_signaldetect (indicates receiver signal is detected with data) | Refer to the Ports & Parameters chapter in volume 2 of the Stratix GX Device Handbook. |
| rx_syncstatus (output signal from pattern detector and word aligner) | Refer to the Ports & Parameters chapter in volume 2 of the Stratix GX Device Handbook. |

Figure 2–18 shows the analog options on page 8 of the altgxb MegaWizard Plug-In Manager.
Notes to Figure 2–18:

1. The **Use V<sub>OD</sub> control signal** option enables dynamic V<sub>OD</sub> adjustment via the optional **tx_vodctrl** input port. If this control signal is not used, set the V<sub>OD</sub> in the MegaWizard Plug-In Manager via the **Select the V<sub>OD</sub> control setting** option. The valid values are based on your transmitter termination value and range from 400 to 1,600 mV.

2. The **Use Preemphasis control signal** option enables dynamic pre-emphasis control using the optional **tx_preemphasisctrl** input port. If this control signal is not used, set the pre-emphasis in the MegaWizard Plug-In Manager using the **Select the preemphasis control setting** option. The valid values are 1 through 5, where 1 is the smallest pre-emphasis value and 5 is the largest. The amount of pre-emphasis is based on your V<sub>OD</sub> values.

Table 2–10 describes the available options on page 8 of the MegaWizard Plug-In Manager for your altgxb custom megafunction variation.

| Table 2–10. MegaWizard Plug-In Manager Options (Page 8 for Analog) (Part 1 of 2) |
|---------------------------------|---------------------------------|
| **altgxb Setting**             | **Description**                 |
| Use external Transmitter       | This option allows you to disable the on-chip termination on tx<sub>out</sub> and instead use external termination. |
| termination                    |                                 |
| Use Voltage Output Differential | The **Use V<sub>OD</sub> control signal** option enables dynamic V<sub>OD</sub> adjustment via the optional tx<sub>vodctrl</sub> input port. |
| (VOD) control signal           |                                 |
Figure 2–19 shows page 9, the Simulation Libraries page, of the MegaWizard Plug-In Manager for the analog feature.

**Table 2–10. MegaWizard Plug-In Manager Options (Page 8 for Analog) (Part 2 of 2)**

<table>
<thead>
<tr>
<th>altgxb Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Select the Voltage Output Differential (VOD) control setting</td>
<td>If this control signal is not used, set the VOD in the MegaWizard Plug-In Manager via the Select the VOD control setting option. The valid values are based on your transmitter termination value and range from 400 to 1,600 mV.</td>
</tr>
<tr>
<td>Use preemphasis control signal</td>
<td>The Use Preemphasis control signal option enables dynamic pre-emphasis control using the optional tx_preemphasisctrl input port.</td>
</tr>
<tr>
<td>Select the preemphasis control setting (0 is the least preemphasis and 5 is the most preemphasis)</td>
<td>If this control signal is not used, set the pre-emphasis in the MegaWizard Plug-In Manager using the Select the preemphasis control setting. The valid values are 1 through 5, where 1 is the smallest pre-emphasis value and 5 is the largest. The amount of pre-emphasis is based on your VOD values.</td>
</tr>
</tbody>
</table>
Figure 2–20 shows page 10 of the MegaWizard Plug-In Manager for the analog feature. You can select optional files on this page. After you make your selections, click Finish to generate the files.

**Figure 2–20. MegaWizard Plug-In Manager - altgxb (Page 10)**

Stratix GX Transceiver Merging

A transceiver block contains four transceivers. In a design, an altgxb instantiation is placed in one or more transceiver blocks and potentially leaves unused transceivers in a block. For example, a six transceiver instantiation completely fills one transceiver block and half fills a second, taking up two full transceiver blocks. If another instantiation is in the design, it is placed the same way. For example, an instantiation of two transmitters takes up a third transceiver block. Merging two of the partially filled transceiver blocks into one transceiver block reduces the resources used and allows a design to fit into a device with fewer transceiver blocks.
The `altgxb` MegaWizard Plug-In Manager in the Quartus II software has a feature that allows merging of similar quads (transceiver blocks). With a few exceptions, transceiver blocks can be merged if the options chosen in the wizard are the same. The Quartus II software merges the transceiver blocks automatically if you turn on the merging option for each instantiation. Table 2–11 shows the considerations for merging.

### Table 2–11. Stratix GX Merging Considerations

<table>
<thead>
<tr>
<th>Merging Rules</th>
<th>Required to Match Between Transceiver Blocks</th>
<th>Not Required to Match Between Transceiver Blocks</th>
</tr>
</thead>
<tbody>
<tr>
<td>MegaWizard Plug-In Manager options</td>
<td>USE_8B_10_MODE</td>
<td>VOD</td>
</tr>
<tr>
<td></td>
<td>USE_DOUBLE_DATA_MODE</td>
<td>Pre-emphasis</td>
</tr>
<tr>
<td></td>
<td>CHANNEL_WIDTH</td>
<td>Equalization</td>
</tr>
<tr>
<td></td>
<td>SYNC_MODE</td>
<td>Number of transmitters</td>
</tr>
<tr>
<td></td>
<td>DATA_RATE</td>
<td>Number of receivers</td>
</tr>
<tr>
<td></td>
<td>TRANSMIT_PROTOCOL</td>
<td></td>
</tr>
<tr>
<td>Input control signals must be shared across transceiver blocks and must be from the same source</td>
<td>Clock</td>
<td></td>
</tr>
<tr>
<td></td>
<td>CRU_CLOCK</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PLL_RESET</td>
<td></td>
</tr>
<tr>
<td></td>
<td>PLL_ENABLE</td>
<td></td>
</tr>
<tr>
<td>The merging partial transceiver blocks must reduce the number of transceiver block when merged</td>
<td>The total number of receivers and transmitters must be ( tx \leq 4 \times n ) and ( rx \leq 4 \times n ), where ( n ) is the reduced number of transceiver blocks remaining after merging.</td>
<td></td>
</tr>
</tbody>
</table>

The Quartus II software does not merge two transceiver blocks if they won’t completely fit into one. It can, however, merge three transceiver blocks into two. Figure 2–21 shows a configuration with three transceiver blocks that can potentially be merged.

### Figure 2–21. Three Transceiver Configuration

- Three Transmitters
- Three Receivers
- Two Transmitters
- Two Receivers
- Three Transmitters
- Three Receivers

In Figure 2–21, two transceiver blocks cannot merge because there would be extra channels remaining. But because there are three transceiver blocks, the Quartus II software can merge them into two with no remaining channels.
If you turn on the merging option, the Quartus II software automatically merges transceiver blocks if possible or provides a warning during compilation if merging is not possible. The merging feature can reduce the transceiver block resources used in your design.