Contents

1. Intel® FPGA SDK for OpenCL™ Intel® Arria® 10 SoC Development Kit Reference Platform Porting Guide.................................................................................................................................................................................. 3
   1.1. Intel Arria 10 SoC Development Kit Reference Platform: Prerequisites........................................3
   1.2. Features of the Intel Arria 10 SoC Development Kit Reference Platform........................................4
   1.3. Intel Arria 10 SoC Development Kit Reference Platform Board Variants........................................6
   1.4. Contents of the Intel Arria 10 SoC Development Kit Reference Platform.................................................. 7
   1.5. Changes in Intel Arria 10 SoC Development Kit Reference Platform from 17.0 to 17.1.................9
   1.6. Changes in Intel Arria 10 SoC Development Kit Reference Platform from 17.1.2 to 18.0.................................................. 10

2. Developing an Intel Arria 10 SoC Custom Platform........................................................................... 12
   2.1. Initializing an Intel Arria 10 SoC Custom Platform......................................................................................... 12
   2.2. Modifying Your Intel Arria 10 SoC Custom Platform..................................................................................... 13
   2.3. Integrating Your Intel Arria 10 SoC Custom Platform with the Intel FPGA SDK for OpenCL................................................. 14
   2.4. Changing the Device Part Number.................................................................................................................. 14
   2.5. Modifying the Kernel PLL Reference Clock.................................................................................................. 15
   2.6. Modifying the Hard Processor System........................................................................................................ 15
   2.7. Guaranteeing Timing Closure in the Intel Arria 10 SoC Custom Platform.................................................. 15
   2.8. Generating the base.qar Post-Fit Netlist for Your Intel Arria 10 SoC FPGA Custom Platform.................................................. 16

3. Building the Software and SD Card Image for the Intel Arria 10 SoC Development Kit Reference Platform.................................................................................................................................................. 18
   3.1. Compiling the Device Tree Blob.................................................................................................................. 18
   3.2. Compiling the Linux Kernel for the Intel Arria 10 SoC Development Kit.................................................. 19
   3.3. Compiling the OpenCL Linux Kernel Driver.................................................................................................. 20
   3.4. Generating Full-Chip Programming File for SD Card Image..................................................................... 21
   3.5. Building the SD Card Image.......................................................................................................................... 22
       3.5.1. Layout of the OpenCL Micro SD Card.................................................................................................. 22
       3.5.2. Creating the SD Card Image.................................................................................................................. 23
       3.5.3. Guidelines on Imaging the Micro SD Card.......................................................................................... 26
   3.6. Known Issues..................................................................................................................................................... 27

1. Intel® FPGA SDK for OpenCL™ Intel® Arria® 10 SoC Development Kit Reference Platform Porting Guide

The Intel® Arria® 10 SoC Development Kit Reference Platform Porting Guide describes the procedures and design considerations for modifying the Intel Arria 10 SoC Development Kit Reference Platform (a10soc) into your own Custom Platform for use with the Intel FPGA SDK for OpenCL™ (1) (2) SDK.

1.1. Intel Arria 10 SoC Development Kit Reference Platform: Prerequisites

The Intel Arria 10 SoC Development Kit Reference Platform Porting Guide assumes that you are an experienced FPGA designer who is familiar with Intel's FPGA design tools and concepts.

Prerequisites for the a10soc Reference Platform:
- An Intel Arria 10 SoC-based accelerator card with working memory interfaces
  Test these interfaces together in the same design using the same version of the Intel Quartus® Prime Pro Edition software that you will use to develop your Custom Platform.
- Intel Quartus Prime Pro Edition software Version 19.1
- Designing with Logic Lock Plus regions
- Intel SoC Embedded Design Suite Version 19.1

General knowledge prerequisites:
- FPGA architecture, including clocking, global routing, and I/Os
- High-speed design
- Timing analysis
- Platform Designer design, and Avalon® and AXI interfaces
- Tcl scripting
- Hard processor systems (HPS)
- DDR4 external memory
- Embedded Linux development

(1) OpenCL and the OpenCL logo are trademarks of Apple Inc. used by permission of the Khronos Group™.

(2) The Intel FPGA SDK for OpenCL is based on a published Khronos Specification, and has passed the Khronos Conformance Testing Process. Current conformance status can be found at www.khronos.org/conformance.
This document also assumes that you are familiar with the following Intel FPGA SDK for OpenCL-specific tools and documentation:

- Custom Platform Toolkit and the *Intel FPGA SDK for OpenCL Custom Platform Toolkit User Guide*
- *Intel FPGA SDK for OpenCL Intel Arria 10 GX FPGA Development Kit Reference Platform Porting Guide*
- *Intel FPGA SDK for OpenCL Cyclone V SoC Development Kit Reference Platform Porting Guide*

**Related Information**

- *Intel FPGA SDK for OpenCL Custom Platform Toolkit User Guide*
- *Intel FPGA SDK for OpenCL Intel Arria 10 GX FPGA Development Kit Reference Platform Porting Guide*
- *Intel FPGA SDK for OpenCL Intel Cyclone V SoC Development Kit Reference Platform Porting Guide*
- *Intel FPGA SDK for OpenCL Intel Stratix V Network Reference Platform Porting Guide*

**1.2. Features of the Intel Arria 10 SoC Development Kit Reference Platform**

Prior to designing an Intel FPGA SDK for OpenCL Custom Platform, decide on design considerations that allow you to fully utilize the available hardware on your computing card.

The Intel Arria 10 SoC Development Kit Reference Platform targets a subset of the hardware features available in the Intel Arria 10 SoC Development Kit.
Figure 1. Hardware Features of the Intel Arria 10 SoC Development Kit

Features of the a10soc Reference Platform:

- **OpenCL Host**
  
  The a10soc Reference Platform uses the Intel SoC HPS as the host that connects to the FPGA fabric via HPS-to-FPGA (H2F) and FPGA-to-HPS (F2H) bridges.

- **OpenCL Global Memory**
  
  The hardware provides two 1-gigabyte (GB) DDR4 SDRAM daughtercards that are mounted on the HiLo connectors (HPS Memory and FPGA Memory in Figure 1 on page 5).

- **FPGA Programming via Partial Reconfiguration (PR) over HPS lightweight bridge (Lw-bridge)**

- **Guaranteed Timing**

  The a10soc Reference Platform relies on the Intel Quartus Prime Pro Edition compiler to provide guaranteed timing closure. The timing-clean a10soc Reference Platform is preserved in the form of a precompiled post-fit netlist (that is, the base.qdb Intel Quartus Prime Partition Database File that is part of the base.qar Intel Quartus Prime Archive File). The Intel FPGA SDK for OpenCL Offline Compiler imports this preserved post-fit netlist into each OpenCL kernel compilation.
1.3. Intel Arria 10 SoC Development Kit Reference Platform Board Variants

The Intel Arria 10 SoC Development Kit Reference Platform includes two board variants.

- a10soc—targets the Intel Arria 10 SoC Development Kit with one DDR4 memory. The DDR4 memory is shared between the HPS host and the FPGA.
- a10soc_2ddr—targets the Intel Arria 10 SoC Development Kit with two DDR4 memories. One DDR4 memory is an added FPGA memory, and the other DDR4 memory is shared between the HPS host and the FPGA.

To compile your OpenCL kernel for a specific board variant, include the `--board=<board_name>` option in your `aoc` command.

For example: `aoc --board=a10soc_2ddr myKernel.cl`

Related Information

Compiling a Kernel for a Specific FPGA Board (`-board=<board_name>`)
1.4. Contents of the Intel Arria 10 SoC Development Kit Reference Platform

Familiarize yourself with the directories and files within the Intel Arria 10 SoC Development Kit Reference Platform because they are referenced throughout this document.

Table 1. Highlights of the Intel Arria 10 SoC Development Kit Reference Platform Directory

<table>
<thead>
<tr>
<th>File or Directory</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>board_env.xml</td>
<td>An XML file that describes the Reference Platform to the Intel FPGA SDK for OpenCL.</td>
</tr>
<tr>
<td>hardware</td>
<td>Contains the Intel Quartus Prime project templates for the two board variants. Each a10soc Reference Platform board variant implements the entire OpenCL hardware system on a given Intel Arria 10 SoC Development Kit. See Table 2 on page 7 for a list of files in this directory.</td>
</tr>
</tbody>
</table>
| arm32             | Directory that contains the following:  
|                   | • A bin subdirectory containing the SDK utilities that are specific to the Intel Arria 10 SoC Development Kit (that is, program and diagnose).  
|                   | • A driver subdirectory containing the OpenCL Linux driver source code.  
|                   | • A lib subdirectory containing the memory-mapped device (MMD) library that is precompiled to 32-bit Linux on ARM® Cortex®-A9 environment. |

Table 2. Contents of the Board Variant Directory

The following table lists the files in the <path_to_a10soc>/hardware/<board_name> directory, where <board_name> is the name of the board variant.

<table>
<thead>
<tr>
<th>File</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>acl_kernel_interface_soc_pr.qsys</td>
<td>Platform Designer system that implements interface to kernel system in board system.</td>
</tr>
<tr>
<td>base.qsf</td>
<td>Intel Quartus Prime Settings File for the base project revision. To compile to base revision, add the -bsp-flow=base argument to aoc command (for example, aoc -bsp-flow=base myKernel.cl). Use this revision when porting the a10soc Reference Platform to your own Custom Platform. The Intel Quartus Prime Pro Edition software compiles this base project revision from source code.</td>
</tr>
<tr>
<td>base.qar</td>
<td>Intel Quartus Prime Archive File containing base.qdb, pr_base.id, and base.sdc. This file is generated by the scripts/post_flow_pr.tcl file during base revision compile, and is used during import revision compilation.</td>
</tr>
<tr>
<td>base.qdb</td>
<td>Intel Quartus Prime Database Export File the contains the precompiled netlist of the static regions of the design.</td>
</tr>
<tr>
<td>pr_base.id</td>
<td>Text file containing a unique number for a given base compilation that the runtime uses to determine whether it is safe to use PR programming.</td>
</tr>
</tbody>
</table>

...continued...
<table>
<thead>
<tr>
<th>File</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>base.sdc</td>
<td>Synopsys Design Constraints File that the Intel Quartus Prime software autogenerates during a base compilation. The base.sdc file is used in the top revision compilation to import all the timing constraints from the static region.</td>
</tr>
<tr>
<td>board.qsys</td>
<td>Platform Designer system that implements the board interfaces (that is, the static region) of the OpenCL hardware system.</td>
</tr>
<tr>
<td>board_spec.xml</td>
<td>XML file that provides the definition of the board hardware interfaces to the SDK.</td>
</tr>
<tr>
<td>DMA_system.qsys</td>
<td>Platform Designer system that implements DMA between HPS memory and FPGA memory in the a10soc_2ddr board variant.</td>
</tr>
<tr>
<td>dual_port_splitter.qsys</td>
<td>Platform Designer system that splits requests on single slave to two channels. Used for utilizing two FPGA2SDRAM ports on HPS.</td>
</tr>
<tr>
<td>flat.qsf</td>
<td>Intel Quartus Prime Settings File for the flat project revision. This file includes all the common settings, such as pin location assignments, that are used in the other revisions of the project (that is, base and top). The base.qsf and top.qsf files include, by reference, all the settings in the flat.qsf file. The Intel Quartus Prime software compiles the flat revision with minimal location constraints. The flat revision compilation does not generate a base.qar file that you can use for future import compilations and does not implement the guaranteed timing flow.</td>
</tr>
<tr>
<td>import_compile.tcl</td>
<td>Tcl script for the SDK-user compilation flow (that is, import revision compilation).</td>
</tr>
<tr>
<td>opencl_bsp_ip.qsf</td>
<td>Intel Quartus Prime Settings File that collects all the required .ip files in a unique location. During flat and base revision compilations, the board.qsys Platform Designer file is added to the opencl_bsp_ip.qsf file.</td>
</tr>
<tr>
<td>quartus.ini</td>
<td>Contains any special Intel Quartus Prime software options that you need when compiling OpenCL kernels for the a10soc Reference Platform.</td>
</tr>
<tr>
<td>top.qpf</td>
<td>Intel Quartus Prime Project File for the OpenCL hardware system.</td>
</tr>
<tr>
<td>top.qsf</td>
<td>Intel Quartus Prime Settings File for the SDK-user compilation flow.</td>
</tr>
<tr>
<td>top.sdc</td>
<td>Synopsys® Design Constraints File that contains board-specific timing constraints.</td>
</tr>
<tr>
<td>top.v</td>
<td>Top-level Verilog Design File for the OpenCL hardware system.</td>
</tr>
<tr>
<td>ip/freeze_wrapper.v</td>
<td>Verilog Design File that implements the freeze logic placed at outputs of the PR region.</td>
</tr>
<tr>
<td>ip/acl_kernel_interface_soc_pr/&lt;file_name&gt;</td>
<td>Directory containing the .ip files that the Intel Quartus Prime Pro Edition software needs to parameterize the acl_kernel_interface_soc_pr component. You must provide both the acl_kernel_interface_soc_pr.qsys file and the corresponding .ip files in this directory to the Intel Quartus Prime Pro Edition software.</td>
</tr>
<tr>
<td>ip/board/&lt;file_name&gt;</td>
<td>Directory containing the .ip files that the Intel Quartus Prime Pro Edition software needs to parameterize the board system. You must provide both the board.qsys file and the corresponding .ip files in this directory to the Intel Quartus Prime Pro Edition software.</td>
</tr>
<tr>
<td>ip/DMA_system/&lt;file_name&gt;</td>
<td>Directory containing the .ip files that the Intel Quartus Prime Pro Edition software needs to parameterize the DMA_system component in a10soc_2ddr board variant.</td>
</tr>
</tbody>
</table>
You must provide both the `DMA_system.qsys` file and the corresponding `.ip` files in this directory to the Intel Quartus Prime Pro Edition software.

Directory containing the `.ip` files that the Intel Quartus Prime Pro Edition software needs to parameterize the `dual_port_splitter` component. You must provide both the `dual_port_splitter.qsys` file and the corresponding `.ip` files in this directory to the Intel Quartus Prime Pro Edition software.

IP that receives interrupts from the OpenCL kernel system and `DMA_system`, and sends single IRQ to the host.

IP that splits requests across multiple channels on burst word boundary.

Tcl script that the base revision compilation uses to generate the `base.sdc` file that contains all the constraints collected in the base revision compilation. The Intel Quartus Prime Pro Edition software uses the `base.sdc` file when compiling the import (top) revision.

Tcl script that generates the `fpga.bin` file. The `fpga.bin` file contains all the necessary files for configuring the FPGA.

Tcl script that implements the guaranteed timing closure flow.

Tcl script that executes before the invocation of the Intel Quartus Prime software compilation. Running the script generates the Platform Designer HDL for `board.qsys` and `kernel_mem.qsys`. It also creates a unique ID for the PR base revision (that is, static region). This unique ID is stored in the `pr_base.id` file.

Tcl script that packages up `base.qdb`, `pr_base.id` and `base.sdc` during base revision compile.

Tcl script that regenerates the BAK cache file in your temporary directory.

### 1.5. Changes in Intel Arria 10 SoC Development Kit Reference Platform from 17.0 to 17.1

Following is a list of what has changed in a10soc Reference Platform from 17.0 to 17.1 release:

<table>
<thead>
<tr>
<th>File</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>import_compiles.tcl</code></td>
<td>Updated the file for incremental and fast compile features.</td>
</tr>
<tr>
<td><code>board_spec.xml</code></td>
<td>Updated the version from 17.0 to 17.1.</td>
</tr>
<tr>
<td><code>quartus.ini</code></td>
<td>Added <code>qhd_skip_pr_revision_type_check=on</code> INI to the file.</td>
</tr>
<tr>
<td><code>scripts/post_flow_pr.tcl</code></td>
<td>Updated the file to:</td>
</tr>
<tr>
<td></td>
<td>• Enable the fast compile feature.</td>
</tr>
<tr>
<td></td>
<td>• Remove manual call to <code>quartus_cpf</code> for creating PR programming file since it now done automatically in the flow.</td>
</tr>
<tr>
<td><code>scripts/create_fpga_bin_pr.tcl</code></td>
<td>Added the Quartus version as part of <code>fpga.bin</code>.</td>
</tr>
<tr>
<td>File</td>
<td>Change</td>
</tr>
<tr>
<td>-------------------------</td>
<td>----------------------------------------------------------------------------------------------------------------------------------------</td>
</tr>
<tr>
<td>scripts/qar_ip_files.tcl</td>
<td>Updated the file to include:</td>
</tr>
<tr>
<td></td>
<td>• Changes required for renaming .qsys files.</td>
</tr>
<tr>
<td></td>
<td>• Changes required for moving other tcl scripts into Intel FPGA SDK for OpenCL.</td>
</tr>
<tr>
<td>scripts/regenerate_cache.tcl</td>
<td>Updated the file to include changes required to move bak_flow.tcl into Intel FPGA SDK for OpenCL.</td>
</tr>
<tr>
<td>scripts/bak_flow.tcl</td>
<td>Moved the file into Intel FPGA SDK for OpenCL.</td>
</tr>
<tr>
<td>scripts/helpers.tcl</td>
<td>Moved the file into Intel FPGA SDK for OpenCL.</td>
</tr>
<tr>
<td>board.qsys</td>
<td>• Moved the base address of PR IP from 0xcf0b0 to 0xcf00.</td>
</tr>
<tr>
<td></td>
<td>• Increased the ACL_VERSIONID to 0xA0C7C1E2 due to the PR IP address change.</td>
</tr>
<tr>
<td></td>
<td>• Synced all IPs.</td>
</tr>
<tr>
<td>hw_mmd_constants.h</td>
<td>Increased the ACL_VERSIONID to 0xA0C7C1E2 due to the PR IP address change.</td>
</tr>
<tr>
<td>base.qar</td>
<td>Updated the file with ACDS 17.1 static region.</td>
</tr>
</tbody>
</table>

### 1.6. Changes in Intel Arria 10 SoC Development Kit Reference Platform from 17.1.2 to 18.0

Following is a list of what has changed in a10soc Reference Platform from 17.1.2 to 18.0 release:

**High-level changes include:**

- Various clean up of `import_compile.tcl, pre_flow_pr, post_flow_pr`
- Clean up of old `top_synth` revision (migrated to new simplified PR flow)
- Fix for write .sdc, in `base_write_sdc.tcl`
- AOC no longer emits .qsys files, it emits just Verilog HDL (`kernel_system.v`) and injects a .qip file into project. Changes needed:
  - Instantiate module `kernel_system` from `kernel_system.v` (in `pr_region.v` now)
  - If you use `add_pipe` in `board_spec.xml`, instantiate pipeline registers in the BSP but within the PR region (see `ip/kernel_mem` and `pr_region.v`)

**Table 4. Changes in a10soc Reference Platform from 17.1.2 to 18.0**

<table>
<thead>
<tr>
<th>File</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>base.qar</td>
<td>Updated with 18.0 static region.</td>
</tr>
<tr>
<td>board_spec.xml</td>
<td>Updated version, static region used resources, removed <code>addpipe</code> parameter, which is no longer needed.</td>
</tr>
<tr>
<td>top.qpf</td>
<td>Removed <code>top_synth</code> revision.</td>
</tr>
<tr>
<td>flat.qsf</td>
<td>Removal of obsolete assignments.</td>
</tr>
<tr>
<td>base.qsf</td>
<td>Removed Platform Designer flow.</td>
</tr>
</tbody>
</table>

*continued...*
<table>
<thead>
<tr>
<th>File</th>
<th>Change</th>
</tr>
</thead>
<tbody>
<tr>
<td>kernel_system_inst</td>
<td>pr_region_inst</td>
</tr>
<tr>
<td>top.qsf</td>
<td>Simplified PR flow.</td>
</tr>
<tr>
<td>opencl_bsp_ip.qsf</td>
<td>Removed Platform Designer flow.</td>
</tr>
<tr>
<td>top.sdc</td>
<td>Removed Platform Designer flow.</td>
</tr>
<tr>
<td>import_compile.tcl</td>
<td>Removed Platform Designer flow, simplified PR flow.</td>
</tr>
<tr>
<td>ip/freeze_wrapper.v</td>
<td>Removed Platform Designer flow.</td>
</tr>
<tr>
<td>scripts/base_write_sdc.tcl</td>
<td>Updated to correct base.sdc ordering.</td>
</tr>
<tr>
<td>scripts/post_flow_pr.tcl</td>
<td>Updated for fast-compilation</td>
</tr>
<tr>
<td>scripts/pre_flow_pr.tcl</td>
<td>Updated for fast-compile, removed Platform Designer flow, and cleaned up (moved some functions into OpenCL SDK).</td>
</tr>
<tr>
<td>scripts/qar_ip_files.tcl</td>
<td>Do not package up opencl_bsp_ip.qsf.</td>
</tr>
<tr>
<td>base.qar</td>
<td>Updated with 18.0 static region.</td>
</tr>
</tbody>
</table>

Files added:
- kernel_mem.qsys
- ip/pr_region.v
- ip/kernel_mem/kernel_mem_mm_bridge_0.ip

Removed files:
- top_synth.qsf, which is obsolete because of simplified PR flow.
2. Developing an Intel Arria 10 SoC Custom Platform

Use the tools available in Intel Arria 10 SoC Development Kit Reference Platform (a10soc) and the Intel FPGA SDK for OpenCL Custom Platform Toolkit together to create your own Custom Platform.

Developing your Custom Platform requires in-depth knowledge of the contents in the following documents and tools:

- **Intel FPGA SDK for OpenCL Custom Platform User Guide**
- **Intel FPGA SDK for OpenCL Intel Arria 10 GX FPGA Development Kit Reference Platform Porting Guide**
- Contents of the SDK Custom Platform Toolkit
- **Cyclone V SoC Development Kit Reference Platform Porting Guide**
- Documentation for all the Intel IP in your Custom Platform
- **Intel FPGA SDK for OpenCL Getting Started Guide**
- **Intel FPGA SDK for OpenCL Programming Guide**

In addition, you must independently verify all IP on your computing card (for example, DDR4 external memory).

**Related Information**

- Intel FPGA SDK for OpenCL Custom Platform Toolkit User Guide
- Intel FPGA SDK for OpenCL Intel Arria 10 GX FPGA Development Kit Reference Platform Porting Guide
- Intel FPGA SDK for OpenCL Intel Cyclone V SoC Development Kit Reference Platform Porting Guide
- Intel FPGA SDK for OpenCL Intel Stratix V Network Reference Platform Porting Guide
- Intel FPGA SDK for OpenCL Getting Started Guide
- Intel FPGA SDK for OpenCL Programming Guide

2.1. Initializing an Intel Arria 10 SoC Custom Platform

To initialize your Intel FPGA SDK for OpenCL Custom Platform, first copy the Intel Arria 10 SoC Development Kit Reference Platform to your own directory and rename it.
1. Copy the contents of the `INTELFPGAOCLSDKROOT/board/a10soc` directory (where `INTELFPGAOCLSDKROOT` points to the location of your Intel FPGA SDK for OpenCL installation) to a directory that you own and rename the directory to `<your_custom_platform>`.

2. Choose one of the board variants in the `<your_custom_platform>/hardware` directory as the basis of your design.

   The `INTELFPGAOCLSDKROOT/board/a10soc` directory includes the following board variants:
   - `a10soc`—includes one DDR4 shared memory between the HPS host and the FPGA
   - `a10soc_2ddr`—includes one DDR4 shared memory and one DDR4 memory for the FPGA

3. Rename the directory of the chosen board variant to match the name of your FPGA board (`<your_custom_platform>/hardware/<board_name>`). Delete the other `a10socdk` board variant that you do not need.

4. Modify the `<your_custom_platform>/board_env.xml` file so that the `name` and `default` fields match the changes you made in 1 on page 13 and 3 on page 13, respectively.

5. Set the environment variable `AOCL_BOARD_PACKAGE_ROOT` variable to point to the location of your Custom Platform.

6. Invoke the command `aoc -list-boards` to confirm that the Intel FPGA SDK for OpenCL Offline Compiler displays the board name in your Custom Platform.

```
> aoc -list-boards
Board list:
  my_board:
```

### 2.2. Modifying Your Intel Arria 10 SoC Custom Platform

After initializing your Intel Arria 10 SoC Custom Platform, modify the existing Intel Quartus Prime design in `<your_custom_platform>` to fit your design needs.

1. Instantiate or edit the HPS IP parameters.

2. Instantiate any controllers required (for example, memory controllers, PR controllers and so on) and I/O channels, if required. You can add the board interface hardware either as Platform Designer components in the `board.qsys` Platform Designer system or as HDL in the `top.v` file.

   The `board.qsys` file and the `top.v` file are in the `<your_custom_platform>/hardware/<board_name>` directory.

3. Modify the `<your_custom_platform>/hardware/<board_name>/flat.qsf` file to use only the pin-outs and settings for your system.

4. Update the offset addresses of controllers in the respective header files in `<your_custom_platform>/arm32/drivers` directory, if you modified any controllers in your design.
2.3. Integrating Your Intel Arria 10 SoC Custom Platform with the Intel FPGA SDK for OpenCL

After modifying the Intel Quartus Prime design files, integrate your Custom Platform with the Intel FPGA SDK for OpenCL.

1. Update the `<your_custom_platform>/hardware/<board_name>/board_spec.xml` file. Ensure that there is at least one global memory interface, and all the global memory interfaces correspond to the exported interfaces from the `board.qsys` Platform Designer System File.

2. Use the `-bsp-flow=flat` attribute to compile the flat revision corresponding to `<your_custom_platform>/hardware/<board_name>/flat.qsf` file without the partitions or Logic Locks.

   Tip: Intel recommends to get a timing clean flat revision compiled before proceeding to the base revision compiles.

   ```sh
   aoc -bsp-flow=flat boardtest.cl -o=bin/boardtest.aocx
   ```

3. Use the `-bsp-flow=base` attribute to compile the base revision corresponding to `<your_custom_platform>/hardware/<board_name>/base.qsf` file.

4. Perform the steps outlined in the `INTELFPGAOCLSDKROOT/board/custom_platform_toolkit/tests/README.txt` file to compile the `INTELFPGAOCLSDKROOT/board/custom_platform_toolkit/tests/boardtest/boardtest.cl` OpenCL kernel source file.

   The environment variable `INTELFPGAOCLSDKROOT` points to the location of the Intel FPGA SDK for OpenCL installation.

5. If compilation fails because of timing failures, fix the errors, or compile `INTELFPGAOCLSDKROOT/board/custom_platform_toolkit/tests/boardtest.cl` with different seeds. To compile the kernel with a different seed, include the `-seed=<N>` option in the `aoc` command (for example, `aoc -seed=2 boardtest.cl`).

2.4. Changing the Device Part Number

When porting the Intel Arria 10 SoC Development Kit Reference Platform to your own board, change the device part number, where applicable, to the part number of the device on your board.

Update the device part number in the following files within the `<your_custom_platform>/hardware/<board_name>` directory:

- In the `flat.qsf` and `opencl_bsp_ip.qsf` files:
  - Change the device part number in the `set global assignment -name DEVICE 10AS066N3F40E2SG` QSF assignment.
  - Update the necessary pin assignment changes.
- The updated device number will appear in the `base.qsf` and `top.qsf` files.
- In the `board.qsys` file, change all occurrences of `10AS066N3F40E2SG`. 
2.5. Modifying the Kernel PLL Reference Clock

The Intel Arria 10 SoC Development Kit Reference Platform uses an external 100 MHz clock as a reference for the I/O PLL. The I/O PLL relies on this reference clock to generate the internal kernel_clk clock, and the kernel_clk2x clock that runs at twice the frequency of kernel_clk. When porting the a10soc Reference Platform to your own board using a different reference clock, update the board.qsys and top.sdc files with the new reference clock speed.

1. In the <your_custom_platform>/hardware/<board_name>/board.qsys file, update the REF_CLK_RATE parameter value on the kernel_clk_gen IP module.

2. In the <your_custom_platform>/hardware/<board_name>/top.sdc file, update the create_clock assignment for kernel_pll_refclk.

After you update the board.qsys and the top.sdc files, the post_flow_pr.tcl script will automatically determine the I/O PLL reference frequency and compute the correct PLL settings.

2.6. Modifying the Hard Processor System

The Intel Arria 10 SoC Development Kit Reference Platform uses HPS as the host system. You can modify the HPS settings in the <your_custom_platform>/hardware/<board_name>/board.qsys file. Regenerate the uboot bootloader after you change the HPS settings.

In the reference design, the HPS IP was instantiated with FPGA-to-HPS interface width set to "128-bit AXI", F2SDRAM port configuration set to "Port Configuration 3" and F2SDRAM0 and F2SDRAM2 enabled.

This instantiation was done to maximize kernel to HPS memory bandwidth. A custom IP module was instantiated between kernel memory interface and the two SDRAM ports to split kernel memory access across the ports.

Attention: You must regenerate the uboot bootloader after you change any HPS settings. For instructions on regenerating the bootloader, refer the Intel SoC Embedded Design Suite User Guide.

Related Information

2.7. Guaranteeing Timing Closure in the Intel Arria 10 SoC Custom Platform

When modifying the Intel Arria 10 SoC Development Kit Reference Platform into your own Custom Platform, ensure that guaranteed timing closure holds true for your Custom Platform.

1. Establish the floorplan of your design.
Important: Consider all design criteria outlined in the FPGA System Design section of the Intel FPGA SDK for OpenCL Custom Platform Toolkit User Guide.

2. Ensure that the AOCL_BOARD_PACKAGE_ROOT environment variable points to your Custom Platform.

3. Compile several seeds of the INTELFPAGAOCLSDKROOT/board/custom_platform_toolkit/tests/boardtest/boardtest.cl file until you generate a design that closes timing cleanly.

   To specify the seed number, include the -seed=<N> option in your aoc command.

4. Copy the base.qar file from the INTELFPAGAOCLSDKROOT/board/a10soc/ directory into your Custom Platform.

5. Use the flat.qsf file in the a10soc Reference Platform as references to determine the type of information you must include in the flat.qsf file for your Custom Platform.

   The base.qsf and top.qsf files automatically inherit all the settings in the flat.qsf file. However, if you need to modify Logic Lock Plus region or PR assignments, only make these changes in the base.qsf file.

6. Ensure that the environment variable CL_CONTEXT_COMPILER_MODE_INTELFPGA=3 is not set.

7. Run the boardtest_host executable.

Related Information
- Intel FPGA SDK for OpenCL Custom Platform Toolkit User Guide
- Intel FPGA SDK for OpenCL Intel Arria 10 GX FPGA Development Kit Reference Platform Porting Guide

2.8. Generating the base.qar Post-Fit Netlist for Your Intel Arria 10 SoC FPGA Custom Platform

To implement a top compilation flow, you must generate a base.qar Intel Quartus Prime Archive File for your Intel Arria 10 SoC Custom Platform.

The steps below represent a general procedure for regenerating the base.qar file:

1. Port the system design and the flat.qsf file to your computing card.

2. Ensure that the AOCL_BOARD_PACKAGE_ROOT environment variable points to your Custom Platform.

3. Compile the INTELFPAGAOCLSDKROOT/board/custom_platform_toolkit/tests/boardtest/boardtest.cl kernel source file using the base revision. Fix any timing failures and recompile the kernel until timing is clean.

   **Attention:** Add the -bsp-flow=base argument to the aoc command to generate a base.qar file during the kernel compilation.

4. Copy the generated base.qar file (which contains the base.qdb and pr_base.id files) into your Custom Platform.

5. Using the default compilation flow, test the base.qdb file across several OpenCL design examples and confirm that the following criteria are satisfied:
- All compilations close timing.
- The OpenCL design examples achieve satisfactory $F_{max}$.
- The OpenCL design examples function on the accelerator board.
3. Building the Software and SD Card Image for the Intel Arria 10 SoC Development Kit Reference Platform

To build the software for the Intel Arria 10 SoC Development Kit Reference Platform, compile the device tree blob, Linux kernel, and OpenCL Linux kernel driver. You also need to prepare the micro SD card image.

3.1. Compiling the Device Tree Blob

You must compile the device tree blob contained in the FAT partition to match your Intel Arria 10 SoC Development Kit Reference Platform. Use the Device Tree Generator (sopc2dts) and the Device Tree Compiler (dtc) to generate the necessary device tree blob.

For detailed information on how to generate the device tree blob, refer to Rocketboards.org.

1. Run base revision compile (aoc -bsp-flow=base) with your a10soc development kit BSP in the following location:

$INTELFPGAOCLSDKROOT/board/a10soc

2. Start an Embedded Command Shell and navigate to the Quartus project directory from your base revision compile.

3. Invoke the following command to generate the .dts Device Tree file, which is a text representation of the Device Tree:

```bash
sopc2dts --input board/board.sopcinfo  \
--output a10soc.dts  \
--board hps_a10_common_board_info.xml  \
--board hps_a10_devkit_board_info.xml  \
--board qsys_top_board_info.xml  \
--bridge-removal all --clocks
```

The board.sopcinfo file is generated during the base revision compilation of your FPGA design. You may download the XML files from the Intel Arria 10 GHRD on Rocketboards.org.

**Attention:** Ensure that the name of the Intel Arria 10 Hard Processor System in your board.qsys file matches the name used in Intel Arria 10 GHRD project you are downloading the XML files from. At the time this document was written, the name of the Intel Arria 10 Hard Processor System in board.qsys and in Intel Arria 10 GHRD project was a10_hps.

Create your copy of the Intel Arria 10 SoC BSP from the SDK, and rename the instance of the Intel Arria 10 Hard Processor System in board.qsys to a10_hps.
4. After you generate the .dts file, modify its contents by performing the following tasks:
   a. In the Device Tree (a10soc.dts), change the compatible field setting to altr, socfpga.

```dts
board_irq_ctrl_0: unknown@0x10000cfa0 {
    compatible = "altr,socfpga";
    reg = <0x00000001 0x0000cfa0 0x00000004>,
        <0x00000001 0x0000cf90 0x00000004>;
    reg-names = "IRQ_Mask_Slave", "IRQ_Read_Slave";
    interrupts = <0 19 4>;
    interrupt-parent = <&a10_hps_arm_gic_0>;
    interrupts = <0 19 4>;
    interrupt-controller;
    #interrupt-cells = <1>;
    clocks = <&config_clk>;
} //end unknown@0x10000cfa0 (board_irq_ctrl_0)
```

Note: The compatible field setting in a10soc.dts must match the driver code in aclsoc.c. If the two strings do not match, the driver installation process does not allow the kernel to probe the device. As a result, the interrupt is not registered and the host code fails.

Code snippet in the aclsoc.c file:

```c
static const struct of_device_id aclsoc_of_match[] = {
    { .compatible = "altr,socfpga" },
    /* end of list */
};
```

5. After you modify the .dts file and it is ready to probed by the platform driver, compile the device tree blob by invoking the following Device Tree Compiler command:

```bash
dtc -f -I dts -O dtb –o a10soc.dtb a10soc.dts
```

This command generates the a10soc.dtb file.

6. Rename the a10soc.dtb file to socfpga_arria10_socdk_sdmmc.dtb.

The socfpga_arria10_socdk_sdmmc.dtb file is needed later in Building the SD Card Image on page 22.

7. If you modify any of the HPS settings in the design, you must regenerate the uboot.

### 3.2. Compiling the Linux Kernel for the Intel Arria 10 SoC Development Kit

Before running OpenCL applications on an Intel Arria 10 SoC board, compile the Linux kernel with the contiguous memory allocator (CMA) feature enabled. Before enabling CMA, recompile the Linux kernel.

1. Review the GSRD Compiling Linux instructions at the RocketBoards.org website for instructions on downloading and rebuilding the Linux kernel source code.

For use with the Intel FPGA SDK for OpenCL, determine which branch to download based on the release notes for the sdimage.img file that you download. For example, if the GSRD 18.1 sdimage.img file was created using Linux kernel v4.9.78 LTSi, look for branch socfpga-4.9.78-ltsi.
Specify your downloaded branch as the test branch name (`test_branch`). You can find the commands you need to run under **Building Kernel & U-Boot Separately From Git Tree** on the GSRD Compiling Linux page.

2. Add the following lines to the bottom of the `arch/arm/configs/socfpga_defconfig` file:

   ```
   CONFIG_MEMORY_ISOLATION=y
   CONFIG_CMA=y
   CONFIG_DMA_CMA=y
   CONFIG_CMA_DEBUG=y
   CONFIG_CMA_SIZE_MBYTES=512
   CONFIG_CMA_SIZE_SEL_MBYTES=y
   CONFIG_CMA_ALIGNMENT=8
   CONFIG_CMAAreas=7
   ```

   **Note:** The building process creates the `arch/arm/configs/socfpga_defconfig` file. This file specifies the settings for the socfpga default configuration.

   The `CONFIG_CMA_SIZE_MBYTES` configuration value sets the upper limit on the total number of physically contiguous memory available. You may increase this value if you require more memory.

3. Run the `make mrproper` command to clean the current configuration.

4. Run the `make ARCH=arm socfpga_defconfig` command.

   `ARCH=arm` indicates that you want to configure the ARM architecture.

   `socfpga_defconfig` indicates that you want to use the default socfpga configuration.

5. Run the `export CROSS_COMPILE=arm-linux-gnueabihf-` command.

   This command sets the `CROSS_COMPILE` environment variable to specify the prefix of the desired tool chain.

6. Run the `make ARCH=arm zImage` command. The resulting image is available in the `arch/arm/boot/zImage` file.

   This image file is used later in **Building the SD Card Image** on page 22.

**Related Information**

Arria 10 Golden System Reference Design (GSRD) - User Manual - Sustaining

### 3.3. Compiling the OpenCL Linux Kernel Driver

Compile the OpenCL Linux kernel driver against the compiled kernel source.

The driver source is available in the Intel FPGA SDK for OpenCL installation directory. Compile the driver yourself on a host machine that has `sudo` and the most recent version of the SoC EDS.
1. Copy the driver source from $INTELFPGAOCLSDKROOT/board/a10soc/arm32/driver/ to a new directory.

2. Set the KDIR value in the driver Makefile to the directory containing the Linux kernel source files that you downloaded in Compiling the Linux Kernel for the Intel Arria 10 SoC Development Kit on page 19.

3. In the new directory that contains the driver source files, run the make clean command.

4. Run the make command to create the aclsoc_drv.ko file. This file is used later in Building the SD Card Image on page 22.

The driver might need to be updated to work with newer version of the Linux kernel if you see the following message while building the kernel driver:

```c
aclsoc_cmd.c:165:14: error: too many arguments to function 'get_user_pages_unlocked'
In file included from aclsoc_cmd.c:50:0
```

To update the driver, make the following changes to $INTELFPGAOCLSDKROOT/board/a10soc/arm32/driver/aclsoc_cmd.c:

a. Find the following code in aclsoc_cmd.c:

```c
ret = get_user_pages_unlocked(target_task, target_task->mm,
    start_page + got * PAGE_SIZE,
    num_pages - got, write, 1,
    p + got);
```

b. Replace that code with the following code:

```c
ret = get_user_pages_remote(target_task, target_task->mm,
    start_page + got * PAGE_SIZE,
    num_pages - got, FOLL_WRITE|FOLL_FORCE,
    p + got, vma);
```

3.4. Generating Full-Chip Programming File for SD Card Image

The full-chip programming file, socfpga.rbf, is in RBF (Raw Binary File) format, and stored in Partition 1 of the SD Card Image. This .rbf file is used to program the Intel Arria 10 SoC FPGA during power up.

Follow one of the following methods to generate the socfpga.rbf file in a directory containing an aocx file for your Intel Arria 10 SoC custom platform:

- If your aocx file is compiled with flat or base revision, execute the following commands:

```bash
aocli binedit <.aocx> get .acl.fpga.bin .temp.fpga.bin
aocli binedit .temp.fpga.bin get .acl.sof .temp.sof
sof2flash --offset=0 --input="/temp.sof" --output="/temp_sof2rbf.flash"
nios2-elf-objcopy -I srec -O binary "/.temp_sof2rbf.flash" "/socfpga.rbf"
rm .temp.fpga.bin .temp.sof .temp_sof2rbf.flash
```

- If your aocx file is compiled with top revision, go to the working directory of this aocx kernel and execute the following commands:

```bash
sof2flash --offset=0 --input="/top.sof" --output="/temp_sof2rbf.flash"
nios2-elf-objcopy -I srec -O binary "/.temp_sof2rbf.flash" "/socfpga.rbf"
rm .temp_sof2rbf.flash
```
After generating the `socfpga.rbf` file, place it in FAT32 partition of the flash card image.

**Remember:** The full-chip programming RBF file is different from the partial reconfiguration RBF file generated during PR import compile.

### 3.5. Building the SD Card Image

To build the SD card image, you need a number of files created or obtained when you followed the instructions earlier in this guide.

#### 3.5.1. Layout of the OpenCL Micro SD Card

The micro SD card that the Arria 10 GSRD uses has three partitions, each containing different parts of the OpenCL SD card image.

<table>
<thead>
<tr>
<th>Location</th>
<th>File Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Partition 1</td>
<td><code>socfpga_arria10_socdk_sdmmc.dtb</code></td>
<td>The device tree blob that describes the peripherals available to the system. Refer to <em>Compiling the Device Tree Blob</em> for more information.</td>
</tr>
<tr>
<td></td>
<td><code>socfpga.rbf</code></td>
<td>The full-chip .rbf (Raw Binary file) file generated from Quartus compile. This is different from the PR .rbf file. Refer to <em>Generating Full-Chip Programming File for SD Card Image</em> on page 21 for more details.</td>
</tr>
<tr>
<td></td>
<td><code>zImage</code></td>
<td>The compressed kernel image. Refer to <em>Recompiling the Linux Kernel for the Intel Arria 10 SoC Development Kit</em> for more information.</td>
</tr>
<tr>
<td>Partition 2</td>
<td>Various <code>rootfs</code> files</td>
<td>Partition 2 is a Linux partition that contains the uncompressed root file system (<code>rootfs</code>). You modify this partition in <em>Creating the SD Card Image</em> on page 23.</td>
</tr>
</tbody>
</table>
| Partition 3 | `uboot_w_dtb-mkpimage.bin` | Partition 3 must be of type a2. The Master Boot Record recognizes the partition and then loads the `uboot_w_dtb-mkpimage.bin` bootloader from it. **Note:** The `uboot_w_dtb-mkpimage.bin` file is written into the a3 partition. *Generating U-boot and device tree section in Arria 10 GSRD user manual or the Boot Tools User Guide* chapter of the *Intel SoC FPGA Embedded Design Suite User Guide* describes how to...
### Related Information

- [Compiling the Device Tree Blob on page 18](#)
- [Compiling the Linux Kernel for the Intel Arria 10 SoC Development Kit on page 19](#)
- [Compiling Linux Kernel and Root Filesystem](#)

### 3.5.2. Creating the SD Card Image

You must modify the GSRD 18.1 `sdimage.img` file to support the Intel Arria 10 SoC BSP and run OpenCL applications.

Before you create the SD card image, download the GSRD 18.1 `sdimage.tar.gz` file from the following URL: [https://rocketboards.org/foswiki/Documentation/GSRD181ReleaseNotes#Release_Contents](https://rocketboards.org/foswiki/Documentation/GSRD181ReleaseNotes#Release_Contents).

Create the SD card partitions and their contents by following the instructions in the following sections:

1. **Partition 1**: Creating Partition 1 of the SD Card Image on page 23.
3. **Partition 3**: Creating Partition 3 of the SD Card Image on page 25.

#### 3.5.2.1. Creating Partition 1 of the SD Card Image

To create partition 1 of the SD card image:

1. Mount the FAT32 partition (partition 1) in the `sdimage.img` file as a loop-back device.

   To mount a partition:
   a. Determine the byte start of the partition within the image with the `/sbin/fdisk -lu image_file` command.
      
      For example, partition number 1 of type W95 FAT has a block offset of 2121728. With 512 bytes per block, the byte offset is 512 bytes x 2121728 = 1086324736 bytes.
   b. Identify a free loop device (for example, `/dev/loop0`) by typing the `losetup -f` command.
   c. Assign your flash card image to the loop block device by invoking the `losetup` command.
      
      For example, if `/dev/loop0` is the free loop device, issue the following command:

      ```
      losetup /dev/loop0 image_file -o <byte offset>
      ```
   d. Mount the loop device.
For example, if /dev/loop0 is the loop device and the mount point is /media/disk1, issue the following command:

```
mount /dev/loop0 /media/disk1
```

Within the image file, /media/disk1 is now a mounted FAT32 partition.

2. Remove all files from the mounted directory, and copy socfpga_arria10_socdk_sdmmc.dtb, socfpga.rbf and zImage to the partition.

3. After you store all the necessary files onto the flash card image, run the following commands:

```
sync
umount /media/disk1
losetup -d /dev/loop0
```

### 3.5.2.2. Creating Partition 2 of the SD Card Image

To create partition 2 of the SD card image:

1. Mount partition 2 in the sdimage.img file as a loop-back device.

To mount a partition:

a. Determine the byte start of the partition within the image by invoking the /sbin/fdisk -lu image_file command.

b. Identify a free loop device (for example, /dev/loop0) by typing the losetup -f command.

c. Assign your flash card image to the loop block device by invoking the losetup command.

For example, if /dev/loop0 is the free loop device, issue the following command:

```
losetup /dev/loop0 image_file -o <byte offset>
```

d. Mount the loop device.

For example, if /dev/loop0 is the loop device and the mount point is media/disk2, issue the following command:

```
mount /dev/loop0 media/disk2
```

Within the image file, media/disk2 is now mounted.

2. From the Intel Download Center for FPGAs, download and unpack the Intel FPGA Runtime Environment for OpenCL Linux Cyclone® V SoC TGZ file:

To download and unpack the file:

a. Go the Intel Download Center for FPGAs page for the Intel FPGA SDK for OpenCL at the following URL: http://fpgasoftware.intel.com/opencl/?edition=pro.

b. Click the RTE tab, select Intel FPGA Runtime Environment for OpenCL Linux SoC TGZ, and click Download to download the file.

c. Unpack the downloaded file (aoc1-rte-<version>.arm32.tgz) to a directory that you own.
3. Place the unpacked aocl-rte-<version>.arm32 directory into the /home/root/opencl_arm32_rte directory on partition 2 of the image file.

4. Copy aclsoc_drv.ko to the /home/root/opencl_arm32_rte/board/a10soc/arm32/driver/ directory on partition 2 of the image file.

5. Create the init_opencl.sh file in the /home/root directory with the following content:

```bash
export INTELFPGAOCLSDKROOT=/home/root/opencl_arm32_rte
export AOCL_BOARD_PACKAGE_ROOT=$INTELFPGAOCLSDKROOT/board/a10soc
export PATH=$INTELFPGAOCLSDKROOT/bin:$PATH
export LD_LIBRARY_PATH=$INTELFPGAOCLSDKROOT/host/arm32/lib:$LD_LIBRARY_PATH
insmod $AOCL_BOARD_PACKAGE_ROOT/arm32/driver/aclsoc_drv.ko
```

The SDK user runs a `source ./init_opencl.sh` command to load the environment variables and the OpenCL Linux kernel driver.

6. After you store all the necessary files onto the flash card image, run the following commands:

```bash
sync
unmount media/disk2
losetup -d /dev/loop0
```

### 3.5.2.3. Creating Partition 3 of the SD Card Image

To create partition 3 of the SD card image:

1. Mount partition 3 in the sdimage.img file as a loop-back device.

   To mount a partition:
   a. Determine the byte start of the partition within the image with the /sbin/fdisk -lu image_file command.
   b. Identify a free loop device (for example, /dev/loop0) by typing the losetup -f command.
   c. Assign your flash card image to the loop block device by invoking the losetup command.

      For example, if /dev/loop0 is the free loop device, issue the following command:
      ```bash
      losetup /dev/loop0 image_file -o <byte offset>
      ```

2. Generate the uboot_w_dtb-mkpimage.bin file:
   a. Run an OpenCL compilation with the -bsp-flow=base option.
   b. Generate U-boot and device tree according to the instructions at the following URL: https://rocketboards.org/foswiki/Documentation/A10GSRDGeneratingUBootAndUBootDeviceTree

      The instructions require the following exceptions or additional information in the Generating Bootloader section:
Step 5: Do not browse to the folder referenced. Browse to the hps_isw_handoff folder in the output directory of your earlier -bsp-flow=base OpenCL compilation.

For an <OpenCL_file>.cl file, the folder is typically <OpenCL_file>/hps_isw_handoff.

Step 9: The rbf_filename field is set to socfpga.rbf. Do not change this value. Leave the value as socfpga.rbf.

3. Update the uboot_w_dtb-mkpimage.bin file by following the instructions in the Updating Individual Elements on the SD card section of Creating and Updating the SD Card page available at the following URL: https://rocketboards.org/foswiki/Documentation/A10GSRDCreatingAndUpdatingTheSDCardLTS

For example, sudo dd if=uboot_w_dtb-mkpimage.bin of=/dev/loop0 bs=64k seek=0.

4. Delete the loop device with the following commands:

```
sync
losetup -d /dev/loop0
```

3.5.3. Guidelines on Imaging the Micro SD Card

After creating all the files in the SD card image, you have several options to image the micro SD card.

General recommendations and resources for imaging the micro SD card:

- Use the Linux fdisk command to create, delete, or modify existing partitions on the GSRD SD card image. Use the Linux dd command to write file systems to the existing partitions on the GSRD SD card image.

  **Important:** To use these commands, you must have extensive Linux knowledge and have sudo on your machine.

- Rocketboards.org provides a python script that generates a .bin file. You can write this .bin file to the micro SD card. Refer to the Creating and Updating the SD Card section of the Arria 10 GSRD v17.1 User Manual for more information.

- Intel provides the alt-boot-disk-util SD card boot utility to create SD boot images. For more information, refer to the SD Card Boot Utility chapter of the Intel SoC FPGA Embedded Design Suite User Guide.

The different partitions in the micro SD card are related to each other. For example, if the OpenCL .rbf file is not programmed onto the FPGA, the driver will not load. In addition, the socfpga.rbf file will not program the board when you boot it up if the .rbf file name does not match the label in the bootloader library. Before modifying the SD card image, consider whether the modification is necessary for your design.

Related Information

- Creating and Updating the SD Card
- Intel FPGA SoC Embedded Design Suite User Guide: SD Card Boot Utility
3.6. Known Issues

Currently, there are several limitations on the usage of the Intel FPGA SDK for OpenCL with the Intel Arria 10 SoC Development Kit Reference Platform.

- You cannot override the vendor and board names that the `CL_DEVICE_VENDOR` and `CL_DEVICE_NAME` strings of the `clGetDeviceInfo()` call reports, respectively.
- If the host allocates constant memory in the shared DDR system (that is, HPS DDR) and it modifies the constant memory after kernel execution, the data in memory might become updated. This issue arises because the FPGA core cannot snoop on CPU-to-HPS DDR transactions.

To prevent subsequent kernel executions from accessing outdated data, implement one of the following workarounds:
  - Do not modify constant memory after its initialization.
  - If you require multiple `__constant` data sets, create multiple constant memory buffers.
  - If available, allocate constant memory in the FPGA DDR on your accelerator board.

- The SDK utility on ARM only supports the `program` and `diagnose` utility commands. The `flash`, `install`, and `uninstall` utility commands are not applicable to the Intel Arria 10 SoC Development Kit for the following reasons:
  - The `install` utility has to compile the `aclsoc_drv` Linux kernel driver and enable it on the SoC. The development machine has to perform the compilation; however, it already contains Linux kernel sources for the SoC. The Linux kernel sources for the development machine are different from those for the SoC. The location of the Linux kernel sources for the SoC is likely unknown to the SDK user. Similarly, the `uninstall` utility is also unavailable to the Intel Arria 10 SoC Development Kit.
  - Also, delivering `aclsoc_drv` to the SoC board is challenging because the default distribution of the Intel Arria 10 SoC Development Kit does not contain Linux kernel `include` files or the GNU Compiler Collection (GCC) compiler.
  - The `flash` utility requires placing a `.rbf` file of an OpenCL design onto the FAT32 partition of the micro SD flash card. Currently, this partition is not mounted when the SDK user powers up the board. Therefore, the best way to update the partition is to use a flash card reader and the development machine.

- When switching between the Intel FPGA SDK for OpenCL Offline Compiler executable files (.aocx) that correspond to different board variants (that is, `a10soc` and `a10soc_2ddr`), you must use the SDK's `program` utility to load the `.aocx` file for the new board variant for the first time. If you simply run the host application using a new board variant but the FPGA contains the image from another board variant, a fatal error might occur.

- When you power up the board, it does not acquire an IP address by default. Invoke the `ifup eth0` command to initiate IP address acquisition.

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| 2019.04.01       | 19.1                       | • Rewrote most part of the Generating Full-Chip Programming File for SD Card Image on page 21 topic.  
• Updated the software versions in Intel Arria 10 SoC Development Kit Reference Platform: Prerequisites on page 3.  
• In Contents of the Intel Arria 10 SoC Development Kit Reference Platform on page 7, made the following changes:  
  — In flat.qsf, removed top_synth.qsf.  
  — In opencl_bsp_ip.qsf, removed acl_ddr4_a10.qsys and acl_ddr4_a10_core.qsys.  
  — Changed quartus_ini to quartus.ini.  
  — Removed top_post.sdc and top_synth.qsf.  
  — In scripts/pre_flow_pr.tcl, changed kernel_system.qsys to kernel_mem.qsys.  
• In Integrating Your Intel Arria 10 SoC Custom Platform with the Intel FPGA SDK for OpenCL on page 14, modified steps 2 and 3 about compiling the base and flat revision.  
• In Changing the Device Part Number on page 14, mentioned about opencl_bsp_ip.qsf and removed top_synth.qsf.  
• In Modifying the Kernel PLL Reference Clock on page 15, removed the last optional step about updating the comment for the kernel_pll_refclk input port.  
• In Guaranteeing Timing Closure in the Intel Arria 10 SoC Custom Platform on page 15, added a step about verifying ACCL_BOARD_PACKAGE_ROOT variable, removed top_synth.qsf from step 5 and removed a step about removing the ACL_DEFAULT_FLOW variable.  
• In Generating the base.qar Post-Fit Netlist for Your Intel Arria 10 SoC FPGA Custom Platform on page 16, added a step about verifying ACCL_BOARD_PACKAGE_ROOT variable. |
| 2019.02.18       | 18.1.2                     | • Revised Building the Software and SD Card Image for the Intel Arria 10 SoC Development Kit Reference Platform on page 18 to reflect the removal of the precompiled Intel Arria 10 Soc Linux SD card images from the Intel FPGA SDK for OpenCL.  
• Updated Contents of the Intel Arria 10 SoC Development Kit Reference Platform on page 7 to reflect the removal of the precompiled Intel Arria 10 Soc Linux SD card images from the Intel FPGA SDK for OpenCL.  
• Updated Revision History table format |
<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>September 2018</td>
<td>2018.09.17</td>
<td>Added Changes in Intel Arria 10 SoC Development Kit Reference Platform from 17.1.2 to 18.0</td>
</tr>
<tr>
<td>November 2017</td>
<td>2017.11.03</td>
<td>• Rebranded references of the following:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>— altera_a10socdk to a10soc</td>
</tr>
<tr>
<td></td>
<td></td>
<td>— Environment variable ALTERAOCLSDKROOT to INTELFPGAOCLSDKROOT.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>— Arria 10 to Intel Arria 10.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>— CL_CONTEXT_COMPILER_MODE_ALTERA to CL_CONTEXT_COMPILER_MODE_INTELFPGA.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>— LogicLock to Logic Lock</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• In Intel Arria 10 SoC Development Kit Reference Platform: Prerequisites on page 3 assumptions added Intel FPGA SDK for OpenCL Intel Arria 10 GX FPGA Development Kit Reference Platform Porting Guide.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• In Features of the Intel Arria 10 SoC Development Kit Reference Platform on page 4, removed the Silicon feature.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• In Modifying Your Intel Arria 10 SoC Custom Platform on page 13, updated step 2 and added step 4.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• In Compiling the Linux Kernel for the Intel Arria 10 SoC Development Kit on page 19, updated the step 8 about creating .rbf file.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Implemented the single dash and --option=value conventions in the following topics:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>— Intel Arria 10 SoC Development Kit Reference Platform Board Variants on page 6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>— Contents of the Intel Arria 10 SoC Development Kit Reference Platform on page 7</td>
</tr>
<tr>
<td></td>
<td></td>
<td>— Initializing an Intel Arria 10 SoC Custom Platform on page 12</td>
</tr>
<tr>
<td></td>
<td></td>
<td>— Integrating Your Intel Arria 10 SoC Custom Platform with the Intel FPGA SDK for OpenCL on page 14</td>
</tr>
<tr>
<td></td>
<td></td>
<td>— Guaranteeing Timing Closure in the Intel Arria 10 SoC Custom Platform on page 15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• In Contents of the Intel Arria 10 SoC Development Kit Reference Platform on page 7:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>— Changed board.qsys, acl_ddr4_a10.qsys and acl_ddr4_a10_core.qsys files as board.qsys, acl_ddr4_a10.qsys and acl_ddr4_a10_core.qsys Platform Designer files.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>— Removed scripts/bak_flow.tcl since it is now moved into OpenCL SDK.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>— Removed scripts/helpers.tcl since it is now moved into OpenCL SDK.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Added Changes in Intel Arria 10 SoC Development Kit Reference Platform from 17.0 to 17.1 on page 9 to list all changes in the reference platform from 17.0 to 17.1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• In Modifying the Hard Processor System on page 15, added a note to regenerate uboot loader for any changes in HPS settings.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• In Changing the Device Part Number on page 14, added a bullet point to update flat.qsf file for pin assignment changes.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• In Generating the base.qar Post-Fit Netlist for Your Intel Arria 10 SoC FPGA Custom Platform on page 16, added a note to add the -bsp-flow=base argument to the aoc command to generate a base.qar file during the kernel compilation.</td>
</tr>
</tbody>
</table>

continued...
<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
</tr>
</thead>
</table>
| May 2017   | 2017.05.08 | • Rebranded various references as follows:  
|            |         | — Rebranded Altera SDK for OpenCL to Intel FPGA SDK for OpenCL.  
|            |         | — Rebranded Altera Offline Compiler to Intel FPGA SDK for OpenCL Offline Compiler.  
|            |         | — Rebranded Altera RTE for OpenCL to Intel FPGA RTE for OpenCL.  
| October 2016 | 2016.10.31 | Initial release. |