4. Hot Socketing and Power-On Reset in MAX II Devices

**Introduction**

MAX® II devices offer hot socketing, also known as hot plug-in or hot swap, and power sequencing support. Designers can insert or remove a MAX II board in a system during operation without undesirable effects to the system bus. The hot socketing feature removes some of the difficulties designers face when using components on printed circuit boards (PCBs) that contain a mixture of 3.3-, 2.5-, 1.8-, and 1.5-V devices.

The MAX II device hot socketing feature provides:

- Board or device insertion and removal
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion

This chapter contains the following sections:

- “MAX II Hot-Socketing Specifications” on page 4–1
- “Power-On Reset Circuitry” on page 4–5

**MAX II Hot-Socketing Specifications**

MAX II devices offer all three of the features required for the hot-socketing capability listed above without any external components or special design requirements. The following are hot-socketing specifications:

- The device can be driven before and during power-up or power-down without any damage to the device itself.
- I/O pins remain tri-stated during power-up. The device does not drive out before or during power-up, thereby affecting other buses in operation.
- Signal pins do not drive the V_{CCIO} or V_{CCINT} power supplies. External input signals to device I/O pins do not power the device V_{CCIO} or V_{CCINT} power supplies via internal paths. This is true if the V_{CCINT} and the V_{CCIO} supplies are held at GND.

> Altera uses GND as reference for the hot-socketing and I/O buffers circuitry designs. You must connect the GND between boards before connecting the V_{CCINT} and the V_{CCIO} power supplies to ensure device reliability and compliance to the hot-socketing specifications.

**Devices Can Be Driven before Power-Up**

Signals can be driven into the MAX II device I/O pins and GCLK[3..0] pins before or during power-up or power-down without damaging the device. MAX II devices support any power-up or power-down sequence (V_{CCIO}, V_{CCIO}, V_{CCIO}, V_{CCIO}, V_{CCINT}), simplifying the system-level design.
Hot Socketing Feature Implementation in MAX II Devices

I/O Pins Remain Tri-Stated during Power-Up

A device that does not support hot-socketing may interrupt system operation or cause contention by driving out before or during power-up. In a hot socketing situation, the MAX II device’s output buffers are turned off during system power-up. MAX II devices do not drive out until the device attains proper operating conditions and is fully configured. Refer to “Power-On Reset Circuitry” on page 4–5 for information about turn-on voltages.

Signal Pins Do Not Drive the Vccio or Vccint Power Supplies

MAX II devices do not have a current path from I/O pins or GCLK [3..0] pins to the Vccio or Vccint pins before or during power-up. A MAX II device may be inserted into (or removed from) a system board that was powered up without damaging or interfering with system-board operation. When hot socketing, MAX II devices may have a minimal effect on the signal integrity of the backplane.

AC and DC Specifications

You can power up or power down the Vccio and Vccint pins in any sequence. During hot socketing, the I/O pin capacitance is less than 8 pF. MAX II devices meet the following hot socketing specifications:

- The hot socketing DC specification is: $|I_{\text{IOpin}}| < 300 \mu A$.
- The hot socketing AC specification is: $|I_{\text{IOpin}}| < 8 \text{ mA}$ for 10 ns or less.

MAX II devices are immune to latch-up when hot socketing. If the TCK JTAG input pin is driven high during hot socketing, the current on that pin might exceed the specifications above.

$I_{\text{IOpin}}$ is the current at any user I/O pin on the device. The AC specification applies when the device is being powered up or powered down. This specification takes into account the pin capacitance but not board trace and external loading capacitance. Additional capacitance for trace, connector, and loading must be taken into consideration separately. The peak current duration due to power-up transients is 10 ns or less.

The DC specification applies when all Vcc supplies to the device are stable in the powered-up or powered-down conditions.

Hot Socketing Feature Implementation in MAX II Devices

The hot socketing feature turns off (tri-states) the output buffer during the power-up event (either Vccint or Vccio supplies) or power-down event. The hot-socket circuit generates an internal HOTSCKT signal when either Vccint or Vccio is below the threshold voltage during power-up or power-down. The HOTSCKT signal cuts off the output buffer to make sure that no DC current (except for weak pull-up leaking) leaks through the pin. When Vcc ramps up very slowly during power-up, Vcc may still be relatively low even after the power-on reset (POR) signal is released and device configuration is complete.
Make sure that the $V_{CCINT}$ is within the recommended operating range even though SRAM download has completed.

Each I/O and clock pin has the circuitry shown in Figure 4–1.

*Figure 4–1. Hot Socketing Circuit Block Diagram for MAX II Devices*

The POR circuit monitors $V_{CCINT}$ and $V_{CCIO}$ voltage levels and keeps I/O pins tri-stated until the device has completed its flash memory configuration of the SRAM logic. The weak pull-up resistor (R) from the I/O pin to $V_{CCIO}$ is enabled during download to keep the I/O pins from floating. The 3.3-V tolerance control circuit permits the I/O pins to be driven by 3.3 V before $V_{CCIO}$ and/or $V_{CCINT}$ are powered, and it prevents the I/O pins from driving out when the device is not fully powered or operational. The hot socket circuit prevents I/O pins from internally powering $V_{CCIO}$ and $V_{CCINT}$ when driven by external signals before the device is powered.

For information about 5.0-V tolerance, refer to the *Using MAX II Devices in Multi-Voltage Systems* chapter in the *MAX II Device Handbook*.

*Figure 4–2 shows a transistor-level cross section of the MAX II device I/O buffers. This design ensures that the output buffers do not drive when $V_{CCIO}$ is powered before $V_{CCINT}$ or if the I/O pad voltage is higher than $V_{CCIO}$. This also applies for sudden voltage spikes during hot insertion. The $V_{PAD}$ leakage current charges the 3.3-V tolerant circuit capacitance.*
The CMOS output drivers in the I/O pins intrinsically provide electrostatic discharge (ESD) protection. There are two cases to consider for ESD voltage strikes: positive voltage zap and negative voltage zap.

A positive ESD voltage zap occurs when a positive voltage is present on an I/O pin due to an ESD charge event. This can cause the N+ (Drain) / P-Substrate junction of the N-channel drain to break down and the N+ (Drain) / P-Substrate / N+ (Source) intrinsic bipolar transistor turn on to discharge ESD current from I/O pin to GND. The dashed line (see Figure 4–3) shows the ESD current discharge path during a positive ESD zap.

**Figure 4–2. Transistor-Level Diagram of MAX II Device I/O Buffers**

![Transistor-Level Diagram of MAX II Device I/O Buffers](image)

**Figure 4–3. ESD Protection During Positive Voltage Zap**

![ESD Protection During Positive Voltage Zap](image)
When the I/O pin receives a negative ESD zap at the pin that is less than \(-0.7\) V (0.7 V is the voltage drop across a diode), the intrinsic P-Substrate/N+ drain diode is forward biased. Therefore, the discharge ESD current path is from GND to the I/O pin, as shown in Figure 4–4.

**Figure 4–4.** ESD Protection During Negative Voltage Zap

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**Power-On Reset Circuitry**

MAX II devices have POR circuits to monitor $V_{\text{CCINT}}$ and $V_{\text{CCIO}}$ voltage levels during power-up. The POR circuit monitors these voltages, triggering download from the non-volatile configuration flash memory (CFM) block to the SRAM logic, maintaining tri-state of the I/O pins (with weak pull-up resistors enabled) before and during this process. When the MAX II device enters user mode, the POR circuit releases the I/O pins to user functionality. The POR circuit of the MAX II (except MAX IIZ) device continues to monitor the $V_{\text{CCINT}}$ voltage level to detect a brown-out condition. The POR circuit of the MAX IIZ device does not monitor the $V_{\text{CCINT}}$ voltage level after the device enters into user mode. More details are provided in the following sub-sections.
Power-Up Characteristics

When power is applied to a MAX II device, the POR circuit monitors $V_{CCINT}$ and begins SRAM download at an approximate voltage of 1.7 V or 1.55 V for MAX IIG and MAX IIZ devices. From this voltage reference, SRAM download and entry into user mode takes 200 to 450 µs maximum, depending on device density. This period of time is specified as $t_{CONFIG}$ in the power-up timing section of the DC and Switching Characteristics chapter in the MAX II Device Handbook.

Entry into user mode is gated by whether all $V_{CCIO}$ banks are powered with sufficient operating voltage. If $V_{CCINT}$ and $V_{CCIO}$ are powered simultaneously, the device enters user mode within the $t_{CONFIG}$ specifications. If $V_{CCIO}$ is powered more than $t_{CONFIG}$ after $V_{CCINT}$, the device does not enter user mode until 2 µs after all $V_{CCIO}$ banks are powered.

For MAX II and MAX IIG devices, when in user mode, the POR circuitry continues to monitor the $V_{CCINT}$ (but not $V_{CCIO}$) voltage level to detect a brown-out condition. If there is a $V_{CCINT}$ voltage sag at or below 1.4 V during user mode, the POR circuit resets the SRAM and tri-states the I/O pins. Once $V_{CCINT}$ rises back to approximately 1.7 V (or 1.55 V for MAX IIG devices), the SRAM download restarts and the device begins to operate after $t_{CONFIG}$ time has passed.

For MAX IIZ devices, the POR circuitry does not monitor the $V_{CCINT}$ and $V_{CCIO}$ voltage levels after the device enters user mode. If there is a $V_{CCINT}$ voltage sag below 1.4 V during user mode, the functionality of the device will not be guaranteed and you must power down the $V_{CCINT}$ to 0 V for a minimum of 10 µs before powering the $V_{CCINT}$ and $V_{CCIO}$ up again. Once $V_{CCINT}$ rises from 0 V back to approximately 1.55 V, the SRAM download restarts and the device begins to operate after $t_{CONFIG}$ time has passed.

Figure 4–5 shows the voltages for POR of MAX II, MAX IIG, and MAX IIZ devices during power-up into user mode and from user mode to power-down or brown-out.

All $V_{CCINT}$ and $V_{CCIO}$ pins of all banks must be powered on MAX II devices before entering user mode.
After SRAM configuration, all registers in the device are cleared and released into user function before I/O tri-states are released. To release clears after tri-states are released, use the $\text{DEV\_CLRn}$ pin option. To hold the tri-states beyond the power-up configuration time, use the $\text{DEV\_OE}$ pin option.
Referenced Documents

This chapter refers to the following documents:

- DC and Switching Characteristics chapter in the MAX II Device Handbook
- Using MAX II Devices in Multi-Voltage Systems chapter in the MAX II Device Handbook

Document Revision History

Table 4–1 shows the revision history for this chapter.

<table>
<thead>
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<th>Date and Revision</th>
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<td></td>
<td>■ Updated Figure 4–5.</td>
<td>■ Added “Referenced Documents” section.</td>
</tr>
<tr>
<td>December 2006, version 1.5</td>
<td>■ Added document revision history.</td>
<td>■ Updated document with MAX IIZ information.</td>
</tr>
<tr>
<td>February 2006, version 1.4</td>
<td>■ Updated “MAX II Hot-Socketing Specifications” section.</td>
<td>■ Updated “AC and DC Specifications” section.</td>
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<tr>
<td></td>
<td>■ Updated “AC and DC Specifications” section.</td>
<td>■ Updated “Power-On Reset Circuitry” section.</td>
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<tr>
<td>June 2005, version 1.3</td>
<td>■ Updated AC and DC specifications on page 4-2.</td>
<td>■ Updated AC and DC specifications on page 4-2.</td>
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<td>■ Updated Figure 4-5.</td>
<td>■ Updated Figure 4-5.</td>
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<tr>
<td>June 2004, version 1.1</td>
<td>■ Corrected Figure 4-2.</td>
<td>■ Corrected Figure 4-2.</td>
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