5. Using MAX V Devices in Multi-Voltage Systems

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This chapter describes how to implement Altera® devices in multi-voltage systems without damaging the device or the system.

Technological advancements in deep submicron processes have lowered the supply voltage levels of semiconductor devices, creating a design environment where devices on a system board may potentially use many different supply voltages such as 5.0, 3.3, 2.5, 1.8, 1.5, and 1.2 V, which can ultimately lead to voltage conflicts.

To accommodate interfacing with a variety of devices on system boards, MAX® V devices have MultiVolt I/O interfaces that allow devices in a mixed-voltage design environment to communicate directly with MAX V devices. The MultiVolt interface separates the power supply voltage (V_{CCINT}) from the output voltage (V_{CCIO}), allowing MAX V devices to interface with other devices using a different voltage level on the same PCB. The 1.8-V input directly powers the core of the MAX V devices.

For more information about hot socketing and power-on reset (POR), refer to the *Hot Socketing and Power-On Reset in MAX V Devices* chapter.

This chapter contains the following sections:

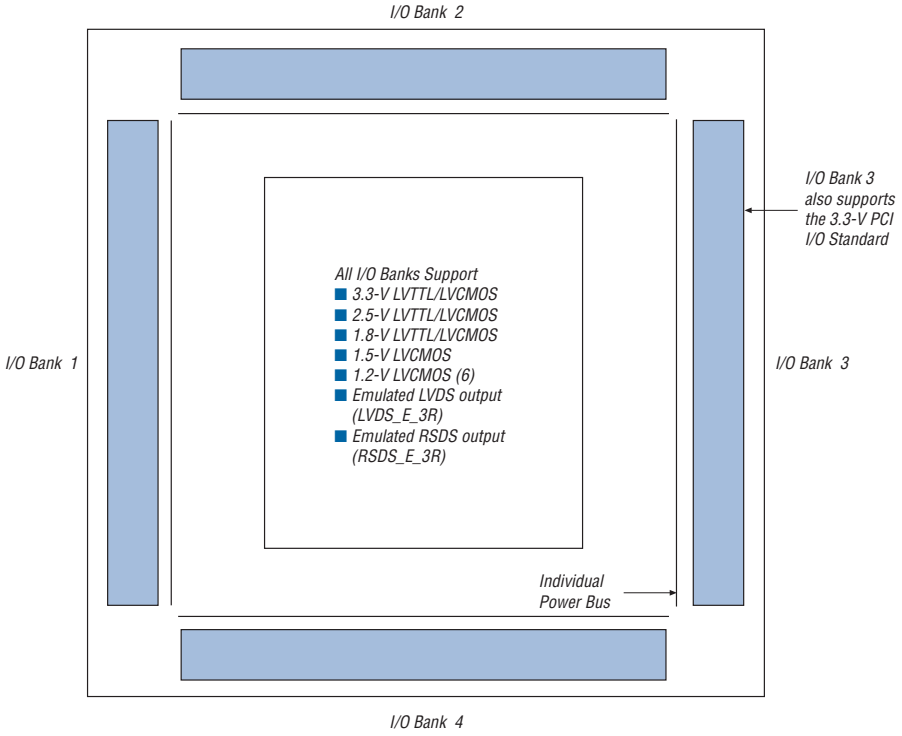
I/O Standards

The I/O buffer of MAX V devices is programmable and supports a wide range of I/O voltage standards. You can program each I/O bank in a MAX V device to comply with a different I/O standard. You can configure all I/O banks with the following standards:

- 3.3-V LVTTL/LVCMOS
- 2.5-V LVTTL/LVCMOS
- 1.8-V LVTTL/LVCMOS
- 1.5-V LVCMOS
- 1.2-V LVCMOS (Not supported in Bank 1)
- Emulated LVDS output (LVDS_E_3R)
- Emulated RSDS output (RSDS_E_3R)

The Schmitt trigger input option is supported by the 3.3-V and 2.5-V I/O standards. The I/O Bank 3 also includes the 3.3-V PCI I/O standard interface capability on the 5M1270Z and 5M2210Z devices. Figure 5–1 shows the I/O standards supported by MAX V devices.

Figure 5–1. I/O Standards Supported by MAX V Devices *(Note 1)*, *(2)*, *(3)*, *(4)*, *(5)*



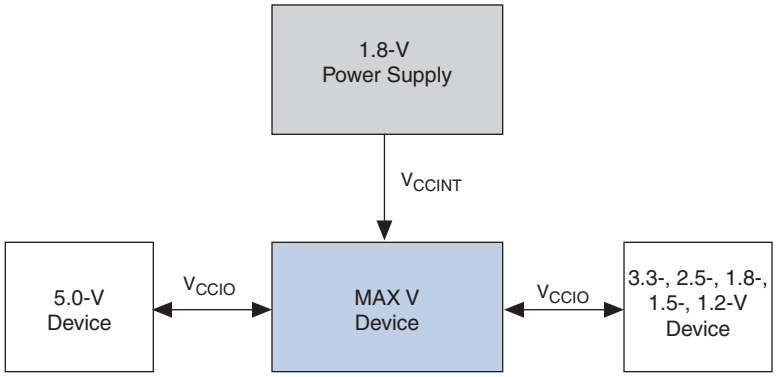
Notes to Figure 5–1:

(1) Figure 5–1 is a top view of the silicon die.
(2) Figure 5–1 is a graphical representation only. For the exact pin locations, refer to the pin list and the Quartus® II software.
(3) 5M40Z, 5M80Z, 5M160Z, 5M240Z, and 5M570Z devices only have two I/O banks.
(4) The 3.3-V PCI I/O standard is only supported in 5M1270Z and 5M2210Z devices.
(5) The Schmitt trigger input option for 3.3-V and 2.5-V I/O standards is supported for all I/O pins.
(6) This I/O standard is not supported in Bank 1.

MultiVolt I/O Operation

MAX V devices allow the device core and I/O blocks to be powered-up with separate supply voltages. The VCCINT pins supply power to the device core and the VCCIO pins supply power to the device I/O buffers. The VCCINT pins are powered-up with 1.8 V for MAX V devices. All the VCCIO pins for a given I/O bank that have MultiVolt capability must be supplied from the same voltage level (for example, 5.0, 3.3, 2.5, 1.8, 1.5, or 1.2 V). Figure 5–2 shows how to implement a multiple-voltage system for MAX V devices.

Figure 5–2. Implementing a Multi-Voltage System with a MAX V Device ***(Note 1)***, ***(2)***



Notes to Figure 5–2:

(1) MAX V devices can drive a 5.0-V transistor-to-transistor logic (TTL) input when V_{CCIO} = 3.3 V. To drive a 5.0-V CMOS, you must have an open-drain setting with an internal I/O clamp diode and external resistor.

(2) MAX V devices can be 5.0-V tolerant with the use of an external resistor and the internal I/O clamp diode on 5M1270Z and 5M2210Z devices.

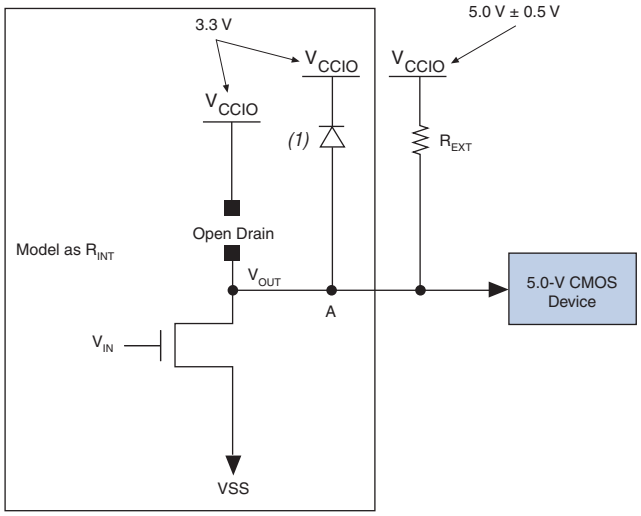
5.0-V Device Compatibility

A MAX V device can drive a 5.0-V TTL device by connecting the VCCIO pins of the MAX V device to 3.3 V. This is possible because the output high voltage (V_{OH}) of a 3.3-V interface meets the minimum high-level voltage of 2.4 V of a 5.0-V TTL device.

A MAX V device may not correctly interoperate with a 5.0-V CMOS device if the output of the MAX V device is connected directly to the input of the 5.0-V CMOS device. If the MAX V device's V_{OUT} is greater than V_{CCIO}, the PMOS pull-up transistor still conducts if the pin is driving high, preventing an external pull-up resistor from pulling the signal to 5.0 V. To make MAX V device outputs compatible with 5.0-V CMOS devices, configure the output pins as open-drain pins with the I/O clamp diode enabled and use an external pull-up resistor.

Figure 5–3 shows MAX V device compatibility with 5.0-V CMOS devices.

Figure 5–3. MAX V Device Compatibility with 5.0-V CMOS Devices



Note to Figure 5–3:

(1) This diode is only active after power-up. MAX V devices require an external diode if driven by 5.0 V before power-up.

The open-drain pin never drives high, only low or tri-state. When the open-drain pin is active, it drives low. When the open-drain pin is inactive, the pin is tri-stated and the trace pulls up to 5.0 V by the external resistor. The purpose of enabling the I/O clamp diode is to protect the MAX V device's I/O pins. The 3.3-V V_{CCIO} supplied to the I/O clamp diodes causes the voltage at point A to clamp at 4.0 V, which meets the MAX V device's reliability limits when the trace voltage exceeds 4.0 V. The device operates successfully because a 5.0-V input is within its input specification.

The I/O clamp diode is only supported in the 5M1270Z and 5M2210Z devices' I/O Bank 3. You must have an external protection diode for the other I/O banks in the 5M1270Z and 5M2210Z devices and all the I/O pins in the 5M40Z, 5M80Z, 5M160Z, 5M240Z, and 5M570Z devices.

The pull-up resistor value must be small enough for a sufficient signal rise time, but large enough so that it does not violate the I_{OL} (output low) specification of the MAX V devices.

The maximum MAX V device I_{OL} depends on the programmable drive strength of the I/O output. Table 5–1 lists the programmable drive strength settings that are available for the 3.3-V LVTTL/LVCMOS I/O standard for MAX V devices. The Quartus II software uses the maximum current strength as the default setting. The PCI I/O standard is always set to **20 mA** with no alternate setting.

Table 5–1. 3.3-V LVTTL/LVCMOS Programmable Drive Strength (Part 1 of 2)

I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)
3.3-V LVTTL	16
	8

Table 5–1. 3.3-V LVTTL/LVCMOS Programmable Drive Strength (Part 2 of 2)

I/O Standard	I_{OH}/I_{OL} Current Strength Setting (mA)
3.3-V LVCMOS	8
	4

To compute the required value of R_{EXT}, first calculate the model of the open-drain transistors on the MAX V device. You can model this output resistor (R_{EXT}) by dividing V_{OL} by I_{OL} ($R_{EXT} = V_{OL}/I_{OL}$). Table 5–2 lists the maximum V_{OL} for the 3.3-V LVTTL/LVCMOS I/O standard for MAX V devices.

For more information about I/O standard specifications, refer to the *DC and Switching Characteristics for MAX V Devices* chapter.

Table 5–2. 3.3-V LVTTL/LVCMOS Maximum V_{OL}

I/O Standard	Voltage (V)
3.3-V LVTTL	0.45
3.3-V LVCMOS	0.20

Select R_{EXT} so that the MAX V device's I_{OL} specification is not violated. You can compute the required pull-up resistor value of R_{EXT} by using the equation: $R_{EXT} = (V_{CC}/I_{OL}) – R_{INT}$. For example, if an I/O pin is configured as a 3.3-V LVTTL with a 16 mA drive strength, given that the maximum power supply (V_{CC}) is 5.5 V, you can calculate the value of R_{EXT} as follows:

Equation 5–1.

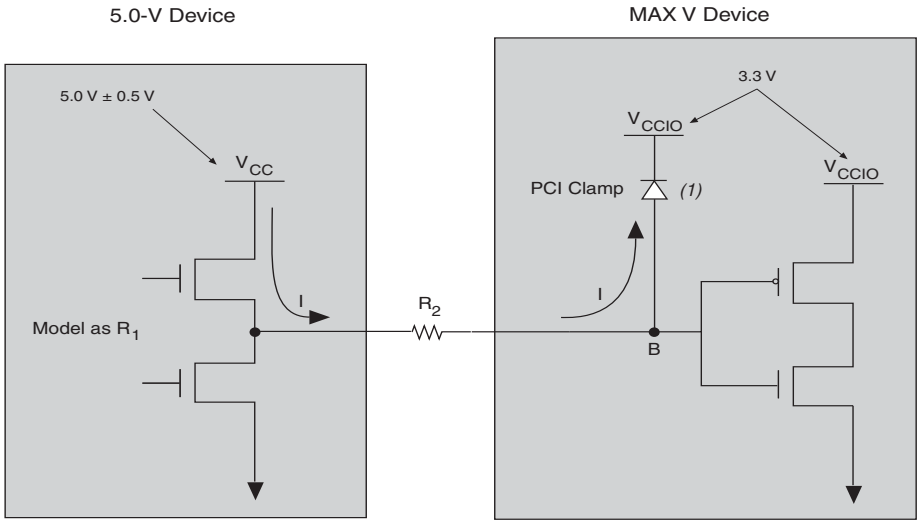
$$R_{EXT} = \frac{(5.5\ V - 0.45\ V)}{16\ mA} = 315.6\ \Omega$$

This resistor value computation assumes worst-case conditions. You can adjust the R_{EXT} value according to the device configuration drive strength. Additionally, if your system does not see a wide variation in voltage-supply levels, you can adjust these calculations accordingly.

Because MAX V devices are 3.3-V, 32-bit, 66-MHz PCI compliant, the input circuitry accepts a maximum high-level input voltage (V_{IH}) of 4.0 V. To drive a MAX V device with a 5.0-V device, you must connect a resistor (R_2) between the MAX V device and the 5.0-V device.

Figure 5–4 shows how to drive a MAX V PCI-compliant device with a 5.0-V device.

Figure 5–4. Driving a MAX V PCI-Compliant Device with a 5.0-V Device



Note to Figure 5–4:

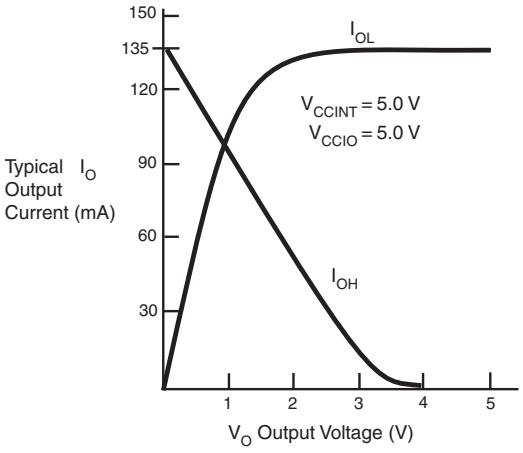
(1) This diode is only active after power-up. MAX V devices require an external diode if driven by 5.0 V before power-up.

If V_{CCIO} for the MAX V devices is 3.3 V and you enabled the I/O clamp diode, the voltage at point B in Figure 5–4 is 4.0 V, which meets the MAX V devices reliability limits when the trace voltage exceeds 4.0 V. To limit large current draw from the 5.0-V device, R_2 must be small enough for a fast signal rise time and large enough so that it does not violate the high-level output current (I_{OH}) specifications of the devices driving the trace.

To compute the required value of R_2, first calculate the model of the pull-up transistors on the 5.0-V device. You can model this output resistor (R_1) by dividing the 5.0-V device supply voltage (V_{CC}) by I_{OH}: $R_1 = V_{CC}/I_{OH}$.

Figure 5–5 shows an example of typical output drive characteristics of a 5.0 V device.

Figure 5–5. Output Drive Characteristics of a 5.0-V Device



As shown in Figure 5–5, R_1 = 5.0 V/135 mA.

The values usually shown in the data sheets reflect typical operating conditions. Subtract 20% from the data sheet value for guard band. When you subtract the 20% from the previous example, the R_1 value is 30.

Select R_2 so that the MAX V device's I_{OH} specification is not violated. For example, if the above device has a maximum I_{OH} of 8 mA, given the I/O clamp diode, $V_{IN} = V_{CCIO} + 0.7\ V = 3.7\ V$. Given that the maximum supply load of a 5.0-V device (V_{CC}) is 5.5 V, calculate value of R_2 as follows:

Equation 5–2.

$$R_2 = \frac{(5.5\ V - 3.7\ V) - (8\ mA \times 30\ \Omega)}{8\ mA} = 194\ \Omega$$

This analysis assumes worst-case conditions. If your system does not see a wide variation in voltage-supply levels, you can adjust these calculations accordingly.

Because 5.0-V device tolerance in MAX V devices requires the use of the I/O clamp, and this clamp is activated only after power-up, 5.0-V signals may not be driven into the device until it is configured. The I/O clamp diode is only supported in the 5M1270Z and 5M2210Z devices' I/O Bank 3. You must have an external protection diode for the other I/O banks for the 5M1270Z and 5M2210Z devices and all the I/O pins in the 5M40Z, 5M80Z, 5M160Z, 5M240Z, and 5M570Z devices.

Recommended Operating Conditions for 5.0-V Compatibility

As mentioned earlier, a 5.0-V tolerance can be supported with the I/O clamp diode enabled with external series/pull-up resistance. To guarantee long term reliability of the device's I/O buffer, there are restrictions on the signal duty cycle that drive the MAX V I/O, which is based on the maximum clamp current. Table 5–3 lists the maximum signal duty cycle for the 3.3-V V_{CCIO} given a PCI clamp current-handling capability.

Table 5–3. Maximum Signal Duty Cycle

V_{IN} (V) *(1)*	I_{CH} (mA) *(2)*	Max Duty Cycle (%)
4.0	5.00	100
4.1	11.67	90
4.2	18.33	50
4.3	25.00	30
4.4	31.67	17
4.5	38.33	10
4.6	45.00	5

Notes to Table 5–3:

(1) V_{IN} is the voltage at the package pin.

(2) The I_{CH} is calculated with a 3.3-V V_{CCIO}. A higher V_{CCIO} value will have a lower I_{CH} value with the same V_{IN}.

For signals with a duty cycle greater than 30% on MAX V input pins, Altera recommends using a V_{CCIO} voltage of 3.0 V to guarantee long-term I/O reliability. For signals with a duty cycle less than 30%, the V_{CCIO} voltage can be 3.3 V.

Power-Up Sequencing

MAX V devices are designed to operate in multi-voltage environments where it may be difficult to control power sequencing. Therefore, MAX V devices are designed to tolerate any possible power-up sequence. Either V_{CCINT} or V_{CCIO} can initially supply power to the device and 3.3-, 2.5-, 1.8-, 1.5-, or 1.2-V input signals can drive the devices without special precautions before V_{CCINT} or V_{CCIO} is applied. MAX V devices can operate with a V_{CCIO} voltage level that is higher than the V_{CCINT} level.

When V_{CCIO} and V_{CCINT} are supplied from different power sources to a MAX V device, a delay between V_{CCIO} and V_{CCINT} may occur. Normal operation does not occur until both power supplies are in their recommended operating range. When V_{CCINT} is powered-up, the IEEE Std. 1149.1 JTAG circuitry is active. If `TMS` and `TCK` are connected to V_{CCIO} and V_{CCIO} is not powered-up, the JTAG signals are left floating. Thus, any transition on `TCK` can cause the state machine to transition to an unknown JTAG state, leading to incorrect operation when V_{CCIO} is finally powered-up. To disable the JTAG state during the power-up sequence, pull `TCK` low to ensure that an inadvertent rising edge does not occur on `TCK`.

Document Revision History

Table 5–4 lists the revision history for this chapter.

Table 5–4. Document Revision History

Date	Version	Changes
June 2017	2017.06.16	Added note to state that 1.2-V LVCMOS is not supported in Bank 1.
December 2010	1.0	Initial release.