

This chapter describes the architecture of the MAX® V device and contains the following sections:

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Functional Description

MAX V devices contain a two-dimensional row- and column-based architecture to implement custom logic. Row and column interconnects provide signal interconnects between the logic array blocks (LABs).

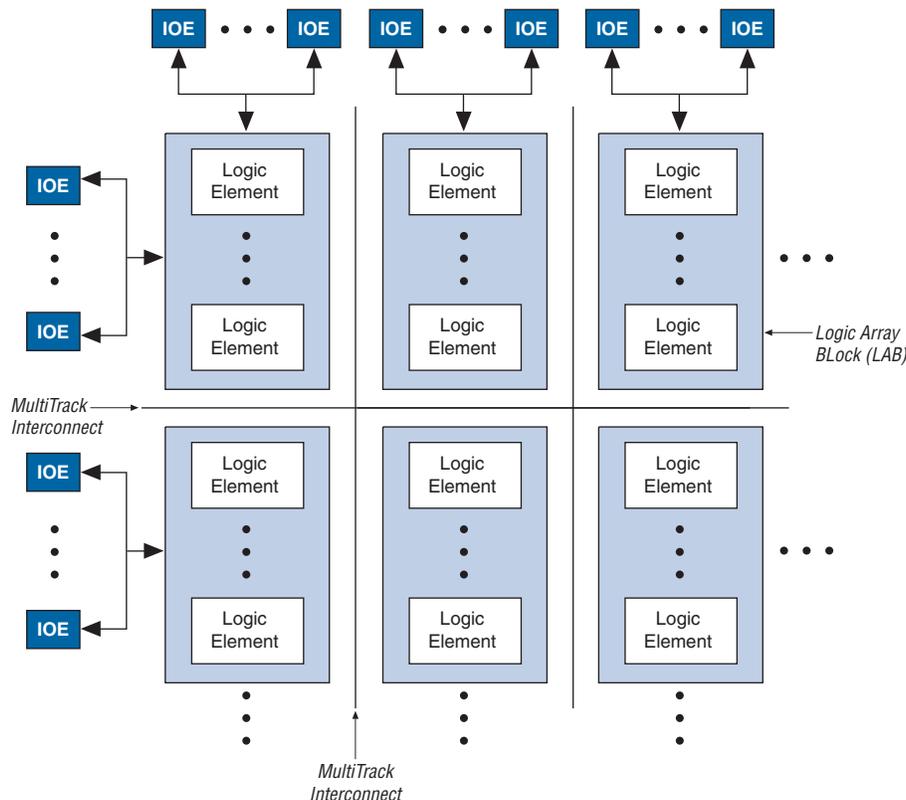
Each LAB in the logic array contains 10 logic elements (LEs). An LE is a small unit of logic that provides efficient implementation of user logic functions. LABs are grouped into rows and columns across the device. The MultiTrack interconnect provides fast granular timing delays between LABs. The fast routing between LEs provides minimum timing delay for added levels of logic versus globally routed interconnect structures.

The I/O elements (IOEs) located after the LAB rows and columns around the periphery of the MAX V device feeds the I/O pins. Each IOE contains a bidirectional I/O buffer with several advanced features. I/O pins support Schmitt trigger inputs and various single-ended standards, such as 33-MHz, 32-bit PCI™, and LVTTTL.

MAX V devices provide a global clock network. The global clock network consists of four global clock lines that drive throughout the entire device, providing clocks for all resources within the device. You can also use the global clock lines for control signals such as clear, preset, or output enable.

Figure 2-1 shows a functional block diagram of the MAX V device.

Figure 2-1. Device Block Diagram



Each MAX V device contains a flash memory block within its floorplan. This block is located on the left side of the 5M40Z, 5M80Z, 5M160Z, and 5M240Z devices. On the 5M240Z (T144 package), 5M570Z, 5M1270Z, and 5M2210Z devices, the flash memory block is located on the bottom-left area of the device. The majority of this flash memory storage is partitioned as the dedicated configuration flash memory (CFM) block. The CFM block provides the non-volatile storage for all of the SRAM configuration information. The CFM automatically downloads and configures the logic and I/O at power-up, providing instant-on operation.

 For more information about configuration upon power-up, refer to the *Hot Socketing and Power-On Reset for MAX V Devices* chapter.

A portion of the flash memory within the MAX V device is partitioned into a small block for user data. This user flash memory (UFM) block provides 8,192 bits of general-purpose user storage. The UFM provides programmable port connections to the logic array for reading and writing. There are three LAB rows adjacent to this block, with column numbers varying by device.

Table 2–1 lists the number of LAB rows and columns in each device, as well as the number of LAB rows and columns adjacent to the flash memory area. The long LAB rows are full LAB rows that extend from one side of row I/O blocks to the other. The short LAB rows are adjacent to the UFM block; their length is shown as width in LAB columns.

Table 2–1. Device Resources for MAX V Devices

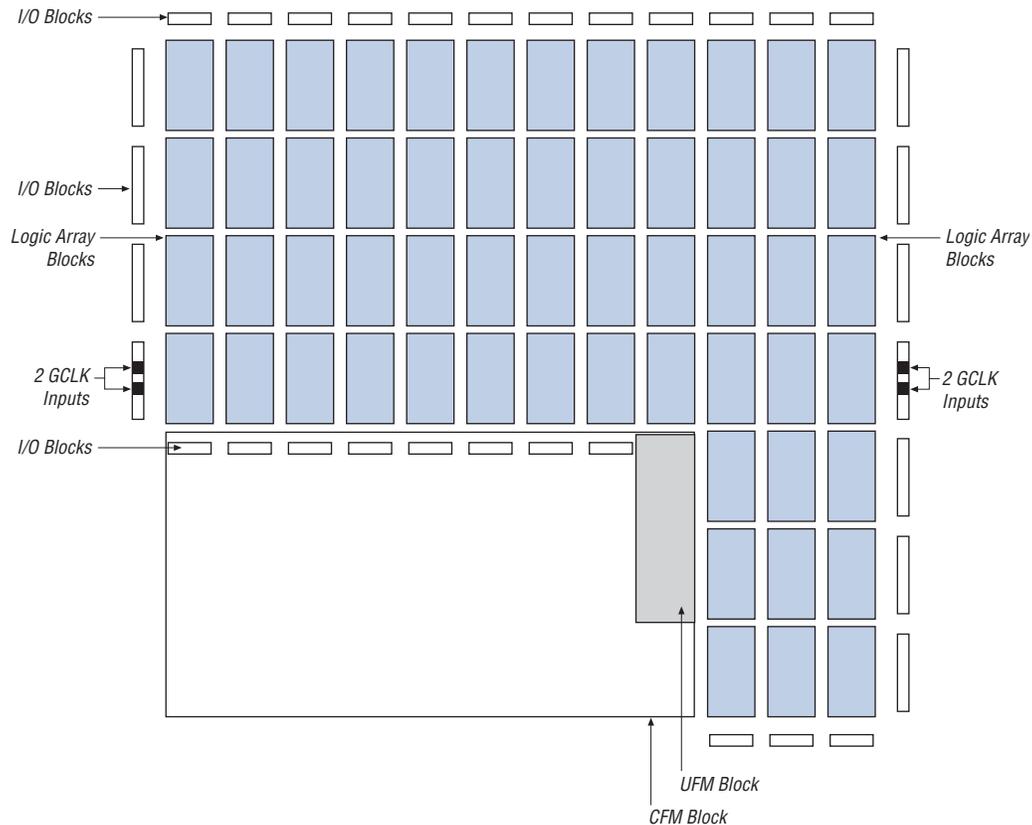
Device	UFM Blocks	LAB Columns	LAB Rows		Total LABs
			Long LAB Rows	Short LAB Rows (Width) (1)	
5M40Z	1	6	4	—	24
5M80Z	1	6	4	—	24
5M160Z	1	6	4	—	24
5M240Z (2)	1	6	4	—	24
5M240Z (3)	1	12	4	3 (3)	57
5M570Z	1	12	4	3 (3)	57
5M1270Z (4)	1	16	7	3 (5)	127
5M1270Z (5)	1	20	10	3 (7)	221
5M2210Z	1	20	10	3 (7)	221

Notes to Table 2–1:

- (1) The width is the number of LAB columns in length.
- (2) Not applicable to T144 package of the 5M240Z device.
- (3) Only applicable to T144 package of the 5M240Z device.
- (4) Not applicable to F324 package of the 5M1270Z device.
- (5) Only applicable to F324 package of the 5M1270Z device.

Figure 2-2 shows a floorplan of a MAX V device.

Figure 2-2. Device Floorplan for MAX V Devices (Note 1)



Note to Figure 2-2:

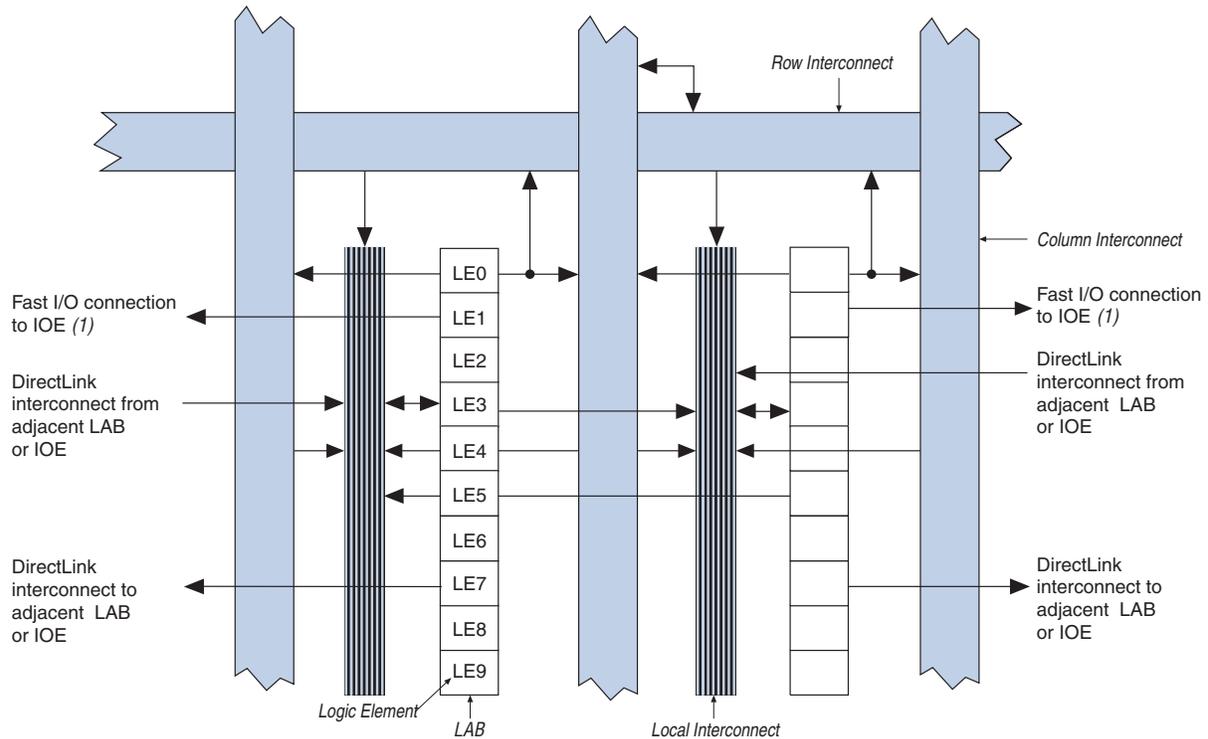
- (1) The device shown is a 5M570Z device. 5M1270Z and 5M2210Z devices have a similar floorplan with more LABs. For 5M40Z, 5M80Z, 5M160Z, and 5M240Z devices, the CFM and UFM blocks are located on the left side of the device.

Logic Array Blocks

Each LAB consists of 10 LEs, LE carry chains, LAB control signals, a local interconnect, a look-up table (LUT) chain, and register chain connection lines. There are 26 possible unique inputs into an LAB, with an additional 10 local feedback input lines fed by LE outputs in the same LAB. The local interconnect transfers signals between LEs in the same LAB. LUT chain connections transfer the LUT output from one LE to the

adjacent LE for fast sequential LUT connections within the same LAB. Register chain connections transfer the output of one LE's register to the adjacent LE's register within an LAB. The Quartus® II software places associated logic within an LAB or adjacent LABs, allowing the use of local, LUT chain, and register chain connections for performance and area efficiency. Figure 2-3 shows the MAX V LAB.

Figure 2-3. LAB Structure for MAX V Devices



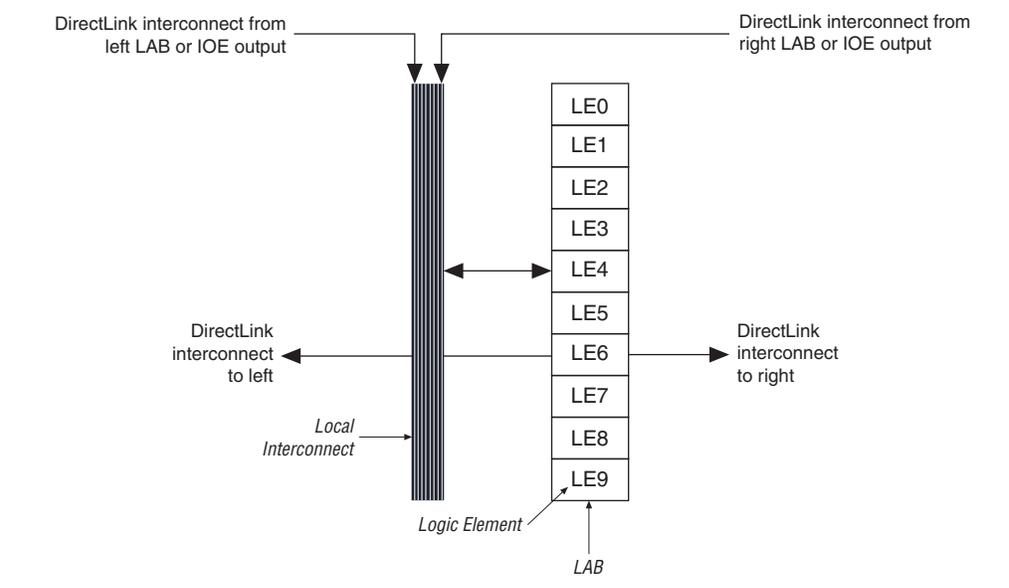
Note to Figure 2-3:

(1) Only from LABs adjacent to IOEs.

LAB Interconnects

Column and row interconnects and LE outputs within the same LAB drive the LAB local interconnect. Adjacent LABs, from the left and right, can also drive an LAB's local interconnect through the DirectLink connection. The DirectLink connection feature minimizes the use of row and column interconnects, providing higher performance and flexibility. Each LE can drive 30 other LEs through fast local and DirectLink interconnects. Figure 2-4 shows the DirectLink connection.

Figure 2-4. DirectLink Connection



LAB Control Signals

Each LAB contains dedicated logic for driving control signals to its LEs. The control signals include two clocks, two clock enables, two asynchronous clears, a synchronous clear, an asynchronous preset/load, a synchronous load, and add/subtract control signals, providing a maximum of 10 control signals at a time. Synchronous load and clear signals are generally used when implementing counters but they can also be used with other functions.

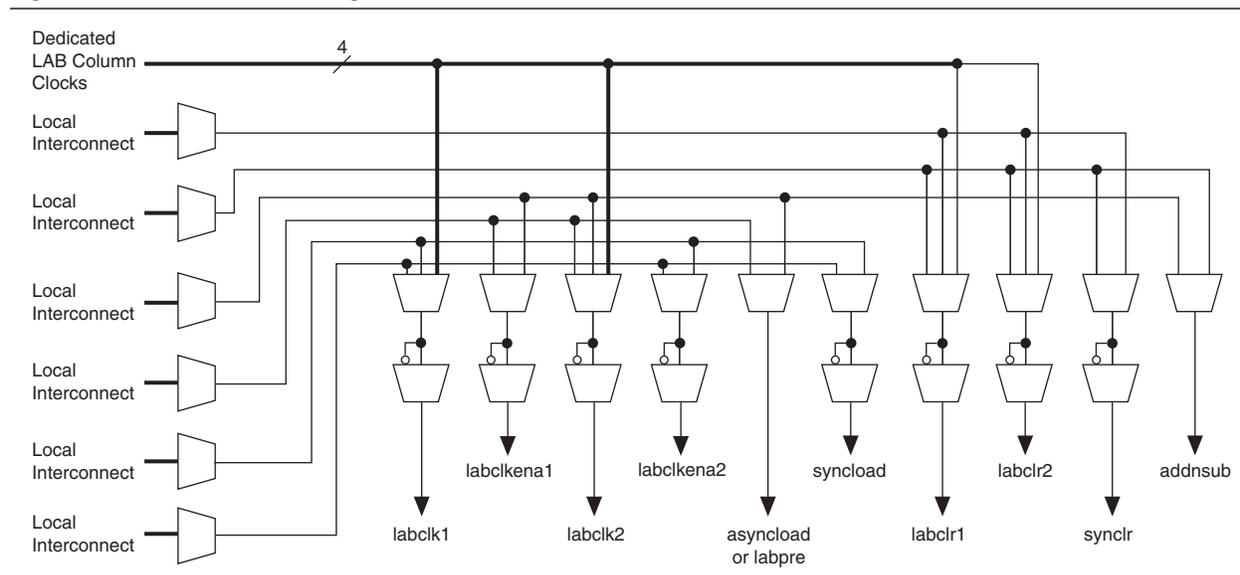
Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked. For example, any LE in a particular LAB using the `labclk1` signal also uses `labckena1`. If the LAB uses both the rising and falling edges of a clock, it also uses both LAB-wide clock signals. Deasserting the clock enable signal turns off the LAB-wide clock.

Each LAB can use two asynchronous clear signals and an asynchronous load/preset signal. By default, the Quartus II software uses a NOT gate push-back technique to achieve preset. If you disable the NOT gate push-back option or assign a given register to power-up high using the Quartus II software, the preset is then achieved using the asynchronous load signal with asynchronous load data input tied high.

With the LAB-wide addsub control signal, a single LE can implement a one-bit adder and subtractor. This signal saves LE resources and improves performance for logic functions such as correlators and signed multipliers that alternate between addition and subtraction depending on data.

The LAB column clocks [3..0], driven by the global clock network, and LAB local interconnect generate the LAB-wide control signals. The MultiTrack interconnect structure drives the LAB local interconnect for non-global control signal generation. The MultiTrack interconnect's inherent low skew allows clock and control signal distribution in addition to data signals. Figure 2-5 shows the LAB control signal generation circuit.

Figure 2-5. LAB-Wide Control Signals



improves device utilization because the device can use the register and the LUT for unrelated functions. Another special packing mode allows the register output to feed back into the LUT of the same LE so that the register is packed with its own fan-out LUT. This mode provides another mechanism for improved fitting. The LE can also drive out registered and unregistered versions of the LUT output.

LUT Chain and Register Chain

In addition to the three general routing outputs, the LEs within a LAB have LUT chain and register chain outputs. LUT chain connections allow LUTs within the same LAB to cascade together for wide input functions. Register chain outputs allow registers within the same LAB to cascade together. The register chain output allows a LAB to use LUTs for a single combinational function and the registers for an unrelated shift register implementation. These resources speed up connections between LABs while saving local interconnect resources. For more information about LUT chain and register chain connections, refer to [“MultiTrack Interconnect” on page 2-14](#).

addnsub Signal

The LE's dynamic adder/subtractor feature saves logic resources by using one set of LEs to implement both an adder and a subtractor. This feature is controlled by the LAB-wide control signal `addnsub`. The `addnsub` signal sets the LAB to perform either $A + B$ or $A - B$. The LUT computes addition; subtraction is computed by adding the two's complement of the intended subtractor. The LAB-wide signal converts to two's complement by inverting the B bits within the LAB and setting carry-in to 1, which adds one to the LSB. The LSB of an adder/subtractor must be placed in the first LE of the LAB, where the LAB-wide `addnsub` signal automatically sets the carry-in to 1. The Quartus II Compiler automatically places and uses the adder/subtractor feature when using adder/subtractor parameterized functions.

LE Operating Modes

The MAX V LE can operate in one of the following modes:

- [“Normal Mode”](#)
- [“Dynamic Arithmetic Mode”](#)

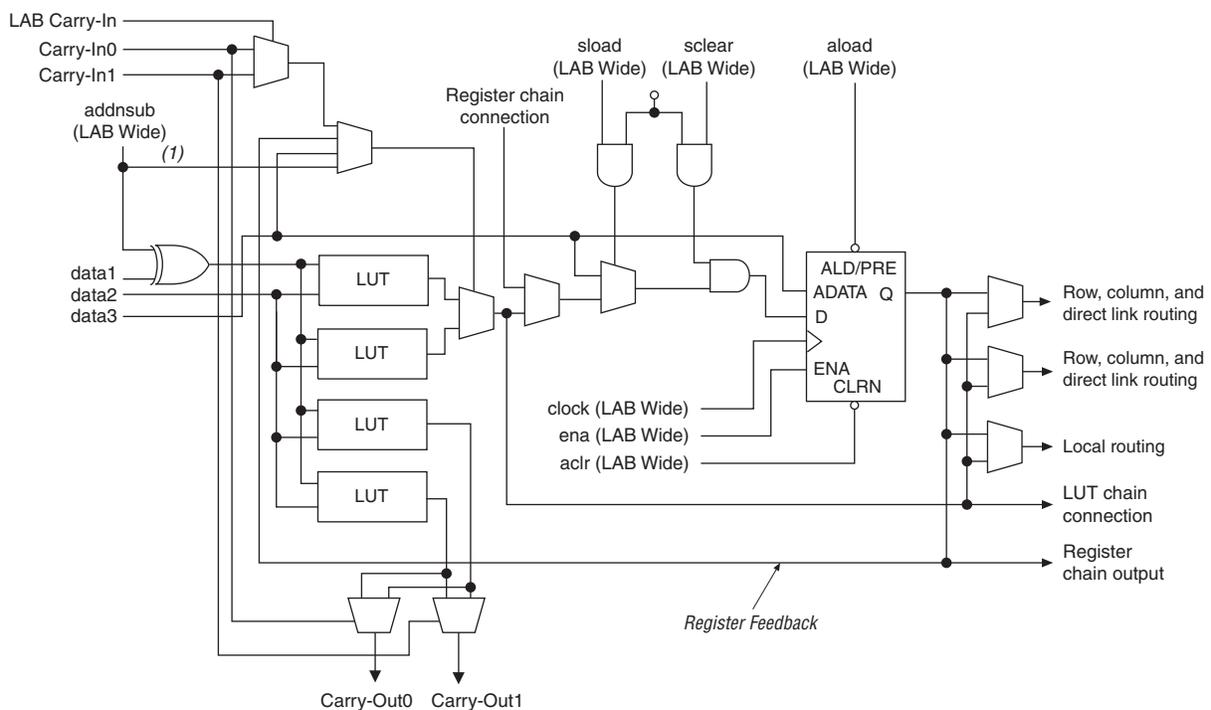
Each mode uses LE resources differently. In each mode, eight available inputs to the LE, the four data inputs from the LAB local interconnect, `carry-in0` and `carry-in1` from the previous LE, the LAB carry-in from the previous carry-chain LAB, and the register chain connection are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset/load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes. The `addnsub` control signal is allowed in arithmetic mode.

The Quartus II software, along with parameterized functions such as the library of parameterized modules (LPM) functions, automatically chooses the appropriate mode for common functions such as counters, adders, subtractors, and arithmetic functions.

The other two LUTs use the data1 and data2 signals to generate two possible carry-out signals: one for a carry of 1 and the other for a carry of 0. The carry-in0 signal acts as the carry-select for the carry-out0 output and carry-in1 acts as the carry-select for the carry-out1 output. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The dynamic arithmetic mode also offers clock enable, counter enable, synchronous up/down control, synchronous clear, synchronous load, and dynamic adder/subtractor options. The LAB local interconnect data inputs generate the counter enable and synchronous up/down control signals. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. The Quartus II software automatically places any registers that are not used by the counter into other LABs. The addnsub LAB-wide signal controls whether the LE acts as an adder or subtractor.

Figure 2-8. LE in Dynamic Arithmetic Mode



Note to Figure 2-8:

(1) The addnsub signal is tied to the carry input for the first LE of a carry chain only.

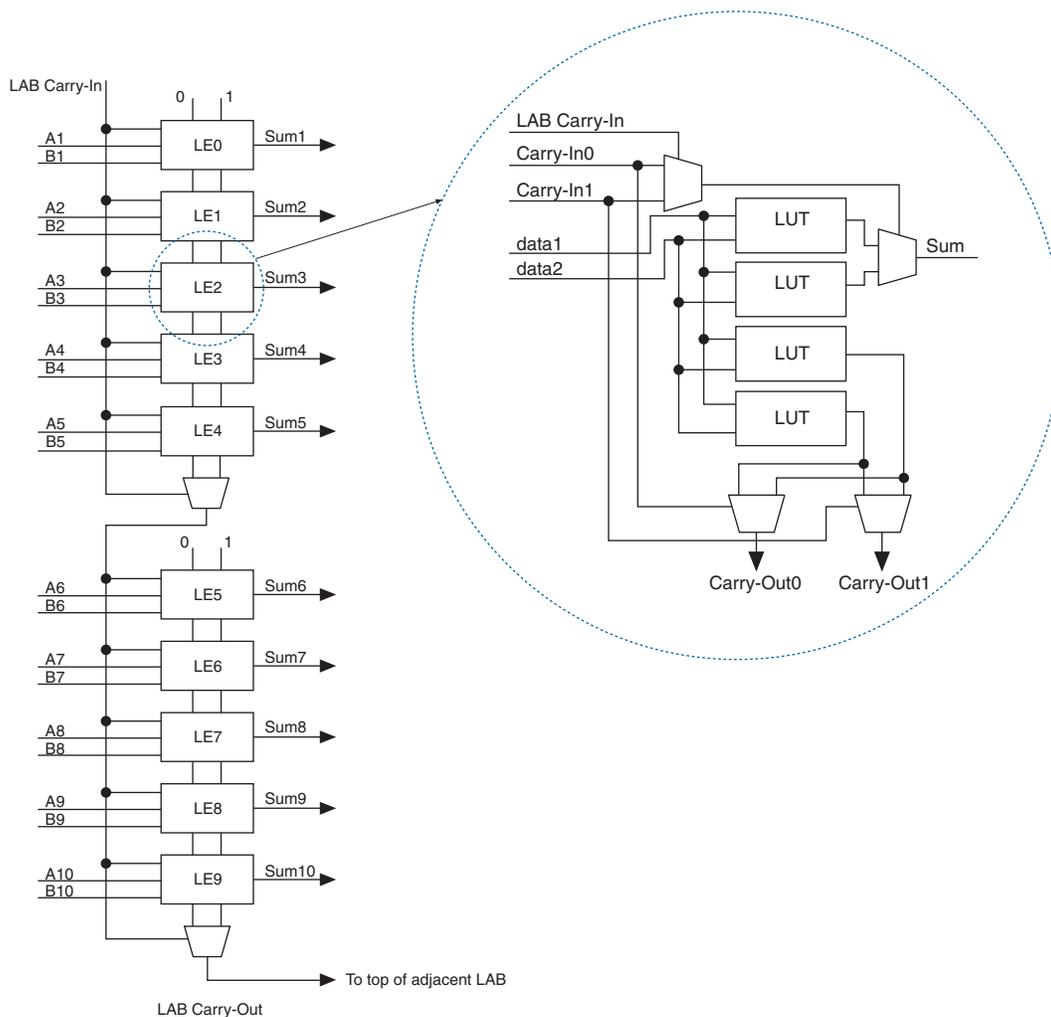
Carry-Select Chain

The carry-select chain provides a very fast carry-select function between LEs in dynamic arithmetic mode. The carry-select chain uses the redundant carry calculation to increase the speed of carry functions. The LE is configured to calculate outputs for a possible carry-in of 0 and carry-in of 1 in parallel. The carry-in0 and carry-in1 signals from a lower-order bit feed forward into the higher-order bit via the parallel carry chain and feed into both the LUT and the next portion of the carry chain. Carry-select chains can begin in any LE within an LAB.

The speed advantage of the carry-select chain is in the parallel pre-computation of carry chains. Because the LAB carry-in selects the precomputed carry chain, not every LE is in the critical path. Only the propagation delays between LAB carry-in generation (LE5 and LE10) are now part of the critical path. This feature allows the MAX V architecture to implement high-speed counters, adders, multipliers, parity functions, and comparators of arbitrary width.

Figure 2-9 shows the carry-select circuitry in an LAB for a 10-bit full adder. One portion of the LUT generates the sum of two bits using the input signals and the appropriate carry-in bit; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT generates carry-out bits. An LAB-wide carry-in bit selects which chain is used for the addition of given inputs. The carry-in signal for each chain, carry-in0 or carry-in1, selects the carry-out to carry forward to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is fed to local, row, or column interconnects.

Figure 2-9. Carry-Select Chain



The Quartus II software automatically creates carry chain logic during design processing, or you can create it manually during design entry. Parameterized functions such as LPM functions automatically take advantage of carry chains for the appropriate functions. The Quartus II software creates carry chains longer than 10 LEs by linking adjacent LABs within the same row together automatically. A carry chain can extend horizontally up to one full LAB row, but does not extend between LAB rows.

Clear and Preset Logic Control

LAB-wide signals control the logic for the register's clear and preset signals. The LE directly supports an asynchronous clear and preset function. The register preset is achieved through the asynchronous load of a logic high. MAX V devices support simultaneous preset/asynchronous load and clear signals. An asynchronous clear signal takes precedence if both signals are asserted simultaneously. Each LAB supports up to two clears and one preset signal.

In addition to the clear and preset ports, MAX V devices provide a chip-wide reset pin (`DEV_CLRn`) that resets all registers in the device. An option set before compilation in the Quartus II software controls this pin. This chip-wide reset overrides all other control signals and uses its own dedicated routing resources without using any of the four global resources. Driving this signal low before or during power-up prevents user mode from releasing clears within the design. This allows you to control when clear is released on a device that has just been powered-up. If not set for its chip-wide reset function, the `DEV_CLRn` pin is a regular I/O pin.

By default, all registers in MAX V devices are set to power-up low. However, this power-up state can be set to high on individual registers during design entry using the Quartus II software.

LE RAM

The Quartus II memory compiler can configure the unused LEs as LE RAM.

MAX V devices support the following memory types:

- FIFO synchronous R/W
- FIFO asynchronous R/W
- 1 port SRAM
- 2 port SRAM
- 3 port SRAM
- shift registers



For more information about memory, refer to the *Internal Memory (RAM and ROM) User Guide*.

MultiTrack Interconnect

In the MAX V architecture, connections between LEs, the UFM, and device I/O pins are provided by the MultiTrack interconnect structure. The MultiTrack interconnect consists of continuous, performance-optimized routing lines used for inter- and intra-design block connectivity. The Quartus II Compiler automatically places critical design paths on faster interconnects to improve design performance.

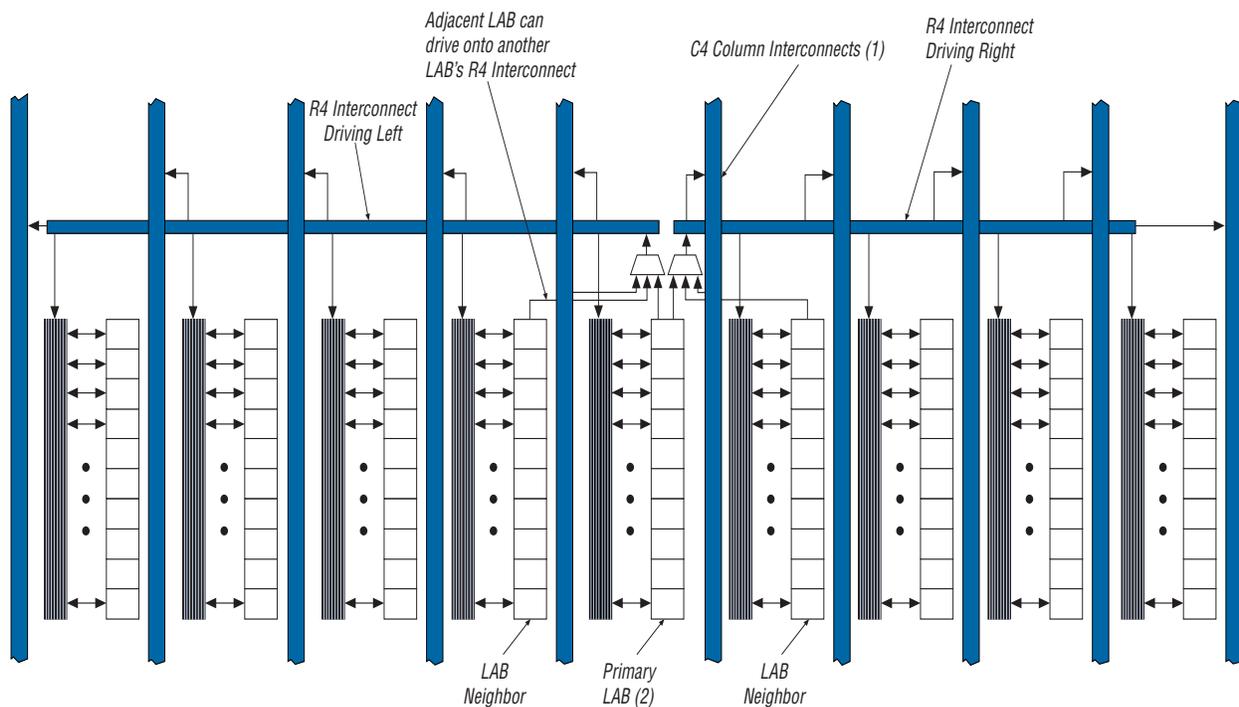
The MultiTrack interconnect consists of row and column interconnects that span fixed distances. A routing structure with fixed length resources for all devices allows predictable and short delays between logic levels instead of large delays associated with global or long routing lines. Dedicated row interconnects route signals to and from LABs within the same row. These row resources include:

- DirectLink interconnects between LABs
- R4 interconnects traversing four LABs to the right or left

The DirectLink interconnect allows an LAB to drive into the local interconnect of its left and right neighbors. The DirectLink interconnect provides fast communication between adjacent LABs and blocks without using row interconnect resources.

The R4 interconnects span four LABs and are used for fast row connections in a four-LAB region. Every LAB has its own set of R4 interconnects to drive either left or right. [Figure 2-10](#) shows R4 interconnect connections from an LAB. R4 interconnects can drive and be driven by row IOEs. For LAB interfacing, a primary LAB or horizontal LAB neighbor can drive a given R4 interconnect. For R4 interconnects that drive to the right, the primary LAB and right neighbor can drive on to the interconnect. For R4 interconnects that drive to the left, the primary LAB and its left neighbor can drive on to the interconnect. R4 interconnects can drive other R4 interconnects to extend the range of LABs they can drive. R4 interconnects can also drive C4 interconnects for connections from one row to another.

Figure 2-10. R4 Interconnect Connections



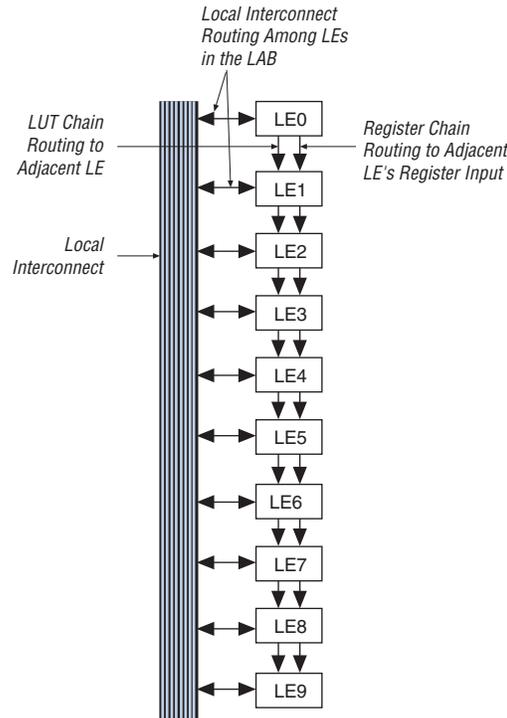
Notes to Figure 2-10:

- (1) C4 interconnects can drive R4 interconnects.
- (2) This pattern is repeated for every LAB in the LAB row.

The column interconnect operates similarly to the row interconnect. Each column of LABs is served by a dedicated column interconnect, which vertically routes signals to and from LABs and row and column IOEs. These column resources include:

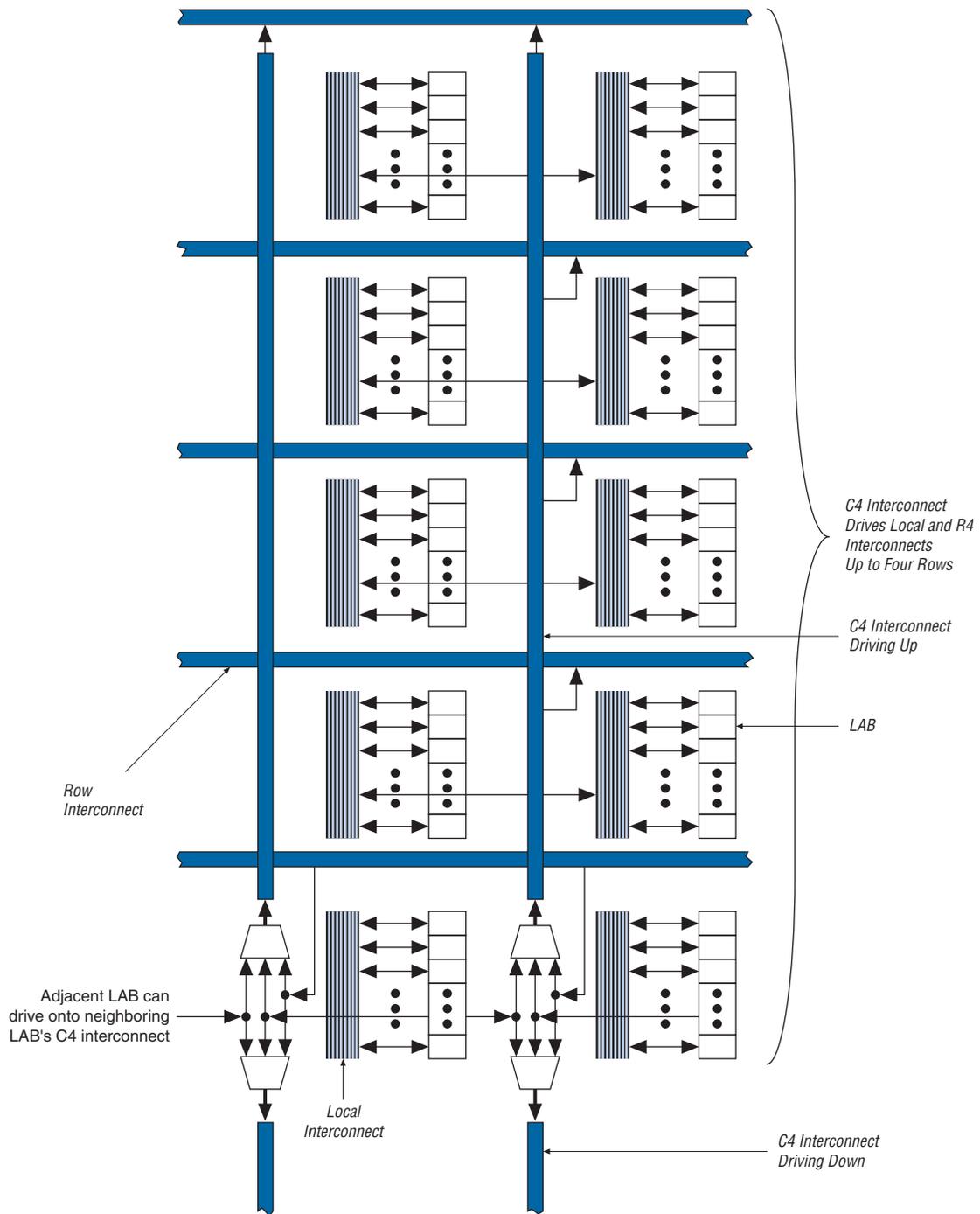
- LUT chain interconnects within an LAB
- Register chain interconnects within an LAB
- C4 interconnects traversing a distance of four LABs in an up and down direction

MAX V devices include an enhanced interconnect structure within LABs for routing LE output to LE input connections faster using LUT chain connections and register chain connections. The LUT chain connection allows the combinational output of an LE to directly drive the fast input of the LE right below it, bypassing the local interconnect. These resources can be used as a high-speed connection for wide fan-in functions from LE 1 to LE 10 in the same LAB. The register chain connection allows the register output of one LE to connect directly to the register input of the next LE in the LAB for fast shift registers. The Quartus II Compiler automatically takes advantage of these resources to improve utilization and performance. Figure 2-11 shows the LUT chain and register chain interconnects.

Figure 2-11. LUT Chain and Register Chain Interconnects

The C4 interconnects span four LABs up or down from a source LAB. Every LAB has its own set of C4 interconnects to drive either up or down. [Figure 2-12](#) shows the C4 interconnect connections from an LAB in a column. The C4 interconnects can drive and be driven by column and row IOEs. For LAB interconnection, a primary LAB or its vertical LAB neighbor can drive a given C4 interconnect. C4 interconnects can drive each other to extend their range as well as drive row interconnects for column-to-column connections.

Figure 2-12. C4 Interconnect Connections (Note 1)



Note to Figure 2-12:

- (1) Each C4 interconnect can drive either up or down four rows.

The UFM block communicates with the logic array similar to LAB-to-LAB interfaces. The UFM block connects to row and column interconnects and has local interconnect regions driven by row and column interconnects. This block also has DirectLink interconnects for fast connections to and from a neighboring LAB. For more information about the UFM interface to the logic array, refer to [“User Flash Memory Block” on page 2-21](#).

Table 2-2 lists the MAX V device routing scheme.

Table 2-2. Routing Scheme for MAX V Devices

Source	Destination										
	LUT Chain	Register Chain	Local (1)	DirectLink (1)	R4 (1)	C4 (1)	LE	UFM Block	Column IOE	Row IOE	Fast I/O (1)
LUT Chain	—	—	—	—	—	—	✓	—	—	—	—
Register Chain	—	—	—	—	—	—	✓	—	—	—	—
Local Interconnect	—	—	—	—	—	—	✓	✓	✓	✓	—
DirectLink Interconnect	—	—	✓	—	—	—	—	—	—	—	—
R4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
C4 Interconnect	—	—	✓	—	✓	✓	—	—	—	—	—
LE	✓	✓	✓	✓	✓	✓	—	—	✓	✓	✓
UFM Block	—	—	✓	✓	✓	✓	—	—	—	—	—
Column IOE	—	—	—	—	—	✓	—	—	—	—	—
Row IOE	—	—	—	✓	✓	✓	—	—	—	—	—

Note to Table 2-2:

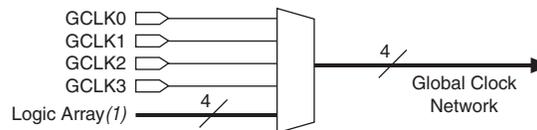
(1) These categories are interconnects.

Global Signals

Each MAX V device has four dual-purpose dedicated clock pins (GCLK[3..0], two pins on the left side and two pins on the right side) that drive the global clock network for clocking, as shown in [Figure 2-13](#). These four pins can also be used as GPIOs if they are not used to drive the global clock network.

The four global clock lines in the global clock network drive throughout the entire device. The global clock network can provide clocks for all resources within the device including LEs, LAB local interconnect, IOEs, and the UFM block. The global clock lines can also be used for global control signals, such as clock enables, synchronous or asynchronous clears, presets, output enables, or protocol control signals such as TRDY and IRDY for the PCI I/O standard. Internal logic can drive the global clock network for internally-generated global clocks and control signals. [Figure 2-13](#) shows the various sources that drive the global clock network.

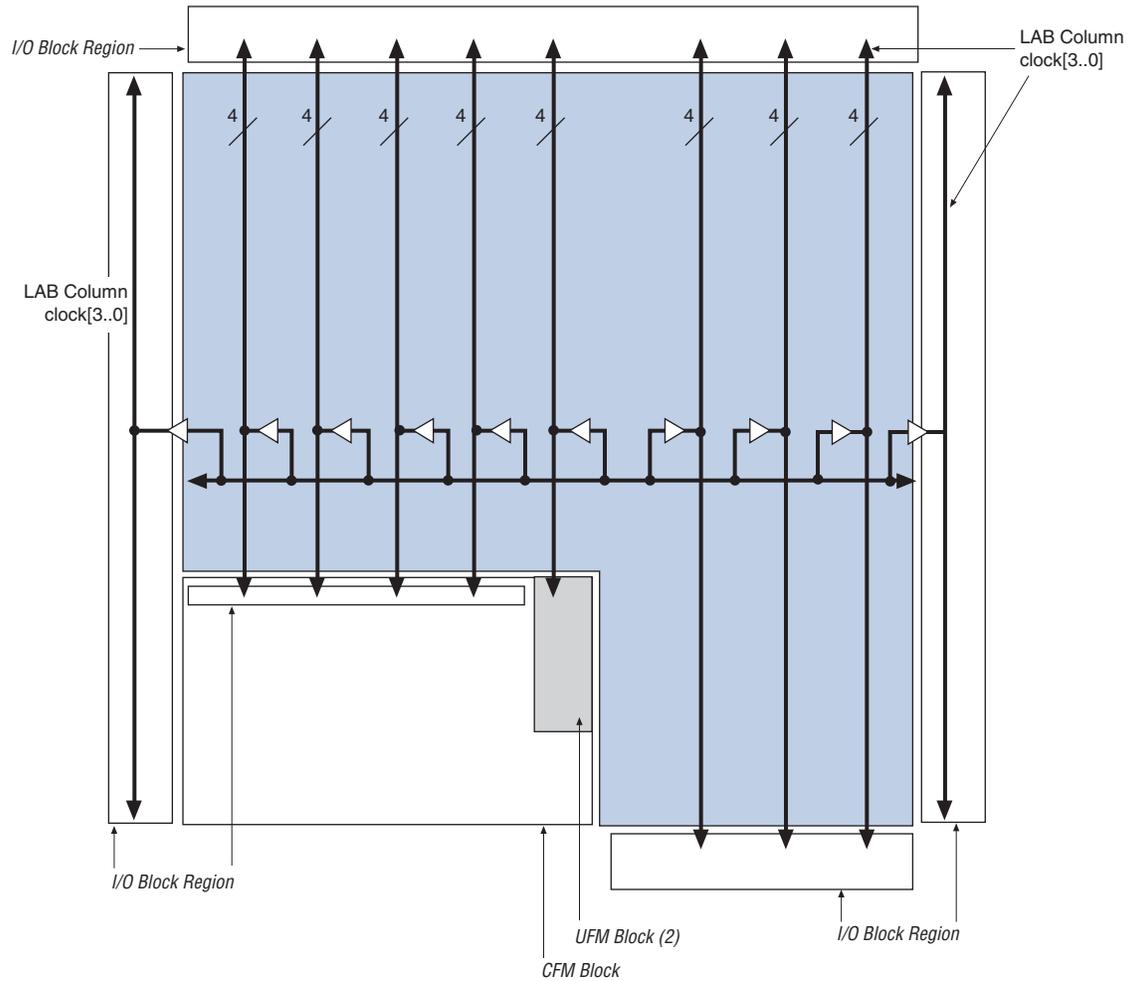
Figure 2-13. Global Clock Generation



Note to [Figure 2-13](#):

(1) Any I/O pin can use a MultiTrack interconnect to route as a logic array-generated global clock signal.

The global clock network drives to individual LAB column signals, LAB column clocks [3..0], that span an entire LAB column from the top to the bottom of the device. Unused global clocks or control signals in an LAB column are turned off at the LAB column clock buffers shown in [Figure 2-14](#). The LAB column clocks [3..0] are multiplexed down to two LAB clock signals and one LAB clear signal. Other control signal types route from the global clock network into the LAB local interconnect. For more information, refer to [“LAB Control Signals”](#) on page 2-6.

Figure 2-14. Global Clock Network (Note 1)**Notes to Figure 2-14:**

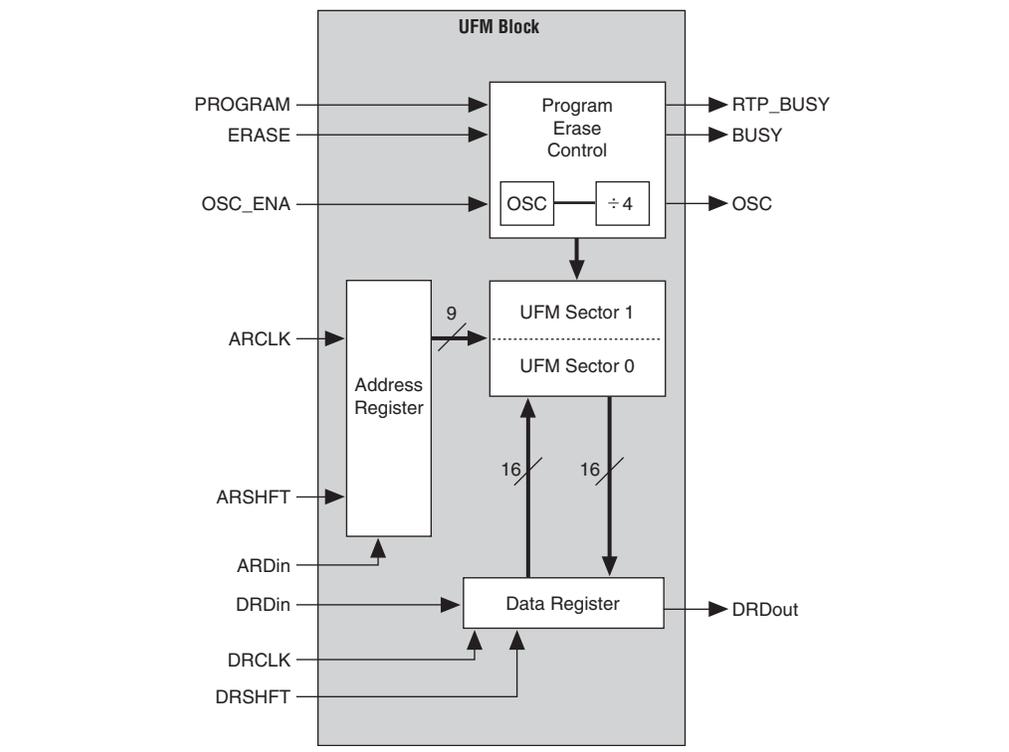
- (1) LAB column clocks in I/O block regions provide high fan-out output enable signals.
- (2) LAB column clocks drive to the UFM block.

User Flash Memory Block

MAX V devices feature a single UFM block, which can be used like a serial EEPROM for storing non-volatile information up to 8,192 bits. The UFM block connects to the logic array through the MultiTrack interconnect, allowing any LE to interface to the UFM block. Figure 2-15 shows the UFM block and interface signals. The logic array is used to create customer interface or protocol logic to interface the UFM block data outside of the device. The UFM block offers the following features:

- Non-volatile storage up to 16-bit wide and 8,192 total bits
- Two sectors for partitioned sector erase
- Built-in internal oscillator that optionally drives logic array
- Program, erase, and busy signals
- Auto-increment addressing
- Serial interface to logic array with programmable interface

Figure 2-15. UFM Block and Interface Signals



UFM Storage

Each device stores up to 8,192 bits of data in the UFM block. Table 2-3 lists the data size, sector, and address sizes for the UFM block.

Table 2-3. UFM Array Size

Device	Total Bits	Sectors	Address Bits	Data Width
5M40Z	8,192	2 (4,096 bits per sector)	9	16
5M80Z	8,192	2 (4,096 bits per sector)	9	16
5M160Z	8,192	2 (4,096 bits per sector)	9	16
5M240Z	8,192	2 (4,096 bits per sector)	9	16
5M570Z	8,192	2 (4,096 bits per sector)	9	16
5M1270Z	8,192	2 (4,096 bits per sector)	9	16
5M2210Z	8,192	2 (4,096 bits per sector)	9	16

There are 512 locations with 9-bit addressing ranging from 000h to 1FFh. The sector 0 address space is 000h to 0FFh and the sector 1 address space is from 100h to 1FFh. The data width is up to 16 bits of data. The Quartus II software automatically creates logic to accommodate smaller read or program data widths. Erasure of the UFM involves individual sector erasing (that is, one erase of sector 0 and one erase of sector 1 is required to erase the entire UFM block). Because sector erase is required before a program or write operation, having two sectors enables a sector size of data to be left untouched while the other sector is erased and programmed with new data.

Internal Oscillator

As shown in Figure 2-15, the dedicated circuitry within the UFM block contains an oscillator. The dedicated circuitry uses this oscillator internally for its read and program operations. This oscillator's divide by 4 output can drive out of the UFM block as a logic interface clock source or for general-purpose logic clocking. The typical OSC output signal frequency ranges from 3.9 to 5.3 MHz, and its exact frequency of operation is not programmable.

The UFM internal oscillator can be instantiated using the MegaWizard™ Plug-In Manager. You can also use the MAX II/MAX V Oscillator megafunction to instantiate the UFM oscillator without using the UFM memory block.

Program, Erase, and Busy Signals

The UFM block's dedicated circuitry automatically generates the necessary internal program and erase algorithm after the PROGRAM or ERASE input signals have been asserted. The PROGRAM or ERASE signal must be asserted until the busy signal deasserts, indicating the UFM internal program or erase operation has completed. The UFM block also supports JTAG as the interface for programming and reading.

 For more information about programming and erasing the UFM block, refer to the *User Flash Memory in MAX V Devices* chapter.

Auto-Increment Addressing

The UFM block supports standard read or stream read operations. The stream read is supported with an auto-increment address feature. Deasserting the ARSHIFT signal while clocking the ARCLK signal increments the address register value to read consecutive locations from the UFM array.

Serial Interface

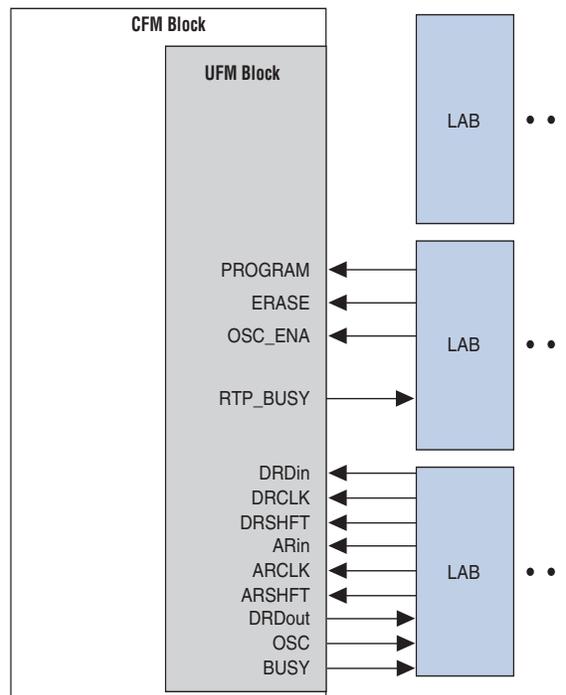
The UFM block supports a serial interface with serial address and data signals. The internal shift registers within the UFM block for address and data are 9 bits and 16 bits wide, respectively. The Quartus II software automatically generates interface logic in LEs for a parallel address and data interface to the UFM block. Other standard protocol interfaces such as SPI are also automatically generated in LE logic by the Quartus II software.

 For more information about the UFM interface signals and the Quartus II LE-based alternate interfaces, refer to the *User Flash Memory in MAX V Devices* chapter.

UFM Block to Logic Array Interface

The UFM block is a small partition of the flash memory that contains the CFM block, as shown in Figure 2-1 and Figure 2-2. The UFM block for the 5M40Z, 5M80Z, 5M160Z, and 5M240Z devices is located on the left side of the device adjacent to the left most LAB column. The UFM blocks for the 5M570Z, 5M1270Z, and 5M2210Z devices are located at the bottom left of the device. The UFM input and output signals interface to all types of interconnects (R4 interconnect, C4 interconnect, and DirectLink interconnect to/from adjacent LAB rows). The UFM signals can also be driven from global clocks, $GCLK[3..0]$. The interface regions for the 5M40Z, 5M80Z, 5M160Z, and 5M240Z devices are shown in Figure 2-16. The interface regions for 5M570Z, 5M1270Z, and 5M2210Z devices are shown in Figure 2-17.

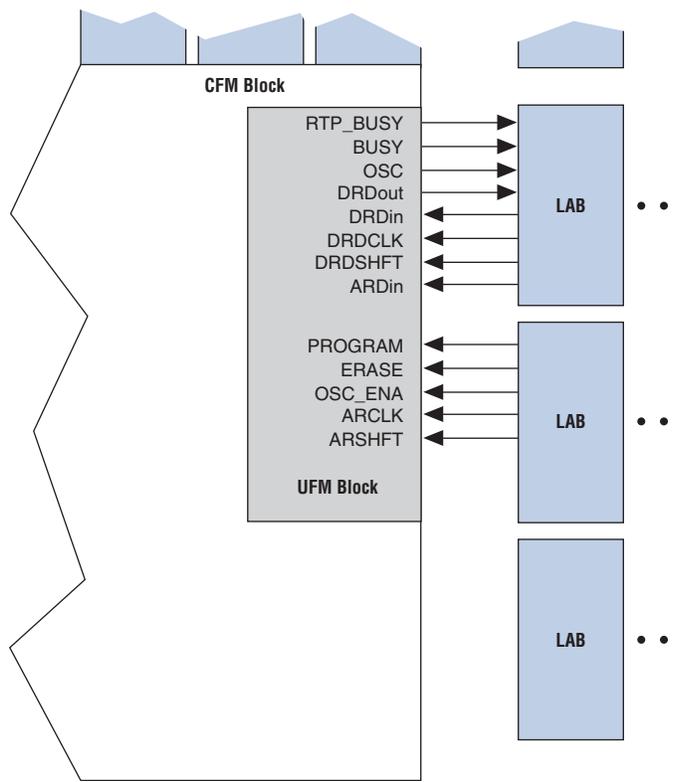
Figure 2-16. 5M40Z, 5M80Z, 5M160Z, and 5M240Z UFM Block LAB Row Interface (Note 1), (2)



Notes to Figure 2-16:

- (1) The UFM block inputs and outputs can drive to and from all types of interconnects, not only DirectLink interconnects from adjacent row LABs.
- (2) Not applicable to the T144 package of the 5M240Z device.

Figure 2-17. 5M240Z, 5M570Z, 5M1270Z, and 5M2210Z UFM Block LAB Row Interface (Note 1)



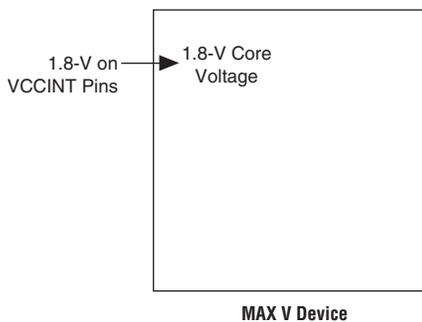
Note to Figure 2-17:

(1) Only applicable to the T144 package of the 5M240Z device.

Core Voltage

The MAX V architecture supports a 1.8-V core voltage on the V_{CCINT} supply. You must use a 1.8-V V_{CC} external supply to power the V_{CCINT} pins.

Figure 2-18. Core Voltage Feature in MAX V Devices



I/O Structure

IOEs support many features, including:

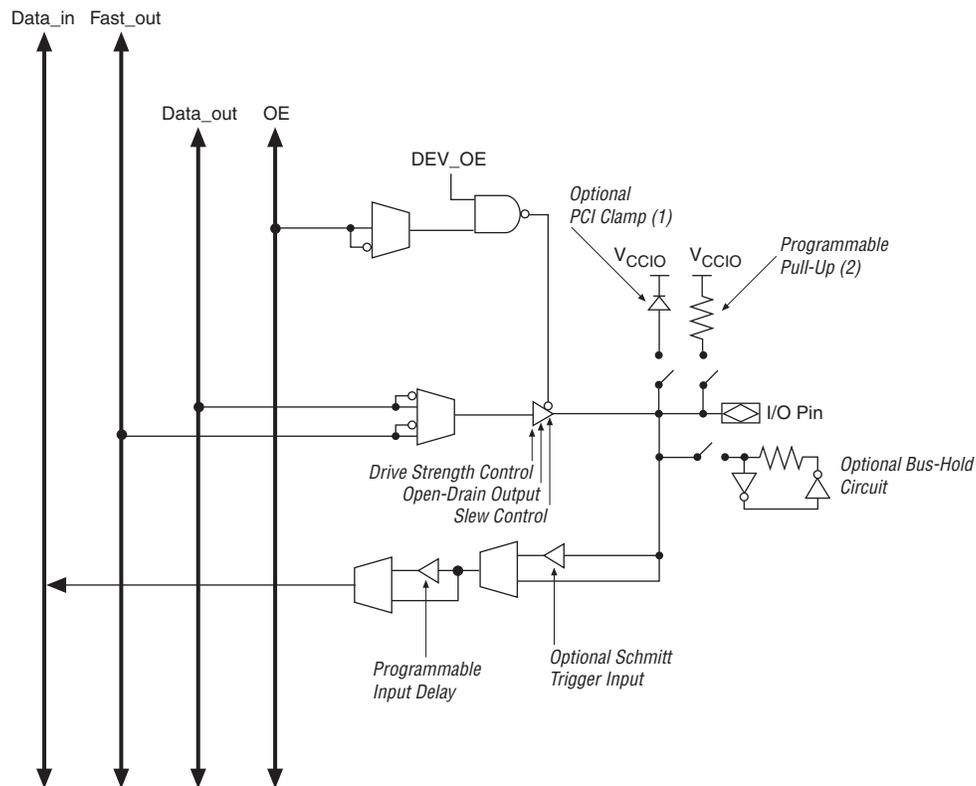
- LVTTTL, LVCMOS, LVDS, and RSDS I/O standards
- 3.3-V, 32-bit, 33-MHz PCI compliance
- JTAG boundary-scan test (BST) support
- Programmable drive strength control
- Weak pull-up resistors during power-up and in system programming
- Slew-rate control
- Tri-state buffers with individual output enable control
- Bus-hold circuitry
- Programmable pull-up resistors in user mode
- Unique output enable per pin
- Open-drain outputs
- Schmitt trigger inputs
- Fast I/O connection
- Programmable input delay

MAX V device IOEs contain a bidirectional I/O buffer. [Figure 2-19](#) shows the MAX V IOE structure. Registers from adjacent LABs can drive to or be driven from the IOE's bidirectional I/O buffers. The Quartus II software automatically attempts to place registers in the adjacent LAB with fast I/O connection to achieve the fastest possible clock-to-output and registered output enable timing. When the fast input registers option is enabled, the Quartus II software automatically routes the register to guarantee zero hold time. You can set timing assignments in the Quartus II software to achieve desired I/O timing.

Fast I/O Connection

A dedicated fast I/O connection from the adjacent LAB to the IOEs within an I/O block provides faster output delays for clock-to-output and t_{PD} propagation delays. This connection exists for data output signals, not output enable signals or input signals. Figure 2-20, Figure 2-21, and Figure 2-22 illustrate the fast I/O connection.

Figure 2-19. IOE Structure for MAX V Devices



Notes to Figure 2-19:

- (1) Available only in I/O bank 3 of 5M1270Z and 5M2210Z devices.
- (2) The programmable pull-up resistor is active during power-up, in-system programming (ISP), and if the device is unprogrammed.

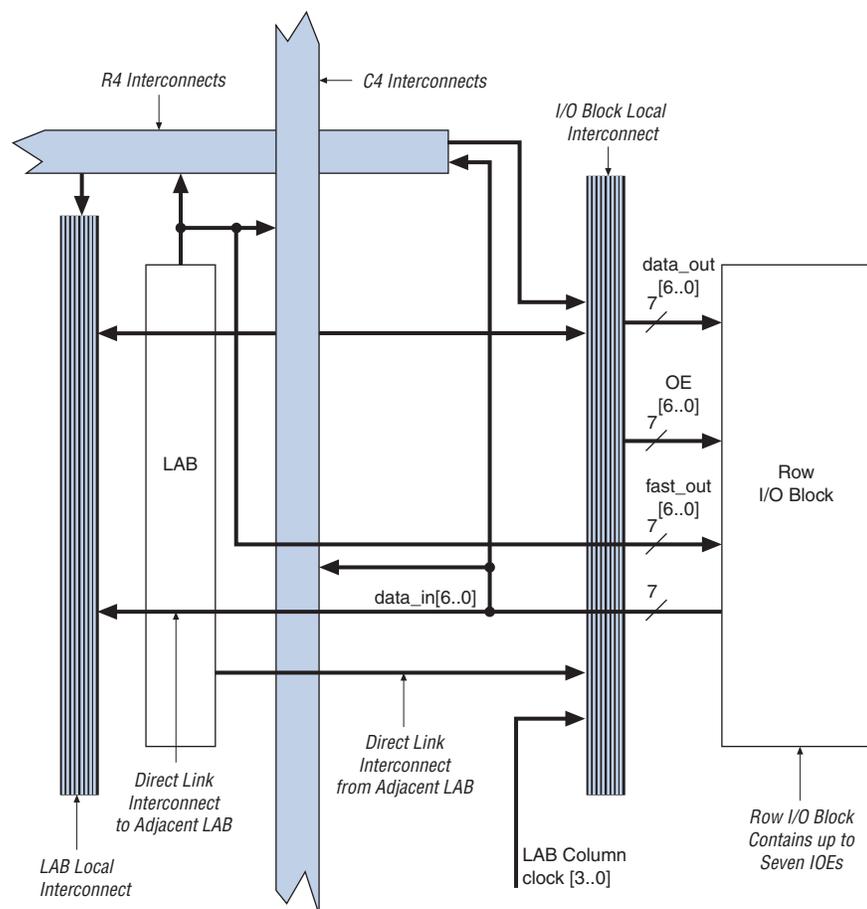
I/O Blocks

The IOEs are located in I/O blocks around the periphery of the MAX V device. There are up to seven IOEs per row I/O block and up to four IOEs per column I/O block. Each column or row I/O block interfaces with its adjacent LAB and MultiTrack interconnect to distribute signals throughout the device. The row I/O blocks drive row, column, or DirectLink interconnects. The column I/O blocks drive column interconnects.

 5M40Z, 5M80Z, 5M160Z, and 5M240Z devices have a maximum of five IOEs per row I/O block.

Figure 2-20 shows how a row I/O block connects to the logic array.

Figure 2-20. Row I/O Block Connection to the Interconnect (Note 1)

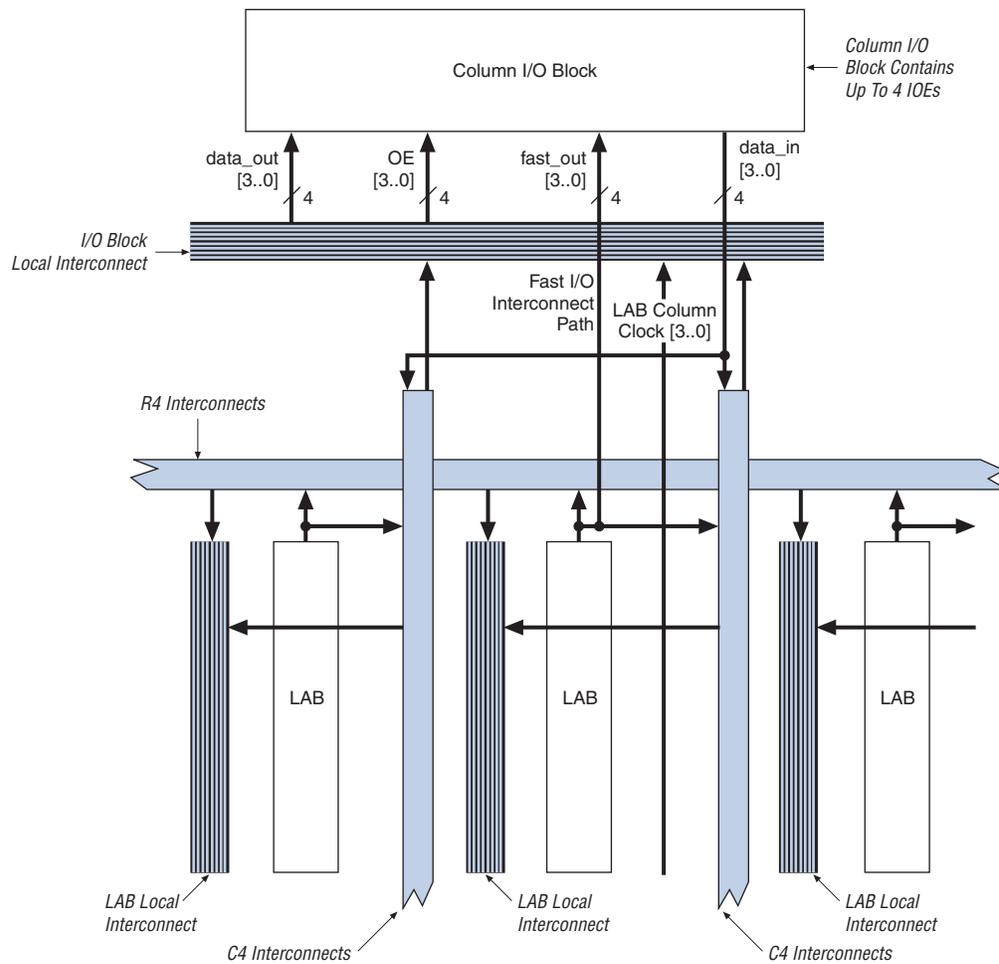


Note to Figure 2-20:

- (1) Each of the seven IOEs in the row I/O block can have one data_out or fast_out output, one OE output, and one data_in input.

Figure 2-21 shows how a column I/O block connects to the logic array.

Figure 2-21. Column I/O Block Connection to the Interconnect (Note 1)



Note to Figure 2-21:

- (1) Each of the four IOEs in the column I/O block can have one `data_out` or `fast_out` output, one `OE` output, and one `data_in` input.

I/O Standards and Banks

Table 2-4 lists the I/O standards supported by MAX V devices.

Table 2-4. MAX V I/O Standards (Part 1 of 2)

I/O Standard	Type	Output Supply Voltage (V_{CCIO}) (V)
3.3-V LVTTTL/LVCMOS	Single-ended	3.3
2.5-V LVTTTL/LVCMOS	Single-ended	2.5
1.8-V LVTTTL/LVCMOS	Single-ended	1.8
1.5-V LVCMOS	Single-ended	1.5
1.2-V LVCMOS	Single-ended	1.2

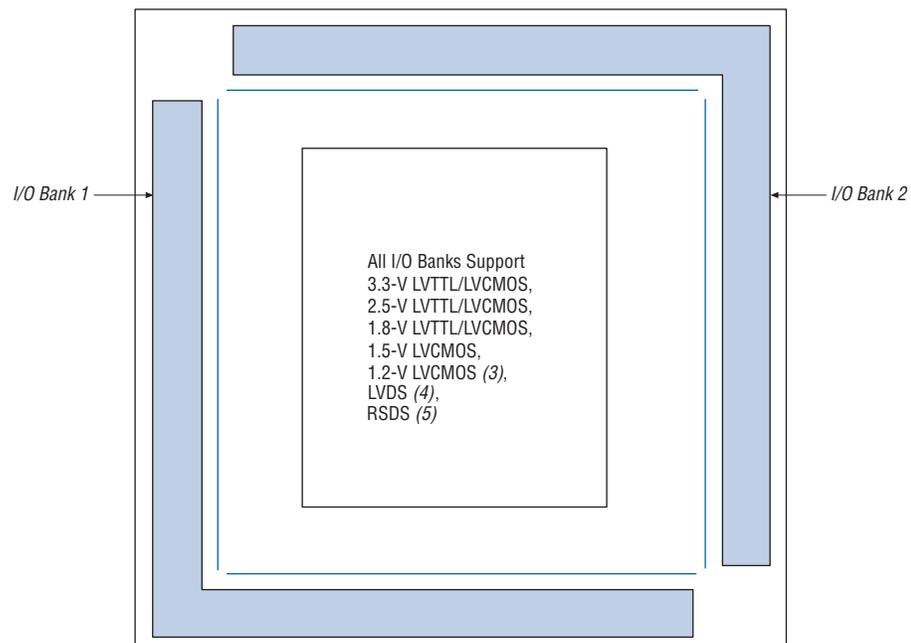
Table 2-4. MAX V I/O Standards (Part 2 of 2)

I/O Standard	Type	Output Supply Voltage (V_{CCIO}) (V)
3.3-V PCI (1)	Single-ended	3.3
LVDS (2)	Differential	2.5
RSDS (3)	Differential	2.5

Notes to Table 2-4:

- (1) The 3.3-V PCI compliant I/O is supported in Bank 3 of the 5M1270Z and 5M2210Z devices.
- (2) MAX V devices only support emulated LVDS output using a three resistor network (LVDS_E_3R).
- (3) MAX V devices only support emulated RSDS output using a three resistor network (RSDS_E_3R).

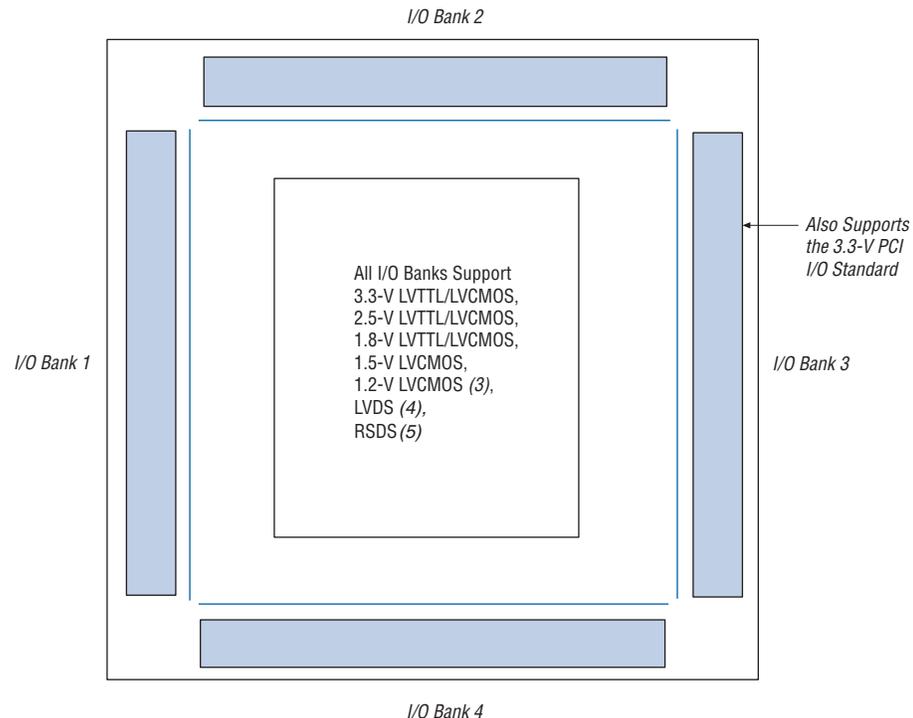
The 5M40Z, 5M80Z, 5M160Z, 5M240Z, and 5M570Z devices support two I/O banks, as shown in Figure 2-22. Each of these banks support all the LVTTTL, LVCMOS, LVDS, and RSDS standards shown in Table 2-4. PCI compliant I/O is not supported in these devices and banks.

Figure 2-22. I/O Banks for 5M40Z, 5M80Z, 5M160Z, 5M240Z, and 5M570Z Devices (Note 1), (2)**Notes to Figure 2-22:**

- (1) Figure 2-22 is a top view of the silicon die.
- (2) Figure 2-22 is a graphical representation only. Refer to the pin list and the Quartus II software for exact pin locations.
- (3) This I/O standard is not supported in Bank 1.
- (4) Emulated LVDS output using a three resistor network (LVDS_E_3R).
- (5) Emulated RSDS output using a three resistor network (RSDS_E_3R).

The 5M1270Z and 5M2210Z devices support four I/O banks, as shown in Figure 2–23. Each of these banks support all of the LVTTTL, LVCMOS, LVDS, and RSDS standards shown in Table 2–4. PCI compliant I/O is supported in Bank 3. Bank 3 supports the PCI clamping diode on inputs and PCI drive compliance on outputs. You must use Bank 3 for designs requiring PCI compliant I/O pins. The Quartus II software automatically places I/O pins in this bank if assigned with the PCI I/O standard.

Figure 2–23. I/O Banks for 5M1270Z and 5M2210Z Devices (Note 1), (2)



Notes to Figure 2–23:

- (1) Figure 2–23 is a top view of the silicon die.
- (2) Figure 2–23 is a graphical representation only. Refer to the pin list and the Quartus II software for exact pin locations.
- (3) This I/O standard is not supported in Bank 1.
- (4) Emulated LVDS output using a three resistor network (LVDS_E_3R).
- (5) Emulated RSDS output using a three resistor network (RSDS_E_3R).

Each I/O bank has dedicated V_{CCIO} pins that determine the voltage standard support in that bank. A single device can support 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V interfaces; each individual bank can support a different standard. Each I/O bank can support multiple standards with the same V_{CCIO} for input and output pins. For example, when V_{CCIO} is 3.3 V, Bank 3 can support LVTTTL, LVCMOS, and 3.3-V PCI. V_{CCIO} powers both the input and output buffers in MAX V devices.

The JTAG pins for MAX V devices are dedicated pins that cannot be used as regular I/O pins. The pins TMS, TDI, TDO, and TCK support all the I/O standards shown in Table 2–4 on page 2–29 except for PCI and 1.2-V LVCMOS. These pins reside in Bank 1 for all MAX V devices and their I/O standard support is controlled by the V_{CCIO} setting for Bank 1.

PCI Compliance

The MAX V 5M1270Z and 5M2210Z devices are compliant with PCI applications as well as all 3.3-V electrical specifications in the *PCI Local Bus Specification Revision 2.2*. These devices are also large enough to support PCI intellectual property (IP) cores. Table 2-5 shows the MAX V device speed grades that meet the PCI timing specifications.

Table 2-5. 3.3-V PCI Electrical Specifications and PCI Timing Support for MAX V Devices

Device	33-MHz PCI
5M1270Z	All Speed Grades
5M2210Z	All Speed Grades

LVDS and RSDS Channels

The MAX V device supports emulated LVDS and RSDS outputs on both row and column I/O banks. You can configure the rows and columns as emulated LVDS or RSDS output buffers that use two single-ended output buffers with three external resistor networks.

Table 2-6. LVDS and RSDS Channels supported in MAX V Devices (Note 1)

Device	64 MBGA	64 EQFP	68 MBGA	100 TQFP	100 MBGA	144 TQFP	256 FBGA	324 FBGA
5M40Z	10 eTx	20 eTx	—	—	—	—	—	—
5M80Z	10 eTx	20 eTx	20 eTx	33 eTx	—	—	—	—
5M160Z	—	20 eTx	20 eTx	33 eTx	33 eTx	—	—	—
5M240Z	—	—	20 eTx	33 eTx	33 eTx	49 eTx	—	—
5M570Z	—	—	—	28 eTx	28 eTx	49 eTx	75 eTx	—
5M1270Z	—	—	—	—	—	42 eTx	90 eTx	115 eTx
5M2210Z	—	—	—	—	—	—	83 eTx	115 eTx

Note to Table 2-6:

(1) eTx = emulated LVDS output buffers (LVDS_E_3R) or emulated RSDS output buffers (RSDS_E_3R).

Schmitt Trigger

The input buffer for each MAX V device I/O pin has an optional Schmitt trigger setting for the 3.3-V and 2.5-V standards. The Schmitt trigger allows input buffers to respond to slow input edge rates with a fast output edge rate. Most importantly, Schmitt triggers provide hysteresis on the input buffer, preventing slow-rising noisy input signals from ringing or oscillating on the input signal driven into the logic array. This provides system noise tolerance on MAX V inputs, but adds a small, nominal input delay.

The JTAG input pins (TMS, TCK, and TDI) have Schmitt trigger buffers that are always enabled.



The TCK input is susceptible to high pulse glitches when the input signal fall time is greater than 200 ns for all I/O standards.

Output Enable Signals

Each MAX V IOE output buffer supports output enable signals for tri-state control. The output enable signal can originate from the GCLK [3..0] global signals or from the MultiTrack interconnect. The MultiTrack interconnect routes output enable signals and allows for a unique output enable for each output or bidirectional pin.

MAX V devices also provide a chip-wide output enable pin (DEV_OE) to control the output enable for every output pin in the design. An option set before compilation in the Quartus II software controls this pin. This chip-wide output enable uses its own routing resources and does not use any of the four global resources. If this option is turned on, all outputs on the chip operate normally when DEV_OE is asserted. When the pin is deasserted, all outputs are tri-stated. If this option is turned off, the DEV_OE pin is disabled when the device operates in user mode and is available as a user I/O pin.

Programmable Drive Strength

The output buffer for each MAX V device I/O pin has two levels of programmable drive strength control for each of the LVTTTL and LVCMOS I/O standards. Programmable drive strength provides system noise reduction control for high performance I/O designs. Although a separate slew-rate control feature exists, using the lower drive strength setting provides signal slew-rate control to reduce system noise and signal overshoot without the large delay adder associated with the slew-rate control feature. Table 2-7 lists the possible settings for the I/O standards with drive strength control. The Quartus II software uses the maximum current strength as the default setting. The PCI I/O standard is always set at 20 mA with no alternate setting.

Table 2-7. Programmable Drive Strength (Note 1)

I/O Standard	IOH/IOL Current Strength Setting (mA)
3.3-V LVTTTL	16
	8
3.3-V LVCMOS	8
	4
2.5-V LVTTTL/LVCMOS	14
	7
1.8-V LVTTTL/LVCMOS	6
	3
1.5-V LVCMOS	4
	2
1.2-V LVCMOS	3

Note to Table 2-7:

- (1) The I_{OH} current strength numbers shown are for a condition of a $V_{OUT} = V_{OH}$ minimum, where the V_{OH} minimum is specified by the I/O standard. The I_{OL} current strength numbers shown are for a condition of a $V_{OUT} = V_{OL}$ maximum, where the V_{OL} maximum is specified by the I/O standard. For 2.5-V LVTTTL/LVCMOS, the I_{OH} condition is $V_{OUT} = 1.7$ V and the I_{OL} condition is $V_{OUT} = 0.7$ V.



The programmable drive strength feature can be used simultaneously with the slew-rate control feature.

Slew-Rate Control

The output buffer for each MAX V device I/O pin has a programmable output slew-rate control that can be configured for low noise or high-speed performance. A faster slew rate provides high-speed transitions for high-performance systems. However, these fast transitions may introduce noise transients into the system. A slow slew rate reduces system noise, but adds a nominal output delay to rising and falling edges. The lower the voltage standard (for example, 1.8-V LVTTTL) the larger the output delay when slow slew is enabled. Each I/O pin has an individual slew-rate control, allowing you to specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges. If no slew-rate control is specified, the Quartus II software defaults to a fast slew rate.



The slew-rate control feature can be used simultaneously with the programmable drive strength feature.

Open-Drain Output

MAX V devices provide an optional open-drain (equivalent to open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write enable signals) that can be asserted by any of several devices. This output can also provide an additional wired-OR plane.

Programmable Ground Pins

Each unused I/O pin on MAX V devices can be used as an additional ground pin. This programmable ground feature does not require the use of the associated LEs in the device. In the Quartus II software, unused pins can be set as programmable GND on a global default basis or they can be individually assigned. Unused pins also have the option of being set as tri-stated input pins.

Bus-Hold

Each MAX V device I/O pin provides an optional bus-hold feature. The bus-hold circuitry can hold the signal on an I/O pin at its last-driven state. Because the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls un-driven pins away from the input threshold voltage where noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals. If the bus-hold feature is enabled, the device cannot use the programmable pull-up option.

The bus-hold circuitry is only active after the device has fully initialized. The bus-hold circuit captures the value on the pin present at the moment user mode is entered.

Programmable Pull-Up Resistor

Each MAX V device I/O pin provides an optional programmable pull-up resistor during user mode. If you enable this feature for an I/O pin, the pull-up resistor holds the output to the V_{CCIO} level of the output pin's bank.

-  The programmable pull-up resistor feature should not be used at the same time as the bus-hold feature on a given I/O pin.
-  The programmable pull-up resistor is active during power-up, ISP, and if the device is unprogrammed.

Programmable Input Delay

The MAX V IOE includes a programmable input delay that is activated to ensure zero hold times. A path where a pin directly drives a register, with minimal routing between the two, may require the delay to ensure zero hold time. However, a path where a pin drives a register through long routing or through combinational logic may not require the delay to achieve a zero hold time. The Quartus II software uses this delay to ensure zero hold times when needed.

MultiVolt I/O Interface

The MAX V architecture supports the MultiVolt I/O interface feature, which allows MAX V devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation (V_{CCINT}), and up to four sets for input buffers and I/O output driver buffers (V_{CCIO}), depending on the number of I/O banks available in the devices where each set of V_{CCIO} pins powers one I/O bank. The 5M40Z, 5M80Z, 5M160Z, 5M240Z, and 5M570Z devices each have two I/O banks while the 5M1270Z and 5M2210Z devices each have four I/O banks.

Connect V_{CCIO} pins to either a 1.2-, 1.5-, 1.8-, 2.5-, or 3.3-V power supply, depending on the output requirements. The output levels are compatible with systems of the same voltage as the power supply (that is, when V_{CCIO} pins are connected to a 1.5-V power supply, the output levels are compatible with 1.5-V systems). When V_{CCIO} pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems. Table 2-8 summarizes MAX V MultiVolt I/O support.

Table 2-8. MultiVolt I/O Support in MAX V Devices (Part 1 of 2) (Note 1)

VCCIO (V)	Input Signal						Output Signal					
	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
1.2	✓	—	—	—	—	—	✓	—	—	—	—	—
1.5	—	✓	✓	✓	✓	—	✓	✓	—	—	—	—
1.8	—	✓	✓	✓	✓	—	✓ (2)	✓ (2)	✓	—	—	—
2.5	—	—	—	✓	✓	—	✓ (3)	✓ (3)	✓ (3)	✓	—	—

Table 2-8. MultiVolt I/O Support in MAX V Devices (Part 2 of 2) (Note 1)

VCCIO (V)	Input Signal						Output Signal					
	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	5.0 V
3.3	—	—	—	✓ (4)	✓	✓ (5)	✓ (6)	✓ (6)	✓ (6)	✓ (6)	✓	✓ (7)

Notes to Table 2-8:

- (1) To drive inputs higher than V_{CCIO} but less than 4.0 V including the overshoot, disable the I/O clamp diode. However, to drive 5.0-V signals to the device, enable the I/O clamp diode to prevent V_I from rising above 4.0 V. Use an external diode if the I/O pin does not support the clamp diode.
- (2) When $V_{CCIO} = 1.8$ V, a MAX V device can drive a 1.2-V or 1.5-V device with 1.8-V tolerant inputs.
- (3) When $V_{CCIO} = 2.5$ V, a MAX V device can drive a 1.2-V, 1.5-V, or 1.8-V device with 2.5-V tolerant inputs.
- (4) When $V_{CCIO} = 3.3$ V and a 2.5-V input signal feeds an input pin, the VCCIO supply current will be slightly larger than expected.
- (5) MAX V devices can be 5.0-V tolerant with the use of an external resistor and the internal I/O clamp diode on the 5M1270Z and 5M2210Z devices. Use an external clamp diode if the internal clamp diode is not available.
- (6) When $V_{CCIO} = 3.3$ V, a MAX V device can drive a 1.2-V, 1.5-V, 1.8-V, or 2.5-V device with 3.3-V tolerant inputs.
- (7) When $V_{CCIO} = 3.3$ V, a MAX V device can drive a device with 5.0-V TTL inputs but not 5.0-V CMOS inputs. For 5.0-V CMOS, open-drain setting with internal I/O clamp diode (available only on 5M1270Z and 5M2210Z devices) and external resistor is required. Use an external clamp diode if the internal clamp diode is not available.

Document Revision History

Table 2-9 lists the revision history for this chapter.

Table 2-9. Document Revision History

Date	Version	Changes
December 2010	1.0	Initial release.