



Intel[®] MAX[®] 10 Power Management User Guide

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1. Intel® MAX® 10 Power Management Overview

Intel® MAX® 10 devices offer the following power supply device options:

- Single-supply device—requires 1 external power supply of 3.0 V or 3.3 V while offering maximum convenience and board simplicity.
- Dual-supply device—requires 2 external power supplies of 1.2 V and 2.5 V while offering the most features, highest performance, and when coupled with high-efficiency Enpirion® Power Solutions, the lowest power solution.

Related Information

- [Intel MAX 10 Power Management Features and Architecture](#) on page 4
Provides information about power management features and architecture.
- [Intel MAX 10 Power Management User Guide Archives](#) on page 21
Provides a list of user guides for previous versions.

2. Intel MAX 10 Power Management Features and Architecture

Intel MAX 10 power optimization features are as follows:

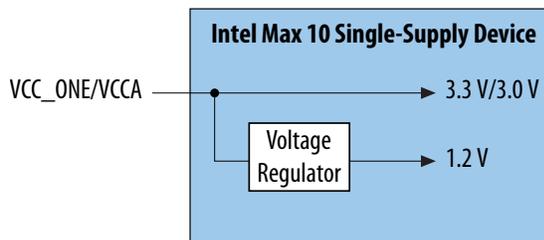
- Single-supply or dual-supply device options
- Power-on reset (POR) circuitry
- Power management controller scheme
- Hot socketing

2.1. Power Supply Device Options

2.1.1. Single-Supply Device

Intel MAX 10 single-supply devices only need either a 3.0- or 3.3-V external power supply. The external power supply serves as an input to the Intel MAX 10 device VCC_{ONE} and VCCA power pins. This external power supply is then regulated by an internal voltage regulator in the Intel MAX 10 single-supply device to 1.2 V. The 1.2-V voltage level is required by core logic operation.

Figure 1. Intel MAX 10 Single-Supply Device

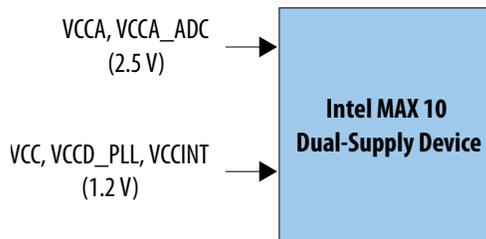


2.1.2. Dual-Supply Device

Intel MAX 10 dual-supply devices require 1.2 V and 2.5 V for the device core logic and periphery operation.



Figure 2. Intel MAX 10 Dual-Supply Device



2.1.3. Comparison of the Intel MAX 10 Power Supply Device Options

Table 1. Comparison of the Intel MAX 10 Power Supply Device Options

Characteristics	Single-Supply Device	Dual-Supply Device
Voltage regulator count ⁽¹⁾	1	2
Core and I/O performance	Low	High

For Intel MAX 10 single-supply devices, only one power supply is required—3.0 V or 3.3 V to power the core of the FPGA. The same power supply can be used to power the I/O if the same 3.0 V or 3.3 V voltage is required. If different I/O voltage is used, then additional voltage regulators will be needed.

For Intel MAX 10 dual-supply devices, two power supplies are required to supply power to the device core, periphery, phase-locked loop (PLL), and analog-to-digital converters (ADC) blocks—1.2 V and 2.5 V. Depending on the I/O standard voltage requirement, you may use two or more voltage regulators.

As the power rails for the FPGA core are supplied externally in the Intel MAX 10 dual-supply devices, the design can be optimized for power by using high efficiency switching power supplies on the board. The power savings will be equal to the increased efficiency of the regulators used compared to the internal linear regulators of the Intel MAX 10 single-supply devices. If linear regulators are used to power the Intel MAX 10 dual-supply devices, the power consumption of the Intel MAX 10 dual-supply devices will be approximately equal to the Intel MAX 10 single-supply devices.

The device performance of the single-supply device is lower than that of the dual-supply device. For the performance difference in terms of LVDS, pseudo-LVDS, digital signal processing (DSP), and internal memory performance, refer to the Intel MAX 10 FPGA device datasheet.

Related Information

Intel MAX 10 FPGA Device Datasheet

Provides details about the Intel MAX 10 performance difference in terms of LVDS, pseudo-LVDS, DSP, and internal memory performance.

⁽¹⁾ This shows the number of power supplies required by the core and periphery of the Intel MAX 10 devices. You may need additional voltage regulators to supply power to the VCCIO if the VCCIO does not have the same voltage level as the core and periphery supply.



2.1.4. Power Supply Design

Designing a power tree for a Intel MAX 10 single- or dual-supply device will vary depending on the static and dynamic power, as well as I/O and other feature utilization, for each specific use case.

The Intel Enpirion portfolio of power management solutions, combined with comprehensive design tools, enable optimized Intel MAX 10 device power supply design. The Enpirion portfolio includes power management solutions that are compatible with all Intel MAX 10 variants.

The *Intel MAX 10 FPGA Device Family Pin Connection Guidelines* provides a more detailed recommendation about how to group inputs to power a Intel MAX 10 device. The Early Power Estimators (EPE) tool for Intel MAX 10 devices provides input rail power requirements and specific device recommendations based on each specific Intel MAX 10 use case.

Individual input rail voltage and current requirements are summarized on the **Report** tab while input rail groupings and specific power supply recommendations can be found on the **Main** and **Enpirion** tabs, respectively.

Warning: Intel MAX 10 single-supply devices have maximum power consumption of V_{CC_ONE} , as listed in the following table. Running a design that goes beyond the maximum power consumption of V_{CC_ONE} of the Intel MAX 10 single-supply device may cause functional issue on the device. Therefore, ensure that your device does not exceed the maximum power consumption of V_{CC_ONE} when you analyze the power consumption of your design using the EPE spreadsheet.

Table 2. Maximum Power Consumption of V_{CC_ONE} for Intel MAX 10 Single-Supply Devices

Device	Maximum Power Consumption (W)
10M02S	0.778
10M04S	1.362
10M08S	1.362
10M16S	2.270
10M25S	2.943
10M40S	5.267
10M50S	5.267

Related Information

- [Enpirion Power Management Solutions](#)
Provides more information about Intel's Power Management IC and Power solutions designed for powering FPGAs.
- [Intel MAX 10 FPGA Device Family Pin Connection Guidelines](#)
Provides a more detailed recommendation about how to group inputs in order to power an Intel MAX 10 device.
- [Early Power Estimators \(EPE\) and Power Analyzer](#)



2.1.4.1. Transient Current

You may observe a transient current at the V_{CCIO} power supply when powering up the Intel MAX 10 devices. The transient current of V_{CCIO} applies to all V_{CCIO} voltage levels supported by the Intel MAX 10 device.

Table 3. Maximum V_{CCIO} Power Supply Transient Current for Intel MAX 10 Devices

Device	Maximum Power Supply Transient Current (mA)	Duration (s)
10M02	220	25% of the ramp time
10M04	290	
10M08	300	
10M16	430	
10M25	510	
10M40	670	
10M50	680	

Note: The value of the transient current is based on the zero decoupling capacitance on the characterization board. The observed value will be less than the published value after adding the decoupling capacitance on your design board. Intel recommends using a soft start regulator that is able to reduce the transient current when the device is powered.

2.2. Power-On Reset Circuitry

The POR circuitry keeps the Intel MAX 10 device in the reset state until all power supplies reach the recommended operating range during device power up. The individual power supply must reach the recommended operating range within the maximum power supply ramp time, t_{RAMP} .

If the ramp time, t_{RAMP} , is not met, the Intel MAX 10 device I/O pins and programming registers remain tri-stated, during which device configuration could fail.

The Intel MAX 10 device POR circuit monitors the following power rails during power up regardless of the power supply device options:

- V_{CC} or regulated V_{CC_ONE}
- V_{CCIO} of banks 1B and 8⁽²⁾
- V_{CCA}

The POR circuitry also ensures V_{CCIO} level of I/O banks 1B and 8⁽²⁾ that contain configuration pins reach an acceptable level before configuration is triggered.

⁽²⁾ V_{CCIO} of banks 1 and 8 for the 10M02 device.



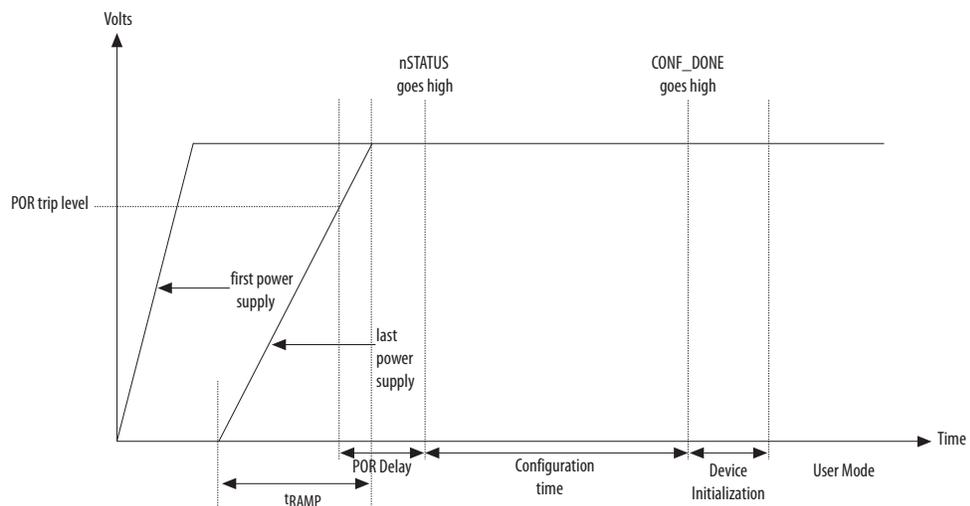
2.2.1. Power Supplies Monitored and Not Monitored by the POR Circuitry

Table 4. Power Supplies Monitored and Not Monitored by the POR Circuitry

Power Supply Device Options	Power Supplies Monitored	Power Supplies Not Monitored
Single-supply device	<ul style="list-style-type: none"> Regulated V_{CC_ONE} V_{CCA} V_{CCIO} ⁽³⁾ 	—
Dual-supply device	<ul style="list-style-type: none"> V_{CC} V_{CCA} V_{CCIO} ⁽³⁾ 	<ul style="list-style-type: none"> V_{CCD_PLL} V_{CCA_ADC} V_{CCINT}

The Intel MAX 10 POR circuitry uses an individual POR-detecting circuitry to monitor each of the configuration-related power supplies independently. The outputs of all the individual POR detectors gate the main POR circuitry. The main POR circuitry waits for all individual POR circuitries to release the POR signal before allowing the control block to start configuring the device. The main POR is released after the last ramp-up power reaches the POR trip level followed by a POR delay.

Figure 3. Monitored Power Supplies Ramp Up



Note: Each individual power supply must reach the recommended operating range within the specified t_{RAMP} .

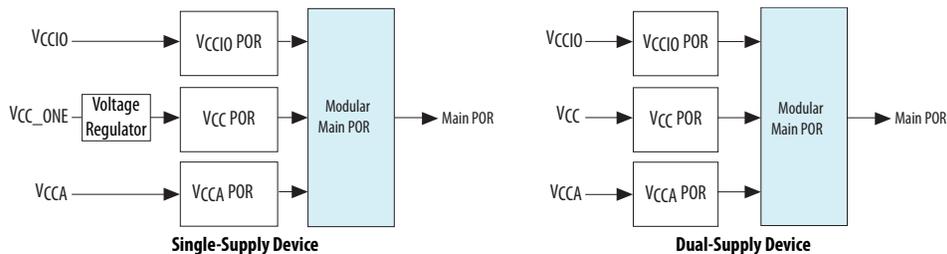
Note: All VCCIO banks must reach the recommended operating level before configuration completes.

Note: The typical value of POR delay is 2.5 ms for Intel MAX 10 devices.

⁽³⁾ For banks 1B and 8 for all Intel MAX 10 devices and banks 1 and 8 for the 10M02 device.



Figure 4. Simplified POR Diagram for Intel MAX 10 Devices



After the Intel MAX 10 device enters user mode, the POR circuit continues to monitor the V_{CCA} and V_{CC} power supplies. This is to detect a brown-out condition during user mode. If either the V_{CCA} or V_{CC} voltages go below the POR trip point during user mode, the main POR signal is asserted. When the main POR signal is asserted, the device is forced into reset state. $V_{CCIO}^{(3)}$ is monitored by the POR circuitry. In the event of the $V_{CCIO}^{(3)}$ voltage drops during user mode, the POR circuit does not reset the device. However, the POR circuit does monitor the V_{CCIO} voltage drop for up to 9 ms after the last power rail reaches its trip point.

2.2.2. Instant-On Support

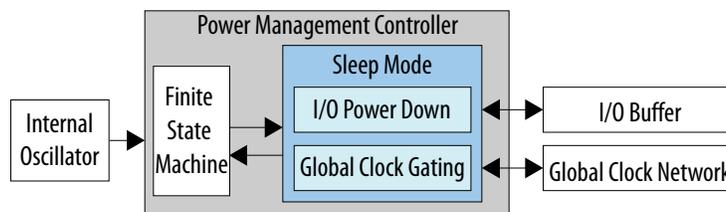
In some applications, it is necessary for a device to wake up very quickly to begin operation. The Intel MAX 10 device offers the instant-on feature to support fast wake-up time applications. With the instant-on feature, Intel MAX 10 devices can directly enter configuration mode with a short delay time after the POR trips for the monitored power supplies.

2.3. Power Management Controller Scheme

The power management controller scheme allows you to allocate some applications in sleep mode during runtime. This enables you to turn off portions of the design, thus reducing dynamic power consumption. You can re-enable your application with a fast wake-up time of less than 1 ms.

2.3.1. Power Management Controller Architecture

Figure 5. Power Management Controller Architecture



The Intel MAX 10 device contains hardware features that enable I/O power down and global clock (GCLK) gating to manage low-power state during sleep mode. You can power down the I/O buffer dynamically when your application is in idle or sleep mode. One example is the digital single lens reflex DSLR camera application where the LVDS I/O needs to be powered down during the idle condition. Without touching any buttons, the screen turns off while the camera is still powered on.



Intel provides a soft power management controller as reference design utilizing low-power features implemented in the Intel MAX 10 devices. You can modify the reference design based on your application. The soft power management controller includes a simple finite state machine (FSM) to manage the low-power state mode by powering down the I/O buffer and GCLK gating during sleep mode.

All Intel MAX 10 devices contain hardware features for clock gating. The 10M16, 10M25, 10M40, and 10M50 devices contain hardware features for I/O power down. With hardware features, you can manage the low-power state during sleep mode by using the soft power management controller that you define.

You can implement the power management controller in FPGA core fabric with a minimum of one I/O port reserved for sleep mode enter and exit signals.

2.3.1.1. Internal Oscillator

The internal oscillator clocks the power management controller operation. The internal oscillator is routed from flash to the core. The internal oscillator enables the power management controller to detect the wake-up event and the sleep mode event. In order to enable the internal oscillator clock when the power management controller is enabled, you have to set `oscena` to 1. For the clock frequency of the internal oscillator, refer to the *Intel MAX 10 FPGA Device Datasheet*.

Related Information

[Intel MAX 10 FPGA Device Datasheet](#)

Provides details about the Intel MAX 10 ramp time requirements, internal oscillator clock frequency, and hot-socketing specifications.

2.3.1.2. I/O Buffer Power Down

The Intel MAX 10 device has a dynamic power-down feature on some of the I/O buffers that have high-static power consumption. The dynamic power-down feature is only applicable for the I/O buffers that have been programmed for the I/O standards in the following table.

Table 5. I/O Buffer Power Down

I/O Buffer	I/O Standards	Control Port	Control Signal Capability
Input	SSTL, HSTL, HSUL, and LVDS	nsleep	1 per I/O bank ⁽⁴⁾
Output	All I/O standards	oe	1 per I/O buffer

During power-up and configuration modes, the soft power management controller is not yet configured and the control signals are forced to 1 (inactive). After configuration mode, when the power management controller is activated, the power management controller will default the control signals to 1. When control signals are 0, the power management controller powers down or tri-states the I/O buffers. Subsequently the I/O is put into the sleep mode.

The Intel MAX 10 device I/O buffers need to maintain the previous states during the sleep mode operation. The previous states in your core logics remain upon exiting the sleep mode.

(4) I/O banks 1A and 1B share one control signal.



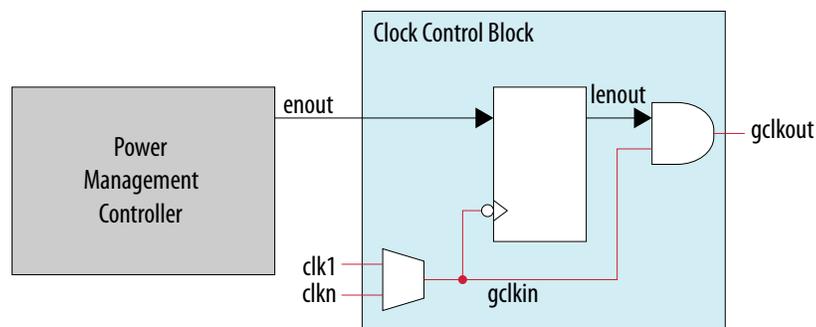
2.3.1.3. Global Clock Gating

The dynamic power-down feature is available in GCLK networks only. You can use the power management controller for the dynamic power-down of a GCLK network by controlling the active high `enout` signal. The GCLK networks serve as low-skew clock sources for functional blocks such as logic array blocks (LABs), DSP, embedded memory, and PLLs.

When a GCLK network is gated, all the logics fed by the GCLK network are in off-state. This reduces the overall power consumption of the device. The dynamic power-down feature allows core logics to control the following power-up and power-down conditions of the GCLK networks:

- Power down synchronously or asynchronously
- Power up asynchronously

Figure 6. GCLK Gating



2.4. Hot Socketing

The Intel MAX 10 device offers hot socketing, which is also known as hot plug-in or hot swap, and power sequencing support without the use of any external devices. You can insert or remove the Intel MAX 10 device on a board in a system during system operation. This does not affect the running system bus or the board that is inserted into the system.

The hot-socketing feature removes some encountered difficulties when using the Intel MAX 10 device on a PCB that contains a mixture of devices with different voltage levels.

With the Intel MAX 10 device hot-socketing feature, you no longer need to ensure a proper power-up sequence for each device on the board. Intel MAX 10 device hot-socketing feature provides:

- Board or device insertion and removal without external components or board manipulation
- Support for any power-up sequence
- Non-intrusive I/O buffers to system buses during hot insertion



2.4.1. Hot-Socketing Specifications

The Intel MAX 10 device is a hot-socketing compliant device that does not need any external components or special design requirements. Hot-socketing support in the Intel MAX 10 device has the following advantages:

- You can drive the devices before power up without damaging the device.
- I/O pins remain tri-stated during power up. The device does not drive out before or during power up, therefore not affecting other buses in operation.

2.4.1.1. Drive Intel MAX 10 Devices Before Power Up

Before or during power up or power down, you can drive signals into I/O pins, dedicated input pins, and dedicated clock pins without damaging the Intel MAX 10 devices.

The Intel MAX 10 device supports any power-up or power-down sequence to simplify system-level design.

2.4.1.2. I/O Pins Remain Tri-stated During Power up

The output buffers of the Intel MAX 10 device are turned off during system power up or power down. The Intel MAX 10 device family does not drive out until the device is configured and working in recommended operating conditions. The I/O pins are tri-stated during power up or power down.

A possible concern for semiconductor devices in general regarding hot-socketing is the potential for latch up. Latch up can occur when electrical subsystems are hot-socketed into an active system. During hot-socketing, the signal pins may be connected and driven by the active system. This occurs before the power supply can provide current to the V_{CC} of the device and ground planes. This condition can lead to latch up and cause a low-impedance path from V_{CC} to ground in the device. As a result, the device extends a large amount of current, possibly causing electrical damage.

The design of the I/O buffers and hot-socketing circuitry ensures that the Intel MAX 10 device family is immune to latch up during hot-socketing.

Related Information

[Intel MAX 10 FPGA Device Datasheet](#)

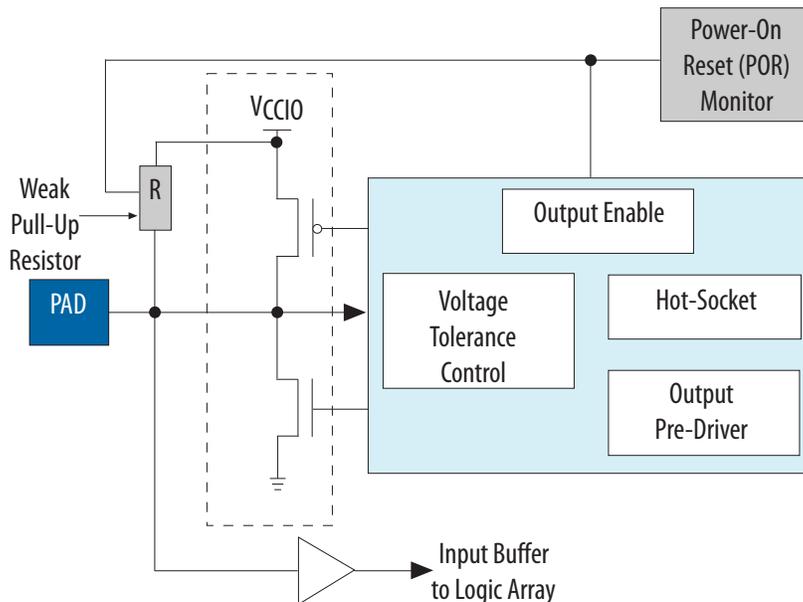
Provides details about the Intel MAX 10 ramp time requirements, internal oscillator clock frequency, and hot-socketing specifications.

2.4.2. Hot-Socketing Feature Implementation

The hot-socketing feature tri-states the output buffer during the power-up (V_{CCIO} or V_{CC} power supplies) or power-down event. The hot-socketing circuitry generates an internal `HOTSCKT` signal when V_{CCIO} or V_{CC} is below the threshold voltage during power up or power down. The `HOTSCKT` signal cuts off the output buffer to ensure that no DC current leaks through the pin. Each I/O pin has the circuitry shown in the following figure. The hot-socketing circuit does not include `CONF_DONE` and `nSTATUS` pins to ensure that these pins are able to operate during configuration. Thus, it is an expected behavior for these pins to drive out during power-up and power-down sequences.



Figure 7. Hot-Socketing Circuitry for Intel MAX 10 Devices



The POR circuit monitors the voltage level of power supplies and keeps the I/O pins tri-stated during power up. The weak pull-up resistor in Intel MAX 10 device I/O elements (IOE) keeps the I/O pins from floating. The voltage tolerance control circuit protects the I/O pins from being driven before V_{CCIO} and V_{CC} supplies are powered up. This prevents the I/O pins from driving out when the device is not in user mode.

Intel uses GND as reference for hot-socketing operation and I/O buffer designs. To ensure proper operation, Intel recommends connecting the GND between boards before connecting the power supplies. This prevents the GND on your board from being pulled up inadvertently by a path to power through other components on your board. A pulled up GND can cause an out-of-specification I/O voltage or current condition with the Intel FPGA.

3. Power Management Controller Reference Design

This reference design utilizes the low-power feature supported in Intel MAX 10 devices. The following figure shows the related block diagrams in the power management controller reference design.

Figure 8. Power Management Controller Block Diagram

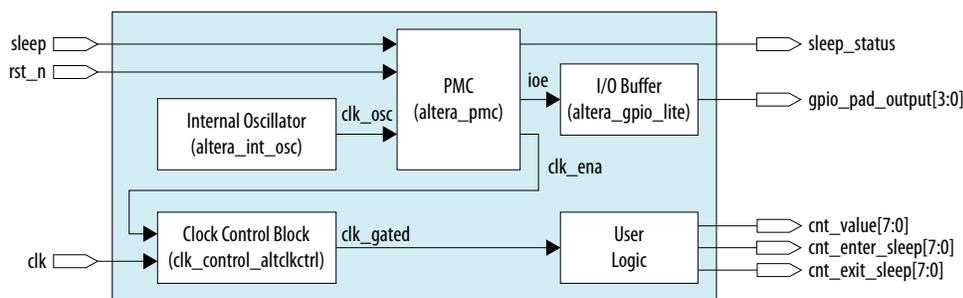


Table 6. Input and Output Ports of the Power Management Controller Reference Design

Port Name	Input/Output	Description
sleep	Input	Sleep control.
rst_n	Input	Active low reset signal.
clk	Input	Clock signal.
sleep_status	Output	Sleep status of the system. This signal is asserted high when the system is entering the sleep mode condition. This signal is de-asserted when the system exits the sleep mode condition completely.
gpio_pad_output[3:0]	Output	General-purpose I/O (GPIO) output ports.
cnt_value[7:0]	Output	Free-running counter value in user logic.
cnt_enter_sleep[7:0]	Output	Counter value when the system is entering sleep mode condition.
cnt_exit_sleep[7:0]	Output	Counter value when the system is exiting sleep mode condition.

The power management controller design is a FSM showing the state of powering down and powering up global clocks (GCLKs) and I/O buffers. The internal oscillator, clock control block, and I/O buffer are intellectual property (IP) that are supported by the Intel Quartus® Prime software and you can instantiate the IPs from the IP catalog. The user logic can be any logical circuitry that are implemented using logic element (LE) and an embedded component such as DSP and internal memory in your design. In this reference design, the user logic used is a free-running 8-bit counter. The cnt_enter_sleep and cnt_exit_sleep ports are used to ensure user logic can



enter and exit sleep mode without data corruption. It is expected for that `cnt_enter_sleep[7:0]` and `cnt_exit_sleep[7:0]` are at the same value after the user logic enter and exit sleep mode. `gpio_pad_output` ports demonstrate tri-stated state of the GPIO when the system is in sleep mode.

Related Information

[Power Management Controller Reference Design](#)

3.1. Clock Control Block

The ALTCLKCTRL Intel FPGA IP core (`clk_control_altclkctrl`) is an IP provided in the Intel Quartus Prime software. This IP is used to control the clock system in the device. The GCLKs that drive through the device can be dynamically powered down by controlling the active high `ena` signal. The `ena` port is an input to the clock control IP block. When this IP is instantiated, select the `ena` port to enable the controls of GCLKs.

Related Information

[ALTCLKCTRL Intel FPGA IP Core User Guide](#)

3.2. I/O Buffer

The GPIO Lite Intel FPGA IP core (`altera_gpio_lite`) is implemented as an input, output, or bidirectional I/O buffer. You can control the power down of these I/O buffers by enabling the `nsleep` port of the input buffer and the `oe` port of the output buffer. The `oe` and `nsleep` ports are pulled low by the power management controller design to power down the I/O buffers during sleep mode. Intel recommends using a separate GPIO Lite Intel FPGA IP core when some of the I/O buffer is not required to be powered down.

Related Information

[GPIO Lite Intel FPGA IP Core References](#)

3.3. Internal Oscillator

Internal Oscillator Intel FPGA IP core (`altera_in_osc`) is a free-running oscillator once you enable it. This oscillator runs throughout the entire power management controller design.

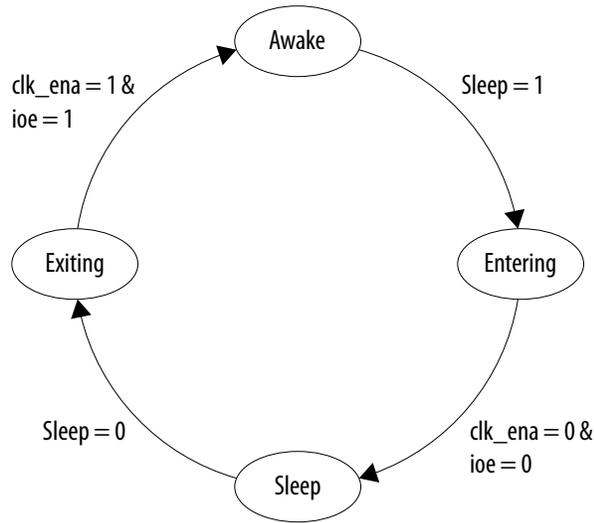
Related Information

[Internal Oscillator Intel FPGA IP Core](#)

3.4. Power Management Controller

The power management controller implements a simple FSM to control the power-up and power-down sequences of the GCLK networks and I/O buffer.

Figure 9. FSM of the Power Management Controller



3.4.1. Entering State

When the power management controller detects a sleep event, the FSM transitions to the Entering state and performs power-down operation on I/O buffers and GCLK networks. A sleep event is detected when the `sleep` signal is asserted. A sleep event could be triggered by an internal or external request.

3.4.2. Sleep State

After the power-down operation on I/O buffers and GCLK networks, the FSM transitions to the Sleep state and waits for the wake-up event. This state is the sleep mode state.

3.4.3. Exiting State

When the power management controller detects a wake-up event, the FSM transitions to the Exiting state and performs power-up operation on I/O buffers and GCLK networks. A wake-up event is detected when the `sleep` signal is de-asserted. A wake-up event could be triggered by an internal or external request such as interruption or time-out on some counters.

3.4.4. Awake State

After the power-up operation on I/O buffers and GCLK networks, the FSM transitions to the Awake state.

This process repeats when a sleep event is initiated again.

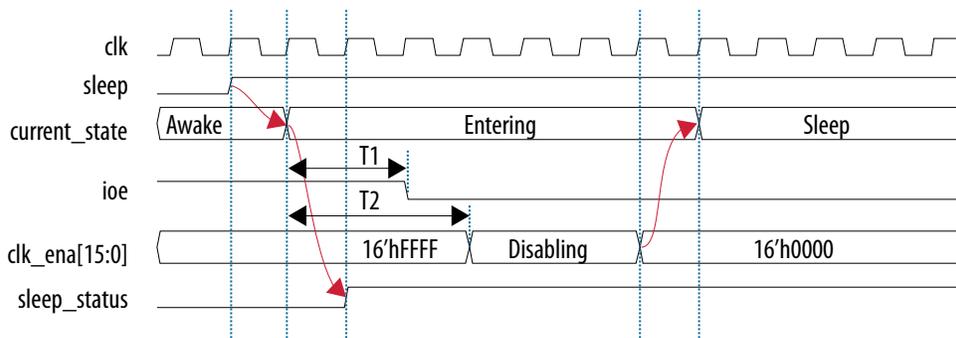


3.5. Entering or Exiting Sleep Mode

During power-up and configuration modes, the `sleep` signal must be low. When the `sleep` signal is asserted, the device immediately enters sleep mode. Upon entering sleep mode, the functionality of the device such as GCLK networks and I/O buffers are dynamically powered down—to minimize dynamic power dissipation. All configuration data is retained when the device is in the sleep mode.

3.5.1. Entering Sleep Mode

Figure 10. Entering Sleep Mode Timing Diagram

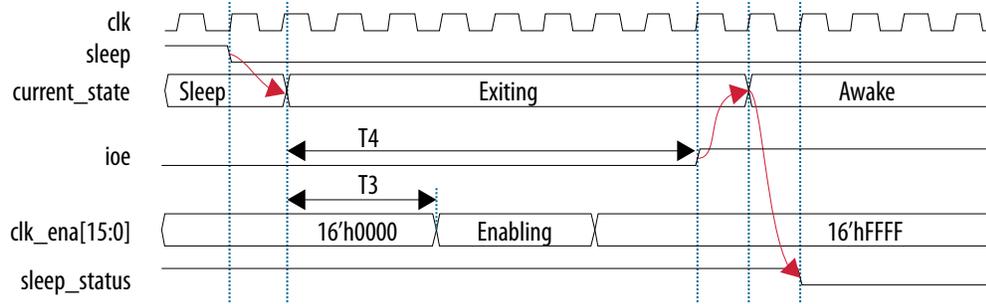


The following sequence occurs when the device enters sleep mode:

1. An internal or external request drives the `sleep` signal high, forcing the device to go into sleep mode.
2. After a delay of T_1 , the power management controller powers down all the I/O buffers by de-asserting `ioe` signal that connects to `oe` and `nsleep` ports of the I/O buffers.
3. After a delay of T_2 , the power management controller turns off all GCLK networks by disabling `clk_ena[15:0]` signal from LSB to MSB. After three clock cycles, the `clk_ena[15:0]` signal is fully disabled and transits into the sleep state.
4. The power management controller remains in sleep state until the `sleep` signal is de-asserted.
5. User logic will latch the running counter value before entering the sleep state and output to `cnt_sleep_enter` port. The running counter is then frozen.
6. `gpio_pad_output` (GPIO) is tri-stated when `ioe` is de-asserted.

3.5.2. Exiting Sleep Mode

Figure 11. Exiting Sleep Mode Timing Diagram



The following sequence occurs when the device exits sleep mode:

1. An internal or external request drives the `sleep` signal low, forcing the device to exit sleep mode.
2. After a delay of `T3`, the power management controller turns on all GCLK networks by enabling `clk_ena[15:0]` signal from LSB to MSB. After three clock cycles, the `clk_ena[15:0]` signal is fully enabled and all GCLK networks are turned on.
3. After a delay of `T4`, the power management controller powers up all the I/O buffers by asserting the `ioe` signal.
4. The power management controller remains in awake state until the `sleep` signal is asserted.
5. User logic will latch the running counter value before the awake state and output to `cnt_sleep_exit` port. The running counter is then release from freeze.
6. `gpio_pad_output` (GPIO) is driving its output value when `ioe` is asserted.

3.5.3. Timing Parameters

The following table lists the definition and minimum value of the `T1`, `T2`, `T3`, and `T4` parameters in the entering sleep mode timing diagram and exiting sleep mode timing diagram, respectively.

Table 7. `T1`, `T2`, `T3`, and `T4` Parameters Minimum Value and Definition

Parameter	Width (bits)	Minimum Value (Clock Cycle)	Description
<code>T1</code>	6	1	<code>ioe</code> disable timing.
<code>T2</code>	6	11	<code>clk_ena</code> disable timing.
<code>T3</code>	6	1	<code>clk_ena</code> enable timing.
<code>T4</code>	6	40	<code>ioe</code> enable timing.

`T1`, `T2`, `T3`, and `T4` can be increased based on your system requirement.



3.6. Hardware Implementation and Current Measurement

This design is implemented using the 10M50DAF484C6 device. You can implement this design using any Intel MAX 10 device. This design runs on the Intel MAX 10 Development Kit Board to show current and power relative between user mode and sleep mode.

The resource utilization of this design is as follows:

- 42,000 LEs (84% of total LEs)—gray counter top module utilizes most of the LEs in the device
- 33 I/O pins (9% of total pins)—covering 3 input pins and 30 output pins

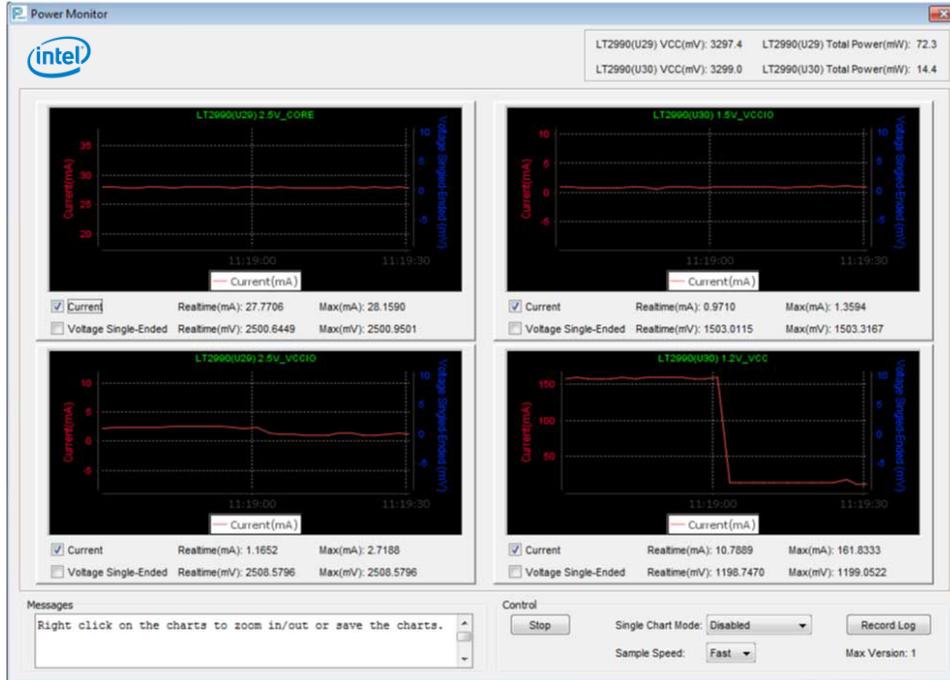
The current in this design is measured using a current monitor component (the Linear Technologies LTC 2990). The measured current is further processed by a pre-programmed design in a MAX II device. The measured current is shown on Intel FPGA power monitor GUI when the PowerMonitor.exe is launched. You will see a current monitor for each of the main supplies to the Intel MAX 10 device as follows:

- 2.5V_CORE⁽⁵⁾
- 2.5V_VCCIO
- 1.5V_VCCIO
- 1.2V_VCC

For design demonstration purpose, the push button is used for sleep control and the LEDs are used for sleep status. Thus, these signals have been inverted on the pin level. To enter sleep mode, press and hold the push button USER_PB0. To release the design to user mode, release the push button USER_PB0. LED0 indicates the sleep status of the device. LED0 is turned on when the device enters sleep mode and is turned off when the device is in user mode. During sleep mode, `gpio_pad_output` ports connecting to LED1–LED4 are tri-stated and then turned off.

⁽⁵⁾ This is 2.5V_VCCA.

Figure 12. Current Monitor for Each Supply



In sleep mode, all GCLK networks are gated and all output buffers are disabled.

Table 8. Comparison of Current and Power Consumption

Current and Power	User Mode	Sleep Mode
1.2V_ICC (mA)	160	11
2.5V_ICCA (mA)	28	28
1.5V_ICCIO (mA)	1.3	1.0
2.5V_ICCIO (mA)	2.7	1.2
Total power (mW)	270	88

The results show an approximate 93% reduction in the core current (1.2V_ICC) consumption and an approximate 56% reduction in I/O current (2.5V_ICCIO) consumption in sleep mode relative to user mode. The total power consumption reduction in this design in sleep mode is about 68%.



4. Intel MAX 10 Power Management User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
15.1	MAX 10 Power Management User Guide
15.0	MAX 10 Power Management User Guide
14.1	MAX 10 Power Management User Guide

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5. Document Revision History for the Intel MAX 10 Power Management User Guide

Document Version	Intel Quartus Prime Version	Changes
2018.07.04	18.0	<ul style="list-style-type: none"> Updated the <i>Power-On Reset Circuitry</i> section to include information that the individual power supply must reach the recommended operating range within the maximum power supply ramp time, t_{RAMP}. Beginning from the Intel Quartus Prime software version 18.0, the name of this IP core has been changed from Clock Control Block (ALTCLKCTRL) IP Core to ALTCLKCTRL Intel FPGA IP Core. Beginning from the Intel Quartus Prime software version 18.0, the name of this IP core has been changed from Altera GPIO Lite IP Core to GPIO Lite Intel FPGA IP Core. Beginning from the Intel Quartus Prime software version 18.0, the name of this IP core has been changed from Internal Oscillator IP Core to Internal Oscillator Intel FPGA IP Core. Updated Powerplay Early Power Estimator (EPE) to Early Power Estimator.

Date	Version	Changes
May 2017	2017.05.26	Updated the Hot-Socketing Feature Implementation section.
February 2017	2017.02.21	Rebranded as Intel.
May 2016	2016.05.02	<ul style="list-style-type: none"> Updated the I/O Pins Remain Tri-stated During Power Up section. Updated the Power Supplies Monitored and Not Monitored by the POR Circuitry section. Updated the information for the single-supply device in the Instant-On Power-Up Sequence Requirement table.
November 2015	2015.11.02	<ul style="list-style-type: none"> Added the Transient Current section. Changed instances of Quartus II to Quartus Prime.
February 2015	2015.02.09	Added the MAX 10 Power Management Controller Reference Design.
December 2014	2014.12.15	<ul style="list-style-type: none"> Updated the MAX 10 Power Management Overview section. Updated the Dual-Supply Device section to update details on power consumption for dual-supply devices. Updated the Power Supply Design section to include the maximum power consumption for each Intel MAX 10 single-supply device. Updated the Power Management Controller Scheme section to include updates on sleep mode.
September 2014	2014.09.22	Initial release.

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