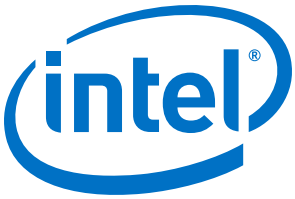

Intel® MAX® 10 General Purpose I/O User Guide

Updated for Intel® Quartus® Prime Design Suite: **20.1**

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Contents

1. Intel® MAX® 10 I/O Overview

The Intel® MAX® 10 general purpose I/O (GPIO) system consists of the I/O elements (IOE) and the GPIO Lite Intel FPGA IP. You can use GPIOs in non-transceiver general applications, memory-like interfaces, or LVDS applications.

- The IOEs contain bidirectional I/O buffers and I/O registers located in I/O banks around the periphery of the device.
- The GPIO Lite IP core supports the GPIO components and features, including double data rate I/O (DDIO), delay chains, I/O buffers, control signals, and clocking.

Related Information

- Intel MAX 10 I/O Architecture and Features on page 6
  Provides information about the architecture and features of the I/Os in Intel MAX 10 devices.
- Intel MAX 10 I/O Design Considerations on page 30
  Provides I/O design guidelines for Intel MAX 10 Devices.
- Intel MAX 10 I/O Implementation Guides on page 41
  Provides guides to implement I/Os in Intel MAX 10 Devices.
- GPIO Lite Intel FPGA IP References on page 46
  Lists the parameters and signals of GPIO Lite IP core for Intel MAX 10 Devices.
- Intel MAX 10 General Purpose I/O User Guide Archives on page 50
  Provides a list of user guides for previous versions of the GPIO Lite IP core.

1.1. Intel MAX 10 Devices I/O Resources Per Package

Table 1. Package Plan for Intel MAX 10 Single Power Supply Devices

Device	Package				
	Type	M153 153-pin MBGA	U169 169-pin UBGA	U324 324-pin UBGA	E144 144-pin EQFP
	Size	8 mm × 8 mm	11 mm × 11 mm	15 mm × 15 mm	22 mm × 22 mm
	Ball Pitch	0.5 mm	0.8 mm	0.8 mm	0.5 mm
10M02		112	130	246	101
10M04		112	130	246	101
10M08		112	130	246	101
10M16		—	130	246	101
10M25		—	—	—	101
10M40		—	—	—	101
10M50		—	—	—	101

Table 2. Package Plan for Intel MAX 10 Dual Power Supply Devices

Device	Package						
	Type	V36 36-pin WLCSP	V81 81-pin WLCSP	U324 324-pin UBGA	F256 256-pin FBGA	F484 484-pin FBGA	F672 672-pin FBGA
	Size	3 mm × 3 mm	4 mm × 4 mm	15 mm × 15 mm	17 mm × 17 mm	23 mm × 23 mm	27 mm × 27 mm
	Ball Pitch	0.4 mm	0.4 mm	0.8 mm	1.0 mm	1.0 mm	1.0 mm
10M02		27	—	160	—	—	—
10M04		—	—	246	178	—	—
10M08		—	56	246	178	250	—
10M16		—	—	246	178	320	—
10M25		—	—	—	178	360	—
10M40		—	—	—	178	360	500
10M50		—	—	—	178	360	500

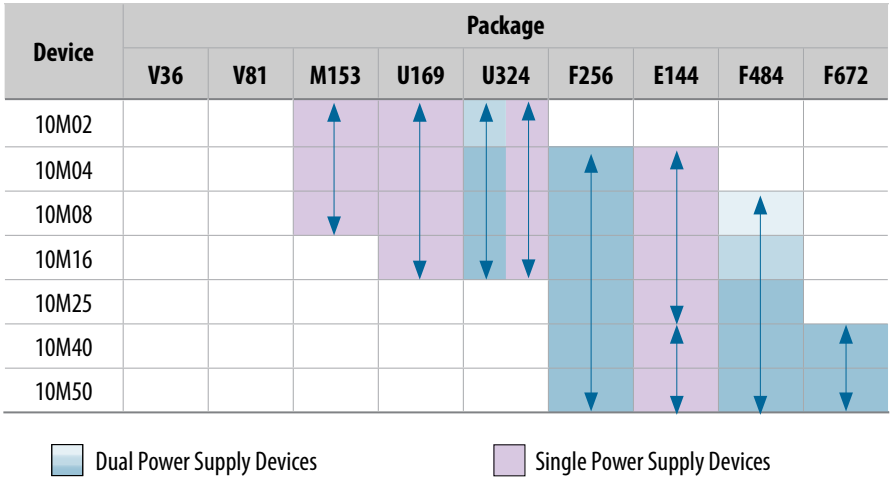
Related Information

Development Kits and Boards, *Intel MAX Design Tools*

1.2. Intel MAX 10 I/O Vertical Migration Support

Figure 1. Migration Capability Across Intel MAX 10 Devices

- The arrows indicate the migration paths. The devices included in each vertical migration path are shaded. Non-migratable devices are omitted. Some packages have several migration paths. Devices with lesser I/O resources in the same path have lighter shades.
- To achieve the full I/O migration across product lines in the same migration path, restrict I/Os usage to match the product line with the lowest I/O count.



Note: Before starting migration work, Intel recommends that you verify the pin migration compatibility through the **Pin Migration View** window in the Intel Quartus® Prime software Pin Planner. For example, not all Intel MAX 10 devices support 1.0 V I/O.

Related Information

Verifying Pin Migration Compatibility on page 44

2. Intel MAX 10 I/O Architecture and Features

The I/O system of Intel MAX 10 devices support various I/O standards. In the Intel MAX 10 devices, the I/O pins are located in I/O banks at the periphery of the devices. The I/O pins and I/O buffers have several programmable features.

Related Information

Intel MAX 10 I/O Overview on page 3

2.1. Intel MAX 10 I/O Standards Support

Intel MAX 10 devices support a wide range of I/O standards, including single-ended, voltage-referenced single-ended, and differential I/O standards.

Table 3. Supported I/O Standards in Intel MAX 10 Devices

The voltage-referenced I/O standards are not supported in the following I/O banks of these device packages:

- All I/O banks of V36 package of 10M02.
- All I/O banks of V81 package of 10M08.
- Banks 1A and 1B of E144 package of 10M50.

I/O Standard	Type	Device Support	Direction		Application	Standard Support
			Input	Output		
3.3 V LVTTL/3.3 V LVCMOS	Single-ended	All	Yes	Yes	General purpose	JESD8-B
3.0 V LVTTL/3.0 V LVCMOS	Single-ended	All	Yes	Yes	General purpose	JESD8-B
2.5 V LVCMOS	Single-ended	All	Yes	Yes	General purpose	JESD8-5
1.8 V LVCMOS	Single-ended	All	Yes	Yes	General purpose	JESD8-7
1.5 V LVCMOS	Single-ended	All	Yes	Yes	General purpose	JESD8-11
1.2 V LVCMOS	Single-ended	All	Yes	Yes	General purpose	JESD8-12
1.0 V LVCMOS(1)	Single-ended	Specific devices(1)	Yes	Yes	General purpose	—
3.0 V PCI	Single-ended	All	Yes	Yes	General purpose	PCI Rev. 2.2
3.3 V Schmitt Trigger	Single-ended	All	Yes	—	General purpose	—

continued...

(1) Available only for the following devices: 10M02SCU324C8G, 10M04SCU324C8G, 10M08SCU324C8G, 10M16SCU324C8G, 10M16SCU169C8G, 10M16SAU169C8G, 10M16DCF484C8G, 10M16DAF484C8G, 10M25DCF484C8G, 10M25DAF484C8G, 10M40DCF484C8G, 10M40DAF484C8G, 10M50DCF484C8G, and 10M50DAF484C8G.

I/O Standard	Type	Device Support	Direction		Application	Standard Support
			Input	Output		
2.5 V Schmitt Trigger	Single-ended	All	Yes	—	General purpose	—
1.8 V Schmitt Trigger	Single-ended	All	Yes	—	General purpose	—
1.5 V Schmitt Trigger	Single-ended	All	Yes	—	General purpose	—
SSTL-2 Class I	Voltage-referenced	All	Yes	Yes	DDR1	JESD8-9B
SSTL-2 Class II	Voltage-referenced	All	Yes	Yes	DDR1	JESD8-9B
SSTL-18 Class I	Voltage-referenced	All	Yes	Yes	DDR2	JESD8-15
SSTL-18 Class II	Voltage-referenced	All	Yes	Yes	DDR2	JESD8-15
SSTL-15 Class I	Voltage-referenced	All	Yes	Yes	DDR3	—
SSTL-15 Class II	Voltage-referenced	All	Yes	Yes	DDR3	—
SSTL-15(2)	Voltage-referenced	All	Yes	Yes	DDR3	JESD79-3D
SSTL-135(2)	Voltage-referenced	All	Yes	Yes	DDR3L	—
1.8 V HSTL Class I	Voltage-referenced	All	Yes	Yes	DDR II+, QDR II+, and RLDRAM 2	JESD8-6
1.8 V HSTL Class II	Voltage-referenced	All	Yes	Yes	DDR II+, QDR II+, and RLDRAM 2	JESD8-6
1.5 V HSTL Class I	Voltage-referenced	All	Yes	Yes	DDR II+, QDR II+, QDR II, and RLDRAM 2	JESD8-6
1.5 V HSTL Class II	Voltage-referenced	All	Yes	Yes	DDR II+, QDR II+, QDR II, and RLDRAM 2	JESD8-6
1.2 V HSTL Class I	Voltage-referenced	All	Yes	Yes	General purpose	JESD8-16A
1.2 V HSTL Class II	Voltage-referenced	All	Yes	Yes	General purpose	JESD8-16A
HSUL-12(2)	Voltage-referenced	All	Yes	Yes	LPDDR2	—
Differential SSTL-2 Class I and II	Differential	All	Yes(3)	Yes(4)	DDR1	JESD8-9B
Differential SSTL-18 Class I and Class II	Differential	All	Yes(3)	Yes(4)	DDR2	JESD8-15

continued...

(2) Available in Intel MAX 10 16, 25, 40, and 50 devices only.

(3) The inputs treat differential inputs as two single-ended inputs and decode only one of them.

(4) The outputs use two single-ended output buffers with the second output buffer programmed as inverted.

I/O Standard	Type	Device Support	Direction		Application	Standard Support
			Input	Output		
Differential SSTL-15 Class I and Class II	Differential	All	Yes(3)	Yes(4)	DDR3	—
Differential SSTL-15	Differential	All	Yes(3)	Yes(4)	DDR3	JESD79-3D
Differential SSTL-135	Differential	All	Yes(3)	Yes(4)	DDR3L	—
Differential 1.8 V HSTL Class I and Class II	Differential	All	Yes(3)	Yes(4)	DDR II+, QDR II+, and RLDRAM 2	JESD8-6
Differential 1.5 V HSTL Class I and Class II	Differential	All	Yes(3)	Yes(4)	DDR II+, QDR II+, QDR II, and RLDRAM 2	JESD8-6
Differential 1.2 V HSTL Class I and Class II	Differential	All	Yes(3)	Yes(4)	General purpose	JESD8-16A
Differential HSUL-12	Differential	All	Yes(3)	Yes(4)	LPDDR2	—
LVDS (dedicated)(5)	Differential	All	Yes	Yes	—	ANSI/TIA/EIA-644
LVDS (emulated, external resistors)	Differential	All	—	Yes	—	ANSI/TIA/EIA-644
Mini-LVDS (dedicated)(5)	Differential	All	—	Yes	—	—
Mini-LVDS (emulated, external resistor)	Differential	Dual supply devices	—	Yes	—	—
RSDS (dedicated)(5)	Differential	All	—	Yes	—	—
RSDS (emulated, external resistor, 1R)	Differential	Dual supply devices	—	Yes	—	—
RSDS (emulated, external resistors, 3R)	Differential	All	—	Yes	—	—
PPDS (dedicated)(5)	Differential	Dual supply devices	—	Yes	—	—
PPDS (emulated, external resistor)	Differential	Dual supply devices	—	Yes	—	—
LVPECL	Differential	All	Yes	—	—	—
Bus LVDS	Differential	All	Yes	Yes(6)	—	—
TMDS	Differential	Dual supply devices	Yes	—	—	—

continued...

(5) You can use dedicated LVDS transmitters only on the bottom I/O banks. You can use LVDS receivers on all I/O banks.

(6) The outputs use two single-ended output buffers with the second output buffer programmed as inverted. A single series resistor is required.

I/O Standard	Type	Device Support	Direction		Application	Standard Support
			Input	Output		
Sub-LVDS	Differential	Dual supply devices	Yes	Yes(7)	—	—
SLVS	Differential	Dual supply devices	Yes	Yes(8)	—	—
HiSpi	Differential	Dual supply devices	Yes	—	—	—

Related Information

- Intel MAX 10 I/O Buffers on page 17
  Provides more information about available I/O buffer types and supported I/O standards.
- LVDS Transmitter I/O Termination Schemes, MAX 10 High-Speed LVDS I/O User Guide
  Provides the required external termination schemes and resistor values for the emulated LVDS, Sub-LVDS, SLVS, emulated RSDS, emulated mini-LVDS, and emulated PPDS I/O standards.

2.1.1. Intel MAX 10 I/O Standards Voltage and Pin Support

Table 4. Intel MAX 10 I/O Standards Voltage Levels and Pin Support

Note: The I/O standards that each pin type supports depends on the I/O standards that the pin's I/O bank supports. For example, only the bottom I/O banks support the LVDS (dedicated) I/O standard. You can use the LVDS (dedicated) I/O standard for the PLL_CLKOUT pin only if the pin is available in your device's bottom I/O banks. To determine the pin's I/O bank locations for your device, check your device's pin out file.

I/O Standard	V_{CCIO} (V)		V_{REF} (V)	Pin Type Support				
	Input	Output		PLL_CLKOUT	MEM_CLK	CLK	DQS	User I/O
3.3 V LVTTL/3.3 V LVCMOS	3.3/3.0/2.5	3.3	—	Yes	Yes	Yes	Yes	Yes
3.0 V LVTTL/3.0 V LVCMOS	3.0/2.5	3.0	—	Yes	Yes	Yes	Yes	Yes
2.5 V LVCMOS	3.0/2.5	2.5	—	Yes	Yes	Yes	Yes	Yes
1.8 V LVCMOS	1.8/1.5	1.8	—	Yes	Yes	Yes	Yes	Yes
1.5 V LVCMOS	1.8/1.5	1.5	—	Yes	Yes	Yes	Yes	Yes
1.2 V LVCMOS	1.2	1.2	—	Yes	Yes	Yes	Yes	Yes
1.0 V LVCMOS	1.0(9)	1.0(9)	—	—	—	Yes	—	Yes

continued...

(7) Requires external termination resistors.

(8) The outputs uses two single-ended output buffers as emulated differential outputs. Requires external termination resistors.

I/O Standard	V_{CCIO} (V)		V_{REF} (V)	Pin Type Support				
	Input	Output		PLL_CLKOUT	MEM_CLK	CLK	DQS	User I/O
3.0 V PCI	3.0	3.0	—	Yes	Yes	Yes	Yes	Yes
3.3 V Schmitt Trigger	3.3	—	—	—	—	Yes	Yes(10)	Yes
2.5 V Schmitt Trigger	2.5	—	—	—	—	Yes	Yes(10)	Yes
1.8 V Schmitt Trigger	1.8	—	—	—	—	Yes	Yes(10)	Yes
1.5 V Schmitt Trigger	1.5	—	—	—	—	Yes	Yes(10)	Yes
SSTL-2 Class I	2.5	2.5	1.25	Yes	Yes	Yes	Yes	Yes
SSTL-2 Class II	2.5	2.5	1.25	Yes	Yes	Yes	Yes	Yes
SSTL-18 Class I	1.8	1.8	0.9	Yes	Yes	Yes	Yes	Yes
SSTL-18 Class II	1.8	1.8	0.9	Yes	Yes	Yes	Yes	Yes
SSTL-15 Class I	1.5	1.5	0.75	Yes	Yes	Yes	Yes	Yes
SSTL-15 Class II	1.5	1.5	0.75	Yes	Yes	Yes	Yes	Yes
SSTL-15	1.5	1.5	0.75	Yes	Yes	Yes	Yes	Yes
SSTL-135	1.35	1.35	0.675	Yes	Yes	Yes	Yes	Yes
1.8 V HSTL Class I	1.8	1.8	0.9	Yes	Yes	Yes	Yes	Yes
1.8 V HSTL Class II	1.8	1.8	0.9	Yes	Yes	Yes	Yes	Yes
1.5 V HSTL Class I	1.5	1.5	0.75	Yes	Yes	Yes	Yes	Yes
1.5 V HSTL Class II	1.5	1.5	0.75	Yes	Yes	Yes	Yes	Yes
1.2 V HSTL Class I	1.2	1.2	0.6	Yes	Yes	Yes	Yes	Yes
1.2 V HSTL Class II	1.2	1.2	0.6	Yes	Yes	Yes	Yes	Yes
HSUL-12	1.2	1.2	0.6	Yes	Yes	Yes	Yes	Yes
Differential SSTL-2 Class I and II	—	2.5	—	Yes	Yes	—	Yes	—
	2.5	—	1.25	—	—	Yes	Yes	—
Differential SSTL-18 Class I and Class II	—	1.8	—	Yes	Yes	—	Yes	—
	1.8	—	0.9	—	—	Yes	Yes	—
Differential SSTL-15 Class I and Class II	—	1.5	—	Yes	Yes	—	Yes	—
	1.5	—	0.75	—	—	Yes	Yes	—
Differential SSTL-15	—	1.5	—	Yes	Yes	—	Yes	—
	1.5	—	0.75	—	—	Yes	Yes	—
Differential SSTL-135	—	1.35	—	Yes	Yes	—	Yes	—
	1.35	—	0.675	—	—	Yes	Yes	—
Differential 1.8 V HSTL Class I and Class II	—	1.8	—	Yes	Yes	—	Yes	—

continued...

(9) Not supported on bank 1B and bank 8.

(10) Bidirectional—use Schmitt Trigger input with LVTTL output.

I/O Standard	V_{CCIO} (V)		V_{REF} (V)	Pin Type Support				
	Input	Output		PLL_CLKOUT	MEM_CLK	CLK	DQS	User I/O
	1.8	—	0.9	—	—	Yes	Yes	—
Differential 1.5 V HSTL Class I and Class II	—	1.5	—	Yes	Yes	—	Yes	—
	1.5	—	0.75	—	—	Yes	Yes	—
Differential 1.2 V HSTL Class I and Class II	—	1.2	—	Yes	Yes	—	Yes	—
	1.2	—	0.6	—	—	Yes	Yes	—
Differential HSUL-12	—	1.2	—	Yes	Yes	—	Yes	—
	1.2	—	0.6	—	—	Yes	Yes	—
LVDS (dedicated)	2.5	2.5	—	Yes	Yes	Yes	—	Yes
LVDS (emulated, external resistors)	—	2.5	—	Yes	Yes	—	—	Yes
Mini-LVDS (dedicated)	—	2.5	—	Yes	Yes	—	—	Yes
Mini-LVDS (emulated, external resistor)	—	2.5	—	Yes	Yes	—	—	Yes
RSDS (dedicated)	—	2.5	—	Yes	Yes	—	—	Yes
RSDS (emulated, external resistor, 1R)	—	2.5	—	Yes	Yes	—	—	Yes
RSDS (emulated, external resistors, 3R)	—	2.5	—	Yes	Yes	—	—	Yes
PPDS (dedicated)	—	2.5	—	Yes	Yes	—	—	Yes
PPDS (emulated, external resistor)	—	2.5	—	Yes	Yes	—	—	Yes
LVPECL	2.5	—	—	—	—	Yes	—	—
Bus LVDS	2.5	2.5	—	—	—	—	—	Yes
TMDS	2.5	—	—	—	—	Yes	—	Yes
Sub-LVDS	2.5	1.8	—	Yes	Yes	Yes	—	Yes
SLVS	2.5	2.5	—	Yes	Yes	Yes	—	Yes
HiSpi	2.5	—	—	—	—	Yes	—	Yes

Related Information

- MAX 10 Device Pin-Out Files
- Intel MAX 10 I/O Standards Support on page 6
- Intel MAX 10 I/O Banks Locations on page 14
- Intel MAX 10 LVDS SERDES I/O Standards Support
- Intel MAX 10 High-Speed LVDS I/O Location

2.2. Intel MAX 10 I/O Elements

The Intel MAX 10 I/O elements (IOEs) contain a bidirectional I/O buffer and five registers for registering input, output, output-enable signals, and complete embedded bidirectional single data rate (SDR) and double data rate (DDR) transfer.

The I/O buffers are grouped into groups of four I/O modules per I/O bank:

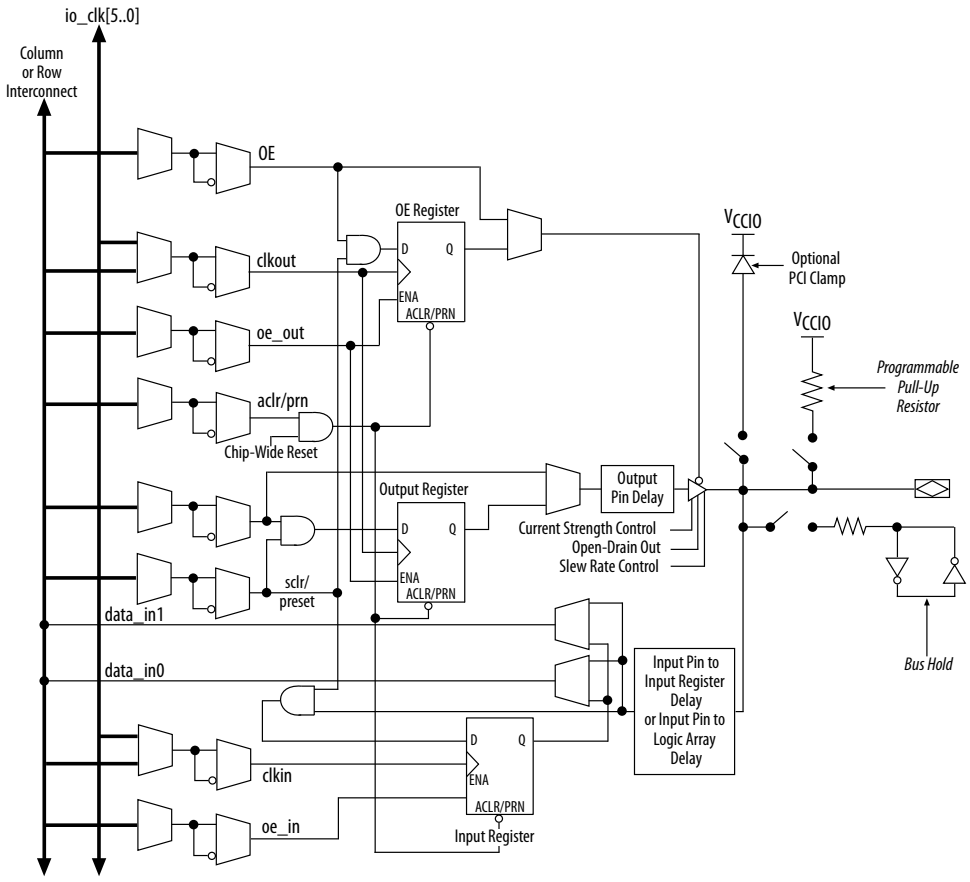
- The Intel MAX 10 devices share the user I/O pins with the VREF, RUP, RDN, CLKPIN, PLLCLKOUT, configuration, and test pins.
- Schmitt Trigger input buffer is available in all I/O buffers.
- When the Intel MAX 10 device is blank or erased, the I/Os are tri-stated.

Each IOE contains one input register, two output registers, and two output-enable (OE) registers:

- The two output registers and two OE registers are used for DDR applications.
- You can use the input registers for fast setup times and output registers for fast clock-to-output times.
- You can use the OE registers for fast clock-to-output enable times.

You can use the IOEs for input, output, or bidirectional data paths. The I/O pins support various single-ended and differential I/O standards.

Figure 2. IOE Structure in Bidirectional Configuration



Related Information

- MAX 10 Power Management User Guide
  Provides more information about the I/O buffers in different power cycles and hot socketing.
- Schmitt-Trigger Input Buffer on page 17

2.2.1. Intel MAX 10 I/O Banks Architecture

The I/O elements are located in a group of four modules per I/O bank:

- High speed DDR3 I/O banks—supports various I/O standards and protocols including DDR3. These I/O banks are available only on the right side of the device.
- High speed I/O banks—supports various I/O standards and protocols except DDR3. These I/O banks are available on the top, left, and bottom sides of the device.
- Low speed I/O banks—lower speeds I/O banks that are located at the top left side of the device.

For more information about I/O pins support, refer to the pinout files for your device.

Related Information

MAX 10 Device Pin-Out Files

2.2.2. Intel MAX 10 I/O Banks Performance

The performance of the I/O banks differs for different I/O standards and I/O bank types. You must ensure that the frequency you specified passes timing check in the Intel Quartus Prime software.

The low speed I/O banks have lower maximum frequency than other I/O banks because of longer propagation delays. However, the delays do not affect the timing parameters such as slew rate, rise time, and fall time.

For details about the location of the high speed and low speed I/O banks, refer to the device pinout files.

Related Information

- High-Speed I/O Specifications
  Provides the performance information for different I/O standards in the low-speed and high-speed I/O banks.
- IBIS Models for Intel Devices
- SPICE Models for Altera Devices

2.2.3. Intel MAX 10 I/O Banks Locations

The I/O banks are located at the periphery of the device.

For more details about the modular I/O banks available in each device package, refer to the relevant device pin-out file.

Figure 3. I/O Banks for 10M02 Devices (Except Single Power Supply U324 Package)

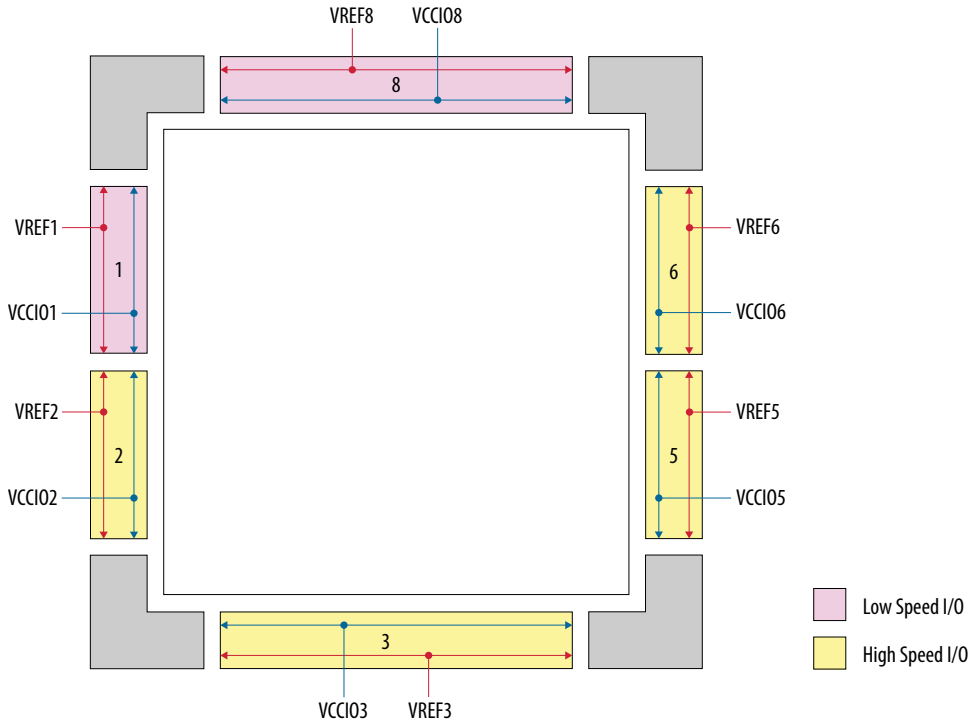


Figure 4. I/O Banks for 10M02 (Single Power Supply U324 Package), 10M04, and 10M08 Devices

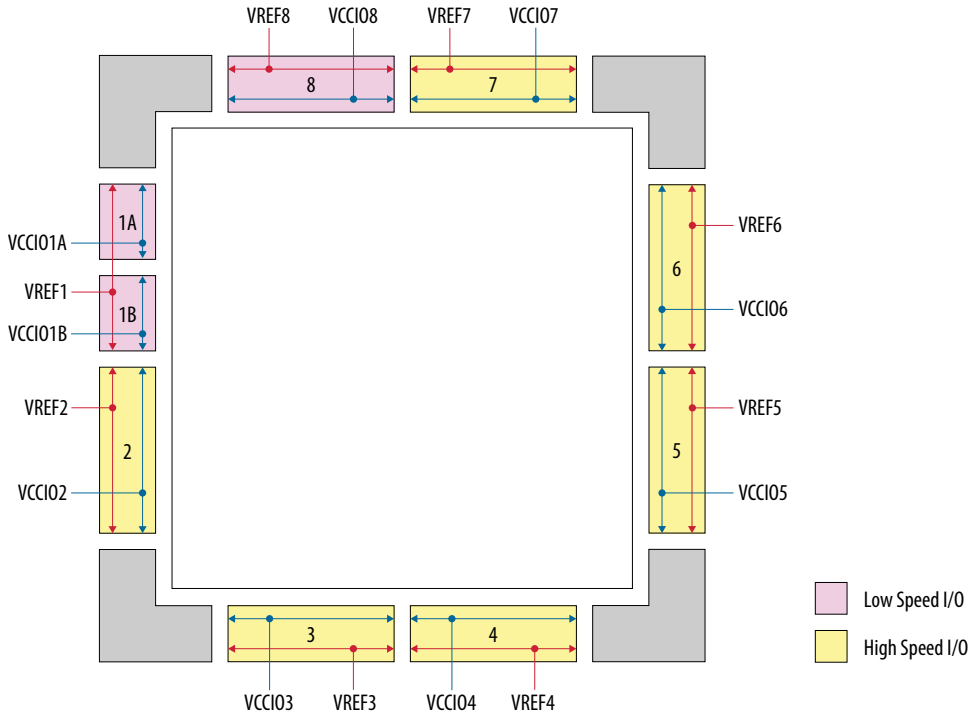
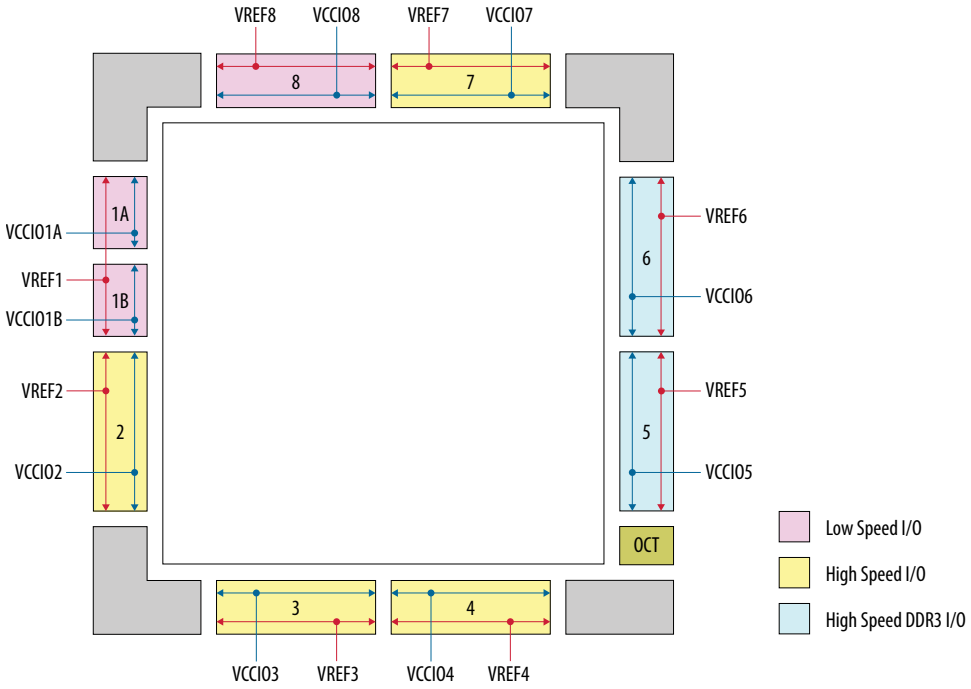


Figure 5. I/O Banks for 10M16, 10M25 , 10M40, and 10M50 Devices



Related Information

- MAX 10 Device Pin-Out Files
- High-Speed I/O Specifications
  Provides the performance information for different I/O standards in the low-speed and high-speed I/O banks.

2.3. Intel MAX 10 I/O Buffers

The general purpose I/Os (GPIOs) in Intel MAX 10 devices consist of LVDS I/O and DDR I/O buffers.

Table 5. Types of GPIO Buffers in Intel MAX 10 Devices

LVDS I/O Buffers	DDR I/O Buffers
• Support differential and single-ended I/O standards. • Available only on I/O banks at the bottom side of the device. • For LVDS, the bottom I/O banks support LVDS transmitter, emulated LVDS transmitter, and LVDS receiver buffers.	• Support differential and single-ended I/O standards. • Available on I/O banks at the left, right, and top sides of the device. • For LVDS, the DDR I/O buffers support only LVDS receiver and emulated LVDS transmitter buffers. • For DDR, only the DDR I/O buffers on the right side of the device supports DDR3 external memory interfaces. DDR3 support is only available for Intel MAX 10 16, 25, 40, and 50 devices.

Related Information

- Intel MAX 10 I/O Standards Support on page 6
- LVDS Transmitter I/O Termination Schemes, MAX 10 High-Speed LVDS I/O User Guide
  Provides the required external termination schemes and resistor values for the emulated LVDS, Sub-LVDS, SLVS, emulated RSDS, emulated mini-LVDS, and emulated PPDS I/O standards.

2.3.1. Schmitt-Trigger Input Buffer

The Intel MAX 10 devices feature selectable Schmitt trigger input buffer on all I/O banks.

The Schmitt trigger input buffer has similar V_{IL} and V_{IH} as the LVTTL I/O standard but with better noise immunity. The Schmitt trigger input buffers are used as default input buffers during configuration mode.

Related Information

MAX 10 Device Datasheet

2.3.2. Programmable I/O Buffer Features

The Intel MAX 10 I/O buffers support a range of programmable features. These features increase the flexibility of I/O utilization and provide an alternative to reduce the usage of external discrete components such as a pull-up resistor and a diode.

Table 6. Summary of Supported Intel MAX 10 Programmable I/O Buffer Features and Settings

Feature	Setting	Condition	Assignment Name	Supported I/O Standards
Open Drain	On, Off (default)	To enable this feature, use the OPNDRN primitive.	—	• 3.0 V and 3.3 V LVTTL • 1.0 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, and 3.3 V LVCMOS • SSTL-2, SSTL-18, SSTL-15, and SSTL-135

continued...

Feature	Setting	Condition	Assignment Name	Supported I/O Standards
				• 1.2 V, 1.5 V, and 1.8 V HSTL • HSUL-12 • 3.0 V PCI
Bus-Hold	On, Off (default)	Disabled if you use the weak pull-up resistor feature.	Enable Bus-Hold Circuitry	• 3.0 V and 3.3 V LVTTL • 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, and 3.3 V LVCMOS • SSTL-2, SSTL-18, SSTL-15, and SSTL-135 • 1.2 V, 1.5 V, and 1.8 V HSTL • HSUL-12 • 3.0 V PCI
Pull-up Resistor	On, Off (default)	Disabled if you use the bus-hold feature.	Weak Pull-Up Resistor	
Slew Rate Control	0 (Slow), 1 (Medium), 2 (Fast). Default is 2.	Disabled if you use OCT.	Slew Rate	• 3.0 V LVTTL • 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.0 V LVCMOS • SSTL-2, SSTL-18, and SSTL-15 • 1.2 V, 1.5 V, and 1.8 V HSTL • Differential SSTL-2, Differential SSTL-18, and Differential SSTL-15 • Differential 1.2 V, 1.5 V, and 1.8 V HSTL
PCI Clamp Diode	On (default for input pins), Off (default for output pins, except 3.0 V PCI)	—	PCI I/O	• 3.0 V and 3.3 V LVTTL • 2.5 V, 3.0 V, and 3.3 V LVCMOS • 3.0 V PCI • 2.5 V, 3.0 V, and 3.3 V Schmitt Trigger
Pre-Emphasis	0 (disabled), 1 (enabled). Default is 1.	—	Programmable Pre-emphasis	• LVDS • RSDS • PPDS • Mini-LVDS
Differential Output Voltage	0 (low), 1 (medium), 2 (high). Default is 2.	—	Programmable Differential Output Voltage (V_{OD})	

2.3.2.1. Programmable Open Drain

The optional open-drain output for each I/O pin is equivalent to an open collector output. If it is configured as an open drain, the logic value of the output is either high-Z or logic low.

Use an external resistor to pull the signal to a logic high.

2.3.2.2. Programmable Bus Hold

Each I/O pin provides an optional bus-hold feature that is active only after configuration. When the device enters user mode, the bus-hold circuit captures the value that is present on the pin by the end of the configuration.

The bus-hold circuitry holds the signal on an I/O pin at its last-driven state until the next input signal is present. Because of this, you do not require an external pull-up or pull-down resistor to hold a signal level when the bus is tri-stated.

User I/O pins can be in either the default weak pull-up state or tri-state during configuration. With the bus-hold feature, if you do not drive the I/O pin externally when it enters user mode from configuration mode:

- The I/O pin state is weak pull-up during configuration—the I/O pin retains the high value when the device enters user mode.
- The I/O pin is tri-stated during configuration—the I/O pin value can be high or low when the device enters user mode.

For each I/O pin, you can individually specify that the bus-hold circuitry pulls non-driven pins away from the input threshold voltage—where noise can cause unintended high-frequency switching. To prevent over-driving signals, the bus-hold circuitry drives the voltage level of the I/O pin lower than the V_{CCIO} level.

If you enable the bus-hold feature, you cannot use the programmable pull-up option. To configure the I/O pin for differential signals, disable the bus-hold feature.

2.3.2.3. Programmable Pull-Up Resistor

Each I/O pin provides an optional programmable pull-up resistor during user mode. The pull-up resistor weakly holds the I/O to the V_{CCIO} level.

If you enable the weak pull-up resistor, you cannot use the bus-hold feature.

2.3.2.4. Programmable Current Strength

You can use the programmable current strength to mitigate the effects of high signal attenuation that is caused by a long transmission line or a legacy backplane.

Table 7. Programmable Current Strength Settings for Intel MAX 10 Devices

The output buffer for each Intel MAX 10 device I/O pin has a programmable current strength control for the I/O standards listed in this table.

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA) (Default setting in bold)
3.3 V LVCMOS	**2**
3.3 V LVTTL	**8**, 4
3.0 V LVTTL/3.0 V LVCMOS	16, **12**, 8, 4
2.5 V LVTTL/2.5 V LVCMOS	16, **12**, 8, 4
1.8 V LVTTL/1.8 V LVCMOS	16, **12**, 10, 8, 6, 4, 2
1.5 V LVCMOS	16, **12**, 10, 8, 6, 4, 2
1.2 V LVCMOS	12, 10, **8**, 6, 4, 2
SSTL-2 Class I	12, **8**
SSTL-2 Class II	**16**
SSTL-18 Class I	12, 10, **8**
SSTL-18 Class II	**16**, 12
SSTL-15 Class I	12, 10, **8**
SSTL-15 Class II	**16**
1.8 V HSTL Class I	12, 10, **8**
1.8 V HSTL Class II	**16**
1.5 V HSTL Class I	12, 10, **8**

continued...

I/O Standard	I_{OH} / I_{OL} Current Strength Setting (mA) (Default setting in bold)
1.5 V HSTL Class II	**16**
1.2 V HSTL Class I	12, 10, **8**
1.2 V HSTL Class II	**14**
BLVDS	**16**, 12, 8
SLVS	**16**, 12, 8
Sub-LVDS	**12**, 8, 4

Note: Intel recommends that you perform IBIS or SPICE simulations to determine the best current strength setting for your specific application.

Related Information

- IBIS Models for Intel Devices
- SPICE Models for Altera Devices

2.3.2.5. Programmable Output Slew Rate Control

You have the option of three settings for programmable slew rate control—0, 1, and 2 with 2 as the default setting. Setting 0 is the slow slew rate and 2 is the fast slew rate.

- Fast slew rate—provides high-speed transitions for high-performance systems.
- Slow slew rate—reduces system noise and crosstalk but adds a nominal delay to the rising and falling edges.

Table 8. Programmable Output Slew Rate Control for Intel MAX 10 Devices

This table lists the single-ended I/O standards and current strength settings that support programmable output slew rate control. For I/O standards and current strength settings that do not support programmable slew rate control, the default slew rate setting is 2 (fast slew rate).

I/O Standard	I_{OH} / I_{OL} Current Strength Supporting Slew Rate Control
3.0 V LVTTL/3.0 V LVCMOS	16, 12, 8
2.5 V LVTTL/2.5 V LVCMOS	16, 12, 8
1.8 V LVTTL/1.8 V LVCMOS	16, 12, 8
1.5 V LVCMOS	16, 12, 10, 8
1.2 V LVCMOS	12, 10, 8
SSTL-2 Class I	12, 8
SSTL-2 Class II	16
SSTL-18 Class I	12, 10, 8
SSTL-18 Class II	16, 12
SSTL-15 Class I	12, 10, 8
SSTL-15 Class II	16
1.8 V HSTL Class I	12, 10, 8
1.8 V HSTL Class II	16

continued...

I/O Standard	I_{OH} / I_{OL} Current Strength Supporting Slew Rate Control
1.5 V HSTL Class I	12, 10, 8
1.5 V HSTL Class II	16
1.2 V HSTL Class I	12, 10, 8
1.2 V HSTL Class II	14

You can specify the slew rate on a pin-by-pin basis because each I/O pin contains a slew rate control. The slew rate control affects both the rising and falling edges.

Note: Intel recommends that you perform IBIS or SPICE simulations to determine the best slew rate setting for your specific application.

2.3.2.6. Programmable IOE Delay

You can activate the programmable IOE delays to ensure zero hold times, minimize setup times, increase clock-to-output times, or delay the clock input signal. This feature helps read and write timing margins because it minimizes the uncertainties between signals in the bus.

Each pin can have a different delay value to ensure signals within a bus have the same delay going into or out of the device.

Table 9. Programmable Delay Chain

Programmable Delays	Intel Quartus Prime Logic Option
Input pin-to-logic array delay	Input delay from pin to internal cells
Input pin-to-input register delay	Input delay from pin to input register
Output pin delay	Delay from output register to output pin
Dual-purpose clock input pin delay	Input delay from dual-purpose clock pin to fan-out destinations

There are two paths in the IOE for an input to reach the logic array. Each of the two paths can have a different delay. This allows you to adjust delays from the pin to the internal logic element (LE) registers that reside in two different areas of the device. You must set the two combinational input delays with the input delay from pin to internal cells logic option in the Intel Quartus Prime software for each path. If the pin uses the input register, one of the delays is disregarded and the delay is set with the input delay from pin to input register logic option in the Intel Quartus Prime software.

The IOE registers in each I/O block share the same source for the preset or clear features. You can program preset or clear for each individual IOE, but you cannot use both features simultaneously. You can also program the registers to power-up high or low after configuration is complete. If programmed to power-up low, an asynchronous clear can control the registers. If programmed to power-up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of the active-low input of another device upon power up. If one register in an IOE uses a preset or clear signal, all registers in the IOE must use that same signal if they require preset or clear. Additionally, a synchronous reset signal is available for the IOE registers.

Related Information

- MAX 10 Device Datasheet

- Timing Closure and Optimization chapter, Volume 2: Design Implementation and Optimization, Intel Quartus Prime Handbook
  Provides more information about the input and output pin delay settings.

2.3.2.7. PCI Clamp Diode

The Intel MAX 10 devices are equipped with optional PCI clamp diode that you can enable for the input and output of each I/O pin. You can use this diode to protect I/O pins during voltage overshoot.

The PCI clamp diode is available in the Intel Quartus Prime software for the following I/O standards:

- 3.3 V LVTTL/3.3 V LVCMOS
- 3.0 V LVTTL/3.0 V LVCMOS
- 2.5 V LVTTL/2.5 V LVCMOS
- 3.0 V PCI
- 3.3 V Schmitt Trigger
- 2.5 V Schmitt Trigger

Dual-purpose configuration pins support the diode in user mode if you do not use the pins as configuration pins for the selected configuration scheme. The dedicated configuration pins do not support the on-chip diode.

Related Information

- Guidelines: Enable Clamp Diode for LVTTL/LVCMOS Input Buffers on page 31
- Guideline: Use Internal PCI Clamp Diode on the Pin, *AN 447: Interfacing Intel FPGA Devices with 3.3/3.0/2.5 V LVTTL/LVCMOS I/O Systems*

2.3.2.8. Programmable Pre-Emphasis

The differential output voltage (V_{OD}) setting and the output impedance of the driver set the output current limit of a high-speed transmission signal. At a high frequency, the slew rate may not be fast enough to reach the full V_{OD} level before the next edge, producing pattern-dependent jitter. Pre-emphasis momentarily boosts the output current during switching to increase the output slew rate.

Pre-emphasis increases the amplitude of the high-frequency component of the output signal. This increase compensates for the frequency-dependent attenuation along the transmission line.

The overshoot introduced by the extra current occurs only during change of state switching. This overshoot increases the output slew rate but does not ring, unlike the overshoot caused by signal reflection. The amount of pre-emphasis required depends on the attenuation of the high-frequency component along the transmission line.

Figure 6. LVDS Output with Programmable Pre-Emphasis

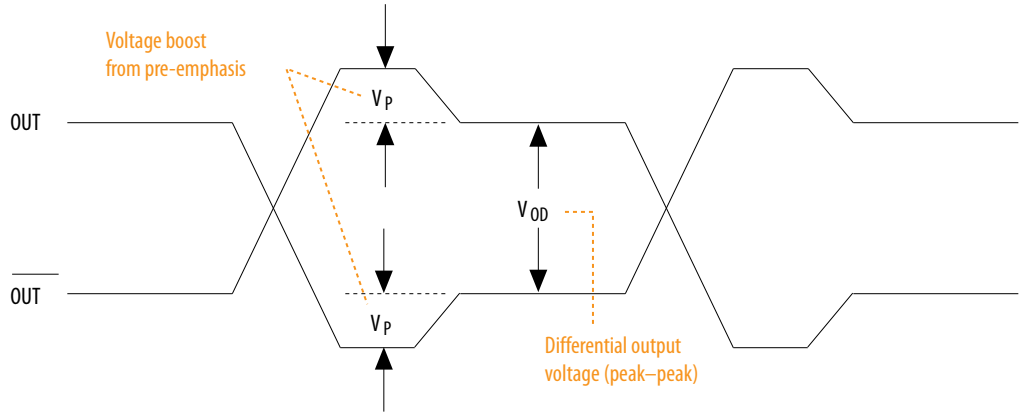


Table 10. Intel Quartus Prime Software Assignment for Programmable Pre-Emphasis

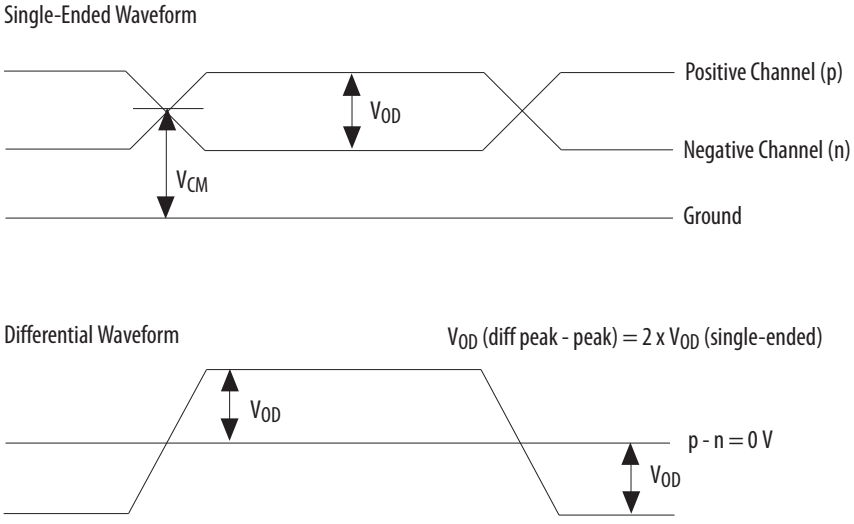
Field	Assignment
To	tx_out
Assignment name	Programmable Pre-emphasis
Allowed values	0 (disabled), 1 (enabled). Default is 1.

2.3.2.9. Programmable Differential Output Voltage

The programmable V_{OD} settings allow you to adjust the output eye opening to optimize the trace length and power consumption. A higher V_{OD} swing improves voltage margins at the receiver end, and a smaller V_{OD} swing reduces power consumption.

Figure 7. Differential V_{OD}

This figure shows the V_{OD} of the differential LVDS output.



You can statically adjust the V_{OD} of the differential signal by changing the V_{OD} settings in the Intel Quartus Prime software Assignment Editor.

Table 11. Intel Quartus Prime Software Assignment Editor—Programmable V_{OD}

Field	Assignment
To	tx_out
Assignment name	Programmable Differential Output Voltage (V_{OD})
Allowed values	0 (low), 1 (medium), 2 (high). Default is 2.

2.3.2.10. Programmable Emulated Differential Output

The Intel MAX 10 devices support emulated differential output where a pair of single-ended output drives out a differential signal.

The emulated differential output feature is supported for the following I/O standards:

- Differential SSTL-2 Class I and II
- Differential SSTL-18 Class I and II
- Differential SSTL-15 Class I and II
- Differential SSTL-15
- Differential SSTL-135
- Differential 1.8 V HSTL Class I and II
- Differential 1.5 V HSTL Class I and II
- Differential 1.2 V HSTL Class I and II
- Differential HSUL-12
- LVDS 3R
- Mini-LVDS 3R
- PPDS 3R
- RSDS 1R and 3R
- BLVDS
- SLVS
- Sub-LVDS

2.3.2.11. Programmable Dynamic Power Down

The Intel MAX 10 16, 25, 40, and 50 devices feature programmable dynamic power down for several I/O standards to reduce the static power consumption.

In these devices, you can apply the programmable dynamic power down feature to the I/O buffers for the following I/O standards:

- Input buffer—SSTL, HSTL, HSUL, LVDS
- Output buffer—LVDS

Related Information

MAX 10 Power Management User Guide
Provides more information about using the programmable dynamic power down feature.

2.4. I/O Standards Termination

Voltage-referenced and differential I/O standards requires different termination schemes.

According to JEDEC standards, the following I/O standards do not specify a recommended termination scheme:

- 3.3-V LVTTL
- 3.0 V LVTTL/3.0 V LVCMOS
- 2.5 V LVTTL/2.5 V LVCMOS
- 1.8 V LVTTL/1.8 V LVCMOS
- 1.5 V LVCMOS
- 1.2 V LVCMOS
- 1.0 V LVCMOS
- 3.0-V PCI

2.4.1. Voltage-Referenced I/O Standards Termination

Voltage-referenced I/O standards require an input reference voltage (V_{REF}) and a termination voltage (V_{TT}). The reference voltage of the receiving device tracks the termination voltage of the transmitting device.

Figure 8. HSTL I/O Standard Termination

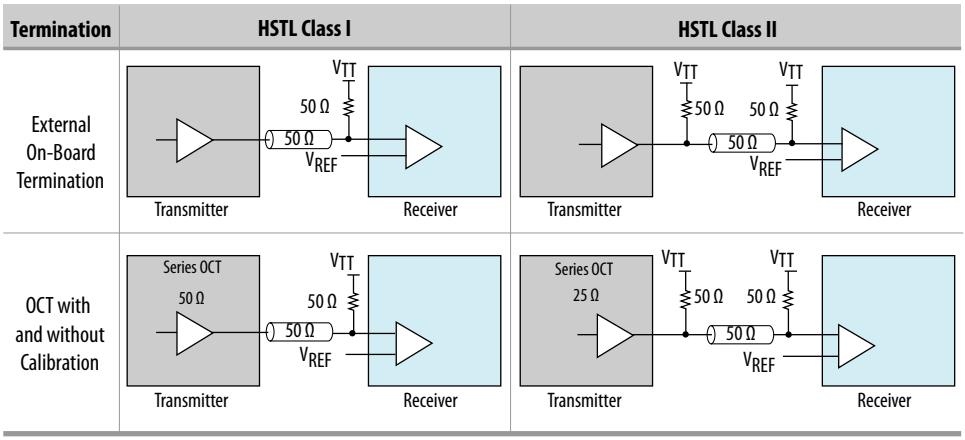
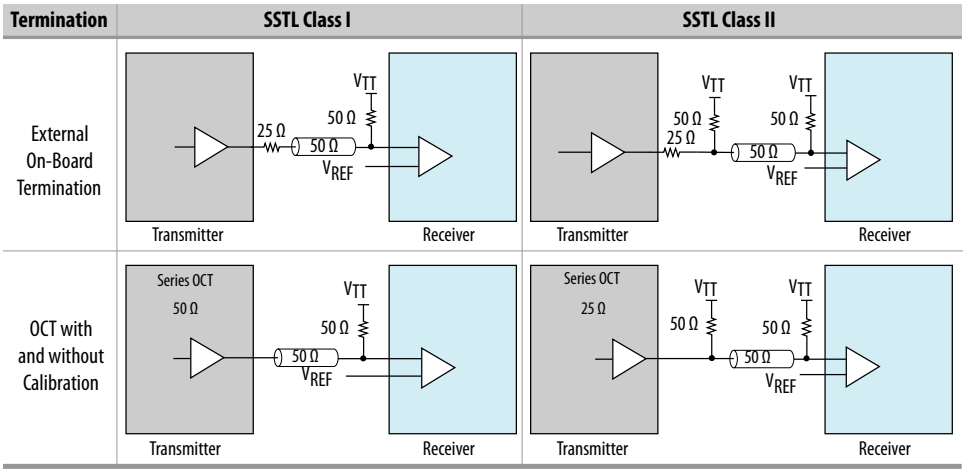


Figure 9. SSTL I/O Standard Termination



2.4.2. Differential I/O Standards Termination

Differential I/O standards typically require a termination resistor between the two signals at the receiver. The termination resistor must match the differential load impedance of the bus.

Figure 10. Differential HSTL I/O Standard Termination

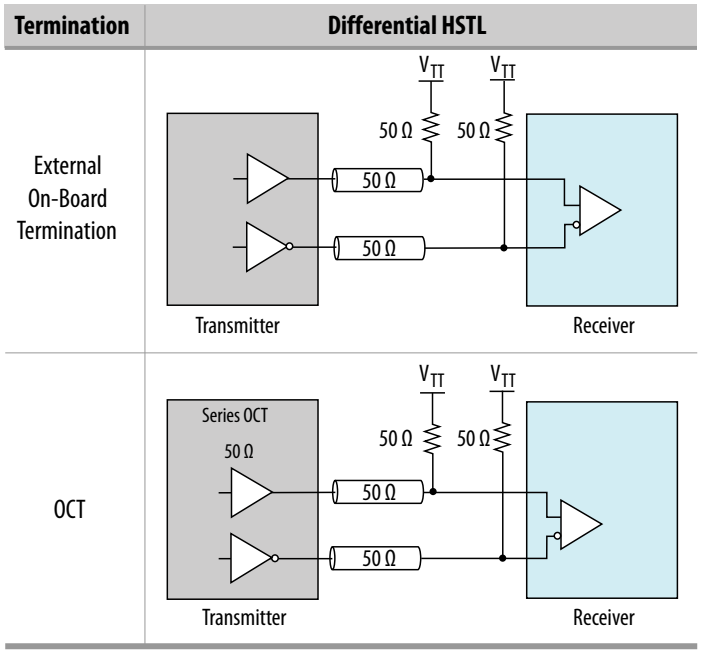
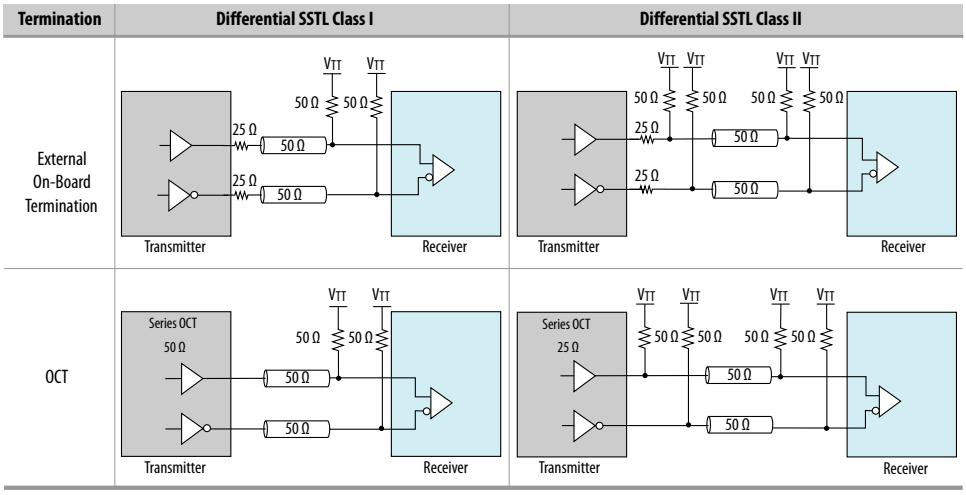


Figure 11. Differential SSTL I/O Standard Termination



Related Information

MAX 10 High-Speed LVDS I/O User Guide
Provides more information about differential I/O external termination.

2.4.3. Intel MAX 10 On-Chip I/O Termination

The on-chip termination (OCT) block in Intel MAX 10 devices provides I/O impedance matching and termination capabilities. OCT maintains signal quality, saves board space, and reduces external component costs.

The Intel MAX 10 devices support serial (R_S) OCT for single-ended output pins and bidirectional pins. For bidirectional pins, OCT is active for output only.

Figure 12. Single-ended I/O Termination (R_S)

This figure shows the single-ended termination scheme supported in Intel MAX 10 device.

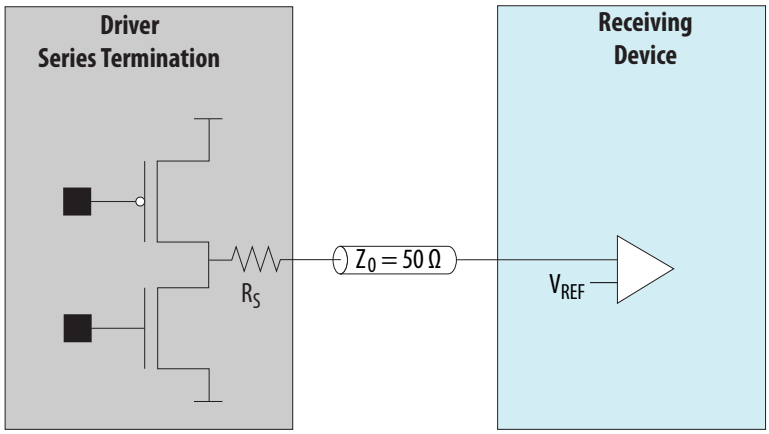


Table 12. OCT Schemes Supported in Intel MAX 10 Devices

Direction	OCT Schemes	Device Support	I/O Bank Support
Output	R_S OCT with calibration	Intel MAX 10 16, 25, 40, and 50 devices	Right bank only
	R_S OCT without calibration	All Intel MAX 10 devices	All I/O banks

2.4.3.1. OCT Calibration

The OCT calibration circuit compares the total impedance of the output buffer to the external resistors connected to the RUP and RDN pins. The circuit dynamically adjusts the output buffer impedance until it matches the external resisters.

Each calibration block comes with a pair of RUP and RDN pins.

During calibration, the RUP and RDN pins are each connected through an external 25 Ω, 34 Ω, 40 Ω, 48 Ω, or 50 Ω resistor for respective on-chip series termination value of 25 Ω, 34 Ω, 40 Ω, 48 Ω, and 50 Ω:

- RUP—connected to VCCIO.
- RDN—connected to GND.

The OCT calibration circuit compares the external resistors to the internal resistance using comparators. The OCT calibration block uses the comparators' output to dynamically adjust buffer impedance.

During calibration, the resistance of the RUP and RDN pins varies. To estimate of the maximum possible current through the external calibration resistors, assume a minimum resistance of 0 Ω on the RUP and RDN pins.

2.4.3.2. R_S OCT in Intel MAX 10 Devices

Table 13. Selectable I/O Standards for R_S OCT

This table lists the output termination settings for R_S OCT with and without calibration on different I/O standards.

- R_S OCT with calibration—supported only on the right side I/O banks of the Intel MAX 10 16, 25, 40, and 50 devices.
- R_S OCT without calibration—supported on all I/O banks of all Intel MAX 10 devices.

I/O Standard	Calibrated OCT (Output)	Uncalibrated OCT (Output)
	R_S (Ω)	R_S (Ω)
3.0 V LVTTL/3.0V LVCMOS	25, 50	25, 50
2.5 V LVTTL/2.5 V LVCMOS	25, 50	25, 50
1.8 V LVTTL/1.8 V LVCMOS	25, 50	25, 50
1.5 V LVCMOS	25, 50	25, 50
1.2 V LVCMOS	25, 50	25, 50
SSTL-2 Class I	50	50
SSTL-2 Class II	25	25

continued...

I/O Standard	Calibrated OCT (Output)	Uncalibrated OCT (Output)
	R_S (Ω)	R_S (Ω)
SSTL-18 Class I	50	50
SSTL-18 Class II	25	25
SSTL-15 Class I	50	50
SSTL-15 Class II	25	25
SSTL-15	34, 40	34, 40
SSTL-135	34, 40	34, 40
1.8 V HSTL Class I	50	50
1.8 V HSTL Class II	25	25
1.5 V HSTL Class I	50	50
1.5 V HSTL Class II	25	25
1.2 V HSTL Class I	50	50
1.2 V HSTL Class II	25	25
HSUL-12	34, 40, 48	34, 40, 48
Differential SSTL-2 Class I	50	50
Differential SSTL-2 Class I	25	25
Differential SSTL-18 Class I	50	50
Differential SSTL-18 Class II	25	25
Differential SSTL-15 Class I	50	50
Differential SSTL-15 Class II	25	25
Differential SSTL-15	34, 40	34, 40
Differential SSTL-135	34, 40	34, 40
Differential 1.8 V HSTL Class I	50	50
Differential 1.8 V HSTL Class II	25	25
Differential 1.5 V HSTL Class I	50	50
Differential 1.5 V HSTL Class II	25	25
Differential 1.2 V HSTL Class I	50	50
Differential 1.2 V HSTL Class II	25	25
Differential HSUL-12	34, 40, 48	34, 40, 48

3. Intel MAX 10 I/O Design Considerations

There are several considerations that require your attention to ensure the success of your designs. Unless noted otherwise, these design guidelines apply to all variants of this device family.

Related Information

Intel MAX 10 I/O Overview on page 3

3.1. Guidelines: V_{CCIO} Range Considerations

There are several V_{CCIO} range considerations because of I/O pin configuration function and I/O bank location.

- Banks 1 and 8 have I/O pins with configuration function. The configuration function of these pins support only 1.5 V to 3.3 V. If you want to access the configuration function of these pins during user mode (run time), for example JTAG pins, the V_{CCIO} of the pin's bank is limited to a range of 1.5 V to 3.3 V. If you want to use I/O standards with 1.2 V to 1.35 V in bank 1 or 8 during user mode, do not use the configuration function of the bank's I/O pins.
- For devices with banks 1A and 1B:
  - If you use the VREF pin or the ADC, you must supply a common V_{CCIO} voltage to banks 1A and 1B.
  - If you do not use the VREF pin or the ADC, you can supply separate V_{CCIO} voltages to banks 1A and 1B.
- If you plan to migrate from devices that has banks 1A and 1B to devices that has only bank 1, ensure that the V_{CCIO} of bank 1A and 1B are the same.
- For the V36 package of the 10M02 device, the V_{CCIO} of these groups of I/O banks must be the same:
  - Group 1—banks 1, 2 and 8
  - Group 2—banks 3, 5, and 6
- For the V81 package of the 10M08 device, the V_{CCIO} of these groups of I/O banks must be the same:
  - Group 1—banks 1A, 1B, and 2
  - Group 2—banks 5 and 6

3.2. Guidelines: Voltage-Referenced I/O Standards Restriction

These restrictions apply if you use the V_{REF} pin.

- If you use a shared VREF pin as an I/O, all voltage-reference input buffers (SSTL, HSTL, and HSUL) are disabled.
- If you use a shared VREF pin as a voltage reference, you must enable the input buffer of specific I/O pin to use the voltage-reference I/O standards.
- The voltage-referenced I/O standards are not supported in the following I/O banks of these device packages:
  - All I/O banks of V36 package of 10M02.
  - All I/O banks of V81 package of 10M08.
  - Banks 1A and 1B of E144 package of 10M50.
- For devices with banks 1A and 1B, if you use the VREF pin, you must supply a common V_{CCIO} to banks 1A and 1B.
- Maximum number of voltage-referenced inputs for each VREF pin is 75% of total number of I/O pads. The Intel Quartus Prime software will provide a warning if you exceed the maximum number.
- Except for I/O pins that you used for static signals, all non-voltage-referenced output must be placed two pads away from a VREF pin. The Intel Quartus Prime software will output an error message if this rule is violated.

Related Information

Intel MAX 10 I/O Standards Support on page 6

3.3. Guidelines: Enable Clamp Diode for LVTTL/LVCMOS Input Buffers

If the input voltage to the LVTTL/LVCMOS input buffers is higher than the V_{CCIO} of the I/O bank, Intel recommends that you enable the clamp diode.

- 3.3 V LVCMOS/LVTTL input buffers—enable clamp diode if V_{CCIO} of the I/O bank is 3.0 V.
- 3.3 V or 3.0 V LVCMOS/LVTTL input buffers—enable clamp diode if V_{CCIO} of the I/O bank is 2.5 V.

By enabling the clamp diode under these conditions, you limit overshoot. However, this does not comply with hot socket current specification.

If you do not enable the clamp diode under these conditions, the signal integrity for the I/O pin is impacted and there will be overshoot problem. In this situation, you must ensure that your board design conforms to the overshoot specifications.

Table 14. Voltage Tolerance Maximum Ratings for 3.3 V or 3.0 V

This table lists the voltage tolerance specifications. Ensure that your board design conforms to these specifications if you do not want to follow the clamp diode recommendation.

Voltage	Minimum (V)	Maximum (V)
V_{CCIO} = 3.3 V	3.135	3.45
V_{CCIO} = 3.0 V	2.85	3.15
V_{IH} (AC)	—	4.1
V_{IH} (DC)	—	3.6
V_{IL} (DC)	–0.3	0.8

Related Information

- PCI Clamp Diode on page 22
- Guideline: Use Internal PCI Clamp Diode on the Pin, *AN 447: Interfacing Intel FPGA Devices with 3.3/3.0/2.5 V LVTTL/LVCMOS I/O Systems*

3.4. Guidelines: Adhere to the LVDS I/O Restrictions Rules

For LVDS applications, adhere to the I/O restriction pin connection guidelines to avoid excessive jitter on the LVDS transmitter output pins. The Intel Quartus Prime software generates a critical warning if these rules are violated.

Related Information

MAX 10 FPGA Device Family Pin Connection Guidelines

3.5. Guidelines: I/O Restriction Rules

For different I/O standards and conditions, you must limit the number of I/O pins. This I/O restriction rule is applicable if you use LVDS transmitters or receivers. Apply this restriction if one or more LVDS I/O standards reside in the I/O bank.

Table 15. Maximum Percentage of I/O Pins Allowed for Specific I/O Standards in an I/O Bank

This table lists the maximum number of general purpose output pins recommended in a bank in terms of percentage to the total number of I/O pins available in an I/O bank if you use these combinations of I/O standards and conditions.

I/O Standard	Condition	Max Output Pins Per Bank (%)
2.5 V LVTTL/LVCMOS	16 mA current strength or 25 Ω OCT	25
	12 mA current strength	30
	8 mA current strength or 50 Ω OCT	45
	4 mA current strength	65
2.5 V SSTL	—	100

Related Information

Guidelines: Placement Restrictions for 1.0 V I/O Pin on page 33

3.6. Guidelines: Placement Restrictions for 1.0 V I/O Pin

To minimize the impact of simultaneous switching noise (SSN) on the I/O pins, ensure that the total mutual inductance (L_m) of the I/O pins in usage surrounding the 1.0 V I/O does not exceed the guidelines in the following table.

Table 16. Total L_m Guidelines for Pins Surrounding the 1.0 V Pin

I/O Standard of Surrounding Pins	Locations Relative to 1.0 V Pin	Total L_m of Surrounding Pins
1.0 V	Within the same bank	The total L_m of the surrounding pins in the bank must not exceed 7.41 nH.
	In an adjacent bank	The total L_m of the surrounding pins in the adjacent bank must not exceed 7.41 nH.
	Within the same bank and in an adjacent bank	The sum of the total L_m of the surrounding pins in both banks must not exceed 7.41 nH.
Other than 1.0 V	In an adjacent bank	The total L_m of the surrounding pins in the adjacent bank must not exceed 1 nH.

Example scenarios where the 1.0 V pin is in bank 3 and surrounding pins are in banks 3 and 4:

- Bank 3 and 4 are both 1.0 V—total L_m of all surrounding pins in both banks must not exceed 7.41 nH.
- Bank 3 is 1.0 V but bank 4 is 2.5 V—total L_m of surrounding pins in bank 3 must not exceed 7.41 nH and total L_m in bank 4 must not exceed 1 nH.

Related Information

- Intel MAX 10 Mutual Coupling (max10-1v-mutual-coupling.zip)
  Provides spreadsheet files that list the mutual inductance values for 1.0 V I/O for the following Intel MAX 10 devices: 10M02SCU324C8G, 10M04SCU324C8G, 10M08SCU324C8G, 10M16SCU324C8G, 10M16SCU169C8G, 10M16SAU169C8G, 10M16DCF484C8G, 10M16DAF484C8G, 10M25DCF484C8G, 10M25DAF484C8G, 10M40DCF484C8G, 10M40DAF484C8G, 10M50DCF484C8G, and 10M50DAF484C8G.
- Calculating the Total Inductance for 1.0 V Pin Placement on page 33

3.6.1. Calculating the Total Inductance for 1.0 V Pin Placement

You can calculate the total inductance of the surrouding pins by using mutual inductance values in the `max10-1v-mutual-coupling.zip` file.

1. Download the `max10-1v-mutual-coupling.zip` file and extract the relevant mutual inductance spreadsheet for your device.
2. In the mutual inductance spreadsheet, identify the pins in use.
3. Calculate the total mutual inductance of the pin and surrounding pins in use to ensure that the placement adheres to the 1.0 V pin placement guideline.
4. If the total inductance is above the guideline restriction, update your design to use other I/O pins that contribute less mutual inductance.

Example 1. Total Mutual Inductance Calculation

Table 17. Total Mutual Inductance Examples

The examples in this table refer to Table 18 on page 34.

Example Condition	Type	Example Result
Pin F5 is assigned with the 1 V I/O standard. The surrounding pins, F4, H3, and H4 are in the same I/O bank and are also assigned with the 1.0 V I/O standard.	Intrabank, all 1.0 V	Total L_m of F4, H3, and H4 does not exceed 7.4 nH. The placement does not violate the restriction.
Pin F5 is assigned with the 1 V I/O standard. The surrounding pins, F4, H3, and H4 are in an adjacent I/O bank and are assigned with the 1.0 V I/O standard.	Interbank, all 1.0 V	Total L_m of F4, H3, and H4does not exceed 7.4 nH. The placement does not violate the restriction.
Pin F5 is assigned with the 1 V I/O standard. The surrounding pins, F4, H3, and H4 are in an adjacent I/O bank and are assigned with the 2.5 V I/O standard.	Interbank, mixed voltages	Total L_m of F4, H3, and H4 exceeds 1.0 nH. Update your design to use other I/O pins with smaller mutual inductance.

Table 18. Example Mutual Inductance Values

Pin Name	Mutual Coupling Pin	Mutual Inductance (nH)
F5	F5	3.496(11)
F5	**F4**	**1.378**
F5	**H3**	**0.273**
F5	J4	0.263
F5	K4	0.222
F5	E4	0.194
F5	F3	0.176
F5	**H4**	**0.175**
F5	E3	0.174
F5	G3	0.167
F5	G4	0.161

Related Information

- Intel MAX 10 Mutual Coupling (max10-1v-mutual-coupling.zip)
  Provides spreadsheet files that list the mutual inductance values for 1.0 V I/O for the following Intel MAX 10 devices: 10M02SCU324C8G, 10M04SCU324C8G, 10M08SCU324C8G, 10M16SCU324C8G, 10M16SCU169C8G, 10M16SAU169C8G, 10M16DCF484C8G, 10M16DAF484C8G, 10M25DCF484C8G, 10M25DAF484C8G, 10M40DCF484C8G, 10M40DAF484C8G, 10M50DCF484C8G, and 10M50DAF484C8G.
- Guidelines: Placement Restrictions for 1.0 V I/O Pin on page 33

(11) Self inductance for pin F5. Omit this value from the L_m calculation.

3.7. Guidelines: Analog-to-Digital Converter I/O Restriction

These restrictions are applicable if you use the analog-to-digital converter (ADC) block.

The Intel Quartus Prime software uses physics-based rules to define the number of I/Os allowed in a particular bank based on the I/O's drive strength. These rules are based on noise calculation to analyze accurately the impact of I/O placement on the ADC performance.

The physics-based rules are available for the following devices starting from these Intel Quartus Prime software versions:

- From Intel Quartus Prime version 14.1—Intel MAX 10 10M04, 10M08, 10M40, and 10M50 devices.
- From Intel Quartus Prime version 15.0.1—Intel MAX 10 10M02, 10M16, and 10M25 devices.

Geometry-Based Rules for Design Estimation

Intel highly recommends that you use the following geometry-based rules to ensure ADC performance. These guidelines help you to estimate the resources available and prevent additional critical warning from versions of the Intel Quartus Prime software that implements the physics-based rules.

Table 19. Geometry-Based I/O Restrictions Related to ADC Usage

This table lists the I/O restrictions by Intel MAX 10 device package if you use the dedicated analog input (ANAIN1 or ANAIN2) or any dual function ADC I/O pins as ADC channel inputs.

Package	Restriction/Guideline
All	Disable all JTAG operation during ADC sampling. The ADC signal-to-noise and distortion ratio (SINAD) is not guaranteed during JTAG operation.
M153 U169 U324 F256 F484 F672	• Banks 1A and 1B—you cannot use GPIO pins in these banks. • Banks 2, 3, 4, 5, 6, and 7—you can use GPIO pins located in these banks. • Bank 8—you can use a percentage of the GPIO pins in this bank based on drive strength: — For an example listing the percentage of GPIO pins allowed in bank 8 for the F484 package, refer to Table 20 on page 36[12]. — Use low drive strength (8 mA and below) and differential I/O standards. — Do not place transmitter pins in this bank. Use banks 2, 3, 4, 5, 6, or 7 instead. — You can use static pins such as RESET or CONTROL. — GPIO pins in this bank are governed by physics-based rules. The Intel Quartus Prime software will issue a critical warning if the I/O settings violate any of the I/O physics-based rule.
E144	• Bank 1A, 1B, 2, and 8—you cannot use GPIO pins in these banks. • Banks 4 and 6—you can use GPIO pins located in these banks. • Banks 3, 5, and 7—you can use a percentage of the GPIO pins in this bank based on drive strength: — For the percentage of GPIO pins allowed, refer to Table 21 on page 36. — Use low drive strength (8 mA and below) and differential I/O standards. — GPIO pins in these banks are governed by physics-based rules. The Intel Quartus Prime software will issue a critical warning if the I/O settings violate any of the I/O physics-based rule.

(12) For all device packages, the software displays a warning message if the number of GPIO pins in bank 8 is more than the allowed percentage.

Table 20. I/O Usage Restriction for Bank 8 in Intel MAX 10 F484 Package

This table lists the percentage of I/O pins available in I/O bank 8 if you use the dedicated analog input (ANAIN1 or ANAIN2) or any dual function ADC I/O pins as ADC channel. Refer to Table 22 on page 36 for the list of I/O standards in each group.

I/O Standards	TX	RX	Total	Availability (%)
Group 1	18	18	36	100
Group 2	16	16	32	89
Group 3	7	11	18	50
Group 4	5	7	12	33
Group 5	4	6	10	28
Group 6	4	4	8	22
Group 7	0	8	8	22

Table 21. I/O Usage Restriction for Banks 3, 5, and 7 in Intel MAX 10 E144 Package

This table lists the percentage of I/O pins available in banks 3, 5, and 7 if you use the dedicated analog input (ANAIN1 or ANAIN2) or any dual function ADC I/O pins as ADC channel inputs. Refer to Table 22 on page 36 for the list of I/O standards in each group.

I/O Standards	Bank 3			Bank 5			Bank 7			Device I/O Availability (%)
	TX	RX	Availability (%)	TX	RX	Availability (%)	TX	RX	Availability (%)	
Group 1	7	8	88	6	6	100	4	3	100	54
Group 2	7	8	88	6	6	100	4	3	100	54
Group 3	4	5	50	6	6	100	2	0	29	45
Group 4	3	4	39	5	5	83	0	0	0	39
Group 5	2	3	28	5	5	83	0	0	0	37
Group 6	1	2	17	5	5	83	0	0	0	35
Group 7	0	0	0	5	5	83	0	0	0	32

Table 22. I/O Standards Groups Categorized According to Drive Strengths

I/O Standard Group	I/O Standards Name and Drive Strength
Group 1	• 2.5 V LVDS • 2.5 V RSDS • BLVDS at 4 mA • SLVS at 4 mA
Group 2	• BLVDS at 8 mA • SLVS at 8 mA • Sub-LVDS at 8 mA • 1.8 V, 1.5 V, and 1.2 V HSTL Class I at 8 mA • SSTL-15 at 34 Ω or 40 Ω • SSTL-135 at 34 Ω or 40 Ω • HSUL-12 at 34 Ω or 40 Ω • SSTL-2 Class I at 8 mA • SSTL-18 Class I at 8 mA • SSTL-15 Class I at 8 mA • 2.5 V and 1.8 V LVTTL at 4 mA

continued...

I/O Standard Group	I/O Standards Name and Drive Strength
	• 2.5 V, 1.8 V, 1.5 V, and 1.2 V LVCMOS at 4 mA • 1.8 V LVTTL at 2 mA • 1.8 V, 1.5 V, and 1.2 V LVCMOS at 2 mA
Group 3	• BLVDS at 12 mA • SLVS at 12 mA • Sub-LVDS at 12 mA • SSTL-2 Class I at 10 mA or 12 mA • SSTL-18 Class I at 10 mA or 12 mA • SSTL-15 Class I at 10 mA or 12 mA • 1.8 V, 1.5 V, and 1.2 V HSTL Class I at 10 mA or 12 mA • SSTL-2 at 50 Ω • SSTL-18 at 50 Ω • SSTL-15 at 50 Ω • 1.8 V, 1.5 V and 1.2 V HSTL at 50 Ω • HSUL-12 at 48 Ω • 2.5 V and 1.8 V LVTTL at 50 Ω • 2.5 V, 1.8 V, 1.5 V, and 1.2 V LVCMOS at 50 Ω • 1.8 V LVTTL at 6 mA or 8 mA • 1.8 V, 1.5 V, and 1.2 V LVCMOS at 6 mA or 8 mA • 1.0 V LVCMOS • 3.0 V LVTTL at 4 mA • 3.0 V LVCMOS at 4 mA
Group 4	• SSTL-18 Class II at 12 mA • 3.0 V LVTTL at 50 Ω • 3.0 V LVCMOS at 50 Ω • 2.5 V LVTTL at 8 mA • 2.5 V LVCMOS at 8 mA • 1.8 V LVTTL at 10 mA or 12 mA • 1.8 V, 1.5 V, and 1.2 V LVCMOS at 10 mA or 12 mA • 3.3 V LVCMOS at 2 mA
Group 5	• SSTL-2 Class II at 16 mA • SSTL-18 Class II at 16 mA • SSTL-15 Class II at 16 mA • 1.8 V and 1.5 V HSTL Class II at 16 mA • 1.2 V HSTL Class II at 14 mA • SSTL-18 at 25 Ω • SSTL-15 at 25 Ω • SSTL-2 at 25 Ω • 1.8 V, 1.5 V, and 1.2 V HSTL at 25 Ω • 2.5 V and 1.8 V LVTTL at 25 Ω • 2.5 V, 1.8 V, 1.5 V, and 1.2 LVCMOS at 25 Ω • 1.8 V LVTTL at 16 mA • 1.8 V and 1.5 V LVCMOS at 16 mA • 2.5 V LVCMOS at 12 mA • 2.5 V LVTTL at 12 mA • 3.0 V LVCMOS at 8 mA • 3.0 V LVTTL at 8 mA • 3.3 V LVTTL at 4 mA or 8 mA
Group 6	• 2.5 V LVTTL at 16 mA • 2.5 V LVCMOS at 16 mA • 3.0 V LVTTL at 12 mA

continued...

I/O Standard Group	I/O Standards Name and Drive Strength
	• 3.0 V LVCMOS at 12 mA • 3.0 V LVTTL at 25 Ω • 3.0 V LVCMOS at 25 Ω
Group 7	• 3.0 V LVTTL at 16 mA • 3.0 V LVCMOS at 16 mA

3.8. Guidelines: External Memory Interface I/O Restrictions

These I/O rules are applicable if you use external memory interfaces in your design.

Two GPIOs Adjacent to DQ Pin Is Disabled

This limitation is applicable to Intel MAX 10 10M16, 10M25, 10M40, and 10M50 devices, and only if you use DDR3 and LPDDR2 SDRAM memory standards.

Table 23. DDR3 and LPDDR2 Memory Interface Widths and Device Packages Where Two GPIOs Adjacent to DQ Pins Are Disabled

This table lists the combination of Intel MAX 10 10M16, 10M25, 10M40, and 10M50 device packages, and DDR3 and LPDDR2 memory interface widths where you cannot use two GPIO pins that are adjacent to the DQ pins.

Device Package	Memory Interface Width (DDR3 and LPPDR2 only)
U324	x8
F484	x8, x16, x24
F672	x8, x16, x24

Total I/O Utilization in Bank Must Be 75 Percent or Less in Some Devices

If you use DDR3 or LPDDR2 SDRAM memory interface standards, you can generally use a maximum of 75 percent of the total number of I/O pins available in a bank. This restriction differs from device to device. In some devices packages you can use all 100 percent of the I/Os. The Intel Quartus Prime software will output an error message if the I/O usage per bank of that device is affected by this rule.

If you use DDR2 memory interface standards, you can assign 25 percent of the I/O pins as input pins only.

3.9. Guidelines: Dual-Purpose Configuration Pin

To use configuration pins as user I/O pins in user mode, you have to adhere to the following guidelines.

Table 24. Dual-Purpose Configuration Pin Guidelines for Intel MAX 10 Devices

Guidelines	Pins
Configuration pins during initialization:	• nCONFIG • nSTATUS • CONF_DONE

continued...

Guidelines	Pins
• Tri-state the external I/O driver and drive an external pull-up resistor[13] or • Use the external I/O driver to drive the pins to the state same as the external weak pull-up resistor	
JTAG pins: • If you intend to switch back and forth between user I/O pins and JTAG pin functions using the JTAGEN pin, all JTAG pins must be assigned as single-ended I/O pins or voltage-referenced I/O pins. Schmitt trigger input is the recommended input buffer. • JTAG pins cannot perform as JTAG pins in user mode if you assign any of the JTAG pin as a differential I/O pin. • You must use the JTAG pins as dedicated pins and not as user I/O pins during JTAG programming. • Do not toggle JTAG pin during the initialization stage. • Put the test access port (TAP) controller in reset state by driving the TDI and TMS pins high and toggle the TCK pin for at least 5 clock cycles before the initialization. • The Signal Tap logic analyzer IP, JTAG-to-Avalon® master bridge IP, and other JTAG-related IPs cannot be used if you enable the JTAG pin sharing feature in your design.	• TDO • TMS • TCK • TDI

Attention: Assign all JTAG pins as single-ended I/O pins or voltage-referenced I/O pins if you enable JTAG pin sharing feature.

Related Information

MAX 10 FPGA Configuration User Guide
Provides more information about the dual-purpose I/O pins in configuration and user modes.

3.10. Guidelines: Clock and Data Input Signal for Intel MAX 10 E144 Package

There is strong inductive coupling on the Intel MAX 10 E144 lead frame package. Glitch may occur on an input pin when an aggressor pin with strong drive strength toggles directly adjacent to it.

PLL Clock Input Pins

The PLL clock input pins are sensitive to SSN jitter. To avoid the PLL from losing lock, do not use the output pins directly on the left and right of the PLL clock input pins.

Data Input Pins

Potential glitch on the data input pin, leading to input read signal failure, can occur in the following conditions:

- The output pin directly adjacent to the data input pin is assigned an unterminated I/O standard, such as LVTTL and LVCMOS, with drive strength of 8 mA or higher.
- The output pin directly adjacent to the data input pin is assigned a terminated I/O standard, such as SSTL, with drive strength of 8 mA or higher.

(13) If you intend to remove the external weak pull-up resistor, Intel recommends that you remove it after the device enters user mode.

Intel recommends that you implement these guidelines to reduce jitter on the data input pin:

- For unterminated I/O standards, implement one of these guidelines:
  - For the directly-adjacent output pin with these unterminated I/O standards, reduce the drive strength as follows:
    - 2.5 V, 3.0 V, and 3.3 V—reduce to 4 mA or below
    - 1.2 V, 1.5 V, and 1.8 V—reduce to 6 mA or below
  - Assign the pins directly on the left and right of the data input pin to a non-toggling signal.
  - Change the data input pin to a Schmitt Trigger input buffer for better noise immunity. If you are using Schmitt Trigger input buffer on the data input pin, you can use the directly-adjacent output pin with unterminated I/O standard at a maximum drive strength of 8 mA.
- For terminated I/O standard, you can use only one pin directly on the left or right of the data input pin as toggling signal, provided that you set the slew rate setting of this pin to "0" (slow slew rate). Otherwise, assign the pins directly on the left and right of the data input pin to a non-toggling signal.

4. Intel MAX 10 I/O Implementation Guides

You can implement your I/O design in the Intel Quartus Prime software. The software contains tools for you to create and compile your design, and configure your device.

The Intel Quartus Prime software allows you to prepare for device migration, set pin assignments, define placement restrictions, setup timing constraints, and customize IP cores. For more information about using the Intel Quartus Prime software, refer to the related information.

Related Information

Intel MAX 10 I/O Overview on page 3

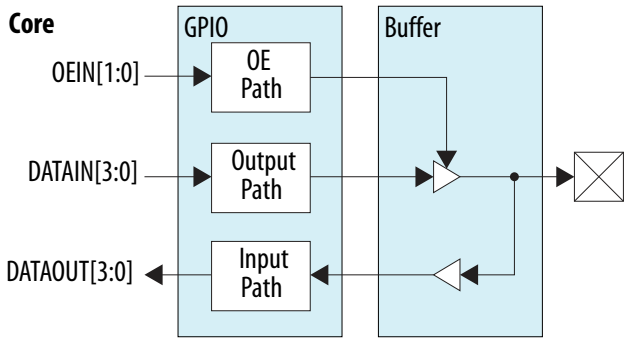
4.1. GPIO Lite Intel FPGA IP

The GPIO Lite IP core supports the Intel MAX 10 GPIO components. To implement the GPIOs in your design, you can customize the GPIO Lite IP core to suit your requirements and instantiate it in your design.

GPIOs are I/Os used in non-transceiver general applications, memory-like interfaces or LVDS applications. The GPIO Lite IP core features the following components:

- Double data rate input/output (DDIO)—A digital component that doubles the data-rate of a communication channel.
- I/O buffers—connect the pads to the FPGA.

Figure 13. High Level View of Single-Ended GPIO



Related Information

- Introduction to Intel FPGA IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.

- Creating Version-Independent IP and Qsys Simulation Scripts
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- Project Management Best Practices
  Guidelines for efficient management and portability of your project and IP files.

4.1.1. GPIO Lite Intel FPGA IP Data Paths

Table 25. GPIO Lite IP Core Data Path Modes

Data Path	Mode		
	Bypass	Single Register	DDR
Input	Data goes from the delay element to the core, bypassing all double data rate I/Os (DDIOs).	The full-rate DDIO operates as a single register.	The full-rate DDIO operates as a regular DDIO.
Output	Data goes from the core straight to the delay element, bypassing all DDIOs.	The full-rate DDIO operates as a single register.	The full-rate DDIO operates as a regular DDIO.
Bidirectional	The output buffer drives both an output pin and an input buffer.	The full-rate DDIO operates as a single register. The output buffer drives both an output pin and an input buffer.	The full-rate DDIO operates as a regular DDIO. The output buffer drives both an output pin and an input buffer. The input buffer drives a set of three flip-flops.

If you use asynchronous clear and preset signals, all DDIOs share these same signals.

4.1.1.1. DDR Input Path

The pad sends data to the input buffer and the input buffer feeds the delay element. From the delay element, the data is fed to the DDIO stage, which consists of three registers:

- `RegAi` samples the data from `pad_in` at the positive clock edge.
- `RegBi` samples the data from `pad_in` at the negative clock edge.
- `RegCi` samples the data from `RegAi` at the negative clock edge.

Figure 14. Simplified View of GPIO Lite IP Core DDR Input Path

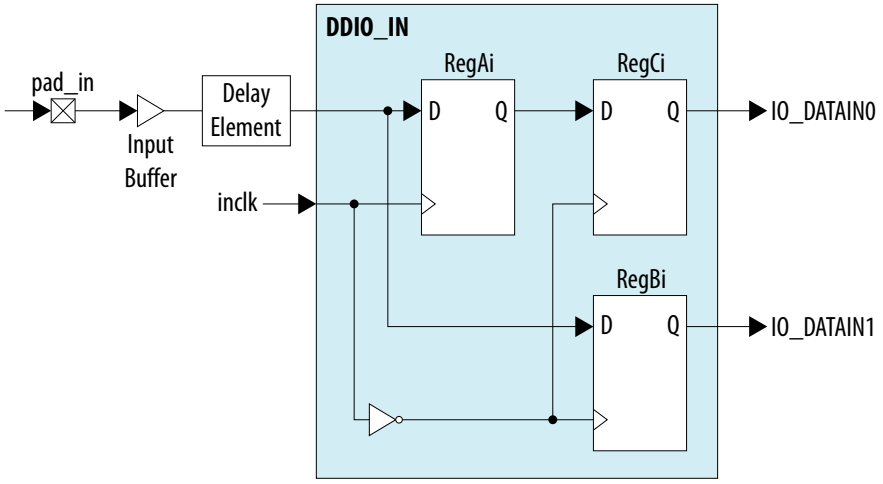
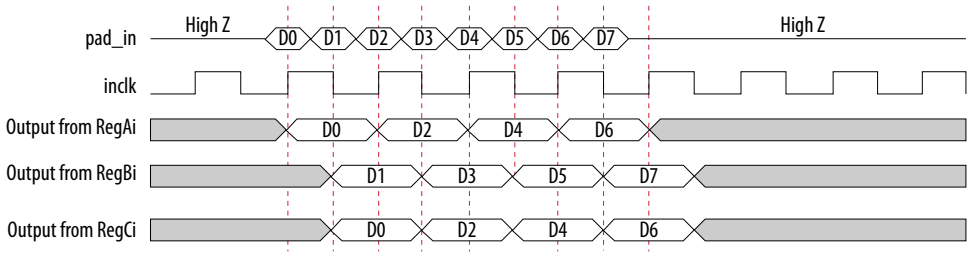
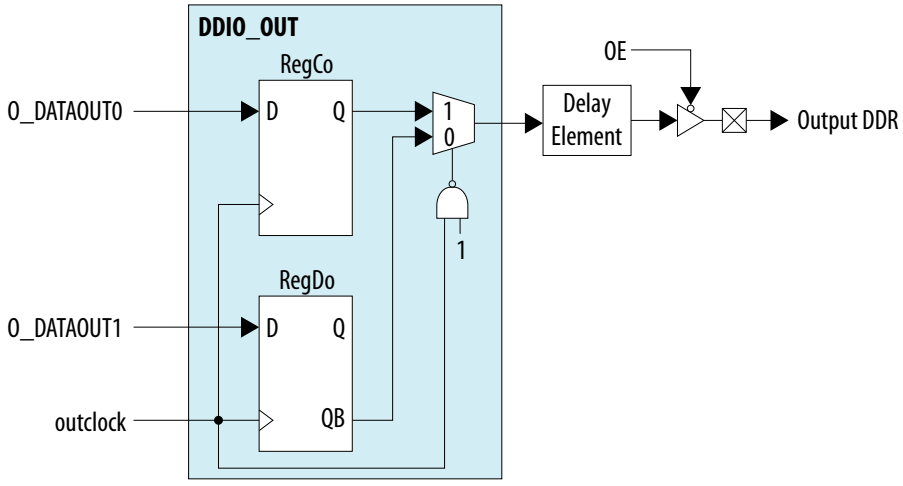


Figure 15. GPIO Lite IP Core Input Path Timing Diagram



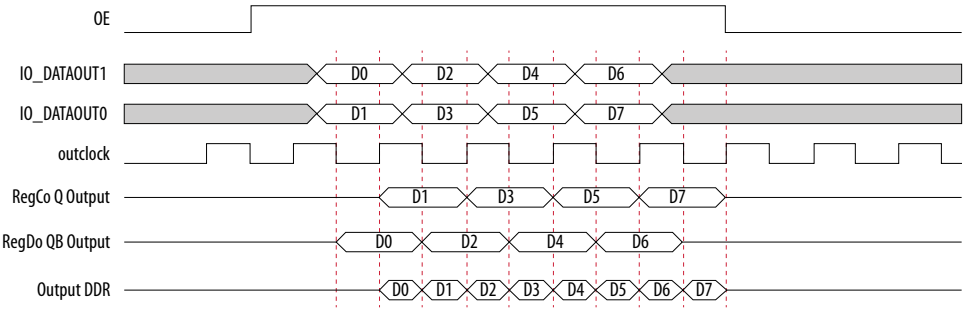
4.1.1.2. DDR Output Path with Output Enable

Figure 16. Simplified View of GPIO Lite IP Core DDR Output Path with Output Enable



- RegCo samples the data from IO_DATAOUT0 at the positive clock edge.
- RegDo samples the data from IO_DATAOUT1 when outclock value is 0.
- Output DDR samples the data from RegCo at the positive clock edge, and from RegDo at the negative clock edge.

Figure 17. GPIO Lite IP Core Output Path Timing Diagram



- The IP core feeds the first bit, D0, through IO_DATAOUT1 to RegDo. The IP core clocks out this bit at the RegDo QB port on a negative clock edge. At the next positive clock edge, the IP core produces the same bit at the multiplexer output.
- The IP core feeds the second bit, D1, through IO_DATAOUT0 to RegCo. The IP core clocks out this bit at the RegCo Q port on a positive clock edge. At the next negative clock edge, the IP core produces the same bit at the multiplexer output.

4.2. Verifying Pin Migration Compatibility

You can use the **Pin Migration View** window in the Intel Quartus Prime software Pin Planner to assist you in verifying whether your pin assignments migrate to a different device successfully.

You can vertically migrate to a device with a different density while using the same device package, or migrate between packages with different densities and ball counts.

1. Open **Assignments ➤ Pin Planner** and create pin assignments.
2. If necessary, perform one of the following options to populate the Pin Planner with the node names in the design:
   — Analysis & Elaboration
   — Analysis & Synthesis
   — Fully compile the design
3. Then, on the menu in **Pin Planner**, click **View ➤ Pin Migration Window**.
4. To select or change migration devices:
   a. Click **Device** to open the **Device** dialog box.
   b. Click **Migration Devices**.
5. To show more information about the pins:
   a. Right-click anywhere in the **Pin Migration View** window and select **Show Columns**.
   b. Then, click the pin feature you want to display.

6. If you want to view only the pins, in at least one migration device, that have a different feature than the corresponding pin in the migration result, turn on **Show migration differences**.
7. Click **Pin Finder** to open the **Pin Finder** dialog box and find and highlight pins with specific functionality.

   If you want to view only the pins found and highlighted by the most recent query in the **Pin Finder** dialog box, turn on **Show only highlighted pins**.
8. To export the pin migration information to a Comma-Separated Value File (**.csv**), click **Export**.

Related Information

Intel MAX 10 I/O Vertical Migration Support on page 5

5. GPIO Lite Intel FPGA IP References

You can set various parameter settings for the GPIO Lite IP core to customize its behaviors, ports, and signals.

The Intel Quartus Prime software generates your customized GPIO Lite IP core according to the parameter options that you set in the parameter editor.

Related Information

Intel MAX 10 I/O Overview on page 3

5.1. GPIO Lite Intel FPGA IP Parameter Settings

You can set the parameter settings for the GPIO Lite IP core in the Intel Quartus Prime software. There are three groups of options: **General**, **Buffer**, and **Registers**.

Table 26. GPIO Lite Parameters - General

Parameter	Condition	Allowed Values	Description
Data direction	—	• input • output • bidir	Specifies the data direction for the GPIO.
Data width	—	1 to 128	Specifies the data width.

Table 27. GPIO Lite Parameters - Buffer

Parameter	Condition	Allowed Values	Description
Use true differential buffer	Data direction = input or output	• On • Off	If turned on, enables true differential I/O buffers and disables pseudo differential I/O buffers.
Use pseudo differential buffer	Data direction = output or bidir	• On • Off	• If turned on in output mode—enables pseudo differential output buffers and disables true differential I/O buffers. • If turned on in bidir mode—enables true differential input buffer and pseudo differential output buffer.
Use bus-hold circuitry	Data direction = input or output	• On • Off	If turned on, the bus hold circuitry can weakly hold the signal on an I/O pin at its last-driven state where the output buffer state will be 1 or 0 but not high-impedance.

continued...

Parameter	Condition	Allowed Values	Description
Use open drain output	Data direction = output or bidir	• On • Off	If turned on, the open drain output enables the device to provide system-level control signals such as interrupt and write enable signals that can be asserted by multiple devices in your system.
Enable oe port	Data direction = output	• On • Off	If turned on, enables user input to the OE port. This option is automatically turned on for bidirectional mode.
Enable nsleep port (only available in selected devices)	Data direction = input or bidir	• On • Off	If turned on, enables the nsleep port. This option is available for the 10M16, 10M25, 10M40, and 10M50 devices.

Table 28. GPIO Lite Parameters - Registers

Parameter	Condition	Allowed Values	Description
Register mode	—	• bypass • single-register • ddr	Specifies the register mode for the GPIO Lite IP core: • **bypass**—specifies a simple wire connection from/to the buffer. • **single-register**—specifies that the DDIO is used as a simple register in single data-rate mode (SDR). The Fitter may pack this register in the I/O. • **ddr**— specifies that the IP core uses the DDIO.
Enable aclr port	• Register mode = ddr	• On • Off	If turned on, enables the ACLR port for asynchronous clears.
Enable aset port	• Data direction = output or bidir • Register mode = ddr • Set registers to power up high (when aclr and aset ports are not used) = off	• On • Off	If turned on, enables the ASET port for asynchronous preset.
Set registers to power up high (when aclr and aset ports are not used)	• Register mode = ddr • Enable aclr port = off • Enable aset port = off • Enable sclr port = off	• On • Off	If you are not using the ACLR and ASET ports: • **On**—specifies that registers power up HIGH. • **Off**—specifies that registers power up LOW.
Enable inclocken/ outclocken ports	Register mode = ddr	• On • Off	• **On**—exposes the clock enable port to allow you to control when data is clocked in or out. This signal prevents data from being passed through without your control. • **Off**—clock enable port is not exposed and data always pass through the register automatically.
Invert din	• Data direction = output • Register mode = ddr	• On • Off	If turned on, inverts the data out output port.
Invert DDIO inclock	• Data direction = input or bidir • Register mode = ddr	• On • Off	• **On**—captures the first data bit on the falling edge of the input clock. • **Off**—captures the first data bit on the rising edge of the input clock.

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Parameter	Condition	Allowed Values	Description
Use a single register to drive the output enable (oe) signal at the I/O buffer	• Data direction = output or bidir • Register mode = single-register or ddr • Use DDIO registers to drive the output enable (oe) signal at the I/O buffer = off	• On • Off	If turned on, specifies that a single register drives the OE signal at the output buffer.
Use DDIO registers to drive the output enable (oe) signal at the I/O buffer	• Data direction = output or bidir • Register mode = ddr • Use a single register to drive the output enable (oe) signal at the I/O buffer = off	• On • Off	If turned on, specifies that the DDR I/O registers drive the OE signal at the output buffer. The output pin is held at high impedance for an extra half clock cycle after the OE port goes high.
Implement DDIO input registers in hard implementation (Only available in certain devices)	• Data direction = input or bidir • Register mode = ddr	• On • Off	• **On**—implements the DDIO input registers using hard block at the I/O edge. • **Off**—implements the DDIO input registers as soft implementation using registers in the FPGA core fabric. This option is applicable only for Intel MAX 10 16, 25, 40, and 50 devices because the DDIO input registers hard block is available only in these devices. To avoid Fitter error, turn this option off for other Intel MAX 10 devices.

5.2. GPIO Lite Intel FPGA IP Interface Signals

Depending on parameter settings you specify, different interface signals are available for the GPIO Lite IP core.

Table 29. Pad Interface Signals

The pad interface connects the GPIO Lite IP core to the pads.

Signal Name	Direction	Description
pad_in	Input	Input pad port if you use the input path.
pad_in_b	Input	Input negative pad port if you use the input path and enable the true or pseudo differential buffers.
pad_out	Output	Output pad port if you use the output path.
pad_out_b	Output	Output negative pad port if you use the output path and enable the true of pseudo differential buffers.
pad_io	Bidirectional	Bidirectional pad port if you use bidirectional paths.
pad_io_b	Bidirectional	Bidirectional negative pad port if you use bidirectional paths and enable true or pseudo differential buffers.

Table 30. Data Interface Signals

The data interface is an input or output interface from the GPIO Lite IP core to the FPGA core.

Signal Name	Direction	Description
din	Input	Data received from the input pin.

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Signal Name	Direction	Description
		Signal width for each input pin: • DDR mode—2 • Other modes—1
dout	Output	Data to send out through the output pin. Signal width for each output pin: • DDR mode—2 • Other modes—1
oe	Input	Control signal that enables the output buffer. This signal is active HIGH.
nsleep	Input	Control signal that enables the input buffer. This signal is active LOW. This signal is available for the 10M16, 10M25, 10M40, and 10M50 devices.

Table 31. Clock Interface Signals

The clock interface is an input clock interface. It consists of different signals, depending on the configuration. The GPIO Lite IP core can have zero, one, two, or four clock inputs. Clock ports appear differently in different configurations to reflect the actual function performed by the clock signal.

Signal Name	Direction	Description
inclock	Input	Input clock that clocks the registers in the input path.
inclocken	Input	Control signal that controls when data is clocked in. This signal is active HIGH.
outclock	Input	Input clock that clocks the registers in the output path.
ouctlocken	Input	Control signal that controls when data is clocked out. This signal is active HIGH.

Table 32. Reset Interface Signals

The reset interface connects the GPIO Lite IP core to the DDIOs.

Signal Name	Direction	Description
aclr	Input	Control signal for asynchronous clear that sets the register output state to 0. This signal is active HIGH.
aset	Input	Control signal for asynchronous preset that sets the register output state to 1. This signal is active HIGH.
sclr	Input	Control signal for synchronous clear that sets the register output to 0. This signal is active HIGH.

6. Intel MAX 10 General Purpose I/O User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
18.1	MAX 10 General Purpose I/O User Guide
17.1	MAX 10 General Purpose I/O User Guide
16.0	MAX 10 General Purpose I/O User Guide
15.1	MAX 10 General Purpose I/O User Guide
15.0	MAX 10 General Purpose I/O User Guide
14.1	MAX 10 General Purpose I/O User Guide

7. Document Revision History for Intel MAX 10 General Purpose I/O User Guide

Document Version	Intel Quartus Prime Version	Changes
2020.11.05	20.1	Updated the guidelines for JTAG pins in table *Dual-Purpose Configuration Pin Guidelines for Intel MAX 10 Devices*.
2020.09.22	20.1	Updated the clamp diode for LVTTL/LVCMOS input buffers guidelines to remove references to "undershoot". The clamp diode manages overshoot voltages only.
2020.08.24	20.1	Updated the table in the I/O restriction rules guideline topic to improve clarity.
2020.06.30	20.1	• Added support for 1.0 V LVCMOS I/O standard. • Added placement restriction guideline for 1.0 V I/O pins.
2019.01.01	18.1	Removed support for 1.0 V LVCMOS I/O standard.
2018.12.20	18.1	• Updated introductory statements about GPIO usage to improve clarity. • Added support for 1.0 V LVCMOS I/O standard for commercial grade devices only. • Added link to the list of Intel MAX 10 develoment kits and boards. • Added statement to clarify that when the Intel MAX 10 device is blank or erased, the I/Os are tri-stated. • Updated the guideline for V_{CCIO} range to improve clarity. • Updated the topic about the PCI clamp diode and added links to related information. • Updated the topic about programmable emulated differential output to improve clarity.

Date	Version	Changes
December 2017	2017.12.15	• Added the U324 package for the Intel MAX 10 single power supply devices. • Updated the I/O vertical migration figure. • Added a topic about the different I/O banks performance. • Updated the GPIO Lite DDR output path figure, timing diagram, and added descriptions to improve clarity. • Updated the description in the guideline topic about I/O restrictions to improve clarity. • Updated the guideline topic about the clock and data input signal for the E144 package to improve clarity. • Updated the guideline topic about the ADC I/O restriction to clarify that the guidelines are geometry-based rules for design estimation purpose.

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Date	Version	Changes
		• Removed all "Preliminary" markers. • Updated the topic about the PCI clamp diode to remove the sentence that mention the active serial (AS) configuration scheme. Intel MAX 10 devices do not support the AS configuration scheme. • Updated the guideline topic about enabling the clamp diode for the LVTTL/LVCMOS input buffers to improve clarity.
February 2017	2017.02.21	Rebranded as Intel.
May 2016	2016.05.02	• Updated the list of supported I/O standards to specify I/O standards that are supported only in dual power supply Intel MAX 10 devices. • Updated the names of emulated differential I/O standards to improve clarity. • Updated the topic about the I/O standards voltage and pin support to clarify that the I/O standards that a pin type supports depends on pin's I/O bank. • Updated the setting information for PCI clamp diode: — On by default for input pins for all supported I/O standards — Off by default for output pins for all supported I/O standards, except 3.0 V PCI • Updated the topic about the ADC I/O restriction: — Added the list of devices with physics-based rules support from Intel Quartus Prime version 15.0.1. — Clarified that the table listing the percentage of GPIOs allowed in bank 8 is an example for the F484 package. For all packages, the Intel Quartus Prime software displays a warning message if you exceed the allowed GPIO percentage.
November 2015	2015.11.02	• Added PCI clamp diode support for the 3.3 V and 2.5 V Schmitt Trigger I/O standards. • Added a table that summarizes the programmable I/O buffer features and settings. • Updated the topics about V_{CCIO} range consideration and VREF I/O standards restriction with guidelines for using different V_{CCIO} supplies in bank 1A and bank 1B. • Added guidelines topic about using the clock and input pins in the E144 package. • Added the **Enable nsleep port** parameter option. • Removed the topics about the IP catalog and parameter editor, generating IP cores, and the files generated by the IP core, and added a link to *Introduction to Intel IP Cores*. • Changed instances of *Quartus II* to *Quartus Prime*.
June 2015	2015.06.10	• Added related link to the Intel MAX 10 device pin-outs in topic about I/O banks locations. The device pin-out files provide more information about available I/O pins in each I/O bank. • Updated the ADC I/O restriction guidelines topic.
May 2015	2015.05.04	• Removed the F672 package of the Intel MAX 10 10M25 device. • Updated footnote for LVDS (dedicated) in the table listing the supported I/O standards to clarify that you can use LVDS receivers on all I/O banks. • Added missing footnote number for the DQS column of the 3.3 V Schmitt Trigger row in the table that lists the I/O standards voltage levels and pin support. • Added a table listing the I/O standards and current strength settings that support programmable output slew rate control. • Updated the topic about external memory interface I/O restrictions to add x24 memory interface width to the F484 package. • Added topic about the programmable differential output voltage.

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Date	Version	Changes
		• Updated the guidelines for voltage-referenced I/O standards to add a list of device packages that do not support voltage-referenced I/O standards. • Updated the topic about the I/O restriction rules to remove statements about the differential pad placement rules. • Renamed the `input_ena` signal name to `nsleep` and updated the relevant description. • Updated the description for the **Invert DDIO inclock** parameter of the GPIO Lite IP core.
December 2014	2014.12.15	Updated the topic about the ADC I/O restriction: • Added information about implementation of physics-based rules in the Intel Quartus Prime software. • Updated the list of I/O standards groups for the ADC I/O restriction.
September 2014	2014.09.22	Initial release.