Intel® MAX® 10 External Memory Interface User Guide

Updated for Intel® Quartus® Prime Design Suite: **16.1**

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1. Intel® MAX® 10 External Memory Interface Overview

The Intel® MAX® 10 devices are capable of interfacing with a broad range of external memory standards. With this capability, you can utilize Intel MAX 10 devices in a wide range of applications such as image processing, storage, communications, and general embedded systems.

The external memory interface solution in Intel MAX 10 devices consist of:

- The I/O elements that support external memory interfaces.
- The UniPHY IP core that allows you to configure the memory interfaces to support different external memory interface standards.

Note: Intel recommends that you construct all DDR2, DDR3, and LPDDR2 SDRAM external memory interfaces using the UniPHY IP core.(1)

Related Information

- Intel MAX 10 External Memory Interface Architecture and Features on page 6
- Intel MAX 10 External Memory Interface Design Considerations on page 17
- Intel MAX 10 External Memory Interface Implementation Guides on page 25
- UniPHY IP References for Intel MAX 10 Devices on page 29
- Documentation: External Memory Interfaces
  Provides more information about external memory system performance specification, board design guidelines, timing analysis, simulation, and debugging.
- External Memory Interface Handbook Volume 1: Intel FPGA Memory Solution Overview and Design Flow
  Provides more information about using Intel FPGA devices for external memory interfaces including Intel FPGA memory solutions and design flow.
- External Memory Interface Handbook Volume 2: Design Guidelines
  Provides more information about using Intel FPGA devices for external memory interfaces including memory selection, board design, implementing memory IPs, timing, optimization, and debugging.
- Functional Description—Intel MAX 10 EMIF IP
  Provides more information about implementing memory IPs for Intel MAX 10 devices.
- Intel MAX 10 DDR3 Reference Design
  Provides DDR3 UniPHY IP core reference design for Intel MAX 10 devices.
- Intel MAX 10 External Memory Interface User Guide Archives on page 42
  Provides a list of user guides for previous versions of the UniPHY IP core.

(1) Licensing terms and costs for UniPHY IP core apply.

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1.1. Intel MAX 10 External Memory Interface Support and Performance

The Intel MAX 10 devices contain circuitry that supports several external memory interface standards.

Table 1. Memory Standards Supported by the Soft Memory Controller for Intel MAX 10 Devices

Contact your local sales representatives for access to the -I6 or -A6 speed grade devices in the Intel Quartus® Prime software.

External Memory Interface Standard	Rate Support	Speed Grade	Voltage (V)	Max Frequency (MHz)
DDR3 SDRAM	Half	–I6	1.5	303
DDR3L SDRAM	Half	–I6	1.35	303
DDR2 SDRAM	Half	–I6	1.8	200
		–I7 and –C7		167
LPDDR2(2)	Half	–I6	1.2	200(3)

Related Information

- External Memory Interface Spec Estimator
  Provides a parametric tool that allows you to find and compare the performance of the supported external memory interfaces in Intel FPGA devices.
- Planning Pin and FPGA Resources chapter, External Memory Interface Handbook
  Provides the maximum number of interfaces supported by Intel MAX 10 devices for each memory standards, pin counts for various external memory interface implementation examples, and information about the clock, address/command, data, data strobe, DM, and optional ECC signals.
- Intel MAX 10 Device Datasheet

(2) Intel MAX 10 devices support only single-die LPDDR2.

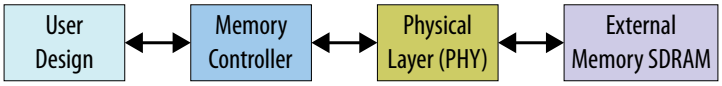
(3) To achieve the specified performance, constrain the memory device I/O and core power supply variation to within ±3%. By default, the frequency is 167 MHz.

2. Intel MAX 10 External Memory Interface Architecture and Features

The external memory interface architecture of Intel MAX 10 devices is a combination of soft and hard IPs.

Figure 1. High Level Overview of Intel MAX 10 External Memory Interface System

This figure shows a high level overview of the main building blocks of the external memory interface system in Intel MAX 10 devices.



- The full rate data capture and write registers use the DDIO registers inside the I/O elements.
- PHY logic is implemented as soft logic in the core fabric.
- The memory controller is the intermediary between the user logic and the rest of the external memory interface system. The memory controller IP is a soft memory controller that operates at half rate. You can also use your own soft memory controller or a soft memory controller IP from Intel's third-party FPGA partners.
- The physical layer (PHY) serves as the bridge between the memory controller and the external memory DRAM device.

Related Information

- Intel MAX 10 External Memory Interface Overview on page 4
- Documentation: External Memory Interfaces
  Provides more information about external memory system performance specification, board design guidelines, timing analysis, simulation, and debugging.
- Intellectual Properties: Memories & Controllers
  Provides a list of memory controller IP solutions from Intel and partners.

2.1. Intel MAX 10 I/O Banks for External Memory Interface

In Intel MAX 10 devices, external memory interfaces are supported only on the I/O banks on the right side of the device. You must place all external memory I/O pins on the I/O banks on the right side of the device.

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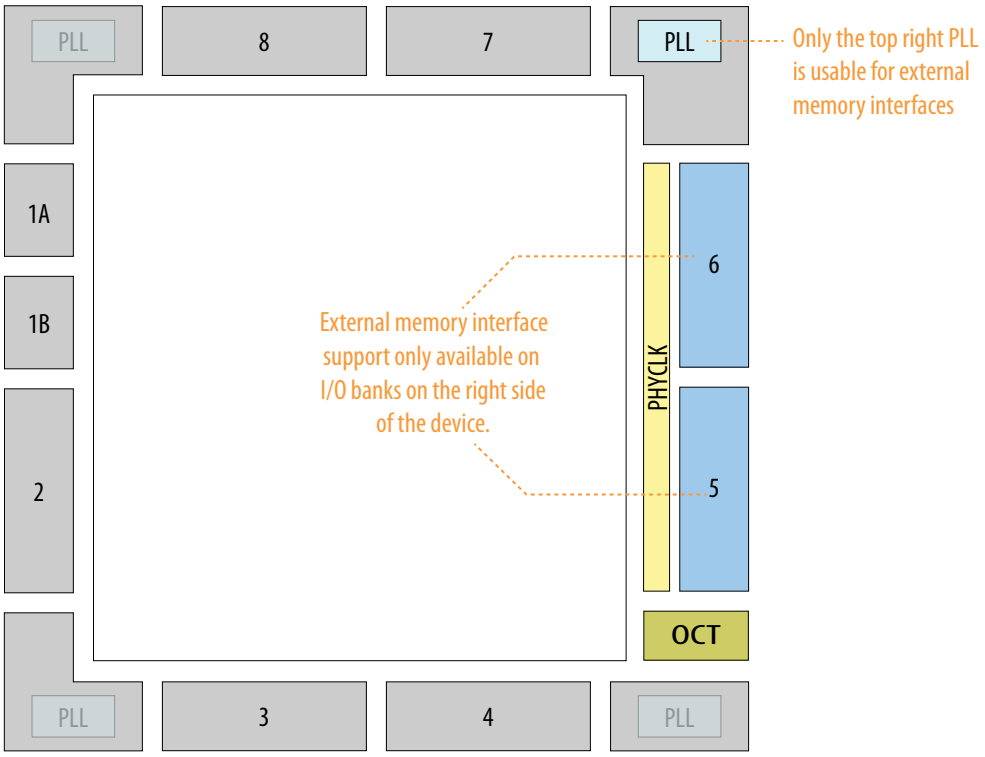
Figure 2. I/O Banks for External Memory Interfaces

This figure represents the top view of the silicon die that corresponds to a reverse view of the device package.



External memory interfaces support is available only for dual supply (DC, DF, and DA) variant on 10M16, 10M25, 10M40, and 10M50 devices.

2.2. Intel MAX 10 DQ/DQS Groups

Different Intel MAX 10 devices and packages support different numbers of DQ/DQS groups for external memory interfaces.

Table 2. Supported DQ/DQS Group Sizes in Intel MAX 10 Devices and Packages

This table lists the number of DQ/DQS groups supported on different Intel MAX 10 devices and packages. Only the I/O banks on the right side of the devices support external memory interfaces.

Device	Package	I/O Bank (Right Side)	Number of DQ Groups
			x8
10M16	F256, U324, and F484	B5	1
		B6	1
10M25	F256	B5	1
		B6	1
	F484	B5	1
		B6	2
10M40	F256	B5	1

continued...

Device	Package	I/O Bank (Right Side)	Number of DQ Groups
			x8
		B6	1
	F484	B5	1
		B6	2
	F672	B5	2
		B6	2
10M50	F256	B5	1
		B6	1
	F484	B5	1
		B6	2
	F672	B5	2
		B6	2

Related Information

Planning Pin and FPGA Resources chapter, External Memory Interface Handbook
Provides the maximum number of interfaces supported by Intel MAX 10 devices for each memory standards, pin counts for various external memory interface implementation examples, and information about the clock, address/command, data, data strobe, DM, and optional ECC signals.

2.3. Intel MAX 10 External Memory Interfaces Maximum Width

Different Intel MAX 10 device packages support different maximum width for external memory interfaces.

Table 3. Supported Maximum External Memory Interface Width in Intel MAX 10 Device Packages

Product Line	Package			
	F256	U324	F484	F672
10M16	• x8 DDR2, DDR3/3L, and LPDDR2 without ECC • x16 LPDDR2 without ECC	• x8 DDR2, DDR3/3L, and LPDDR2 without ECC • x16 DDR2, and DDR3/3L with or without ECC • x16 LPDDR2 without ECC	• x8 DDR2, DDR3/3L, and LPDDR2 without ECC • x16 DDR2, and DDR3/3L with or without ECC • x16 LPDDR2 without ECC	—
10M25	• x8 DDR2, DDR3/3L, and LPDDR2 without ECC • x16 LPDDR2 without ECC	—	• x8 DDR2, DDR3/3L and LPDDR2 without ECC • x16 DDR2, and DDR3/3L with or without ECC • x24 DDR2, and DDR3/3L with ECC • x16 LPDDR2 without ECC	• x8 DDR2, DDR3/3L, and LPDDR2 without ECC • x16 DDR2, and DDR3/3L with or without ECC • x24 DDR2, and DDR3/3L with ECC • x16 LPDDR2 without ECC
10M40	• x8 DDR2, DDR3/3L and LPDDR2 without ECC • x16 LPDDR2 without ECC	—	• x8 DDR2, DDR3/3L, and LPDDR2 without ECC • x16 DDR2, and DDR3/3L with or without ECC • x24 DDR2, and DDR3/3L with ECC • x16 LPDDR2 without ECC	• x8 DDR2, DDR3/3L, and LPDDR2 without ECC • x16 DDR2, and DDR3/3L with or without ECC • x24 DDR2, and DDR3/3L with ECC • x16 LPDDR2 without ECC
10M50	• x8 DDR2, DDR3/3L, and LPDDR2 without ECC • x16 LPDDR2 without ECC	—	• x8 DDR2, DDR3/3L, and LPDDR2 without ECC • x16 DDR2, and DDR3/3L with or without ECC • x24 DDR2, and DDR3/3L with ECC • x16 LPDDR2 without ECC	• x8 DDR2, DDR3/3L, and LPDDR2 without ECC • x16 DDR2, and DDR3/3L with or without ECC • x24 DDR2, and DDR3/3L with ECC • x16 LPDDR2 without ECC

2.4. Intel MAX 10 Memory Controller

Intel MAX 10 devices use the HPC II external memory controller.

Table 4. Features of the Intel MAX 10 Memory Controller

Feature	Description
Half-Rate Operation	The controller and user logic can run at half the memory clock rate.
Controller Latency	The controller has a low best-case time between a read request or a write request on the local interface, and the memory command being sent to the AFI interface.
Data Reordering	The memory controller will reorder read and write requests as necessary to achieve the most efficient throughput of data.

continued...

Feature	Description
Starvation Control	The controller implements a starvation counter to limit the length of time that a command can go unserved. This counter ensures that lower-priority requests are not overlooked indefinitely due to data reordering. You can set a starvation limit, to ensure that a waiting command is served immediately, when the starvation counter reaches the specified limit.
Priority Bypass	The memory controller accepts user requests to bypass the priority established by data reordering. When the controller detects a high-priority request, it allows that request to bypass the current queue. The high-priority request is then processed immediate, reducing latency.
Standard Interface	The memory controller uses Avalon® streaming as its native interface, allowing the flexibility to extend to Avalon memory-mapped interface, AXI, or a proprietary protocol with an adapter.
Avalon Memory-Mapped Data Slave Local Interface	The controller supports the Intel Avalon memory-mapped protocol.
Bank Management	The memory controller will intelligently keep a page open based on incoming traffic, improving efficiency, especially for random traffic.
Streaming Reads and Writes	The memory controller has the ability to issue reads or writes continuously to sequential addresses each clock cycle, if the bank is open. This feature allows for the passage of large amounts of data, with high efficiency.
Bank Interleaving	The memory controller has the ability to issue reads or writes continuously to random addresses. The bank addresses must be correctly cycled by user logic.
Predictive Bank Management	The memory controller has the ability to issue bank management commands early, so that the correct row is already open when a read or write request occurs. This feature allows for increased efficiency.
Quasi-1T Address/Command Half-Rate	One controller clock cycle equals two memory clock cycles in a half-rate interface. To maximize command bandwidth, the memory controller provides the option to allow two memory commands on every controller clock cycle. The controller is constrained to issue a row command on the first clock phase and a column command on the second clock phase, or vice versa. Row commands include activate and precharge commands; column commands include read and write commands.
Built-In Burst Adaptor	The memory controller has the ability to accept bursts of arbitrary size on the local interface, and map these to efficient memory commands.
Self-Refresh Controls and User Auto-Refresh Controls	The memory controller has the ability to issue self-refresh commands and allow user auto-refresh through a sideband interface.
Enable Auto Power-Down	The memory controller has the ability to power-down if no commands are received.

2.5. Intel MAX 10 External Memory Read Datapath

In Intel MAX 10 devices, instead of using DQS strobes, the memory interface solution uses internal read capture clock to capture data directly in the double data rate I/O (DDIO) registers in the I/O elements.

- The PLL supplies memory clock to the DRAM device and generates read capture clock that is frequency-locked to the incoming data stream. The read capture clock and the incoming read data stream have an arbitrary phase relationship.
- For maximum timing margin, calibration sequence is used to position the read capture clock within the optimum sampling position in the read data eye.
- Data is captured directly in the DDIO registers implemented in the I/O periphery.

2.5.1. DDR Input Registers

The DDR input capture registers in Intel MAX 10 devices are implemented in the I/O periphery.

Figure 3. External Memory Interface Read Datapath

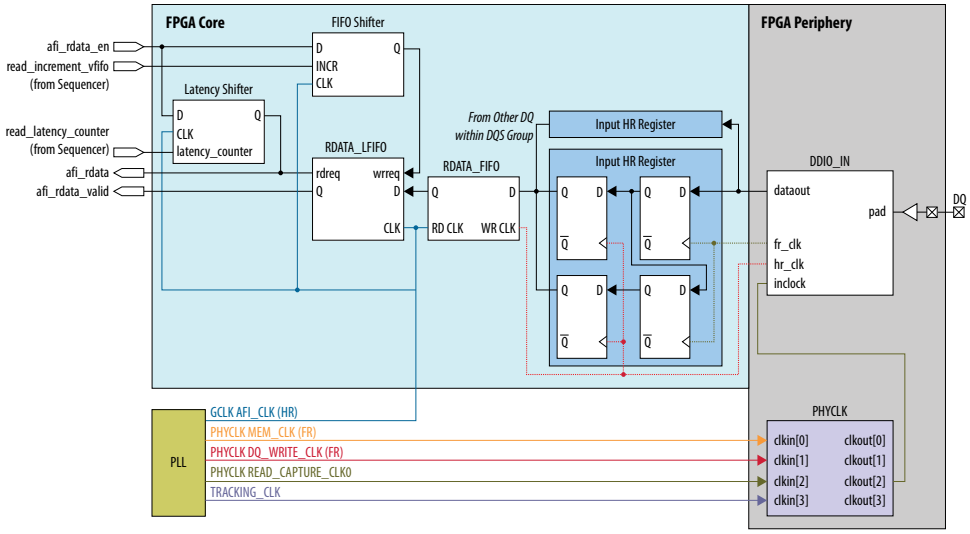
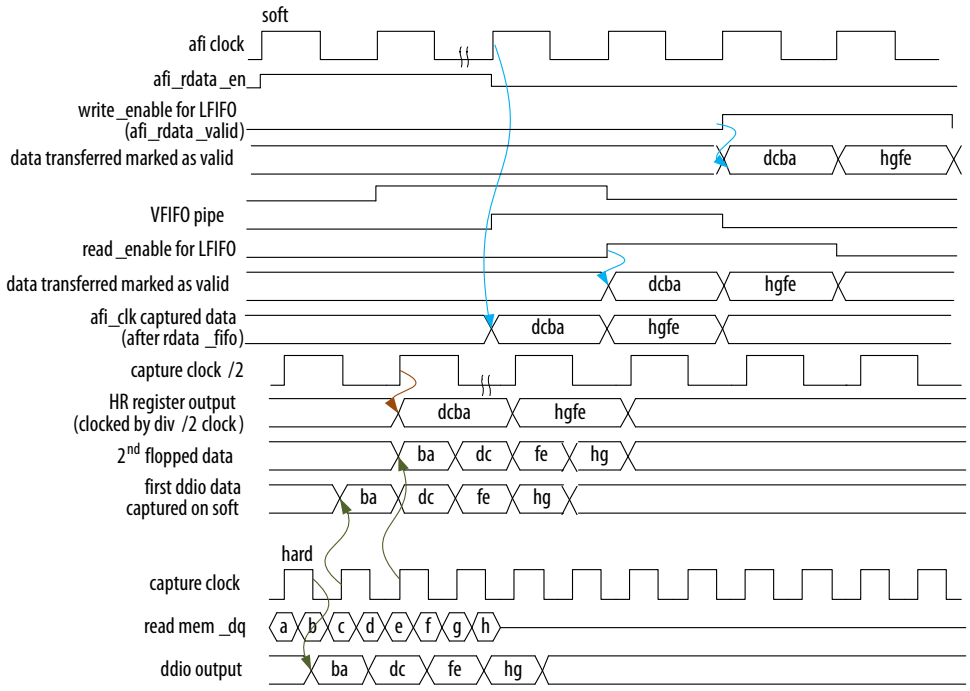


Figure 4. External Memory Interface Read Datapath Timing



In Intel MAX 10 external memory interfaces, post-amble is not a concern because the read data strobe signal, DQS, is not used during read operation.

2.6. Intel MAX 10 External Memory Write Datapath

For all DDR applications supported by Intel MAX 10 devices, the DQS strobe is sent to the external DRAM as center-aligned to the write DQ data.

The clock that clocks DDIO registers of the DQ output is phase-shifted –90º from the clock that drives the DDIO registers of the DQS strobe. This create a DQS strobe that is center-aligned to the DQ data.

The external memory write datapath is not calibrated.

2.6.1. DDR Output Registers

A dedicated DDIO write block is implemented in the DDR output and output enable paths.

Figure 5. External Memory Interface Write Datapath

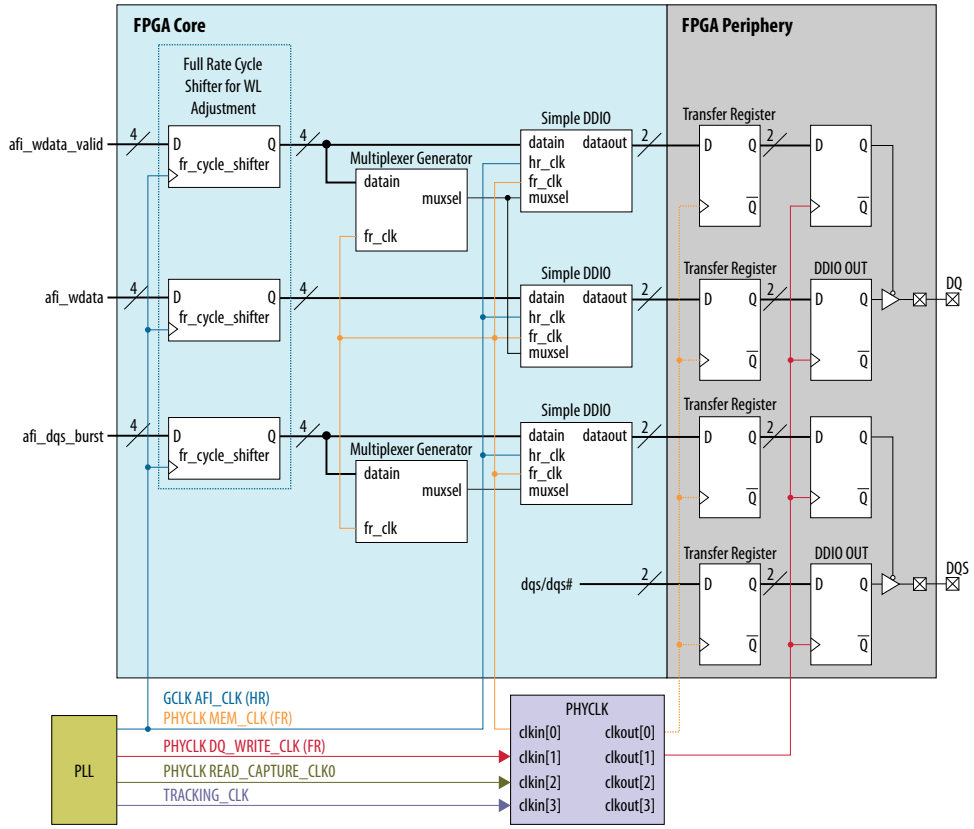
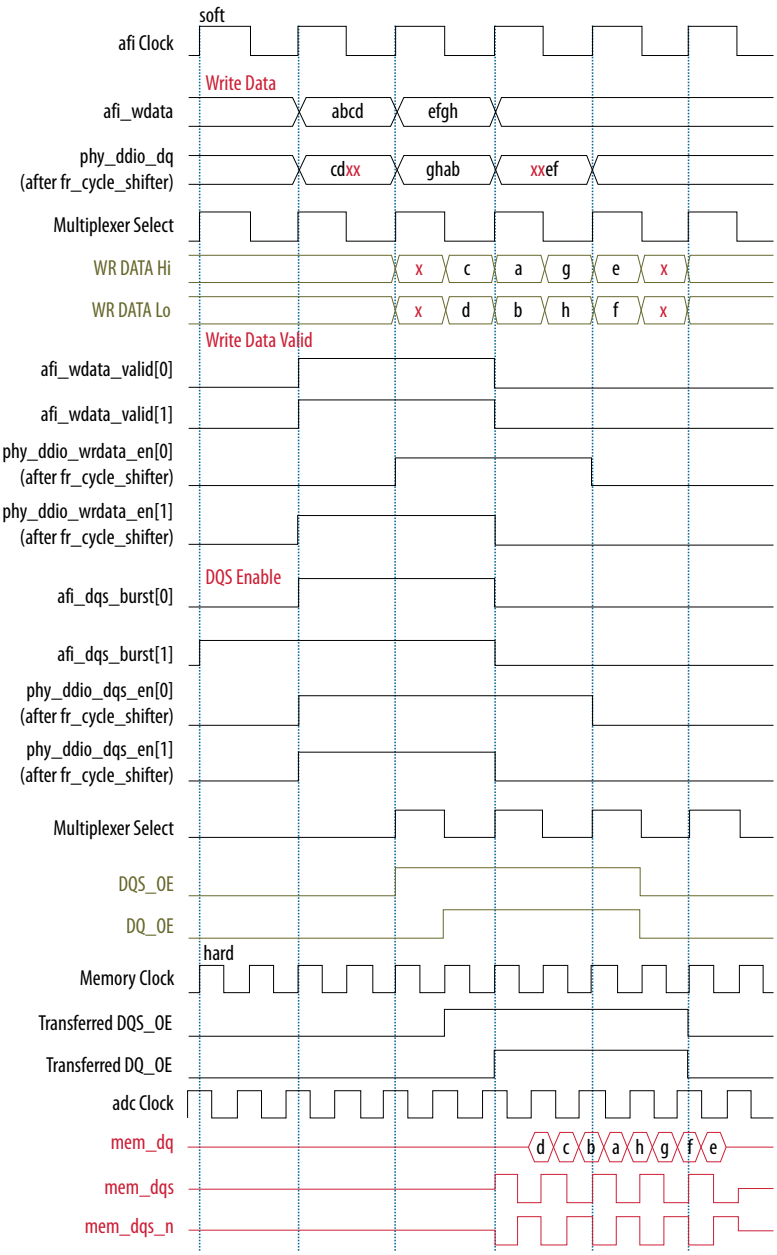


Figure 6. External Memory Interface Write Datapath Timing



2.7. Intel MAX 10 Address/Command Path

Intel's soft memory controller IP and PHY IP operate at half rate and issue address/command instructions at half-rate.

- You must send the address/command instructions to the external DRAM center-aligned with respect to the external memory clock (CK/CK#).
- For LPDDR2 applications, the address/command path is double data rate (DDR). Dedicated DDIO output registers in the I/O periphery clocks out the address/command instructions to the external DRAM.
- For DDR2/3 applications, the address/command path is single data rate (SDR). Instead of dedicated DDIO output registers, simple output I/O registers in the I/O periphery clocks out the address/command instructions to the external DRAM device.

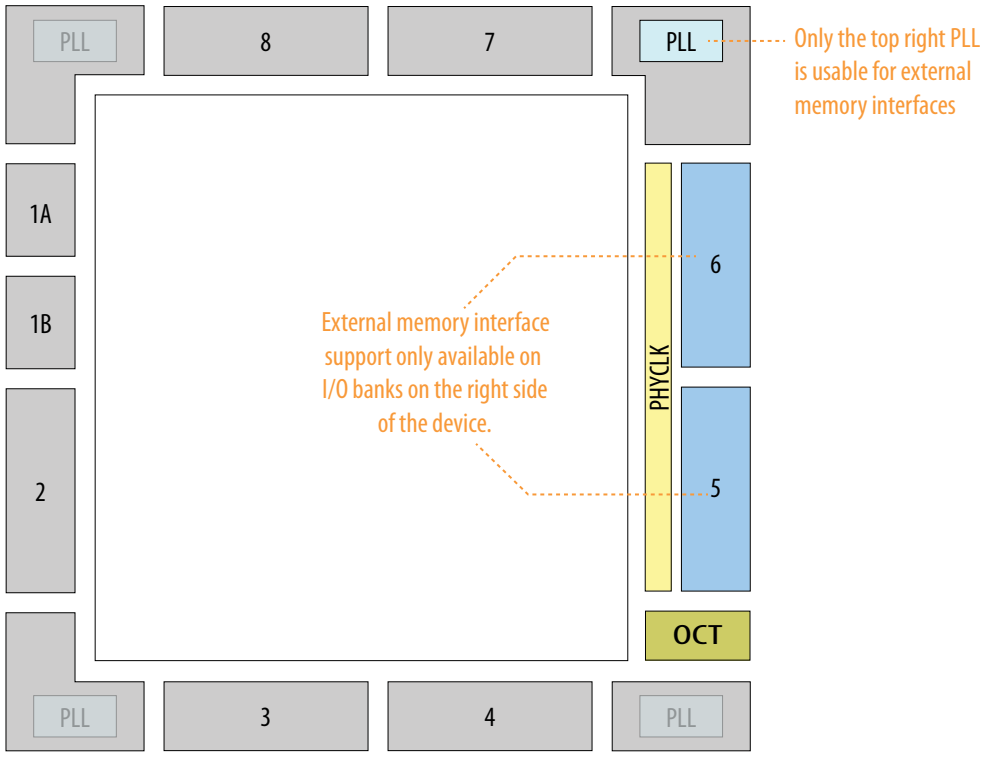
2.8. Intel MAX 10 PHY Clock (PHYCLK) Network

The PHYCLK network is a dedicated high-speed and low skew balanced clock tree that provides better clock skew for external memory interface applications.

In Intel MAX 10 devices, only the top right PLL is routed to the PHYCLK tree. Therefore, the PHYCLK tree is available only for the I/O banks on the right side of the Intel MAX 10 10M16, 10M25, 10M40, and 10M50 devices.

Figure 7. I/O Banks for External Memory Interfaces

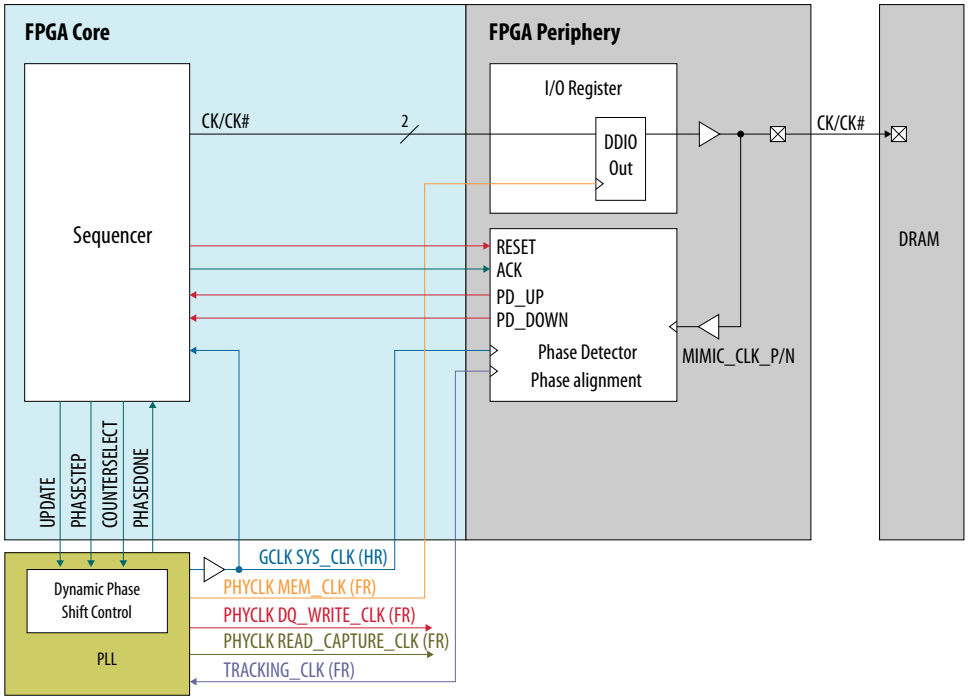
This figure represents the top view of the silicon die that corresponds to a reverse view of the device package.



2.9. Phase Detector for VT Tracking

There may be variations in the read and write paths caused by voltage and temperature changes. The phase detector keeps track of the variation of the mimic clock to optimize the system timing.

Figure 8. VT Tracking System Overview



In the Intel MAX 10 external memory interface solution, the memory clocks are used to mimic the read and write paths. The memory clock pins loop back to the phase detector as a mimic clock. The phase detector provides any variation of the mimic clock to the sequencer. The sequencer adjusts the read capture clock to match the clock phase change.

2.10. On-Chip Termination

The Intel MAX 10 devices support calibrated on-chip series termination (R_S OCT) on the right side I/O banks.

- To use the calibrated OCT, use the RUP and RDN pins for each R_S OCT control block.
- You can use each OCT calibration block to calibrate one type of termination with the same V_{CCIO}.

You must set the RUP and RDN resistor values according to the R_S OCT value. For example, if the R_S OCT value is 34 Ω, then the set both RUP and RDN value to 34 Ω.

Related Information

Intel MAX 10 On-Chip I/O Termination
Provides more information about OCT.

2.11. Phase-Locked Loop

For the external memory interface, the PLL generates the memory clock, write clock, capture clock, and the logic–core clock.

- The memory clock provides clock for DQS write strobe, and address and command signals.
- The write clock that is shifted –90° from the memory clock provides clock for DQ signals during memory writes.

You can use the PLL reconfiguration feature to calibrate the read–capture phase shift to balance the setup and hold margins. At startup, the sequencer calibrates the capture clock.

For external memory interfaces in Intel MAX 10 devices, you must use the top right PLL (PLL 2).

Related Information

PLL Locations
Provides more information about PLL location and availability in different Intel MAX 10 packages.

2.12. Intel MAX 10 Low Power Feature

The Intel MAX 10 low power feature is automatically activated when the self refresh or low power down modes are activated. The low power feature sends the `afi_mem_clk_disable` signal to stop the clock used by the controller.

To conserve power, the Intel MAX 10 UniPHY IP core performs the following functions:

- Tri-states the address and command signals except CKE and RESET_N signals
- Disables the input buffer of DDR input

Note: The Intel MAX 10 low power feature is available from version 15.0 of the Intel Quartus Prime software. To enable this feature, regenerate your Intel MAX 10 UniPHY IP core using the Intel Quartus Prime software version 15.0 or later.

3. Intel MAX 10 External Memory Interface Design Considerations

There are several considerations that require your attention to ensure the success of your designs. Unless noted otherwise, these design guidelines apply to all variants of this device family.

Related Information

- Intel MAX 10 External Memory Interface Overview on page 4
- Planning Pin and FPGA Resources chapter, External Memory Interface Handbook
  Provides pin planning guidelines for implementing external memory interfaces with Intel FPGA devices.

3.1. Intel MAX 10 DDR2 and DDR3 Design Considerations

3.1.1. DDR2/DDR3 External Memory Interface Pins

In DDR2/DDR3 interfaces, the Intel MAX 10 devices use data (DQ), data strobe (DQS), clock, address, and command pins to interface with external memory devices. The devices also use the data mask (DM) pins to enable data masking.

Related Information

DDR2/DDR3 Recommended Termination Schemes for Intel MAX 10 Devices on page 19

3.1.1.1. Intel MAX 10 Data and Data Clock (Data Strobe) Pins

For the Intel MAX 10 external memory interfaces, the DQ pins are the data pins for bidirectional read and write, and the DQS pins are the data strobe pins used only during write operations.

The Intel MAX 10 devices support bidirectional data strobes. Connect the bidirectional DQ data signals to the same Intel MAX 10 device DQ pins. The DQS pin is used only during write mode. In read mode, the Intel MAX 10 PHY generates the read capture clock internally and ignores the DQS signal. However, you must still connect DQS signal to the Intel MAX 10 DQS pin.

Related Information

Guidelines: Reading the Intel MAX 10 Pin-Out Files on page 24

3.1.1.1.1. Intel MAX 10 I/O Bank DQ/DQS Support for DDR2/DDR3

For DDR2/DDR3 SDRAM, I/O banks 5 and 6 in Intel MAX 10 devices can support DQ and DQS signals with DQ-bus widths of 8, 16 and 24 bits.

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- For DDR2 and DDR3 SDRAM interfaces, the devices use ×8 mode DQS group regardless of the interface width.
- If you need to support wider interfaces, use multiple ×8 DQ groups.
- You can use any unused DQ pins as regular user I/O pins if they are not used as memory interface signals.
- The x24 interface is implemented through x16 + ECC.

Related Information

Intel MAX 10 DQ/DQS Groups on page 7
Provides the supported DQ/DQS groups for each device.

3.1.1.2. Data Mask Pins

In Intel MAX 10 devices, the data mask (DM) pins are pre-assigned in the device pinouts. Although the Intel Quartus Prime Fitter treats the DQ and DM pins in a DQS group equally for placement purposes, the pre-assigned DQ and DM pins are the preferred pins.

Each group of DQS and DQ signals has one DM pin:

- You require data mask (DM) pins only while writing to the external memory devices.
- A low signal on the DM pin indicates that the write is valid.
- Driving the DM pin high causes the memory to mask the DQ signals.
- Similar to the DQ output signals, the DM signals are clocked by the –90º shifted clock.

3.1.1.3. DDR2/DDR3 Error Correction Coding Pins

Some DDR2 and DDR3 SDRAM devices support error correction coding (ECC). ECC is a method of detecting and automatically correcting errors in data transmission.

- In 24-bit DDR2 or DDR3 SDRAM, there are eight ECC data pins and 16 data pins.
- Connect the DDR2 and DDR3 SDRAM ECC pins to a separate DQS or DQ group in the Intel MAX 10 device.
- The memory controller needs additional logic to encode and decode the ECC data.

Related Information

ALTECC (Error Correction Code: Encoder/Decoder) chapter, Integer Arithmetic IP Cores User Guide
Provides more information about ALTECC_ENCODER and ALTECC_DECODER IPs that implement ECC functionality.

3.1.1.4. DDR2/DDR3 Address and Control/Command Pins

For DDR2/DDR3 interfaces, the address signals and the control or command signals are sent at a single data rate.

You can use any of the user I/O pins on banks 5 & 6 of Intel MAX 10 devices to generate the address and control or command signals to the external memory device.

3.1.1.5. Memory Clock Pins

At the external memory device, the memory clock signals (CK and CK#) are used to capture the address signals, and the control or command signals.

In Intel MAX 10 devices, the double data rate I/O (DDIO) registers are used to generate the CK/CK# signals.

The memory clock pins are predefined and are listed in the device pinout files. Refer to the relevant device pinout files to determine the locations of the memory clock pins.

Related Information

- Pin Connection Guidelines Tables, Planning Pin and FPGA Resources chapter, External Memory Interface Handbook
  Provides more information about CK/CK# pins placement.
- Intel MAX 10 Device Pin-Out Files

3.1.2. DDR2/DDR3 Recommended Termination Schemes for Intel MAX 10 Devices

If you are creating interfaces with multiple DDR2 or DDR3 components where the address, command, and memory clock pins are connected to more than one load, follow these steps:

1. Simulate the system to get the new slew rate for the DQ/DQS, DM, address and command, and clock signals.
2. Use the derated t_{IS} and t_{IH} specifications from the DDR2 or DDR3 datasheet based on the simulation results.
3. If timing deration causes your interface to fail timing requirements, consider duplication of these signals to lower their loading, and hence improve timing.

Note: Class I and Class II termination schemes in the following tables refer to drive strength and not physical termination.

Table 5. Termination Recommendations for Intel MAX 10 DDR2 Component

Signal Type	SSTL 18 I/O Standard	FPGA–End Discrete Termination	Memory–End Termination 1	Memory I/O Standard
DQ/DQS	Class I Rs = 50 Ω	50 Ω parallel to V_{TT} discrete	ODT75(4)	HALF(5)
DM	Class I Rs = 50 Ω	—	ODT75(4)	HALF(5)
Address and command	Class I with maximum drive strength	—	56 Ω parallel to V_{TT} discrete	—
Clock	Differential Class I Rs = 50 Ω	—	• x1 = 100 Ω differential(6) • x2 = 200 Ω differential(7)	—

(4) ODT75 vs. ODT50 on the memory has the effect of opening the eye more, with a limited increase in overshoot/undershoot.

(5) HALF is reduced drive strength.

(6) x1 is a single-device load.

Table 6. On Board Termination Recommendation for Intel MAX 10 DDR3 Component

For Intel MAX 10 devices, on board termination is required for DDR3 component.

I/O Standard	R_S OCT	On Board Termination	
		FPGA–End	Memory-End
SSTL 15 Class 1	50 Ω without calibration	80 Ω resistor	40 Ω resistor

Table 7. Supported External Memory Interface Termination Scheme for DDR3 and DDR2

Memory Interface Standard	I/O Standard	R_S OCT	R_{UP}, R_{DN} (Ω)
DDR3	SSTL-15	25	25
		34	34
		40	40
		50	50
DDR3L	SSTL-135	34	34
		40	40
DDR2	SSTL-18	25	25
		50	50

Related Information

Planning Pin and FPGA Resources
Provides more information about termination and signal duplication.

3.2. LPDDR2 Design Considerations

Note: Intel MAX 10 devices support single-die LPDDR2 only.

3.2.1. LPDDR2 External Memory Interface Pins

In LPDDR2 interfaces, the Intel MAX 10 devices use data (DQ), data strobe (DQS), clock, command, and address pins to interface with external memory devices. The devices also use the data mask (DM) pins to enable data masking.

3.2.1.1. Intel MAX 10 Data and Data Clock (Data Strobe) Pins

For the Intel MAX 10 external memory interfaces, the DQ pins are the data pins for bidirectional read and write, and the DQS pins are the data strobe pins used only during write operations.

The Intel MAX 10 devices support bidirectional data strobes. Connect the bidirectional DQ data signals to the same Intel MAX 10 device DQ pins. The DQS pin is used only during write mode. In read mode, the Intel MAX 10 PHY generates the read capture clock internally and ignores the DQS signal. However, you must still connect DQS signal to the Intel MAX 10 DQS pin.

(7) x2 is a two-device load.

Related Information

Guidelines: Reading the Intel MAX 10 Pin-Out Files on page 24

3.2.1.1.1. Intel MAX 10 I/O Bank DQ/DQS Support for LPDDR2

For LPDDR2 SDRAM, I/O banks 5 and 6 in Intel MAX 10 devices can support DQ and DQS signals with DQ-bus widths of 8 and 16 bits.

- For LPDDR2 SDRAM interfaces, the devices use ×8 mode DQS group regardless of the interface width.
- If you need to support wider interfaces, use multiple ×8 DQ groups.
- You can use any unused DQ pins as regular user I/O pins if they are not used as memory interface signal.

Related Information

Intel MAX 10 DQ/DQS Groups on page 7
Provides the supported DQ/DQS groups for each device.

3.2.1.2. Data Mask Pins

In Intel MAX 10 devices, the data mask (DM) pins are pre-assigned in the device pinouts. Although the Intel Quartus Prime Fitter treats the DQ and DM pins in a DQS group equally for placement purposes, the pre-assigned DQ and DM pins are the preferred pins.

Each group of DQS and DQ signals has one DM pin:

- You require data mask (DM) pins only while writing to the external memory devices.
- A low signal on the DM pin indicates that the write is valid.
- Driving the DM pin high causes the memory to mask the DQ signals.
- Similar to the DQ output signals, the DM signals are clocked by the –90º shifted clock.

3.2.1.3. LPDDR2 Address and Control/Command Pins

For LPDDR2 interfaces, the address signals and the control or command signals are sent at double data rate.

You can use any of the user I/O pins on banks 5 & 6 of Intel MAX 10 devices to generate the address and control or command signals to the external memory device.

3.2.1.4. Memory Clock Pins

At the external memory device, the memory clock signals (CK and CK#) are used to capture the address signals, and the control or command signals.

In Intel MAX 10 devices, the double data rate I/O (DDIO) registers are used to generate the CK/CK# signals.

The memory clock pins are predefined and are listed in the device pinout files. Refer to the relevant device pinout files to determine the locations of the memory clock pins.

Related Information

- Pin Connection Guidelines Tables, Planning Pin and FPGA Resources chapter, External Memory Interface Handbook
  Provides more information about CK/CK# pins placement.
- Intel MAX 10 Device Pin-Out Files

3.2.2. LPPDDR2 Power Supply Variation Constraint

For an LPDDR2 interface that targets 200 MHz, constrain the memory device I/O and core power supply variation to within ±3%.

- Memory I/O power supply pin is VDDQ
- Memory core power supply pin is VDD

Related Information

Intel MAX 10 Power Management User Guide

3.2.3. LPDDR2 Recommended Termination Schemes for Intel MAX 10 Devices

Table 8. Supported External Memory Interface Termination Scheme for LPDDR2

Memory Interface Standard	I/O Standard	R_S OCT	R_{UP}, R_{DN} (Ω)
LPDDR2	HSUL-12	34, 40, 48	34, 40, 48

3.3. Guidelines: Intel MAX 10 DDR3, DDR2, and LPDDR2 External Memory Interface I/O Limitation

While implementing certain external memory interface standards, the number of I/O pins available is limited.

- While implementing DDR2—for 25 percent of the remaining I/O pins available in I/O banks 5 and 6, you can assign them only as input pins.
- While implementing DDR3 or LPDDR2—the I/O pins listed in the following table are not available for use. Of the remaining I/O pins, you can assign only 75 percent of the available I/O pins in I/O banks 5 and 6 for normal I/O operation.

Table 9. Unavailable I/O Pins While Implementing DDR3 or LPDDR2 External Memory Interfaces in Certain Device Packages—Preliminary

Device	Package			
	F256	U324	F484	F672
10M16	N16 P16	R15 P15 R18 P18 E16 D16	U21 U22 M21 L22 F21 F20 E19	—

continued...

Device	Package			
	F256	U324	F484	F672
			F18	
10M25	N16 P16	—	U21 U22 M21 L22 F21 F20 E19 F18 F17 E17	—
10M40 10M50	N16 P16	—	U21 U22 M21 L22 F21 F20 E19 F18 F17 E17	W23 W24 U25 U24 T24 R25 R24 P25 K23 K24 J23 H23 G23 F23 G21 G22

3.4. Guidelines: Intel MAX 10 Board Design Requirement for DDR2, DDR3, and LPDDR2

- For DDR2, DDR3, and LPDDR2 interfaces, the maximum board skew between pins must be lower than 40 ps. This guideline applies to all pins (address, command, clock, and data).
- To minimize unwanted inductance from the board via, Intel recommends that you keep the PCB via depth for V_{CCIO} banks below 49.5 mil.
- For devices with DDR3 interface implementation, onboard termination is required for the DQ, DQS, and address signals. Intel recommends that you use termination resistor value of 80 Ω to V_{TT}.
- For the DQ, address, and command pins, keep the PCB trace routing length less than six inches for DDR3, or less than three inches for LPDDR2.

Related Information

- External Memory Interface Handbook Volume 1: Intel FPGA Memory Solution Overview and Design Flow
  Provides more information about using Intel FPGA devices for external memory interfaces including Intel FPGA memory solutions and design flow.

- External Memory Interface Handbook Volume 2: Design Guidelines
  Provides more information about using Intel FPGA devices for external memory interfaces including memory selection, board design, implementing memory IPs, timing, optimization, and debugging.
- Functional Description—Intel MAX 10 EMIF IP
  Provides more information about implementing memory IPs for Intel MAX 10 devices.
- Intel MAX 10 FPGA Signal Integrity Design Guidelines
  Provides design guidelines related to signal integrity for Intel MAX 10 devices.

3.5. Guidelines: Reading the Intel MAX 10 Pin-Out Files

For the maximum number of DQ pins and the exact number per group for a particular Intel MAX 10 device, refer to the relevant device pin-out files.

In the pin-out files, the DQS and DQSn pins denote the differential data strobe/clock pin pairs. The DQS and DQSn pins are listed in the Intel MAX 10 pin-out files as DQS*X*R and DQSn*X*R:

- *X* indicates the DQ/DQS grouping number.
- R indicates the location of the group which is always on the right side of the device.

4. Intel MAX 10 External Memory Interface Implementation Guides

You can implement your external memory interface design in the Intel Quartus Prime software. The software contains tools for you to create and compile you design, and configure your device.

In the Intel Quartus Prime software, you can instantiate and configure the UniPHY IP core to suit your memory interface requirement.

Related Information

- Intel MAX 10 External Memory Interface Overview on page 4
- External Memory Interface Handbook Volume 1: Intel FPGA Memory Solution Overview and Design Flow
  Provides more information about using Intel FPGA devices for external memory interfaces including Intel FPGA memory solutions and design flow.
- External Memory Interface Handbook Volume 2: Design Guidelines
  Provides more information about using Intel FPGA devices for external memory interfaces including memory selection, board design, implementing memory IPs, timing, optimization, and debugging.
- Functional Description—Intel MAX 10 EMIF IP
  Provides more information about implementing memory IPs for Intel MAX 10 devices.
- Intel MAX 10 DDR3 Reference Design
  Provides DDR3 UniPHY IP core reference design for Intel MAX 10 devices.

4.1. UniPHY IP Core

The UniPHY IP core allows you to control the soft IP of the Intel MAX 10 external memory interface solution.

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*Other names and brands may be claimed as the property of others.

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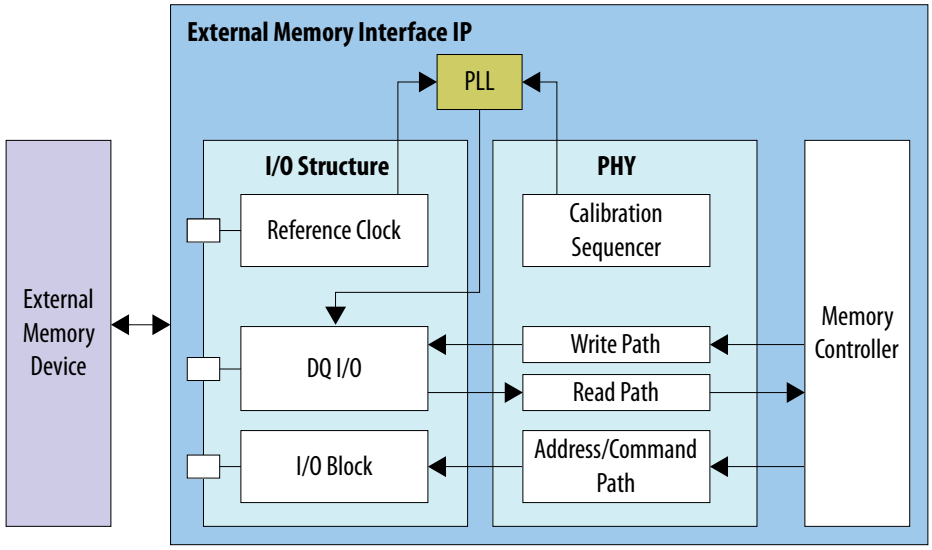
Figure 9. Intel MAX 10 UniPHY IP Core Block Diagram

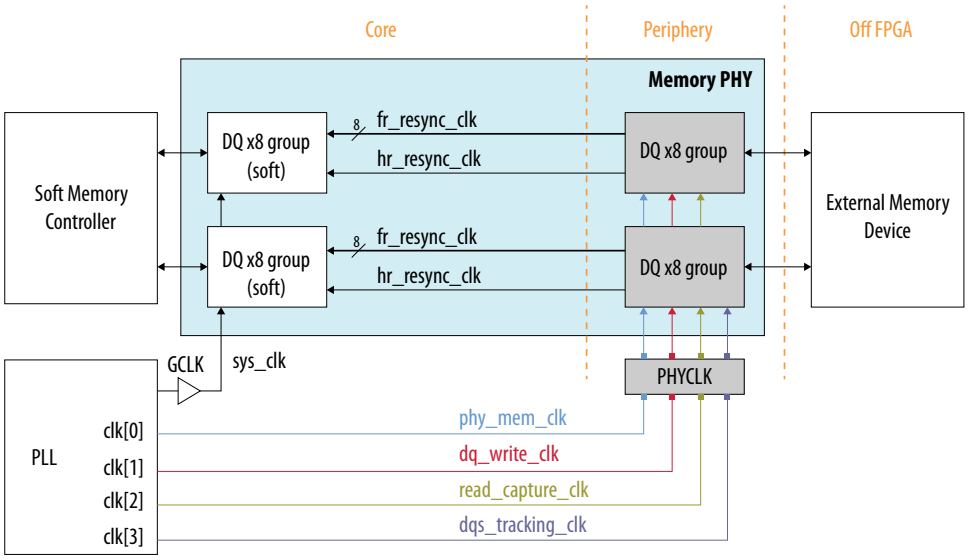


Related Information

- Introduction to Intel FPGA IP Cores
  Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- Creating Version-Independent IP and Qsys Simulation Scripts
  Create simulation scripts that do not require manual updates for software or IP version upgrades.
- Project Management Best Practices
  Guidelines for efficient management and portability of your project and IP files.

4.2. LPDDR2 External Memory Interface Implementation

Figure 10. Top Level View of LPDDR2 Architecture in Intel MAX 10 Devices



Related Information

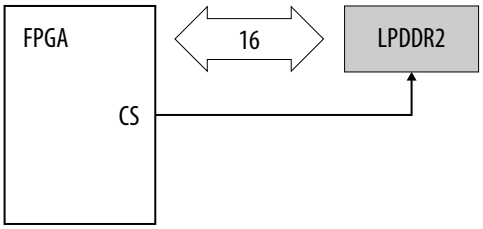
Planning Pin and FPGA Resources chapter, External Memory Interface Handbook
Provides the maximum number of interfaces supported by Intel MAX 10 devices for each memory standards, pin counts for various external memory interface implementation examples, and information about the clock, address/command, data, data strobe, DM, and optional ECC signals.

4.2.1. Supported LPDDR2 Topology

For LPDDR2, the external memory interface IP for Intel MAX 10 devices uses one capture clock and one tracking clock with one discrete device.

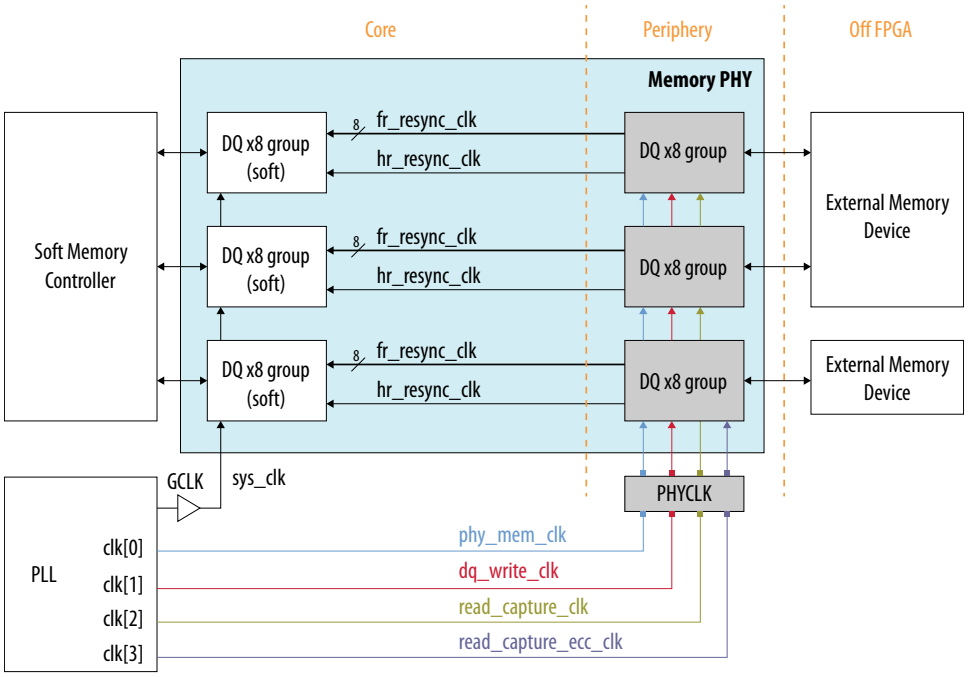
Figure 11. Supported Topology for LPDDR2 Memory Interfaces

This figure shows the supported LPDDR2 topology. Only one discrete LPDDR2 device is supported with a 16 bit maximum interface width. The memory interface IP in Intel MAX 10 devices generates LPDDR2 IPs targeted for this configuration only.



4.3. DDR2 and DDR3 External Memory Interface Implementation

Figure 12. Top Level View of DDR2, DDR3, or DDR3L Architecture in Intel MAX 10 Devices



Related Information

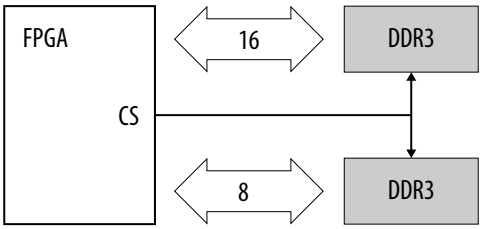
Planning Pin and FPGA Resources chapter, External Memory Interface Handbook
Provides the maximum number of interfaces supported by Intel MAX 10 devices for each memory standards, pin counts for various external memory interface implementation examples, and information about the clock, address/command, data, data strobe, DM, and optional ECC signals.

4.3.1. Intel MAX 10 Supported DDR2 or DDR3 Topology

For DDR2 or DDR3/DDR3L, the external memory interface IP for Intel MAX 10 devices uses two capture clocks with two discrete devices.

Figure 13. Supported Topology for DDR2 or DDR3 Memory Interfaces

This figure shows the supported DDR2/DDR3 topology. One clock captures the lower 16 bit of data and the other clock captures the top 8 bit of data. The memory interface IP in Intel MAX 10 devices generates DDR2 or DDR3/DDR3L IPs targeted for this configuration only.



5. UniPHY IP References for Intel MAX 10 Devices

For Intel MAX 10 devices, there are three variations of the UniPHY IPs:

- DDR2 SDRAM Controller with UniPHY Intel FPGA IP
- DDR3 SDRAM Controller with UniPHY Intel FPGA IP
- LPDDR2 SDRAM Controller with UniPHY Intel FPGA IP

Related Information

- Intel MAX 10 External Memory Interface Overview on page 4
- External Memory Interface Handbook Volume 1: Intel FPGA Memory Solution Overview and Design Flow
  Provides more information about using Intel FPGA devices for external memory interfaces including Intel FPGA memory solutions and design flow.
- External Memory Interface Handbook Volume 2: Design Guidelines
  Provides more information about using Intel FPGA devices for external memory interfaces including memory selection, board design, implementing memory IPs, timing, optimization, and debugging.
- Functional Description—Intel MAX 10 EMIF IP
  Provides more information about implementing memory IPs for Intel MAX 10 devices.

5.1. UniPHY Parameter Settings for Intel MAX 10

You can set the parameter settings for the UniPHY IP core in the Intel Quartus Prime software. There are six groups of options: **PHY Settings**, **Memory Parameters**, **Memory Timing**, **Board Settings**, **Controller Settings**, and **Diagnostics**.

Note: Intel MAX 10 devices are not supported in the EMIF Debug Toolkit.

5.1.1. UniPHY Parameters—PHY Settings

There are three groups of options: **General Settings**, **Clocks**, and **Advanced PHY Settings**.

Table 10. PHY Settings - General Settings

Parameter	Description
Speed Grade	Specifies the speed grade of the targeted FPGA device that affects the generated timing constraints and timing reporting. *Note:* For Intel MAX 10 devices, DDR3 and LPDDR2 is supported only for speed grade –6, and DDR2 for speed grades –6 and –7.
Generate PHY only	Turn on this option to generate the UniPHY IP without a memory controller.

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Parameter	Description
	When you turn on this option, the AFI interface is exported so that you can easily connect your own memory controller.

Table 11. PHY Settings - Clocks

Parameter	Description
Memory clock frequency	The frequency of the clock that drives the memory device. Use up to 4 decimal places of precision. To obtain the maximum supported frequency for your target memory configuration, refer to the External Memory Spec Estimator page on www.intel.com.
Achieved memory clock frequency	The actual frequency the PLL generates to drive the external memory interface (memory clock).
PLL reference clock frequency	The frequency of the input clock that feeds the PLL. Use up to 4 decimal places of precision.
Rate on Avalon-MM interface	The width of data bus on the Avalon memory-mapped interface. The Intel MAX 10 supports only **Half** rate, which results in a width of 4× the memory data width.
Achieved local clock frequency	The actual frequency the PLL generates to drive the local interface for the memory controller (AFI clock).

Table 12. DDR3 SDRAM PHY Settings - Advanced PHY Settings

Parameter	Description
Supply voltage	The supply voltage and sub-family type of memory. This option is available for DDR3 SDRAM only.
I/O standard	The I/O standard voltage. Set the I/O standard according to your design's memory standard.
Reconfigurable PLL location	If you set the PLL used in the UniPHY IP memory interface to be reconfigurable at run time, you must specify the location of the PLL. This assignment generates a PLL that can only be placed in the given sides.

Related Information

External Memory Interface Spec Estimator
Provides a parametric tool that allows you to find and compare the performance of the supported external memory interfaces in Intel FPGA devices.

5.1.2. UniPHY Parameters—Memory Parameters

There are three groups of options: **Memory Parameters**, **Memory Topology**, and **Memory Initialization Options**.

Table 13. Memory Parameters

Use the **Memory Parameters** options group to apply the memory parameters from your memory manufacturer's data sheet.

Parameter	Description
Memory vendor	The vendor of the memory device. Select the memory vendor according to the memory vendor you use. For memory vendors that are not listed in the setting, select JEDEC with the nearest memory parameters and edit the parameter values according to the values of
	continued...

Parameter	Description
	the memory vendor that you use. However, if you select a configuration from the list of memory presets, the default memory vendor for that preset setting is automatically selected.
Memory format	The format of the memory device. This parameter is automatically set to **Discrete Device**.
Memory device speed grade	The maximum frequency at which the memory device can run.
Total interface width	The total number of DQ pins of the memory device. Limited to 8 to 24 bits.
DQ/DQS group size	The number of DQ bits per DQS group.
Number of DQS groups	The number of DQS groups is calculated automatically from the **Total interface width** and the **DQ/DQS group size** parameters.
Number of chip selects	The number of chip-selects the IP core uses for the current device configuration. Specify the total number of chip-selects according to the number of memory device.
Number of clocks	The width of the clock bus on the memory interface.
Row address width	The width of the row address on the memory interface.
Column address width	The width of the column address on the memory interface.
Bank-address width	The width of the bank address bus on the memory interface.
Enable DM pins	Specifies whether the DM pins of the memory device are driven by the FPGA. You can turn off this option to avoid overusing FPGA device pins when using x4 mode memory devices. When you are using x4 mode memory devices, turn off this option for DDR3 SDRAM. You must turn on this option if you are using Avalon byte enable.
DQS# Enable	Turn on differential DQS signaling to improve signal integrity and system performance. This option is available for DDR2 SDRAM only.

Table 14. Memory Parameters - Memory Initialization Options (DDR3 SDRAM)

This table lists the memory initialization options for DDR3 SDRAM.

Parameter		Description
Mode Register 0	**Read burst type**	Specifies accesses within a given burst in sequential or interleaved order. Specify sequential ordering for use with the memory controller. Specify interleaved ordering only for use with an interleaved-capable custom controller, when the **Generate PHY only** parameter is enabled on the PHY Settings tab.
	DLL precharge power down	Specifies whether the DLL in the memory device is off or on during precharge power-down.
	Memory CAS latency setting	The number of clock cycles between the read command and the availability of the first bit of output data at the memory device and also interface frequency. Refer to memory vendor data sheet speed bin table. Set this parameter according to the target memory speed grade and memory clock frequency.
Mode Register 1	**Output drive strength setting**	The output driver impedance setting at the memory device. To obtain the optimum signal integrity performance, select the optimum setting based on the board simulation results.
	Memory additive CAS latency setting	The posted CAS additive latency of the memory device. Enable this feature to improve command and bus efficiency, and increase system bandwidth. For more information about optimizing the memory controller, refer to related information.

continued...

Parameter		Description
	ODT Rtt nominal value	The on-die termination resistance at the memory device. To obtain the optimum signal integrity performance, select the optimum setting based on the board simulation results.
Mode Register 2	**Auto selfrefresh method**	Disable or enable auto selfrefresh.
	Selfrefresh temperature	Specifies the selfrefresh temperature as **Normal** or **Extended**.
	Memory write CAS latency setting	The number of clock cycles from the releasing of the internal write to the latching of the first data in, at the memory device and also interface frequency. Refer to memory vendor data sheet speed bin table and set according to the target memory speed grade and memory clock frequency.
	Dynamic ODT (Rtt_WR) value	The mode of the dynamic ODT feature of the memory device. This is used for multi-rank configurations. For more guidelines about DDR2 and DDR3 SDRAM board layout, refer to the related information. To obtain the optimum signal integrity performance, select the optimum setting based on the board simulation results.

Table 15. Memory Parameters - Memory Initialization Options (DDR2 SDRAM)

This table lists the memory initialization options for DDR2 SDRAM.

Parameter		Description
Mode Register 0	**Burst length**	Specifies the burst length.
	Read burst type	Specifies accesses within a given burst in sequential or interleaved order. Specify sequential ordering for use with the memory controller. Specify interleaved ordering only for use with an interleaved-capable custom controller, when the **Generate PHY only** parameter is enabled on the PHY Settings tab.
	DLL precharge power down	Determines whether the DLL in the memory device is in slow exit mode or in fast exit mode during precharge power down. For more information, refer to memory vendor data sheet.
	Memory CAS latency setting	Determines the number of clock cycles between the READ command and the availability of the first bit of output data at the memory device. For more information, refer to memory vendor data sheet speed bin table. Set this parameter according to the target memory speed grade and memory clock frequency.
Mode Register 1	**Output drive strength setting**	Determines the output driver impedance setting at the memory device. To obtain the optimum signal integrity performance, select the optimum setting based on the board simulation results.
	Memory additive CAS latency setting	Determines the posted CAS additive latency of the memory device. Enable this feature to improve command and bus efficiency, and increase system bandwidth.
	Memory on-die termination (ODT) setting	Determines the on-die termination resistance at the memory device. To obtain the optimum signal integrity performance, select the optimum setting based on the board simulation results.
Mode Register 2	**SRT Enable**	Determines the selfrefresh temperature (SRT). Select **1x refresh rate** for normal temperature (0-85C)or select **2x refresh rate** for high temperature (>85C).

Table 16. Memory Parameters - Memory Initialization Options (LPDDR2 SDRAM)

This table lists the memory initialization options for LPDDR2 SDRAM.

Parameter		Description
Mode Register 1	**Burst Length**	Specifies the burst length.
	Read Burst Type	Specifies accesses within a given burst in sequential or interleaved order. Specify sequential ordering for use with the memory controller. Specify interleaved ordering only for use with an interleaved-capable custom controller, when the **Generate PHY only** parameter is enabled on the PHY Settings tab.
Mode Register 2	**Read latency setting**	Determines the number of clock cycles between the READ command and the availability of the first bit of output data at the memory device. Set this parameter according to the target memory interface frequency. Refer to memory data sheet and also target memory speed grade.
Mode Register 3	**Output drive strength settings**	Determines the output driver impedance setting at the memory device. To obtain the optimum signal integrity performance, select the optimum setting based on the board simulation results.

Related Information

- External Memory Interface Handbook Volume 1: Intel FPGA Memory Solution Overview and Design Flow
  Provides more information about using Intel FPGA devices for external memory interfaces including Intel FPGA memory solutions and design flow.
- External Memory Interface Handbook Volume 2: Design Guidelines
  Provides more information about using Intel FPGA devices for external memory interfaces including memory selection, board design, implementing memory IPs, timing, optimization, and debugging.
- Functional Description—Intel MAX 10 EMIF IP
  Provides more information about implementing memory IPs for Intel MAX 10 devices.

5.1.3. UniPHY Parameters—Memory Timing

Use the **Memory Timing** options to apply the memory timings from your memory manufacturer's data sheet.

Table 17. Memory Timing

For each parameter, refer to the memory vendor data sheet.

Parameter	Applies To	Description	Set According To
tIS (base)	DDR2, DDR3, LPDDR2	Address and control setup to CK clock rise.	Memory speed grade
tIH (base)	DDR2, DDR3, LPDDR2	Address and control hold after CK clock rise.	Memory speed grade
tDS (base)	DDR2, DDR3, LPDDR2	Data setup to clock (DQS) rise.	Memory speed grade
tDH (base)	DDR2, DDR3, LPDDR2	Data hold after clock (DQS) rise.	Memory speed grade
tDQSQ	DDR2, DDR3, LPDDR2	DQS, DQS# to DQ skew, per access.	Memory speed grade

continued...

Parameter	Applies To	Description	Set According To
tQHS	DDR2, LPDDR2	DQ output hold time from DQS, DQS# (absolute time value).	Memory speed grade
tQH	DDR3	DQ output hold time from DQS, DQS# (percentage of tCK).	Memory speed grade
tDQSCK	DDR2, DDR3	DQS output access time from CK/CK#.	Memory speed grade
tDQSCK (max)	LPDDR2		
tDQSCK Delta Short	LPDDR2	Absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a contiguous sequence of bursts within a 160 ns rolling window.	Memory speed grade
tDQSCK Delta Medium	LPDDR2	Absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a contiguous sequence of bursts within a 1.6 µs rolling window.	Memory speed grade
tDQSCK Delta Long	LPDDR2	Absolute value of the difference between any two tDQSCK measurements (within a byte lane) within a contiguous sequence of bursts within a 32ms rolling window.	Memory speed grade
tDQSS	DDR2, DDR3, LPDDR2	First latching edge of DQS to associated clock edge (percentage of tCK).	Memory speed grade
tDQSH	DDR2, LPDDR2	DQS Differential High Pulse Width (percentage of tCK). Specifies the minimum high time of the DQS signal received by the memory.	Memory speed grade
tQSH	DDR3		
tDSH	DDR2, DDR3, LPDDR2	DQS falling edge hold time from CK (percentage of tCK).	Memory speed grade
tDSS	DDR2, DDR3, LPDDR2	DQS falling edge to CK setup time (percentage of tCK).	Memory speed grade
tINIT	DDR2, DDR3, LPDDR2	Memory initialization time at power-up.	Memory speed grade
tMRD	DDR2, DDR3	Load mode register command period.	Memory speed grade
tMRW	LPDDR2		
tRAS	DDR2, DDR3, LPDDR2	Active to precharge time.	Memory speed grade
tRCD	DDR2, DDR3, LPDDR2	Active to read or write time.	Memory speed grade
tRP	DDR2, DDR3, LPDDR2	Precharge command period.	Memory speed grade
tREFI	DDR2, DDR3	Refresh command interval.	Memory speed grade and temperature range
tREFIab	LPDDR2	Refresh command interval (all banks).	Memory speed grade
tRFC	DDR2, DDR3	Auto-refresh command interval.	Memory device capacity
tRFCab	LPDDR2	Auto-refresh command interval (all banks).	Memory device capacity
tWR	DDR2, DDR3, LPDDR2	Write recovery time.	Memory speed grade

continued...

Parameter	Applies To	Description	Set According To
tWTR	DDR2, DDR3, LPDDR2	Write to read period. Calculate the value based on the memory clock frequency.	Memory speed grade and memory clock frequency
tFAW	DDR2, DDR3, LPDDR2	Four active window time.	Memory speed grade and page size
tRRD	DDR2, DDR3, LPDDR2	RAS to RAS delay time. Calculate the value based on the memory clock frequency.	Memory speed grade, page size and memory clock frequency
tRTP	DDR2, DDR3, LPDDR2	Read to precharge time. Calculate the value based on the memory clock frequency.	Memory speed grade and memory clock frequency

5.1.4. UniPHY Parameters—Board Settings

There are three groups of options: **Setup and Hold Derating**, **Channel Signal Integrity**, and **Board Skews**.

Table 18. Board Settings - Setup and Hold Derating

The slew rate of the output signals affects the setup and hold times of the memory device, and thus the write margin. You can specify the slew rate of the output signals to see their effect on the setup and hold times of both the address and command signals and the DQ signals, or alternatively, you may want to specify the setup and hold times directly. You should enter information derived during your PCB development process of prelayout (line) and postlayout (board) simulation.

Parameter	Description
Derating method	Derating method. The default settings are based on Intel internal board simulation data. To obtain accurate timing analysis according to the condition of your board, Intel recommends that you perform board simulation and enter the slew rate in the Intel Quartus Prime software to calculate the derated setup and hold time automatically or enter the derated setup and hold time directly.
CK/CK# slew rate (differential)	CK/CK# slew rate (differential).
Address/Command slew rate	Address and command slew rate.
DQS/DQS# slew rate (Differential)	DQS and DQS# slew rate (differential).
DQ slew rate	DQ slew rate.
tIS	Address/command setup time to CK.
tIH	Address/command hold time from CK.
tDS	Data setup time to DQS.
tDH	Data hold time from DQS.

Table 19. Board Settings - Channel Signal Integrity

Channel signal integrity is a measure of the distortion of the eye due to intersymbol interference, crosstalk, or other effects. Typically, when going from a single-rank configuration to a multi-rank configuration there is an increase in the channel loss, because there are multiple stubs causing reflections. Although the Intel Quartus Prime timing models include some channel uncertainty, you must perform your own channel signal integrity simulations and enter the additional channel uncertainty, relative to the reference eye, into the parameter editor.

Parameter	Description
Derating method	Choose between default Intel settings (with specific Intel boards) or manually enter board simulation numbers obtained for your specific board.
Address and command eye reduction (setup)	The reduction in the eye diagram on the setup side (or left side of the eye) due to ISI on the address and command signals compared to a case when there is no ISI. (For single rank designs, ISI can be zero; in multirank designs, ISI is necessary for accurate timing analysis.)
Address and command eye reduction (hold)	The reduction in the eye diagram on the hold side (or right side of the eye) due to ISI on the address and command signals compared to a case when there is no ISI.
Write DQ eye reduction	The total reduction in the eye diagram due to ISI on DQ signals compared to a case when there is no ISI. Intel assumes that the ISI reduces the eye width symmetrically on the left and right side of the eye.
Read DQ eye reduction	
Write Delta DQS arrival time	The increase in variation on the range of arrival times of DQS compared to a case when there is no ISI. Intel assumes that the ISI causes DQS to further vary symmetrically to the left and to the right.
Read Delta DQS arrival time	

Table 20. Board Settings - Board Skews

PCB traces can have skews between them that can reduce timing margins. Furthermore, skews between different chip selects can further reduce the timing margin in multiple chip-select topologies. This section allows you to enter parameters to compensate for these variations.

Note: Intel recommends that you use the Board Skew Parameter Tool to help you calculate the board skews. For more information, refer to the related information section.

Parameter	Description
Maximum CK delay to DIMM/ device	The delay of the longest CK trace from the FPGA to the memory device is expressed by the following equation: $$max_r\left[max_n\left(CK_{n\_r}PathDelay\right)\right]$$ Where *n* is the number of memory clock and *r* is number rank of device.
Maximum DQS delay to DIMM/ device	The delay of the longest DQS trace from the FPGA to the memory device, whether on a DIMM or the same PCB as the FPGA is expressed by the following equation: $$max_r\left[max_n\left(DQS_{n\_r}PathDelay\right)\right]$$ Where *n* is the number of DQS and *r* is number of rank of DIMM/device. For example in dual-rank DIMM implementation, if there are 2 DQS in each rank DIMM, the maximum DQS delay is expressed by the following equation: $$max(DQS_1PathDelay\ rank\ 1, DQS_2PathDelay\ rank\ 1, DQS_1PathDelay\ rank\ 2, DQS_2PathDelay\ rank\ 2)$$

continued...

Parameter	Description
Minimum delay difference between CK and DQS	The minimum skew or smallest positive skew (or largest negative skew) between the CK signal and any DQS signal when arriving at the same DIMM/device over all DIMMs/devices is expressed by the following equation: $$min_r \left[\begin{matrix} min \\ n,m \end{matrix} \right] \{ (CK_{n\_r} Delay - DQS_{m\_r} Delay) \}$$ Where *n* is the number of memory clock, *m* is the number of DQS, and *r* is the number of rank of DIMM/device. For example in dual-rank DIMM implementation, if there are 2 pairs of memory clock and 4 DQS signals (two for each clock) for each rank DIMM, the minimum delay difference between CK and DQS is expressed by the following equation: $$min \begin{Bmatrix} (CK_{1\_1} Delay - DQS_{1\_1} Delay), (CK_{1\_1} Delay - DQS_{2\_1} Delay), (CK_{2\_1} Delay - DQS_{3\_1} Delay), (CK_{2\_1} Delay - DQS_{4\_1} Delay) \\ (CK_{1\_2} Delay - DQS_{1\_2} Delay), (CK_{1\_2} Delay - DQS_{2\_2} Delay), (CK_{2\_2} Delay - DQS_{3\_2} Delay), (CK_{2\_1} Delay - DQS_{4\_2} Delay) \end{Bmatrix}$$ This parameter value affects the write leveling margin for DDR3 interfaces with leveling in multi-rank configurations. This parameter value also applies to non-leveling configurations of any number of ranks with the requirement that DQS must have positive margins in Timequest Report DDR. For multiple boards, the minimum skew between the CK signal and any DQS signal when arriving at the same DIMM over all DIMMs is expressed by the following equation, if you want to use the same design for several different boards: $$\underset{b}{\overset{boards}{Min}} \left[\underset{g}{\overset{groups}{Min}} \left[CK_{g\_b} - DQS_{g\_b} \right] \right]$$
Maximum delay difference between CK and DQS	The maximum skew or smallest negative skew (or largest positive skew) between the CK signal and any DQS signal when arriving at the same DIMM/device over all DIMMs/devices is expressed by the following equation: $$max_r \left[\begin{matrix} max \\ n,m \end{matrix} \{ (CK_{n\_r} Delay - DQS_{m\_r} Delay) \} \right]$$ Where *n* is the number of memory clock, *m* is the number of DQS, and *r* is the number of rank of DIMM/device. For example in dual-rank DIMM implementation, if there are 2 pairs of memory clock and 4 DQS signals (two for each clock) for each rank DIMM, the maximum delay difference between CK and DQS is expressed by the following equation: $$max \begin{Bmatrix} (CK_{1\_1} Delay - DQS_{1\_1} Delay), (CK_{1\_1} Delay - DQS_{2\_1} Delay), (CK_{2\_1} Delay - DQS_{3\_1} Delay), (CK_{2\_1} Delay - DQS_{4\_1} Delay) \\ (CK_{1\_2} Delay - DQS_{1\_2} Delay), (CK_{1\_2} Delay - DQS_{2\_2} Delay), (CK_{2\_2} Delay - DQS_{3\_2} Delay), (CK_{2\_1} Delay - DQS_{4\_2} Delay) \end{Bmatrix}$$ This value affects the write Leveling margin for DDR3 interfaces with leveling in multi-rank configurations. This parameter value also applies to non-leveling configurations of any number of ranks with the requirement that DQS must have positive margins in Timequest Report DDR. For multiple boards, the maximum skew (or largest positive skew) between the CK signal and any DQS signal when arriving at the same DIMM over all DIMMs is expressed by the following equation, if you want to use the same design for several different boards: $$\underset{b}{\overset{boards}{Max}} \left[\underset{g}{\overset{groups}{Max}} \left[CK_{g\_b} - DQS_{g\_b} \right] \right]$$
Maximum skew within DQS group	The largest skew among DQ and DM signals in a DQS group. This value affects the read capture and write margins for DDR2 and DDR3 SDRAM interfaces in all configurations (single or multiple chip-select, DIMM or component). For multiple boards, the largest skew between DQ and DM signals in a DQS group is expressed by the following equation:

continued...

Parameter	Description
	$\underset{b}{\overset{boards}{Max}}\left[\underset{g}{\overset{groups}{Max}}\left[maxDQ_{g\_b} - minDQ_{g\_b}\right]\right]$
Maximum skew between DQS groups	The largest skew between DQS signals in different DQS groups. This value affects the resynchronization margin in memory interfaces without leveling such as DDR2 SDRAM and discrete-device DDR3 SDRAM in both single- or multiple chip-select configurations. For multiple boards, the largest skew between DQS signals in different DQS groups is expressed by the following equation, if you want to use the same design for several different boards: $\underset{b}{\overset{boards}{Max}}\left[\underset{g}{\overset{groups}{Max}}\left[DQS_{g\_b}\right] - \underset{b}{\overset{boards}{Min}}\left[\underset{g}{\overset{boards}{Min}}\left[DQS_{g\_b}\right]\right]\right]$
Average delay difference between DQ and DQS	The average delay difference between each DQ signal and the DQS signal, calculated by averaging the longest and smallest DQ signal delay values minus the delay of DQS. The average delay difference between DQ and DQS is expressed by the following equation: $\frac{\sum_{n=1}^{n=n}\left[\left(\frac{Longest\ DQ\ PathDelay\ in\ DQS_n\ group + Shortest\ DQ\ PathDelay\ in\ DQS_n\ group}{2}\right) - DQS_n PathDelay\right]}{n}$ where *n* is the number of DQS groups. For multi-rank or multiple CS configuration, the equation is: $\frac{\sum_{r=1}^{r=r}\left[Average\ delay\ difference\ between\ DQ\ and\ DQS\ in\ rank\ r\right]}{r}$
Maximum skew within address and command bus	The largest skew between the address and command signals for a single board is expressed by the following equation: $\frac{(MaxACdelay - MinCKdelay) - (MinACdelay - MaxCKdelay)}{2}$ For multiple boards, the largest skew between the address and command signals is expressed by the following equation, if you want to use the same design for several different boards: $\frac{\underset{b}{\overset{boards}{Max}}\left[(MaxAC_b - MinCK_b) - \underset{b}{\overset{boards}{Min}}(MaxAC_b - MinCK_b)\right]}{2}$
Average delay difference between address and command and CK	A value equal to the average of the longest and smallest address and command signal delay values, minus the delay of the CK signal. The value can be positive or negative. Positive values represent address and command signals that are longer than CK signals; negative values represent address and command signals that are shorter than CK signals. The average delay difference between address and command and CK is expressed by the following equation: $\frac{\sum_{n=1}^{n=n}\left[\left(\frac{Longest\ AC\ PathDelay + Shortest\ AC\ PathDelay}{2}\right) - CK_n PathDelay\right]}{n}$ where *n* is the number of memory clocks. For multi-rank or multiple CS configuration, the equation is:

Parameter	Description
	$\frac{\sum\binom{r=r}{r=1}[Average\ delay\ difference\ between\ AC\ and\ CK\ in\ rank\ r]}{r}$ The Intel Quartus Prime software uses this skew to optimize the delay of the address and command signals to have appropriate setup and hold margins for DDR2 and DDR3 SDRAM interfaces. You should derive this value through board simulation. For multiple boards, the average delay difference between address and command and CK is expressed by the following equation, if you want to use the same design for several different boards: $\underset{b}{\overset{boards}{Avg}}\left[\left(\frac{MaxAC_b + MinAC_b}{2}\right) - \left(\frac{MaxCK_b + MinCK_b}{2}\right)\right]$

Related Information

- Analizing Timing of Memory IP chapter, External Memory Interface Handbook
  Provides more information about derating method and measuring eye reduction.
- Board Skew Parameter Tool

5.1.5. UniPHY Parameters—Controller Settings

There are four groups of options: **Avalon Interface**, **Low Power Mode**, **Efficiency**, and **Configuration, Status and Error Handling**.

Table 21. Controller Settings - Avalon Interface

Parameter	Descriptions
Generate power-of-2 data bus widths for Qsys or SOPC Builder	Rounds down the Avalon memory-mapped interface side data bus to the nearest power of 2. You must enable this option for Qsys systems. If this option is enabled, the Avalon data buses are truncated to 256 bits wide. One Avalon read-write transaction of 256 bit width maps to four memory beat transactions, each of 72 bits (8 MSB bits are zero, while 64 LSB bits carry useful content). The four memory beats may comprise an entire burst length-of-4 transaction, or part of a burst-length-of-8 transaction.
Generate SOPC Builder compatible resets	This option is not required when using the MegaWizard Plug-in Manager or Qsys.
Maximum Avalon-MM burst length	Specifies the maximum burst length on the Avalon memory-mapped bus. Affects the AVL_SIZE_WIDTH parameter.
Enable Avalon-MM byte-enable signal	When you turn on this option, the controller adds the byte enable signal (avl_be) for the Avalon memory-mapped bus to control the data mask (mem_dm) pins going to the memory interface. You must also turn on **Enable DM pins** if you are turning on this option. When you turn off this option, the byte enable signal (avl_be) is not enabled for the Avalon memory-mapped bus, and by default all bytes are enabled. However, if you turn on **Enable DM pins** with this option turned off, all write words are written.
Avalon interface address width	The address width on the Avalon memory-mapped interface.
Avalon interface data width	The data width on the Avalon memory-mapped interface.

Table 22. Controller Settings - Low Power Mode

Parameter	Description
Enable Self-Refresh Controls	Enables the self-refresh signals on the controller top-level design. These controls allow you to control when the memory is placed into self-refresh mode.
Enable Deep Power-Down Controls	Enables the Deep-Powerdown signals on the controller top level. These controls allow you to control when the memory is placed in Deep-Powerdown mode. This option is available only for LPDDR2 SDRAM.
Enable Auto Power-Down	Allows the controller to automatically place the memory into power-down mode after a specified number of idle cycles. Specifies the number of idle cycles after which the controller powers down the memory in the auto-power down cycles parameter.
Auto Power-Down Cycles	The number of idle controller clock cycles after which the controller automatically powers down the memory. The legal range is from 1 to 65,535 controller clock cycles.

Table 23. Controller Settings - Efficiency

Parameter	Description
Enable User Auto-Refresh Controls	Enables the user auto-refresh control signals on the controller top level. These controller signals allow you to control when the controller issues memory autorefresh commands.
Enable Auto-Precharge Control	Enables the autoprecharge control on the controller top level. Asserting the autoprecharge control signal while requesting a read or write burst allows you to specify whether the controller should close (autoprecharge) the currently open page at the end of the read or write burst.
Local-to-Memory Address Mapping	Allows you to control the mapping between the address bits on the Avalon memory-mapped interface and the chip, row, bank, and column bits on the memory: • **Chip-Row-Bank-Col**—improves efficiency with sequential traffic. • **Chip-Bank-Row-Col**—improves efficiency with random traffic. • **Row-Chip-Bank-Col**—improves efficiency with multiple chip select and sequential traffic.
Command Queue Look-Ahead Depth	Selects a look-ahead depth value to control how many read or writes requests the look-ahead bank management logic examines. Larger numbers are likely to increase the efficiency of the bank management, but at the cost of higher resource usage. Smaller values may be less efficient, but also use fewer resources. The valid range is from 1 to 16.
Enable Reordering	Allows the controller to perform command and data reordering that reduces bus turnaround time and row/bank switching time to improve controller efficiency.
Starvation limit for each command	Specifies the number of commands that can be served before a waiting command is served. The valid range is from 1 to 63.

Table 24. Controller Settings - Configuration, Status and Error Handling

Parameter	Description
Enable Configuration and Status Register Interface	Enables run-time configuration and status interface for the memory controller. This option adds an additional Avalon memory-mapped slave port to the memory controller top level, which you can use to change or read out the memory timing parameters, memory address

continued...

Parameter	Description
	sizes, mode register settings and controller status. If Error Detection and Correction Logic is enabled, the same slave port also allows you to control and retrieve the status of this logic.
CSR port host interface	Specifies the type of connection to the CSR port. The port can be exported, internally connected to a JTAG Avalon Master, or both: • **Internal (JTAG)**—connects the CSR port to a JTAG Avalon Master. • **Avalon-MM Slave**—exports the CSR port. • **Shared**—exports and connects the CSR port to a JTAG Avalon Master.
Enable Error Detection and Correction Logic	Enables ECC for single-bit error correction and double-bit error detection. Intel MAX 10 devices supports ECC only for 16 bits + 8 bits ECC memory configuration.
Enable Auto Error Correction	Allows the controller to perform auto correction when a single-bit error is detected by the ECC logic. To turn this on, you must first turn on **Enable Error Detection and Correction Logic**.

5.1.6. UniPHY Parameters—Diagnostics

There is one option group supported for Intel MAX 10 devices: **Simulation Options**.

Table 25. Diagnostics - Simulation Options

Parameter	Description
Enable verbose memory model output	Turn on this option to display more detailed information about each memory access during simulation.

6. Intel MAX 10 External Memory Interface User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
16.0	MAX 10 External Memory Interface User Guide
15.1	MAX 10 External Memory Interface User Guide
15.0	MAX 10 External Memory Interface User Guide
14.1	MAX 10 External Memory Interface User Guide

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7. Document Revision History for the Intel MAX 10 External Memory Interface User Guide

Document Version	Intel Quartus Prime Version	Changes
2021.04.01	16.1	• Updated Table *Termination Recommendations for Intel MAX 10 DDR2 Component*: — Changed *SSTL 18 I/O Standard* for *DQ/DQS, DM and Clock* Signal Type. — Added *FGPA - End Discrete Termination* for *Address and Command* Signal Type. — Changed *Memory-End Termination 1* for *DM* Signal Type. — Added *Memory I/O Standard* for *DM* Signal Type.
2020.10.15	16.1	• Renamed the document as *Intel MAX 10 External Memory Interface User Guide*. • Updated *Intel MAX 10 I/O Banks for External Memory Interface*. • Updated for latest Intel branding standards.

Date	Version	Changes
February 2017	2017.02.21	• Rebranded as Intel.
October 2016	2016.10.28	• Updated Memory Standards Supported by the Soft Memory Controller for MAX 10 devices table.
May 2016	2016.05.02	• Updated UniPHY IP core parameter settings for LPDDR2, DDR2 and DDR3. • Updated Supported Maximum External Memory Interface Width in Intel MAX 10 Device Packages table. • Added Intel MAX 10 External Memory Interface User Guide Archives table. • Updated DDR2, DDR3 and LPDDR2 can use only user I/O pins from banks 5 and 6 of Intel MAX 10 devices to generate address and control or command signals..
November 2015	2015.11.02	• Added links to Intel MAX 10 DDR3 UniPHY IP core reference design. • Added topic that lists the maximum external memory interface widths supported for different Intel MAX 10 device packages. • Removed the topics about the IP catalog and parameter editor, generating IP cores, and the files generated by the IP core, and added a link to *Introduction to Altera IP Cores*. • Changed instances of *Quartus II* to *Quartus Prime*.
May 2015	2015.05.11	Added on board termination recommendation for DDR3 component.

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Date	Version	Changes
May 2015	2015.05.04	• Updated the footnote in the topic about external memoy interface support and performance to specify that the default maximum frequency for LPDDR2 is 167 MHz. • Removed the F672 package from the 10M25 device. • Removed the note about contacting Altera for DDR3, DDR3L, DDR2, and LPDDR2 external memory interface support. The Intel Quartus Prime software supports these external memory interfaces from version 15.0. • Added a topic about the PHYCLK network. • Moved information about recommended LPDDR2 termination scheme into a new topic under LPDDR2 design considerations section. The information was previously in the topic about recommended DDR2/ DDR3 termination schemes. • Updated the guidelines about board design requirement to improve clarity. • Updated and added related information links to relevant information. • Added a topic about the low power feature available from version 15.0 of the Intel Quartus Prime software. • Updated the topic about the phase detector to add a figure showing the VT tracking system overview.
December 2014	2014.12.15	• Changed Altera MAX 10 EMIF IP core to UniPHY IP core. • Removed reference to DIMM in a footnote under the table that lists the termination recommendations for DDR2 component. The UniPHY IP core for Intel MAX 10 does not support DIMM. • Added a list of the MAX 10 memory controller features. • Added "Preliminary" tag to the table that lists the I/Os unavailable in certain MAX 10 packages while implementing DDR3 or LPDDR2 external memory interfaces. • Updated the board design requirement with additional guidelines. • Added information for the MAX 10 external memory interface UniPHY IP core. This addition includes the chapters about external memory interface implementation and IP core references. • Edited texts and added related information links to improve clarity.
September 2014	2014.09.22	Initial release.