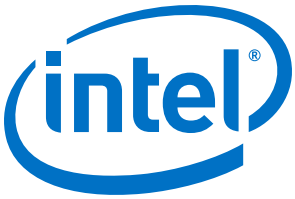

Intel® MAX® 10 FPGA Signal Integrity Design Guidelines

M10-SIDG | 2017.12.15
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Intel® MAX® 10 FPGA Signal Integrity Design Guidelines

Today's complex FPGA system design is incomplete without addressing the integrity of signals coming in to and out of the FPGA. Simultaneous switching noise (SSN) often leads to the degradation of signal integrity by causing signal distortion, thereby reducing the noise margin of a system.

To avoid signal integrity issues, Intel recommends that you follow the design considerations, I/O placement guidelines, and board design guidelines for Intel® MAX® 10 devices regarding:

- I/O placement rules
- Voltage-referenced I/O standards
- High-speed LVDS, phase-locked loops (PLLs), and clocking
- External memory interfaces
- Analog to digital converter

Intel recommends that you perform SSN analysis early in your FPGA design, before the layout of your PCB.

Definitions

The terminology used in this document includes the following terms:

- **Aggressor**: An output or bidirectional signal that contributes to the noise for a victim I/O pin
- **PDN**: Power distribution network
- **QH**: Quiet high signal level on a pin
- **QHN**: Quiet high noise on a pin, measured in volts
- **QL**: Quiet low signal level on a pin
- **QLN**: Quiet low noise on a pin, measured in volts
- **SI**: Signal integrity (a superset of SSN, covering all noise sources)
- **SSN**: Simultaneous switching noise
- **SSO**: Simultaneous switching output (which are either the output or bidirectional pins)
- **Victim**: An input, output, or bidirectional pin that is analyzed during SSN analysis. During SSN analysis, each pin is analyzed as a victim. If a pin is an output or bidirectional pin, the same pin acts as an aggressor signal for other pins.

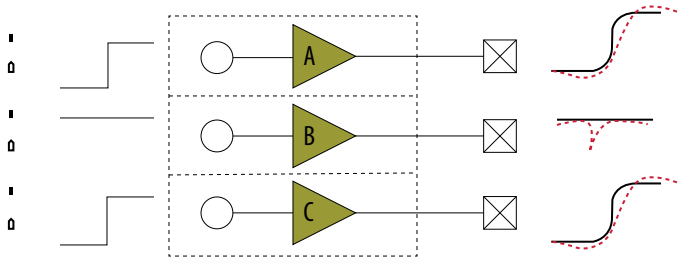
Understanding SSN

SSN is defined as a noise voltage induced onto a single victim I/O pin on a device due to the switching behavior of other aggressor I/O pins on the device. SSN can be divided into two types of noise: voltage noise and timing noise.

In a sample system with three pins, two of the pins (A and C) are switching, while one pin (B) is quiet. If the pins are driven in isolation, the voltage waveforms at the output of the buffers appear without noise interference, as shown by the solid curves at the left of the figure. However, when pins A and C are switching simultaneously, the noise generated by the switching is injected onto other pins. This noise manifests itself as a voltage noise on pin B and timing noise on pins A and C.

Figure 1. System with Three Pins

In this figure, the dotted curves show the voltage noise on pin B and timing noise on pins A and C.



Voltage noise is measured as the change in voltage of a signal due to SSN. When a signal is QH, it is measured as the change in voltage toward 0 V. When a signal is QL, it is measured as the change in voltage toward V_{CC}.

Voltage noise can be caused by SSOs under two worst-case conditions:

- The victim pin is high and the aggressor pins (SSOs) are switching from low to high
- The victim pin is low and the aggressor pins (SSOs) are switching from high to low

Figure 2. Quiet High Output Noise Estimation on Pin B

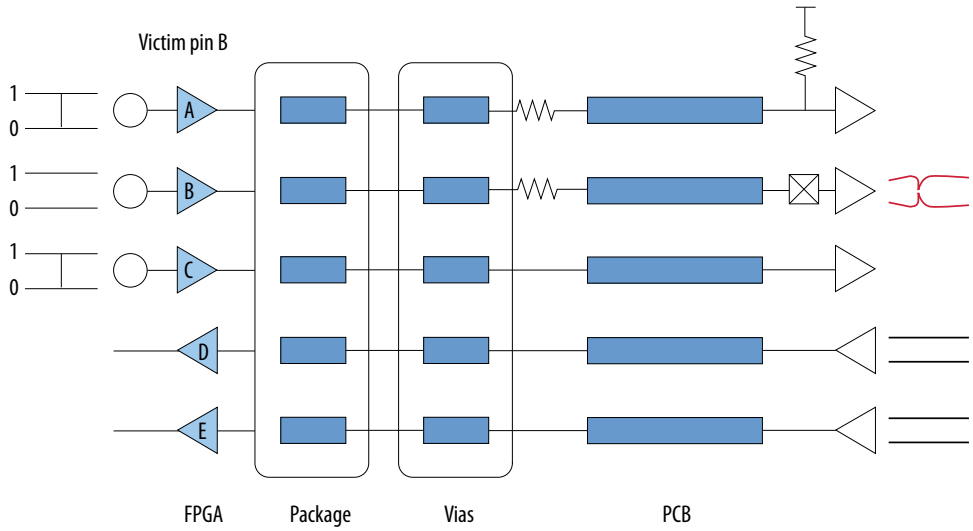
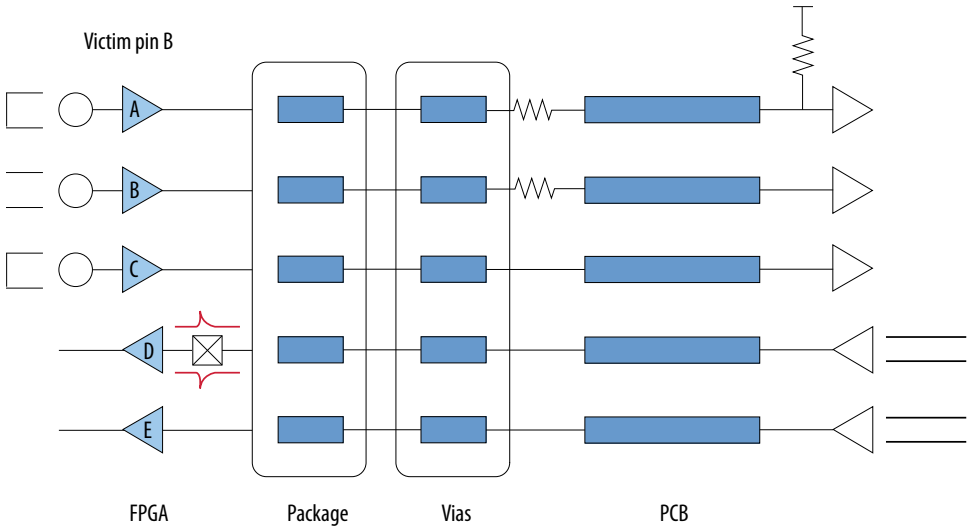
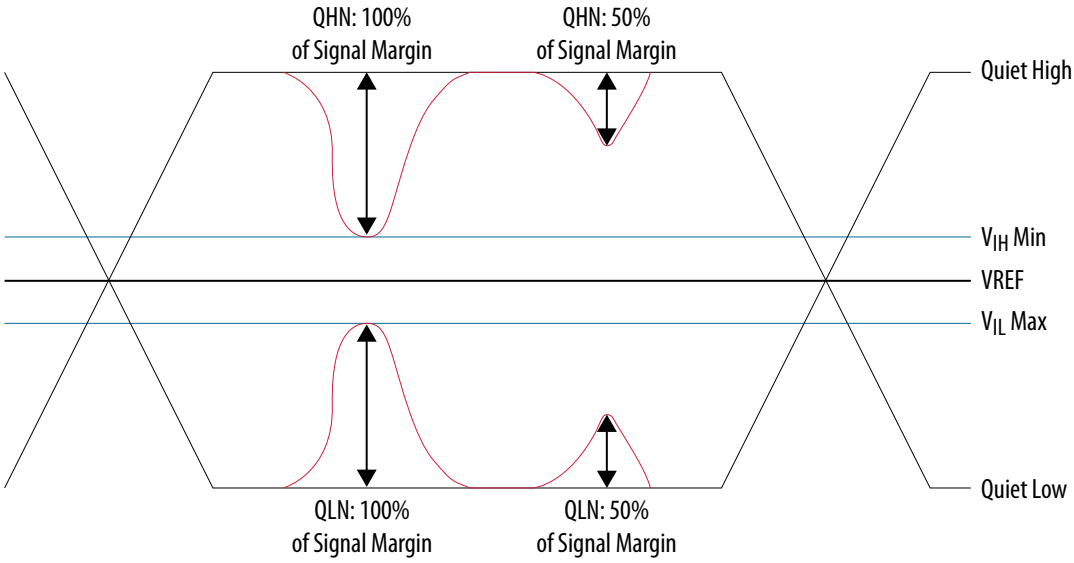


Figure 3. Quiet Low Input Noise Estimation for Pin D



SSN can occur in any system, but the induced noise does not always result in failures. Voltage functional errors are caused by SSN on quiet victim pins only when the voltage values on the quiet pins change by a large voltage that the logic listening to that signal reads a change in the logic value. For QH signals, a voltage functional error occurs when noise events cause the voltage to fall below V_{IH}. Similarly, for QL signals, a voltage functional error occurs when noise events cause the voltage to rise above V_{IL}. Because V_{IH} and V_{IL} of the Intel device are different for different I/O standards, and because signals have different quiet voltage values, the absolute amount of SSN, measured in volts, cannot be used to determine if a voltage failure occurs. Instead, to assess the level of impact by SSN, you can quantify the SSN in terms of the percentage of signal margin in Intel devices.

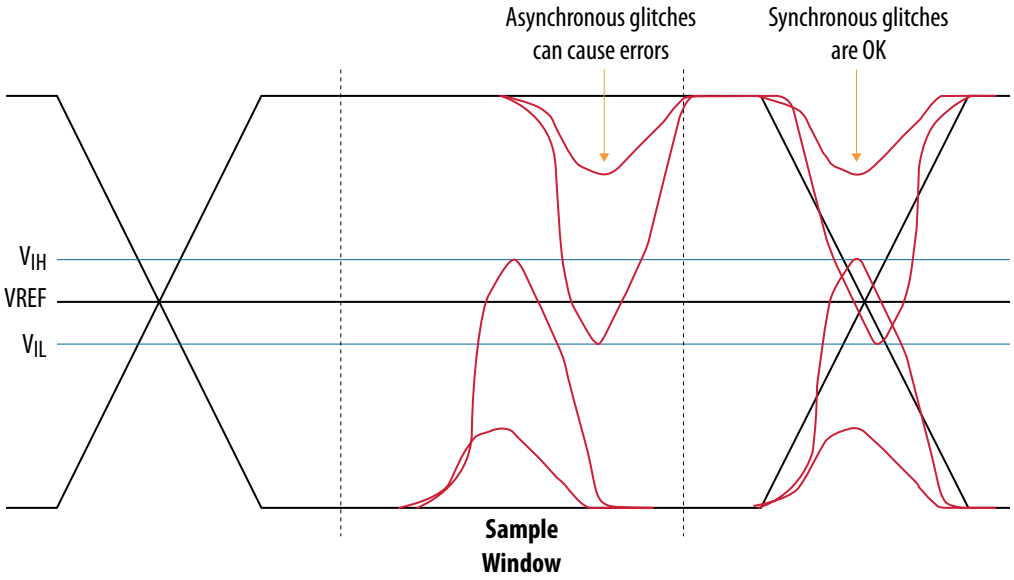
Figure 4. Reporting Noise Margins



The figure shows four noise events, two on QH signals and two on QL signals. The two noise events on the right-side of the figure consume 50 percent of the signal margin and do not cause voltage functional errors. However, the two noise events on the left side of the figure consume 100 percent of the signal margin, which can cause a voltage functional error.

Noise caused by aggressor signals is synchronously related to the victim pin outside of the sampling window of a receiver. This noise affects the switching time of a victim pin but is not considered an input threshold violation failure.

Figure 5. Synchronous Voltage Noise with No Functional Error



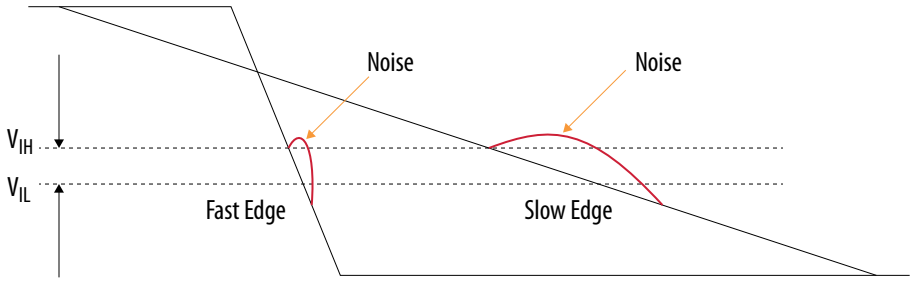
Guidelines: Clock and Asynchronous Control Input Signal

Input clock signal and asynchronous signals are sensitive signals. If signal interference happens at the signal edge, it can cause double sampling issue in internal logic.

PLLs are sensitive to SSN jitter generated by nearby I/O pins. Intel recommends that you do not use unterminated I/O standards in the same bank as the input clock signal to the PLL. Intel also recommends instantiating the input clock signal with full rail voltage.

Because edge noise is closer to the noise threshold (gap between maximum V_{IL} and minimum V_{IH}), the tolerable noise margin is smaller than the data signal. If the noise falls within the threshold range, sampling failure occurs.

Figure 6. Noise for Slow and Fast Clock Edges



Slower clock edges are more susceptible to jitter because the threshold range is wider than fast clock edges. Additionally, very slow clock edges are exposed to a larger amount of switching noise from the board to the device.

Follow these recommendations to avoid signal integrity issues:

- Design with faster input clock edges.
- Set the unused pin to a programmable ground pin to help in shielding the signal interference.
- Terminate all unused pin. Unterminated unused pins can cause signal interference between the input clock pin and the unused pins when there is signal toggling. You can set the unused pin to:
  - Weak pull-up resistor to create high impedance termination; or
  - Programmable ground to help in shielding signal interference.
- Reduce the slew rate or current strength of the adjacent strong aggressor pin.
- Turn on the Schmitt trigger on the input buffer.
- Avoid using dedicated LVDS signal as single-ended input clock signal. The strong mutual coupling originally targeted for LVDS signals can create distortion on single–ended input clock signal coming from another LVDS terminal.

Related Links

Guidelines: Data Input Pin on page 8

Schmitt-Trigger Input Buffer

The Intel MAX 10 devices feature selectable Schmitt trigger input buffer on all I/O banks.

The Schmitt trigger input buffer has similar V_{IL} and V_{IH} as the LVTTL I/O standard but with better noise immunity. The Schmitt trigger input buffers are used as default input buffers during configuration mode.

Guidelines: Data Input Pin

For data input signals, fast edge rates cause simultaneously switching input (SSI) noise problem on the wide data bus.

The noise margin is measured at the V_{IH} or V_{IL} instead of the signal edges.

Table 1. Maximum Recommended Data Input Signal Edge Rate for Intel MAX 10 Devices

This table lists the recommended maximum data input signal edge rate with regards to the percentage of I/O pins usage in an I/O bank.

Percentage of Simultaneous Switching Pins in I/O Bank	Recommended Maximum Data Input Signal Edge Rate
50% to 100%	0.6 V/ns
25% to 49%	1.0 V/ns
0% to 24%	1.5 V/ns

Note: If an input pin has an adjacent pin that operates as a toggling output, the edge rate of the input signal to the input pin must be 1.5 V/ns or faster.

If the data input signal exceeds the recommended signal edge rate, you can apply similar approach as the clock input signal to improve the signal integrity.

Related Links

Guidelines: Clock and Asynchronous Control Input Signal on page 6

Guidelines: Clock and Data Input Signal for Intel MAX 10 E144 Package

There is strong inductive coupling on the Intel MAX 10 E144 lead frame package. Glitch may occur on an input pin when an aggressor pin with strong drive strength toggles directly adjacent to it.

PLL Clock Input Pins

The PLL clock input pins are sensitive to SSN jitter. To avoid the PLL from losing lock, do not use the output pins directly on the left and right of the PLL clock input pins.

Data Input Pins

Potential glitch on the data input pin, leading to input read signal failure, can occur in the following conditions:

- The output pin directly adjacent to the data input pin is assigned an unterminated I/O standard, such as LVTTL and LVCMOS, with drive strength of 8 mA or higher.
- The output pin directly adjacent to the data input pin is assigned a terminated I/O standard, such as SSTL, with drive strength of 8 mA or higher.

Intel recommends that you implement these guidelines to reduce jitter on the data input pin:

- For unterminated I/O standards, implement one of these guidelines:
  - For the directly-adjacent output pin with these unterminated I/O standards, reduce the drive strength as follows:
    - 2.5 V, 3.0 V, and 3.3 V—reduce to 4 mA or below
    - 1.2 V, 1.5 V, and 1.8 V—reduce to 6 mA or below
  - Assign the pins directly on the left and right of the data input pin to a non-toggling signal.
  - Change the data input pin to a Schmitt Trigger input buffer for better noise immunity. If you are using Schmitt Trigger input buffer on the data input pin, you can use the directly-adjacent output pin with unterminated I/O standard at a maximum drive strength of 8 mA.
- For terminated I/O standard, you can use only one pin directly on the left or right of the data input pin as toggling signal, provided that you set the slew rate setting of this pin to "0" (slow slew rate). Otherwise, assign the pins directly on the left and right of the data input pin to a non-toggling signal.

Guidelines: I/O Restriction Rules

For different I/O standards and conditions, you must limit the number of I/O pins. This I/O restriction rule is applicable if you use LVDS transmitters or receivers. Apply this restriction if one or more LVDS I/O standards reside in the I/O bank.

Table 2. Maximum Percentage of I/O Pins Allowed for Specific I/O Standards in an I/O Bank

This table lists the maximum number of general purpose output pins recommended in a bank in terms of percentage to the total number of I/O pins available in an I/O bank if you use these combinations of I/O standards and conditions.

I/O Standard	Condition	Max Pins Per Bank (%)
2.5 V LVTTL/LVCMOS	16 mA current strength and 25 Ω OCT (fast and slow slew rate)	25
	12 mA current strength (fast and slow slew rate)	30
	8 mA current strength (fast and slow slew rate) and 50 Ω OCT (fast slew rate)	45
	4 mA current strength (fast and slow slew rate)	65
2.5 V SSTL	—	100

Guidelines: Analog-to-Digital Converter I/O Restriction

These restrictions are applicable if you use the analog-to-digital converter (ADC) block.

The Intel Quartus® Prime software uses physics-based rules to define the number of I/Os allowed in a particular bank based on the I/O's drive strength. These rules are based on noise calculation to analyze accurately the impact of I/O placement on the ADC performance.

The physics-based rules are available for the following devices starting from these Intel Quartus Prime software versions:

- From Intel Quartus Prime version 14.1—Intel MAX 10 10M04, 10M08, 10M40, and 10M50 devices.
- From Intel Quartus Prime version 15.0.1—Intel MAX 10 10M02, 10M16, and 10M25 devices.

Geometry-Based Rules for Design Estimation

Intel highly recommends that you use the following geometry-based rules to ensure ADC performance. These guidelines help you to estimate the resources available and prevent additional critical warning from versions of the Intel Quartus Prime software that implements the physics-based rules.

Table 3. Geometry-Based I/O Restrictions Related to ADC Usage

This table lists the I/O restrictions by Intel MAX 10 device package if you use the dedicated analog input (ANAIN1 or ANAIN2) or any dual function ADC I/O pins as ADC channel inputs.

Package	Restriction/Guideline
All	Disable all JTAG operation during ADC sampling. The ADC signal-to-noise and distortion ratio (SINAD) is not guaranteed during JTAG operation.
M153 U169 U324 F256 F484 F672	• Banks 1A and 1B—you cannot use GPIO pins in these banks. • Banks 2, 3, 4, 5, 6, and 7—you can use GPIO pins located in these banks. • Bank 8—you can use a percentage of the GPIO pins in this bank based on drive strength: — For an example listing the percentage of GPIO pins allowed in bank 8 for the F484 package, refer to Table 4 on page 11(1). — Use low drive strength (8 mA and below) and differential I/O standards. — Do not place transmitter pins in this bank. Use banks 2, 3, 4, 5, 6, or 7 instead. — You can use static pins such as RESET or CONTROL. — GPIO pins in this bank are governed by physics-based rules. The Intel Quartus Prime software will issue a critical warning I/O settings violates any of the I/O physic-based rule.
E144	• Bank 1A, 1B, 2, and 8—you cannot use GPIO pins in these banks. • Banks 4 and 6—you can use GPIO pins located in these banks. • Banks 3, 5, and 7—you can use a percentage of the GPIO pins in this bank based on drive strength: — For the percentage of GPIO pins allowed, refer to Table 5 on page 11. — Use low drive strength (8 mA and below) and differential I/O standards. — GPIO pins in these banks are governed by physics-based rules. The Intel Quartus Prime software will issue a critical warning I/O settings violates any of the I/O physic-based rule.

(1) For all device packages, the software displays a warning message if the number of GPIO pins in bank 8 is more than the allowed percentage.

Table 4. I/O Usage Restriction for Bank 8 in Intel MAX 10 F484 Package

This table lists the percentage of I/O pins available in I/O bank 8 if you use the dedicated analog input (ANAIN1 or ANAIN2) or any dual function ADC I/O pins as ADC channel. Refer to Table 6 on page 11 for the list of I/O standards in each group.

I/O Standards	TX	RX	Total	Availability (%)
Group 1	18	18	36	100
Group 2	16	16	32	89
Group 3	7	11	18	50
Group 4	5	7	12	33
Group 5	4	6	10	28
Group 6	4	4	8	22
Group 7	0	8	8	22

Table 5. I/O Usage Restriction for Banks 3, 5, and 7 in Intel MAX 10 E144 Package

This table lists the percentage of I/O pins available in banks 3, 5, and 7 if you use the dedicated analog input (ANAIN1 or ANAIN2) or any dual function ADC I/O pins as ADC channel inputs. Refer to Table 6 on page 11 for the list of I/O standards in each group.

I/O Standards	Bank 3			Bank 5			Bank 7			Device I/O Availability (%)
	TX	RX	Availability (%)	TX	RX	Availability (%)	TX	RX	Availability (%)	
Group 1	7	8	88	6	6	100	4	3	100	54
Group 2	7	8	88	6	6	100	4	3	100	54
Group 3	4	5	50	6	6	100	2	0	29	45
Group 4	3	4	39	5	5	83	0	0	0	39
Group 5	2	3	28	5	5	83	0	0	0	37
Group 6	1	2	17	5	5	83	0	0	0	35
Group 7	0	0	0	5	5	83	0	0	0	32

Table 6. I/O Standards Groups Categorized According to Drive Strengths

I/O Standard Group	I/O Standards Name and Drive Strength
Group 1	• 2.5 V LVDS • 2.5 V RSDS • BLVDS at 4 mA • SLVS at 4 mA
Group 2	• BLVDS at 8 mA • SLVS at 8 mA • Sub-LVDS at 8 mA • 1.8 V, 1.5 V, and 1.2 V HSTL Class I at 8 mA • SSTL-15 at 34 Ω or 40 Ω • SSTL-135 at 34 Ω or 40 Ω • HSUL-12 at 34 Ω or 40 Ω • SSTL-2 Class I at 8 mA • SSTL-18 Class I at 8 mA • SSTL-15 Class I at 8 mA • 2.5 V and 1.8 V LVTTL at 4 mA

continued...

I/O Standard Group	I/O Standards Name and Drive Strength
	• 2.5 V, 1.8 V, 1.5 V, and 1.2 V LVCMOS at 4 mA • 1.8 V LVTTL at 2 mA • 1.8 V, 1.5 V, and 1.2 V LVCMOS at 2 mA
Group 3	• BLVDS at 12 mA • SLVS at 12 mA • Sub-LVDS at 12 mA • SSTL-2 Class I at 10 mA or 12 mA • SSTL-18 Class I at 10 mA or 12 mA • SSTL-15 Class I at 10 mA or 12 mA • 1.8 V, 1.5 V, and 1.2 V HSTL Class I at 10 mA or 12 mA • SSTL-2 at 50 Ω • SSTL-18 at 50 Ω • SSTL-15 at 50 Ω • 1.8 V, 1.5 V and 1.2 V HSTL at 50 Ω • HSUL-12 at 48 Ω • 2.5 V and 1.8 V LVTTL at 50 Ω • 2.5 V, 1.8 V, 1.5 V, and 1.2 V LVCMOS at 50 Ω • 1.8 V LVTTL at 6 mA or 8 mA • 1.8 V, 1.5 V, and 1.2 V LVCMOS at 6 mA or 8 mA • 3.0 V LVTTL at 4 mA • 3.0 V LVCMOS at 4 mA
Group 4	• SSTL-18 Class II at 12 mA • 3.0 V LVTTL at 50 Ω • 3.0 V LVCMOS at 50 Ω • 2.5 V LVTTL at 8 mA • 2.5 V LVCMOS at 8 mA • 1.8 V LVTTL at 10 mA or 12 mA • 1.8 V, 1.5 V, and 1.2 V LVCMOS at 10 mA or 12 mA • 3.3 V LVCMOS at 2 mA

continued...

I/O Standard Group	I/O Standards Name and Drive Strength
Group 5	• SSTL-2 Class II at 16 mA • SSTL-18 Class II at 16 mA • SSTL-15 Class II at 16 mA • 1.8 V and 1.5 V HSTL Class II at 16 mA • 1.2 V HSTL Class II at 14 mA • SSTL-18 at 25 Ω • SSTL-15 at 25 Ω • SSTL-2 at 25 Ω • 1.8 V, 1.5 V, and 1.2 V HSTL at 25 Ω • 2.5 V and 1.8 V LVTTL at 25 Ω • 2.5 V, 1.8 V, 1.5 V, and 1.2 LVCMOS at 25 Ω • 1.8 V LVTTL at 16 mA • 1.8 V and 1.5 V LVCMOS at 16 mA • 2.5 V LVCMOS at 12 mA • 2.5 V LVTTL at 12 mA • 3.0 V LVCMOS at 8 mA • 3.0 V LVTTL at 8 mA • 3.3 V LVTTL at 4 mA or 8 mA
Group 6	• 2.5 V LVTTL at 16 mA • 2.5 V LVCMOS at 16 mA • 3.0 V LVTTL at 12 mA • 3.0 V LVCMOS at 12 mA • 3.0 V LVTTL at 25 Ω • 3.0 V LVCMOS at 25 Ω
Group 7	• 3.0 V LVTTL at 16 mA • 3.0 V LVCMOS at 16 mA

Guidelines: Voltage-Referenced I/O Standards Restriction

These restrictions apply if you use the V_{REF} pin.

- If you use a shared VREF pin as an I/O, all voltage-reference input buffers (SSTL, HSTL, and HSUL) are disabled.
- If you use a shared VREF pin as a voltage reference, you must enable the input buffer of specific I/O pin to use the voltage-reference I/O standards.
- The voltage-referenced I/O standards are not supported in the following I/O banks of these device packages:
  - All I/O banks of V36 package of 10M02.
  - All I/O banks of V81 package of 10M08.
  - Banks 1A and 1B of E144 package of 10M50.
- For devices with banks 1A and 1B, if you use the VREF pin, you must supply a common V_{CCIO} to banks 1A and 1B.
- Maximum number of voltage-referenced inputs for each VREF pin is 75% of total number of I/O pads. The Intel Quartus Prime software will provide a warning if you exceed the maximum number.
- Except for I/O pins that you used for static signals, all non-voltage-referenced output must be placed two pads away from a VREF pin. The Intel Quartus Prime software will output an error message if this rule is violated.

Guidelines: Adhere to the LVDS I/O Restrictions Rules

For LVDS applications, adhere to the I/O restriction pin connection guidelines to avoid excessive jitter on the LVDS transmitter output pins. The Intel Quartus Prime software generates a critical warning if these rules are violated.

Guidelines: Enable Clamp Diode for LVTTL/LVCMOS Input Buffers

If the input voltage to the LVTTL/LVCMOS input buffers is higher than the V_{CCIO} of the I/O bank, Intel recommends that you enable the clamp diode.

- 3.3 V LVCMOS/LVTTL input buffers—enable clamp diode if V_{CCIO} of the I/O bank is 3.0 V.
- 3.3 V or 3.0 V LVCMOS/LVTTL input buffers—enable clamp diode if V_{CCIO} of the I/O bank is 2.5 V.

By enabling the clamp diode under these conditions, you limit overshoot or undershoot. However, this does not comply with hot socket current specification.

If you do not enable the clamp diode under these conditions, the signal integrity for the I/O pin is impacted and there will be overshoot or undershoot problem. In this situation, you must ensure that your board design coreduce firefox cachenforms to the overshoot/undershoot specifications.

Table 7. Voltage Tolerance Maximum Ratings for 3.3 V or 3.0 V

This table lists the voltage tolerance specifications. Ensure that your board design conforms to these specifications if you do not want to follow the clamp diode recommendation.

Voltage	Minimum (V)	Maximum (V)
V_{CCIO} = 3.3 V	3.135	3.45
V_{CCIO} = 3.0 V	2.85	3.15
V_{IH} (AC)	—	4.1
V_{IH} (DC)	—	3.6
V_{IL} (DC)	–0.3	0.8

Guidelines: External Memory Interface I/O Restrictions

These I/O rules are applicable if you use external memory interfaces in your design.

Two GPIOs Adjacent to DQ Pin Is Disabled

This limitation is applicable to Intel MAX 10 10M16, 10M25, 10M40, and 10M50 devices, and only if you use DDR3 and LPDDR2 SDRAM memory standards.

Table 8. DDR3 and LPDDR2 Memory Interface Widths and Device Packages Where Two GPIOs Adjacent to DQ Pins Are Disabled

This table lists the combination of Intel MAX 10 10M16, 10M25, 10M40, and 10M50 device packages, and DDR3 and LPDDR2 memory interface widths where you cannot use two GPIO pins that are adjacent to the DQ pins.

Device Package	Memory Interface Width (DDR3 and LPPDR2 only)
U324	x8
F484	x8, x16, x24
F672	x8, x16, x24

Total I/O Utilization in Bank Must Be 75 Percent or Less in Some Devices

If you use DDR3 or LPDDR2 SDRAM memory interface standards, you can generally use a maximum of 75 percent of the total number of I/O pins available in a bank. This restriction differs from device to device. In some devices packages you can use all 100 percent of the I/Os. The Intel Quartus Prime software will output an error message if the I/O usage per bank of that device is affected by this rule.

If you use DDR2 memory interface standards, you can assign 25 percent of the I/O pins as input pins only.

Guidelines: ADC Ground Plane Connection

For the ADC and V_{REF} pins, use the REFGND pin as the analog ground plane connection.

Guidelines: Board Design for ADC Reference Voltage Pin

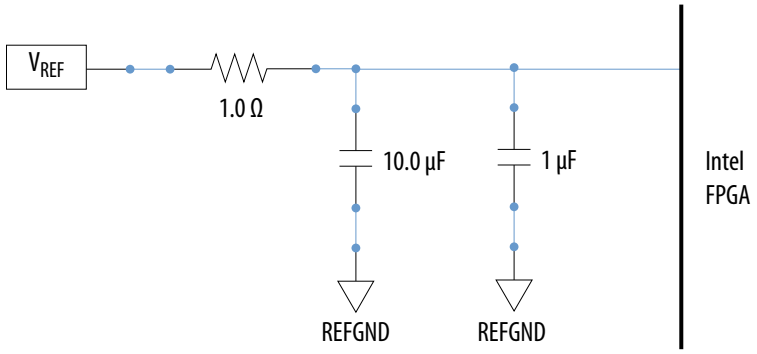
The crosstalk requirement for analog to digital signal is -100 dB up to 2 GHz. There is no parallel routing between analog input signals and I/O traces. Route the V_{REF} traces as adjacent as possible to REFGND.

If a REFGND plane is not possible, route the analog input signal as adjacent as possible to REFGND.

There is one ADC reference voltage pin in each Intel MAX 10 device. This pin uses REFGND as ground reference. Keep the trace resistance less than 0.8 Ω.

Figure 7. RC Filter Design Example for Reference Voltage Pin

Place the RC filter as close as possible to the analog input pin.



Guidelines: Board Design for Analog Input

The crosstalk requirement for analog to digital signal is -100 dB up to 2 GHz. There must be no parallel routing between analog input signals and I/O traces, and between analog input signals and FPGA I/O signal traces.

- The ADC presents a switch capacitor load to the driving circuit. Therefore, the total RC constant, including package, trace, and parasitic driver must be less than 42.4 ns. This consideration is to ensure that the input signal is fully settled during the sampling phase.
- If you reduce the total sampling rate, you can calculate the required settling time as $0.45 \div F_S > 10.62 \times RC\ constant$.
- To gain more total RC margin, Intel recommends that you make the driver source impedance as low as possible:
  - For non-prescaler channel—less than 1 kΩ
  - For prescaler channel—less than 11 Ω

  Note: Not adhering to the source impedance recommendation may impact parameters such as total harmonic distortion (THD), signal-to-noise and distortion ratio (SINAD), differential non-linearity (DNL), and integral non-linearity (INL).

Trace Routing

- If possible, route the switching I/O traces on different layers.
- There is no specific requirement for input signal trace impedance. However, the DC resistance for the input trace must be as low as possible.
- Route the analog input signal traces as adjacent as possible to REFGND if there is no REFGND plane.
- Use REFGND as ground reference for the ADC input signal.
- For prescaler-enabled input signal, set the ground reference to REFGND. Performance degrades if the ground reference of prescaler-enabled input signal is set to common ground (GND).

Input Low Pass Filter Selection

- Intel recommends that you place a low pass filter to filter out high frequency noise being aliased back onto the input signal.
- Place the low pass filter as close as possible to the analog input signals.
- The cut off frequency depends on the analog input frequency. Intel recommends that the $F_{cutoff\ @\ -3dB}$ is at least two times the input frequency.
- You can download the ADC input SPICE model for ADC front end board design simulation from the Intel website.

Table 9. RC Constant and Filter Value

This table is an example of the method to quantify the RC constant and identify the RC filter value.

Total RC Constant = $(R_{DRIVER} + R_{BOARD} + R_{PACKAGE} + R_{FILTER}) \times (C_{DRIVER} + C_{BOARD} + C_{PACKAGE} + C_{FILTER} + C_{PIN})$

Driver		Board		Package		Pin Capacitance (pF)	RC Filter		$F_{cutoff\ @\ -3dB}$ (MHz)	Total RC Constant (ns)	Settling Time (ns)
R (Ω)	C (pF)	R (Ω)	C (pF)	R (Ω)	C (pF)		R (Ω)	C (pF)			
5	2	5	17	3	5	6	60	550	4.82	42.34	42.4
10	2	5	17	3	5	6	50	580	5.49	41.48	42.4

Figure 8. Passive Low Pass Filter Example

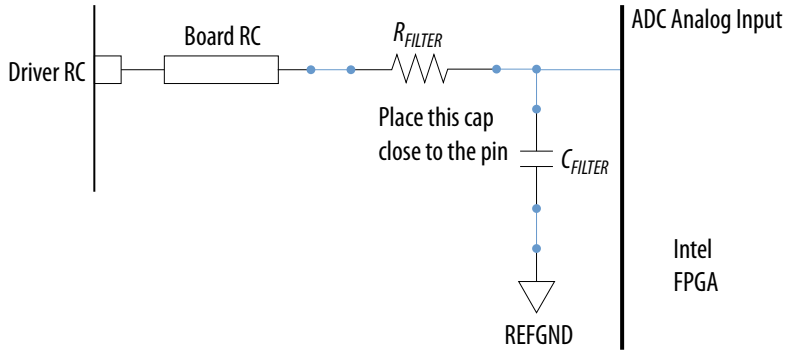
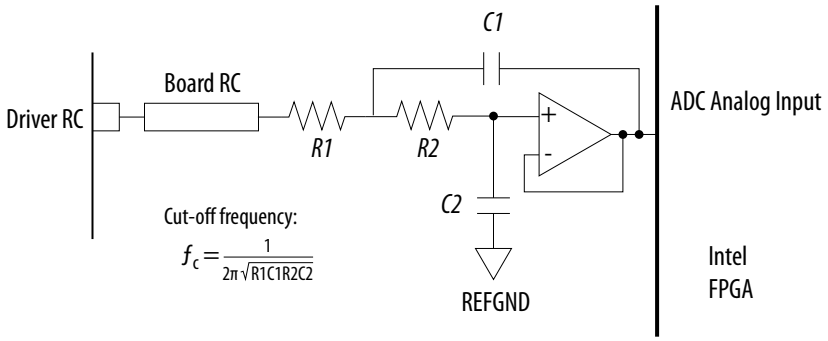


Figure 9. First Order Active Low Pass Filter Example

This figure is an example. You can design *n*th order active low pass filter.



Related Links

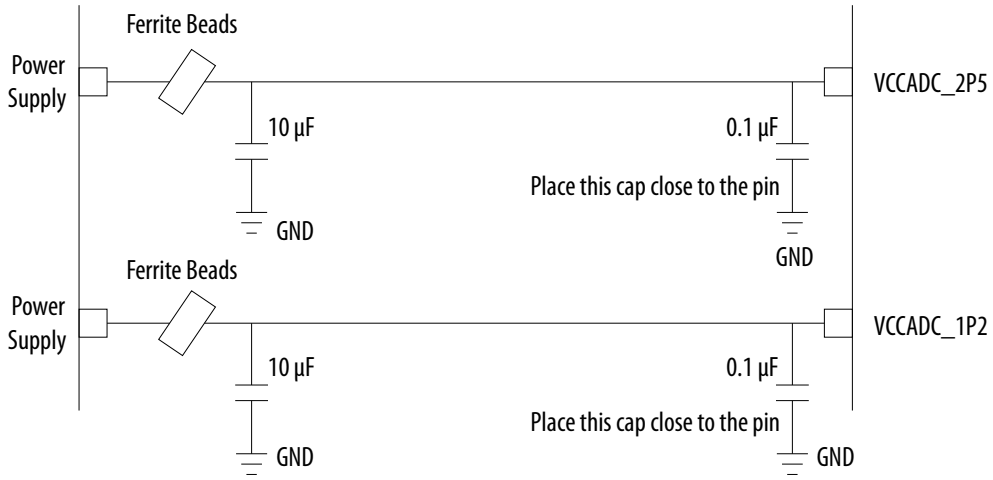
SPICE Models for Intel FPGAs
Provides the MAX 10 ADC spice model download.

Guidelines: Board Design for Power Supply Pin and ADC Ground (REFGND)

The crosstalk requirement for analog to digital signal is -100 dB up to 2 GHz. There must be no parallel routing between power, ground, and surrounding general purpose I/O traces. If a power plane is not possible, route the power and ground traces as wide as possible.

- To reduce IR drop and switching noise, keep the impedance as low as possible for the ADC power and ground. The maximum DC resistance for power is 1.5 Ω.
- The power supplies connected to the ADC should have ferrite beads in series followed by a 10 µF capacitor to the ground. This setup ensures that no external noise goes into the device power supply pins.
- Decouple each of the device power supply pin with a 0.1 µF capacitor. Place the capacitor as close as possible to the device pin.

Figure 10. Recommended RC Filter for Power Traces



There is no impedance requirement for the REFGND. Intel recommends that you use the lowest impedance with the most minimum DC resistance possible. Typical resistance is less than 1 Ω.

Intel recommends that you set a REFGND plane that extends as close as possible to the corresponding decoupling capacitor and FPGA:

- If possible, define a complete REFGND plane in the layout.
- Otherwise, route the REFGND using a trace that is as wide as possible from the island to the FPGA pins and decoupling capacitor.
- The REFGND ground is the analog ground plane for the ADC V_{REF} and analog input.
- Connect REFGND ground to the system digital ground through ferrite beads. You can also evaluate the ferrite bead option by comparing the impedance with the frequency specifications.

Guidelines: Intel MAX 10 Board Design Requirement for DDR2, DDR3, and LPDDR2

- For DDR2, DDR3, and LPDDR2 interfaces, the maximum board skew between pins must be lower than 40 ps. This guideline applies to all pins (address, command, clock, and data).
- To minimize unwanted inductance from the board via, Intel recommends that you keep the PCB via depth for V_{CCIO} banks below 49.5 mil.
- For devices with DDR3 interface implementation, onboard termination is required for the DQ, DQS, and address signals. Intel recommends that you use termination resistor value of 80 Ω to V_{TT}.
- For the DQ, address, and command pins, keep the PCB trace routing length less than six inches for DDR3, or less than three inches for LPDDR2.

Document Revision History for MAX 10 FPGA Signal Integrity Design Guidelines

Date	Version	Changes
December 2017	2017.12.15	• Updated the description in the guideline topic about I/O restrictions to improve clarity. • Updated the guideline topic about the clock and data input signal for the E144 package to improve clarity. • Updated the guideline topic about the ADC I/O restriction to clarify that the guidelines are geometry-based rules for design estimation purpose. • Updated the guideline topic about enabling the clamp diode for the LVTTL/LVCMOS input buffers to improve clarity.
March 2017	2017.03.02	Added a note to the guideline about the data input pin to specify that the signal to the input pin must be 1.5 V/ns or faster if an adjacent pin operates as a toggling output.
February 2017	2017.02.21	Rebranded as Intel.

continued...

Date	Version	Changes
November 2015	2015.11.02	• Added recommendation about instantiating the input clock signal with full rail voltage in *Guidelines: Clock and Asynchronous Control Input Signal*. • Added a new topic: *Guidelines: Clock and Data Input Signal for Intel MAX 10 E144 Package* • Updated the description in the Maximum Percentage of I/O Pins Allowed for Specific I/O Standards in an I/O Bank table in *Guidelines: I/O Restriction Rules.* • Changed instances of *Quartus II* to *Quartus Prime*.
June 2015	2015.06.11	• Added recommendation about not using unterminated I/O standards in the same bank as the input clock signal to the PLL. • Updated the board design guidelines for analog input. • Updated the ADC I/O restriction guidelines topic.
May 2015	2015.05.04	• Updated the guidelines for voltage-referenced I/O standards to add a list of device packages that do not support voltage-referenced I/O standards. • Updated the topic about the I/O restriction rules to remove statements about the differential pad placement rules. • Updated the topic about external memory interface I/O restrictions to add x24 memory interface width to the F484 package. • Removed statements about availability of the threshold trigger feature in a future version of the Intel Quartus Prime software. The feature is now available from version 15.0 of the software. • Updated the RC constant and filter value and the filter design example figure to clarify the source of the example values. • Removed notes about contacting Intel for the ADC pin RLC filter design. • Updated the guidelines about board design requirement for DDR2, DDR3, and LPDDR2 to improve clarity.
December 2014	2014.12.15	Initial release.