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The Intel® HLS Compiler Standard Edition User Guide provides instructions on synthesizing, verifying, and simulating IP that you design for Intel FPGA products. The Intel High Level Synthesis (HLS) Compiler is sometimes referred to as the i++ compiler, reflecting the name of the compiler command.

Compared to traditional RTL development, the Intel HLS Compiler offers the following advantages:

- Fast and easy verification
- Algorithmic development in C++
- Automatic integration of RTL verification with a C++ testbench
- Powerful microarchitecture optimizations

In this publication, `<quartus_installdir>` refers to the location where you installed Intel Quartus® Prime Design Suite.

The default Intel Quartus Prime Design Suite installation location depends on your operating system:

**Windows**  
C:\intelFPGA_pro\19.4

**Linux**  
/home/<username>/intelFPGA_pro/19.4

About the Intel HLS Compiler Standard Edition Documentation Library

Documentation for the Intel HLS Compiler Standard Edition is split across a few publications. Use the following table to find the publication that contains the Intel HLS Compiler information that you are looking for:

<table>
<thead>
<tr>
<th>Table 1. Intel High Level Synthesis Compiler Documentation Library</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Title and Description</strong></td>
</tr>
<tr>
<td><strong>STD</strong></td>
</tr>
<tr>
<td><strong>Release Notes</strong></td>
</tr>
<tr>
<td>Link</td>
</tr>
<tr>
<td>Provide late-breaking information about the Intel HLS Compiler.</td>
</tr>
<tr>
<td><strong>Getting Started Guide</strong></td>
</tr>
<tr>
<td>Link</td>
</tr>
<tr>
<td>Get up and running with the Intel HLS Compiler by learning how to initialize your compiler environment and reviewing the various design examples and tutorials provided with the Intel HLS Compiler.</td>
</tr>
<tr>
<td><strong>User Guide</strong></td>
</tr>
<tr>
<td>Link</td>
</tr>
<tr>
<td>Provides instructions on synthesizing, verifying, and simulating intellectual property (IP) that you design for Intel FPGA products. Go through the entire development flow of your component from creating your component and testbench up to integrating your component IP into a larger system with the Intel Quartus Prime software.</td>
</tr>
</tbody>
</table>

*Other names and brands may be claimed as the property of others.*
<table>
<thead>
<tr>
<th>Title and Description</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Reference Manual</td>
<td>Link</td>
</tr>
<tr>
<td>Provides reference information about the features supported by the Intel HLS Compiler. Find details on Intel HLS Compiler command options, header files, pragmas, attributes, macros, declarations, arguments, and template libraries.</td>
<td></td>
</tr>
<tr>
<td>Best Practices Guide</td>
<td>Link</td>
</tr>
<tr>
<td>Provides techniques and practices that you can apply to improve the FPGA area utilization and performance of your HLS component. Typically, you apply these best practices after you verify the functional correctness of your component.</td>
<td></td>
</tr>
<tr>
<td>Quick Reference</td>
<td>Link</td>
</tr>
<tr>
<td>Provides a brief summary of Intel HLS Compiler declarations and attributes on a single two-sided page.</td>
<td></td>
</tr>
</tbody>
</table>

The Intel High Level Synthesis (HLS) Compiler parses and compiles your design to an x86-64 object or RTL code optimized for Intel FPGA device families. It also creates an executable testbench. Use the x86-64 object to quickly test and debug the function of your design.

You can use the same testbench to verify your design both when it is compiled to x86-64 instructions or to HDL.

The Intel HLS Compiler Standard Edition is command-line compatible with the g++ compiler, and supports most of the g++ compiler flags. See the Intel High Level Synthesis Compiler Standard Edition Reference Manual for a full list of compiler flags.

The Intel HLS Compiler recognizes the same file name extensions as g++, namely .c, .C, .cc, .cpp, .CPP, .C++, .cp, and .cxx. The compiler treats all of these file types as C++. The compiler does not explicitly support C, other than as a subset of C++.

Important: The Intel HLS Compiler Standard Edition treats all input files as C++98. The compiler does not support files conforming to newer C++ standards.

When you target the compilation to an FPGA, the Intel HLS Compiler outputs an executable and a project directory. The default executable is a.out on Linux and a.exe on Windows. The default project directory is a.prj, and it contains the following outputs:

- Generated IP
- High-Level Design Reports (report.html)
- Verification testbench files
- Quartus project that you can use to accurately estimate area requirements and fMAX for your design

To specify the name of the compiler output, include the -o <result> option in your i++ command, where <result> is the name of the executable. This command creates a project directory called <result>.prj.

Running the executable file runs your testbench. When you target the compilation to an x86-64 architecture, the output executable runs your design on your CPU like a regular C++ program. The output executable runs very quickly compared to running a simulation of your component RTL. When you target the compilation to an FPGA architecture, the output executable simulates your component RTL. This simulation can take a long time to run.
2.1. High Level Synthesis Design Flow

The Intel High Level Synthesis (HLS) Compiler helps speed your IP development by letting you compile your IP component C++ code to different targets, depending on where you are in your IP development cycle.

The typical design flow when you use the Intel HLS Compiler Standard Edition consists of the following stages:

1. Creating your component and testbench.
   You can write a complete C++ application that contains both your component code and your testbench code.
   For details, see Creating a High-Level Synthesis Component and Testbench on page 8.

2. Verify the functionality of your component algorithm and testbench.
   Verify the functionality by compiling your design to an x86-64 executable and running the executable. For details, see Verifying the Functionality of Your Design on page 10.

3. Optimize and refine the FPGA performance of your component.
   Optimize the FPGA performance of your component by compiling your design for an FPGA target device and reviewing the High-Level Design Reports to see where you can optimize your component. This step generates RTL code for your component. For details, see Optimizing and Refining Your Component on page 11.
   After initial optimizations, you can see where to further refine your component by simulating your component. For details, see Simulating Your Design on page 13.

4. Synthesize your component with Intel Quartus Prime software.
   For details, see Synthesize your Component with Intel Quartus Prime Standard Edition on page 17.
   Synthesizing your component generates accurate quality-of-results (QoR) metrics like FPGA area utilization and $f_{\text{MAX}}$.

5. Integrate your IP into a system with Intel Quartus Prime or Platform Designer (formerly Qsys).
   For details, see Integrating your IP into a System on page 18.

The following flowchart shows a coarse-grained progression through the stages of a typical Intel High Level Synthesis (HLS) Compiler design flow.
Figure 1. Overview of Procedure for Synthesizing IP for Intel FPGA Products

1. Create component and test bench
2. Compile design with the following command to generate IP and a testbench executable to verify your design in simulation:
   ```
i++ -march="<FPGA_family_or_part_number>"
   ```
3. Compile design with `g++` or `i++ -march=x86-64` for functional verification
   (Note: You can debug your design using GDB, even for an `i++ x86-64` output)
4. Run a Quartus Prime compilation on the project in the `<result>.prj/quartus` directory to generate QoR metrics from Quartus Prime software

2.2. The Project Directory

The project directory (`<result>.prj`) that the Intel HLS Compiler Standard Edition outputs has four subdirectories.

Table 2. Subdirectories within the .prj Directory

<table>
<thead>
<tr>
<th>Directory</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>components</td>
<td>Contains a folder for each component, and all HDL and IP files that are needed to use that component in a design.</td>
</tr>
<tr>
<td>verification</td>
<td>Contains all the files for the verification testbench.</td>
</tr>
<tr>
<td>reports</td>
<td>Contains reports with information that is useful for analyzing the hardware implementation of the synthesized components.</td>
</tr>
<tr>
<td>quartus</td>
<td>Contains an Intel Quartus Prime project that instantiates the components. You can compile this Intel Quartus Prime project to generate more detailed timing and area reports. Do not use the contents of this subdirectory to integrate your component in a design. Use the contents of the components directory.</td>
</tr>
</tbody>
</table>
3. Creating a High-Level Synthesis Component and Testbench

The Intel HLS Compiler Standard Edition converts individual functions into RTL components. Any function that is not compiled into an RTL component is treated as part of your testbench and is compiled to x86-64 instructions. You can test your components by calling them from your `main()` function and verifying that the output is correct.

While the compiler supports C++98, you can often achieve better component performance by using the supported subset of C99 whenever possible. The compiler is capable of synthesizing some C++ constructs, which might be easier for you to use to create cleaner code.


The Intel HLS Compiler Standard Edition compiles all the code in the function or functions that you label as components, and any code that these components call, to an RTL representation.

You can identify a function in your C++ application that you want to synthesize into an IP core in one of the following ways:

- Insert the `component` keyword in the source code before the top-level C++ function to be synthesized.
- Specify the function on the command line by using the `--component <component_list>` option of the `i++` command.

To use this option, your component must be configured with C-linkage using the `extern "C"` specification. For example:

```c
extern "C" int myComponent(int a, int b)
```
Important: Components are synthesized for all functions labeled with the component keyword and all for all components listed in the --component <component_list> option of the i++ command. Avoid combining these methods because you might unexpectedly synthesize unwanted components.

If you do not want components synthesized for a function, ensure that you do not have the component attribute specified in the function and ensure that the function is not specified in the --component <component_list> option of the i++ command.

You can see which components were synthesized in the Area Analysis by Source section of the high-level design report (<name>.prj/reports/report.html). For more information about the high-level design report, see The Intel HLS Compiler High-Level Design Reports (report.html) on page 11.

The HLS compiler creates an executable to run on the CPU. The compiler then sends any calls to functions that you declared as components to simulation of the synthesized IP core, and the simulation results are returned.

3.1. Intel HLS Compiler Standard Edition Compiler-Defined Preprocessor Macros

The Intel HLS Compiler Standard Edition has built-in macros that you can use to customize your code to create flow-dependent behaviors.

<table>
<thead>
<tr>
<th>Tool Invocation</th>
<th><strong>INTELFPGA_COMPILER</strong></th>
</tr>
</thead>
<tbody>
<tr>
<td>g++ or cl</td>
<td>Undefined</td>
</tr>
<tr>
<td>i++ -march=x86-64</td>
<td>1910</td>
</tr>
<tr>
<td>i++ -march=&quot;&lt;FPGA_family_or_part_number&gt;&quot;</td>
<td>1910</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Tool Invocation</th>
<th>HLS_SYNTHESES</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Testbench Code</td>
</tr>
<tr>
<td>g++ or cl</td>
<td>Undefined</td>
</tr>
<tr>
<td>i++ -march=x86-64</td>
<td>Undefined</td>
</tr>
<tr>
<td>i++ -march=&quot;&lt;FPGA_family_or_part_number&gt;&quot;</td>
<td>Undefined</td>
</tr>
</tbody>
</table>
4. Verifying the Functionality of Your Design

Verify the functionality of your design by compiling your component and testbench to an x86-64 executable that you can debug with a native C++ debugger.

Compiling your design to an x86-64 executable is faster than compiling your component to RTL. This faster compilation time lets you debug and refine your component algorithms quickly before you move on to see how your component is implemented in hardware.

You can compile your component and testbench to an x86-64 executable for functional verification with any of the following methods:

- Use the `i++ -march=x86-64` command.
- On Linux systems, use the `g++` command.
- On Windows systems, use Microsoft Visual Studio.

Ensure that you set your compiler command to include debug information. The `i++` command generates debug information by default.

On Linux systems, you can use GDB to debug your component and testbench if you use the `g++` compiler or the `i++ -march=x86-64` command to compile your code for functional verification.

On Windows systems, you can use the Visual Studio debugger only if you compile your component and testbench with the Visual Studio compiler. You must specify the `/Zi` flag to enable debug information.


You can automate the process by using a makefile or a batch script. Use the makefiles and scripts provided in the Intel HLS Compiler Standard Edition example designs and tutorials as guides for creating your own makefiles or batch scripts.
5. Optimizing and Refining Your Component

After you have verified the functionality of your component and testbench, you can compile your component to RTL and review the high-level design report to further optimize and refine your component design. The high-level design report shows estimates of various aspects of how your component will be implemented in hardware. By compiling your component to RTL and reviewing the high-level design report, you can see how your code changes affect your component hardware implementation without needing to run a simulation or a synthesizing hardware through a full Quartus compilation.

To compile your component to RTL without running a simulation, issue the following command:

```
i++ -march="<FPGA_family_or_part_number>" --simulator none
```

You can also compile your component with a ModelSim* simulation testbench by omitting the `--simulator none` option. Compiling without a simulation test bench is faster, but you cannot measure component latency or create waveforms without simulation.

The Intel HLS Compiler High-Level Design Reports (report.html)

The High-Level Design Reports are a collection of reports accessed through an HTML file called `report.html` that you can view in a web browser. You can find the high-level design report in the `<name>.prj/reports` folder created when you compile your component to RTL.

Use the high-level design report to review information about your component, including the following information:

- Loop information, including unroll status, pipelining status, and initiation interval
- Component visualization including load-store units, component interfaces, loops, and local memory systems

After you simulate your component, the verification statistics report is populated with information such as component latency and the occupancy of I/O interfaces. For more details about your simulation, generate and view ModelSim waveforms.

After you synthesize your component with Intel Quartus Prime software, the following additional information is available in the report:

- Maximum clock frequency ($f_{\text{MAX}}$)
- Accurate area usage estimate

For more information about the high-level design report and how to use it to optimize and refine your component, see Reviewing the High Level Design Reports (report.html) on page 20.
For information about techniques that you can apply to optimize and refine your component, see Intel High Level Synthesis Compiler Standard Edition Best Practices Guide.
6. Simulating Your Design

When compiling your component to RTL, the Intel HLS Compiler Standard Edition links your design C++ testbench with an RTL-compiled version of your component that runs in an RTL simulator.

The Intel HLS Compiler Standard Edition uses Mentor Graphics® ModelSim software to simulate your design. You must have ModelSim installed to use the Intel HLS Compiler. For a list of supported versions of the ModelSim software, refer to the EDA Interface Information section in the Intel Quartus Prime Software and Device Support Release Notes.

- To verify the functional correctness of your component with your C++ testbench, run the executable that the compiler generates by targeting the FPGA architecture. By default, the name of the executable is a.out (Linux) or a.exe (Windows).

Example command you might invoke for a simple single-file design:

Linux: i++ -march="Arria10" [...] design.cpp && ./a.out

Windows: i++ -march="Arria10" [...] design.cpp && a.exe

Related Information
- Mentor Graphics ModelSim Software Prerequisites for the Intel HLS Compiler
- EDA Interface Information (Intel Quartus Prime Standard Edition) Software

6.1. Generation of the Verification Testbench Executable

When you include -march="<FPGA_family_or_part_number>" in your i++ command, the HLS compiler identifies the components and performs high-level synthesis on them. It then generates an executable to run a verification testbench.

The HLS compiler performs the following tasks to generate the verification executable:

1. Parses your design, and extracts the functions and symbols necessary for component synthesis to the FPGA. The HLS compiler also extracts the functions and symbols necessary for compiling the C++ testbench.
2. Compiles the testbench code to generate an x86-64 executable that also runs the simulator.
3. Compiles the code for component synthesis to the FPGA. This compilation generates RTL for the component and an interface to the x86-64 executable testbench.
6.2. Debugging during Verification

By default, the HLS compiler instructs the simulator not to log any signals because logging signals slows the simulation, and the waveforms files can be very large. However, you can configure the compiler to save these waveforms for debugging purposes.

To enable signal logging in the simulator, invoke the `i++` command with the `-ghdl` option in your `i++` command, as follows:

```
i++ -march="<FPGA_family_or_part_number>" -ghdl <input files>
```

**Remember:** After you compile your component and testbench with the `-ghdl` option, run the resulting executable to run the simulation and generate the waveform. By default, the name of the executable is `a.out` (Linux) or `a.exe` (Windows).

When the simulation finishes, open the `vsim.wlf` file inside the `<result>.prj/verification` directory to view the waveform.

To view the waveform after the simulation finishes:

1. In ModelSim, open the `vsim.wlf` file inside the `<result>.prj/verification` directory.
2. Right-click the `<component_name>_inst` block and select **Add Wave**.

You can now view the component top-level signals: `start`, `busy`, `stall`, `done`, parameters, and outputs. Use the waveform to see how the component interacts with its interfaces.

**Tip:** When you view the simulation waveform in ModelSim, the simulation clock period is set to a default value of 1000 picoseconds (ps). To synchronize the **Time** axis to show one cycle per tick mark, change the time resolution from picoseconds (ps) to nanoseconds (ns):

a. Right-click the timeline and select **Grid, Timeline & Cursor Control**.

b. Under **Timeline Configuration**, set the **Time units** to **ns**.

6.3. High-Throughput Simulation (Asynchronous Component Calls) Using Enqueue Function Calls

An explicit call to a component in simulation is a blocking call. To be consistent with C++ language conventions, the testbench waits for a return value from the component before continuing execution. This blocking call results in serial execution of the component. You can test how well successive invocations of your component can be pipelined by queuing inputs to the component before executing the component. You can queue inputs to a component that has explicit interfaces by using enqueue function calls from the cosimulation library. Estimate the throughput of your component by dividing the component fMAX by the component initiation interval (II), which indicates approximately how many times your component is invoked per second.
Table 5. Functions from Cosimulation Library for Queuing Inputs to the Component with Explicit Interfaces

<table>
<thead>
<tr>
<th>Function</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><code>ihc_hls_enqueue(void* retptr, void* funcptr, ...)</code></td>
<td>This function enqueues one invocation of an HLS component. The return value is stored in the first argument which should be a pointer to the return type. The component does not execute until the <code>ihc_hls_component_run_all()</code> function is invoked.</td>
</tr>
<tr>
<td><code>ihc_hls_enqueue_noret(void* funcptr, ...)</code></td>
<td>This function is similar to <code>ihc_hls_enqueue(void* retptr, void* funcptr, ...)</code>, except that it does not have an output pointer to capture return values.</td>
</tr>
<tr>
<td><code>ihc_hls_component_run_all (void* funcptr)</code></td>
<td>This function executes all enqueued calls to the specified component in a pipelined fashion.</td>
</tr>
</tbody>
</table>

6.3.1. Execution Model

Execution of enqueued component calls only occurs when the `ihc_hls_component_run_all(void* funcptr)` function is called. All externally visible side effects of the execution (for example, return data, pointers, or masters) are not visible in the testbench until the `ihc_hls_component_run_all()` function explicitly triggers the execution.

6.3.2. Comparison of Explicit and Enqueued Function Calls

The `ihc_hls_enqueue` and `ihc_hls_enqueue_noret` functions allow a new invocation of a component to start every cycle if the component can be pipelined with a component initiation interval (II) of one. If the component II is greater than one, then the component invocation starts after II number of cycles.

Figure 2 on page 16 illustrates the waveform of the signals for the component `dut`. The testbench does not include any enqueue function calls.

```
#include "HLS/hls.h"
#include <stdio.h>

component int dut(int a, int b) {
    return a*b;
}

int main (void) {
    int x1, x2, x3;
    x1 = dut(1, 2);
    x2 = dut(3, 4);
    x3 = dut(5, 6);
    printf("x1 = %d, x2 = %d, x3 = %d\n", x1, x2, x3);
    return 0;
}
```
Figure 2. **Waveform Diagram of the Signals for Component dut Without Enqueue Function Calls**

![Waveform Diagram for Component dut Without Enqueue Function Calls](image)

Figure 3 on page 16 illustrates the waveform of the signals for the component `dut` when the testbench includes enqueue function calls. Observe how the component is passed new data each clock cycle, and compare this waveform with the earlier waveform.

```c
#include "HLS/hls.h"
#include <stdio.h>

component int dut(int a, int b) {
    return a*b;
}

int main (void) {
    int x1, x2, x3;
    ihc_hls_enqueue(&x1, &dut, 1, 2);
    ihc_hls_enqueue(&x2, &dut, 3, 4);
    ihc_hls_enqueue(&x3, &dut, 5, 6);
    ihc_hls_component_run_all(&dut);
    printf("x1 = %d, x2 = %d, x3 = %d\n", x1, x2, x3);
    return 0;
}
```

Figure 3. **Waveform Diagram of the Signals for Component dut With Enqueue Function Calls**

![Waveform Diagram for Component dut With Enqueue Function Calls](image)
7. Synthesize your Component with Intel Quartus Prime Standard Edition

When you are satisfied with the predicted performance of your component, you can then perform the longer hardware synthesis compilation with Intel Quartus Prime Standard Edition. This compilation also generates accurate area and performance ($f_{\text{MAX}}$) estimates for your design, however your design is not expected to cleanly close timing in the Intel Quartus Prime reports.

After the Intel Quartus Prime compilation completes, the high level design report shows the area and performance data for your components. These estimates are more accurate than estimates generated when you compile your component with the Intel HLS Compiler.

Typical Intel Quartus Prime compilation times can take minutes to hours depending on the size and complexity of your components.

To synthesize your component and generate quality of results (QoR) data, do one of the following actions:

- Instruct the HLS compiler to run the Intel Quartus Prime compilation flow automatically after synthesizing the components. Include the `--quartus-compile` option in your `i++` command.

```bash
i++ -march="<FPGA_family_or_part_number>" --quartus-compile ...
```

- If you have generated the RTL for your component, navigate to the `quartus` directory and compile the Intel Quartus Prime project by running the following command:

```bash
quartus_sh --flow compile quartus_compile
```

*Tip:* Add the path to `quartus_sh` (Linux) or `quartus_sh.exe` (Windows) to your PATH environment variable.
8. Integrating your IP into a System

To integrate your HLS compiler-generated IP into a system with Intel Quartus Prime, you must be familiar with Intel Quartus Prime Standard Edition as well as the Platform Designer (formerly Qsys) system integration tool included with Intel Quartus Prime. The `<result>.prj/components` directory contains all the files you need to include your IP in an Intel Quartus Prime project. The IP that the HLS compiler generates for each component is self contained. You can move the folders in the `components` directory to a different location or machine if desired.

**Important prerequisite for Intel® Max® 10 FPGA users:**
If you develop your component IP for Intel MAX® 10 devices and you want to integrate your component IP into a system that you are developing in Intel Quartus Prime, ensure that the Intel Quartus Prime settings file (.qsf) for your system contains one of the following lines:

- `set_global_assignment -name INTERNAL_FLASH_UPDATE_MODE "SINGLE IMAGE WITH ERAM"`
- `set_global_assignment -name INTERNAL_FLASH_UPDATE_MODE "SINGLE COMP IMAGE WITH ERAM"`

When you compile a component for the Intel MAX 10 device family with the Intel HLS Compiler, the generated Intel Quartus Prime example project contains all of the required QSF settings for your component. However, the Intel Quartus Prime project for the system into which you integrate your component might not have the required QSF setting.

### 8.1. Adding the HLS Compiler-Generated IP into an Intel Quartus Prime Standard Edition Project

To use the IP generated by the Intel HLS Compiler Standard Edition in an Intel Quartus Prime Standard Edition project, you must first add the `.qsys` file to the project.

The `.qsys` file contains information to add to all of the necessary HDL files for the component. It also applies to any component-specific Intel Quartus Prime Settings File (QSF) settings that are necessary for IP synthesis.

1. Create an Intel Quartus Prime Standard Edition project.
2. Click **Project ➤ Add/Remove Files in Project**.
3. In the **Settings** dialog box, browse to and select the component `.qsys` file.
For example, `<result>.prj/components/<component_name>/
<component_name>.qsys`

4. Instantiate the component top-level module in the Intel Quartus Prime project. For an example on how to instantiate the component's top-level module, refer to the `<result>.prj/components/<component_name>/
<component_name>_inst.v` file.

**8.2. Adding the HLS Compiler-Generated IP into a Platform Designer System**

To use the HLS compiler-generated IP in a Platform Designer (formerly Qsys) System, you must first add the directory to the IP search path or the IP Catalog.

In Platform Designer, if your HLS compiler-generated IP does not appear in the IP Catalog, perform the following tasks:

1. In Intel Quartus Prime, click **Tools ➤ Options**.
2. In the **Options** dialog box, under Category, expand **IP Settings** and click **IP Catalog Search Locations**.
3. In the **IP Catalog Search Locations** dialog box, add the path to the directory that contains the `.qsys` file to IP Search Paths. To find all the components, specify the path as `<result>.prj/components/**/*`.
4. In **IP Catalog**, add your IP to the Platform Designer system by selecting it from the HLS project directory.

For more information about Platform Designer, see "Creating a System with Platform Designer (Standard)" in *Intel Quartus Prime Standard Edition Handbook Volume 1: Design and Compilation*. 
A. Reviewing the High Level Design Reports 
(report.html)

After compiling your component, the Intel HLS Compiler Standard Edition generates an HTML report that helps you analyze various component aspects, such as area, loop structure, memory usage, and component pipeline. To launch the high level design report, open the following file in a web browser: <result>.prj/reports/report.html.

A.1. High Level Design Report Layout

The High Level Design Report (report.html) is divided into the following four main sections:

- Reports menu
- Analysis pane
- Source code pane
- Details pane

[Diagram of report.html layout]

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Reports Menu

You can select a report to view an analysis of different parts of your component design. All reports are interlinked. Click View reports to see the list of available reports.

Analysis Pane

The analysis pane displays detailed information of the report you selected from the reports menu.

Source Code Pane

The source code pane displays the code for all the source files in your component.

To select between different source files in your component, click the pull-down menu at the top of the source code pane. To collapse the source code pane, do one of the following actions:

- Click the X icon beside the source code pane pull-down menu.
- Click the vertical ellipsis icon on the right-hand side of the Reports menu and then select Show/Hide source code.

If you previously collapsed the source code pane and want to expand it, click the vertical ellipse icon on the right-hand side of the Reports menu and then select Show/Hide source code.

The source code is displayed when you have not specified the -g0 compiler command option when you compiled your code.
Details Pane

For each line that appears in a loop analysis or area report, the Details pane shows additional information, if available, that elaborates on the comment in the Details column report. To collapse the Details pane, do one of the following actions:

- Click the X icon on the right-hand side of the Details pane.
- Click the vertical ellipsis icon on the right-hand side of the Reports menu and then select Show/Hide details.

A.2. Reviewing the Report Summary

The report summary gives you a quick overview of the results of compiling your design including a summary of each component in your design and a summary of the estimated resources that each component in your design uses.

The report summary is divided into the following sections: Info, Quartus Fit Summaries, Estimated Resource Usage, and Compile Warnings.
A. Reviewing the High Level Design Reports (report.html)

The Info section shows general information about the compile including the following items:

- Name of the project
- Target FPGA family and device
- Intel Quartus Prime version
- HLS compiler version
- The command that was used to compile the design
- The date and time at which the reports were generated
Quartus Fit Summaries

After you compile your design with Intel Quartus Prime Standard Edition software, the sections that summarize the compilation results are populated. The following sections appear on the Summary page:

- Quartus Fit Clock Summary
- Quartus Fit Resource Utilization Summary

The Quartus Fit Clock Summary section shows the maximum clock frequency that can be achieved for the design.

The Quartus Fit Resource Utilization Summary section shows the total area utilization both for the entire design, and for each component individually. There is no breakdown of area information by source line.

Estimated Resource Usage

The Estimated Resource Usage section shows a summary of the estimated resources used by each component in your design, as well as the total resources used for all components.

Compile Warnings

The Compile Warnings section shows the compiler warnings generated during the compilation.

A.3. Reviewing Loop Information

The Throughput Analysis section of the high-level design reports (<result>.prj/reports/report.html) file contains information about all the loops in your design and their unroll statuses. This loop analysis report helps you examine whether the Intel HLS Compiler Standard Edition is able to maximize the throughput of your component.

You can use the loop analysis report to help determine where to deploy one or more of the following pragmas on your loops:

- #pragma unroll
  For details about #pragma unroll, see "Loop Unrolling (unroll Pragma)" in Intel High Level Synthesis Compiler Standard Edition Reference Manual.

- #pragma loop_coalesce

- #pragma ii

- #pragma max_concurrency
  For details about #pragma max_concurrency, see "Loop Concurrency (max_concurrency Pragma)" in Intel High Level Synthesis Compiler Standard Edition Reference Manual.
1. Click **Throughput Analysis ➤ Loop Analysis**.
2. In the analysis pane, select **Show fully unrolled loops** to obtain information about the loops in your design.

### A.3.1. Loop Analysis Example

Figure 4 on page 26 shows an example High Level Design Report (report.html) file that shows the loop analysis of a component design taken from the `transpose_and_fold.cpp` file (part of the tutorial files provided in `<quartus_installdir>/hls/examples/tutorials/best_practices/loop_memory_dependency`).

Consider the following example code snippet for `transpose_and_fold.cpp`:

```c++
01: #include "HLS/hls.h"
02: #include <stdio.h>
03: #include <stdlib.h>
04:
05: #define SIZE 32
06:
07: typedef ihc::stream_in<int> my_operand;
08: typedef ihc::stream_out<int> my_result;
09:
10: component void transpose_and_fold(my_operand &data_in, my_result &res)
11: {
12:   int i;
13:   int j;
14:   int in_buf[SIZE][SIZE];
15:   int tmp_buf[SIZE][SIZE];
16:   for (i = 0; i < SIZE * SIZE; i++) {
17:     in_buf[i / SIZE][i % SIZE] = data_in.read();
18:     tmp_buf[i / SIZE][i % SIZE] = 0;
19:   }
20:
21: #ifdef USE_IVDEP
22: #pragma ivdep safelen(SIZE)
23: #endif
24:   for (j = 0; j < SIZE * SIZE * SIZE; j++) {
25:     #pragma unroll
26:     for (i = 0; i < SIZE; i++) {
27:       tmp_buf[j % SIZE][i] += in_buf[i % SIZE];
28:     }
29:   }
30:   for (i = 0; i < SIZE * SIZE; i++) {
31:     res.write(tmp_buf[i / SIZE][i % SIZE]);
32:   }
33: }
```
Figure 4. Loop Analysis Report of the transpose_and_fold Component

The transpose_and_fold component has four loops. The loop analysis report shows that the compiler performed different kinds of loop optimizations:

- The loop on line 26 is fully unrolled, as defined by `#pragma unroll`.
- The loops on lines 16 and 30 are pipelined with an II value of $\sim 1$. The value is $\sim 1$ because both loops contain access to streams that could stall. If these access stall, then the loop II becomes greater than 1.

The `Block1.start` loop in the loop analysis report is not present in the code. It is an implicit infinite loop that the compiler adds to allow the component to run continuously, instead of only once. In hardware, the component run continuously and checks its inputs to see if it should start executing.

A.4. Reviewing Component Area Usage

The High Level Design Report (report.html) provides a detailed breakdown of the estimated FPGA area usage.

The estimated area usage information correlates with, but does not necessarily match, the resource usage results from the Intel Quartus Prime Standard Edition software. Use the estimated area usage to identify parts of the design with large area overhead. You can also use the estimates to compare area usage between different designs. Do not use the estimated area usage information for final resource utilization planning.

The Quartus Fit Summary section of the High Level Design Report Summary page is populated after compiling your design with Intel Quartus Prime software. After that compilation, the following sections appear on the Summary page:

- Quartus Fit Clock Summary
- Quartus Fit Resource Utilization Summary

The Quartus Fit Clock Summary section shows the maximum clock frequencies that can be achieved for the design.

The Quartus Fit Resource Utilization Summary section shows the total area utilization both for the entire design, and for each component individually. There is no breakdown of area information by source line.
Tip: Compiling your component using the Intel Quartus Prime software might take several hours. In contrast, the Intel HLS Compiler can generate the High Level Design Report in minutes for most designs.

Before compiling your design with Intel Quartus Prime software, the High Level Design Report looks like the following example:

```
Summary

Info
Project Name:/a
Target Family, Device: Arria 1010AX115U1F451SG
i++ Version:19.1.0 Build 670
Quartus Version: 10.1.0 Build 670
Command:i++ -march=arria10 transpose_and_fold.cpp -- simulator none
Reports Generated At:Mon Dec 9 15:34:31 2019

Quartus Fit Summary
Run Quartus compile to populate this section. See details for more information.

Estimated Resource Usage

<table>
<thead>
<tr>
<th>Component Name</th>
<th>ALUTs</th>
<th>FFs</th>
<th>RAMs</th>
<th>DSPs</th>
</tr>
</thead>
<tbody>
<tr>
<td>transpose_and_fold</td>
<td>6056</td>
<td>4876</td>
<td>42</td>
<td>0</td>
</tr>
<tr>
<td>Total</td>
<td>6058 (1%)</td>
<td>4876 (0%)</td>
<td>42 (2%)</td>
<td>0 (0%)</td>
</tr>
<tr>
<td>Available</td>
<td>854400</td>
<td>1708800</td>
<td>2713</td>
<td>1518</td>
</tr>
</tbody>
</table>

Compile Warnings
None
```

After compiling your design with Intel Quartus Prime software, the High Level Design Report looks like the following example. The Quartus Fit Summary section is now populated.
A.4.1. Area Analysis Example

You have the option to review the area analysis of your design based on source line or system.

Area Analysis of System

Area analysis of system shows an area breakdown that is closest to the actual hardware implemented in the FPGA.
The **System** entry in the Area Analysis of System report refers to all the components in the design. Expanding the **System** entry allows you to view all the components in the design. In this example, there is only one component (that is, `transpose_and_fold`).

**Figure 5. Breakdown of Area Usage by System**

![Area Analysis Table]

**Area Analysis by Source**

Area analysis by source shows an approximation of how each line of the source code affects area. In the area analysis by source view, the report shows the area hierarchically.
The System entry in the area report refers to all the components in the design. Expanding the System entry allows you to view all the components in the design. In this example, there is only one component (that is, transpose_and_fold).

Each line in the report contains state and corresponding information. In the figure below, the example area report shows that on line 17, where a stream of data is stored to in_buf, the consumed area is used for computing the pointer value and then storing it. On line 14, area consumption is a result of in_buf using 16 RAM blocks and some logic.

**A.5. Viewing Component Design**

The High Level Design Report (report.html) contains reports that show different views into the structure, interfaces, datapaths, and computation flows in your component.

The Intel HLS Compiler Standard Edition provides the following reports about your component design:
• **Component Viewer**
The Component Viewer report shows branching in your component.

• **Component Memory Viewer**
The Component Memory Viewer report shows the data connections across the memory system of your component.

### A.5.1. Reviewing Component Interfaces

The Component Viewer shows a visual representation of the interfaces in your component. You can view details about the following interface arguments: default, pointer, pass-by-reference, Avalon Memory-Mapped (MM), and Avalon Streaming.

Some interface arguments in your component can be marked as being stable. A stable interface argument is an argument that does not change while your component executes, but the argument might change between component executions. In the Component Viewer, a stable node does not have any edge connection.

The Component Viewer displays the different interfaces as outlined in the following sections:

• **Default Interface Arguments** on page 31
• **Pointer, Pass-By-Reference, and Avalon MM Master Interface Arguments** on page 33
• **Avalon MM Slave Register Interface Arguments** on page 35
• **Avalon MM Slave Memory Interface Arguments** on page 37
• **Avalon Streaming Interface Arguments** on page 39

### Default Interface Arguments

Default interface arguments are any scalars or simple structs. The Component Viewer connects the default argument nodes to the corresponding channel read (RD) node.

```c
#include "HLS/hls.h"
#include "stdio.h"

struct coordinate_t {
    int x;
    int y;
};

cOMPONENT int default_comp(int b, coordinate_t p) {
    return b + p.x;
}
```
For each default interface argument node, you can view details about the node when you hover over the node:
**Pointer, Pass-By-Reference, and Avalon MM Master Interface Arguments**

Pointer interfaces, pass-by-reference interfaces, Avalon MM master interfaces, and global variables all correspond to addresses to memory outside of your component. Similarly to the default interface arguments, these nodes connect to the corresponding channel read (RD) node for your component.

```c
#include "HLS/hls.h"
#include "stdio.h"

component int master_comp(
  int *pointer_d,
  ihc::mm_master<int, ihc::aspace<3>, ihc::awidth<4>,
  ihc::dwidth<32>, ihc::latency<1>, ihc::align<4> > &master_i,
  int &result
)
{
  result = *pointer_d + *master_i;
  return result;
}
```

---

**A. Reviewing the High Level Design Reports (**report.html**)**

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33
The Component Viewer shows the following details for these interface arguments:

- **Stable**: Describes whether the interface argument is stable. That is, whether the `hls_stable_argument` attribute was applied.
- **Data width**: The width of the memory-mapped data bus in bits.
- **Address width**: The width of the memory-mapped address bus in bits.
- **Latency**: The guaranteed latency from when the read command exits the component to when the external memory returns valid read data. The latency is measured in clock cycles.
- **Maximum burst**: The maximum number of data transfers that can associate with a read or write transaction. For fixed latency interfaces, this value is set to 1.
- **Alignment**: The byte alignment of the base pointer address. The Intel HLS Compiler uses this information to determine the amount of coalescing that is possible for loads and stores to this pointer.
The Component Viewer shows the following details for global memories:

- **Memory address space number**: The memory address space number for global memory.
- **Number of banks**: The number of memory banks contained in the memory.
- **Argument Name**: The names of arguments that access the global memory.

### Avalon MM Slave Register Interface Arguments

When you label an interface argument as an Avalon MM slave register (hls_avalon_slave_register_argument), then the interface argument is implemented in the control and status register (CSR) slave interface. The Component Viewer puts the slave register arguments inside a CSR container.

```c
#include "HLS/hls.h"
#include "stdio.h"

component int slavereg_comp(
    int hls_avalon_slave_register_argument slave scalar_f,
    int* hls_avalon_slave_register_argument slave_pointer_g
```
The resulting memory map is described in the automatically generated header file `<component_name>_csr.h`. This header file is available in the menu in the source code pane. Clicking on the CSR container node in the Component Viewer also opens up the header file.
If you use the `hls_avalon_slave_component` macro, then the “do” and “return” streams (control and status registers) are implemented in the CSR interface:

```c
#include "HLS/hls.h"
#include "stdio.h"

hls_avalon_slave_component
component int slavereg_comp(
    int hls_avalon_slave_register_argument slave_scalar_f,
    int* hls_avalon_slave_register_argument slave_pointer_g
) {
    return slave_scalar_f + *slave_pointer_g;
}
```

### Avalon MM Slave Memory Interface Arguments

When you declare a pointer argument as a slave memory, the Component Viewer shows the slave memory interface with a `<slave memory name>` LD/ST node that is connected to the Local Memory node in the component.

```c
#include "HLS/hls.h"
#include "stdio.h"
```
If you look at the same Avalon MM slave memory interface in the Component Memory Viewer report, the same `<slave memory name> LD/ST` node is shown to be connected to an external `<slave memory name>` LD/ST port.
Avalon Streaming Interface Arguments

A streaming interface is shown in the Component Viewer by a `<stream name>` node connected to the corresponding RD node (for `stream_in<>`) or WR node (for `stream_out<>`).

```c
#include "HLS/hls.h"
#include "stdio.h"

component int stream_comp(
    ihc::stream_in<int> &stream_in_c,
    ihc::stream_out<int> &stream_out_e,
    int scalar_b
) {

    stream_out_e.write(scalar_b + 1);
    return stream_in_c.read() + scalar_b * 2;
}
```
The Component Viewer shows the following details for streaming interface arguments:

**Width**

The width of the data bus in bits.

The Component Viewer shows the following details for streaming interface arguments:

**stream_stream_in_c Info**

- Width: 32 bits
- Depth: 0
- Bits per symbol: 32 bits
- Uses Packets: No
- Uses Valid: Yes

**stream_stream_out_e Info**

- Width: 32 bits
- Depth: 0
- Bits per symbol: 32 bits
- Uses Packets: No
- Uses Ready: Yes
A. Reviewing Memory Replication and Stallable LSU Information

The Component Viewer report in the High Level Design Report (report.html) shows an abstracted netlist of your kernel design. In the Component Viewer, you can visualize load-store units (LSUs) between a component and different memories, streams, and loops.

Consider the following code excerpt from the transpose_and_fold component (part of the tutorial files provided in <QPDS_installdir>/hls/examples/tutorials/loop_memory_dependency):

```c
#include "HLS/hls.h"
#include "stdio.h"
#include "stdlib.h"

#define SIZE 32

typedef altera::stream_in<int> my_operand;
typedef altera::stream_out<int> my_result;

void transpose_and_fold(my_operand &a, my_operand &b, my_result &c) {
    int i;
    int j;
    int a_buf[SIZE][SIZE], b_buf[SIZE][SIZE];
    for (i = 0; i < SIZE * SIZE; i++) {
        a_buf[i / SIZE][i % SIZE] = a.read();
        b_buf[i / SIZE][i % SIZE] = b.read();
    }
    #ifdef USE_IVDEP
    #pragma ivdep
    #endif
    for (j = 0; j < SIZE * SIZE * SIZE; j++) {
        #pragma unroll
        for (i = 0; i < SIZE; i++)
            b_buf[j % SIZE][i] += a_buf[i][j % SIZE];
    }
    for (i = 0; i < SIZE * SIZE; i++)
        b_buf[i] += a_buf[i];
}
```

A.5.2. Reviewing Memory Replication and Stallable LSU Information

The Component Viewer report in the High Level Design Report (report.html) shows an abstracted netlist of your kernel design. In the Component Viewer, you can visualize load-store units (LSUs) between a component and different memories, streams, and loops.

Consider the following code excerpt from the transpose_and_fold component (part of the tutorial files provided in <QPDS_installdir>/hls/examples/tutorials/loop_memory_dependency):

```c
#include "HLS/hls.h"
#include "stdio.h"
#include "stdlib.h"

#define SIZE 32

typedef altera::stream_in<int> my_operand;
typedef altera::stream_out<int> my_result;

void transpose_and_fold(my_operand &a, my_operand &b, my_result &c) {
    int i;
    int j;
    int a_buf[SIZE][SIZE], b_buf[SIZE][SIZE];
    for (i = 0; i < SIZE * SIZE; i++) {
        a_buf[i / SIZE][i % SIZE] = a.read();
        b_buf[i / SIZE][i % SIZE] = b.read();
    }
    #ifdef USE_IVDEP
    #pragma ivdep
    #endif
    for (j = 0; j < SIZE * SIZE * SIZE; j++) {
        #pragma unroll
        for (i = 0; i < SIZE; i++)
            b_buf[j % SIZE][i] += a_buf[i][j % SIZE];
    }
    for (i = 0; i < SIZE * SIZE; i++)
        b_buf[i] += a_buf[i];
}
```
30     c.write(b_buf[i / SIZE][i % SIZE]);
31   }
32 }

The figure below shows that Block3 is highlighted in red to prompt you to review the loop. Because loop analysis of Block3 shows that it is a pipelined loop with an II value of 2, the loop pipeline might affect the throughput of your design. The Component Viewer shows that the II value is caused by a memory dependency on loads to the b_buf variable.

Figure 7.  Component View of the transpose_and_fold Component
By hovering your mouse pointer over a node, you can view the tooltip and details that provide more information on the LSU. In the figure below, the tooltip shows information like the latency and that the LSU is stall-free.

**Figure 8. Detailed View of Node and Tooltip**

The Component Viewer allows you to select the type of connections you want to view. Selecting **Control** instructs the system viewer to display the connections between blocks and loops. Selecting **Memory** instructs the function view of the Graph Viewer to display the connections to and from global and local memories. Selecting **Streams** instructs the system viewer to display the connections reading from and writing to streams.
A.5.3. Viewing Your Component Memory System

Data movement is a bottleneck in many algorithms. The Component Memory Viewer in the High Level Design Report (report.html) shows you how the Intel HLS Compiler Standard Edition interprets the data connections across the memory system of your component. Use the Component Memory Viewer to help you identify data movement bottlenecks in your component design.
Some patterns in memory accesses can cause undesired arbitration in the load-store units (LSUs), which can affect the throughput performance of your component. Use the Component Memory Viewer to find where you might have unwanted arbitration in the LSUs.

The Component Memory Viewer has the following panes:

**Memory List**

The Memory List pane shows you a hierarchy of components, memories in that component, and the corresponding memory banks.

Clicking a memory name in the list displays a graphical representation of the memory in the Component memory viewer pane. Also, the line in your code where you declared the memory is highlighted in the Source Code pane.

Clearing a check box for a memory bank collapses that bank in the Component Memory Viewer pane, which can help you to focus on specific memory banks when you view a complex memory design. By default, all banks in component memory are selected and shown in the Component Memory Viewer pane.
The Component Memory Viewer pane shows you connections between loads and stores to specific logical ports on the banks in a memory system. The following types of nodes might be shown in the Component Memory Viewer pane, depending on the component memory system:

- **Memory node**: The component memory.
- **Bank node**: A bank in the memory. Only banks selected in the Memory List pane are shown. Select banks in the Memory List pane to help you focus on specific memory banks when you view a complex memory design.
- **Port node**: The logical port for a bank. There are three types of port:
  - **R**: A read-only port
  - **W**: A write-only port
  - **RW**: A read and write port
- **LSU node**: A store (ST) or load (LD) node connected to the memory.
- **Arbitration node**: An arbitration (ARB) node shows that LSUs compete for access to a shared port node, which can lead to stalls.
- **Port-sharing node**: A port-sharing node (SHARE) shows that LSUs have mutually exclusive access to a shared port node, so the load-store units are free from stalls.

Hover over any node to view the attributes of that node.

Hover over an LSU node to highlight the path from the LSU node to all of the ports that the LSU connects to.

Hover over a port node to highlight the path from the port node to all of the LSUs that store to the port node.

Click a node to select it and have the node attributes displayed in the Details pane.

The Details pane shows the attributes of the node selected in the Component Memory Viewer pane. For example, when you select a memory in a component, the Details pane shows information such as the width and depths of the memory banks, as well as any user-defined HLS attributes that you specified in your source code.

The content of the Details pane persists until you select a different node in the Component Memory Viewer pane.

### A.6. Reviewing Your Component Verification Results

For each component that the testbench calls, the verification statistics report provides information such as the number and type of invocations, latency, initiation interval, and throughput.

The verification statistics report becomes available after you simulate your component.
Important:

- The data presented in the verification statistics report might be dependent on the input values to the component from the test bench.
- The verification statistics report only reports the component loop initiation interval (II) values and throughput for enqueued invocations.

The following example verification statistics report is for a component `dut` that has been run once as a simple function call and 100 times as an enqueued invocation:

<table>
<thead>
<tr>
<th>Verification Statistics</th>
<th>Invocation</th>
<th>Latency (not measured)</th>
<th># Invocations</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test component invocations</td>
<td>100</td>
<td>4.4</td>
<td>100</td>
<td>Link for details</td>
</tr>
<tr>
<td>Explicit component invocations (Single Location)</td>
<td>1</td>
<td>4.4</td>
<td>100</td>
<td>Link for details</td>
</tr>
<tr>
<td>Enqueued component invocations (Single Location)</td>
<td>100</td>
<td>4.4</td>
<td>100</td>
<td>1.1</td>
</tr>
</tbody>
</table>

For components that use explicit streams, such as `ihc::stream_in<>` or `ihc::stream_out<>`, the verification statistics report also provides the throughput for each individual stream, as shown in the details pane:

A.7. Accessing HLD FPGA Reports in JSON Format

The High-Level Design Report data for the Intel HLS Compiler Standard Edition is also available as JSON-formatted data.

The JSON files containing the report data are available in the `<result>.prj/reports/lib/json` directory. The directory provides the following `.json` files:

Table 6. JSON Files in the `<result>.prj/reports/lib/json Directory

<table>
<thead>
<tr>
<th>File</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>area.json</td>
<td>Area Analysis of System</td>
</tr>
<tr>
<td>area_src.json</td>
<td>Area Analysis of Source</td>
</tr>
<tr>
<td>info.json</td>
<td>Summary</td>
</tr>
<tr>
<td>loops.json</td>
<td>Loop Analysis</td>
</tr>
<tr>
<td>mav.json</td>
<td>Component Viewer</td>
</tr>
<tr>
<td>lmv.json</td>
<td>Component Memory Viewer</td>
</tr>
<tr>
<td>quartus.json</td>
<td>Summary</td>
</tr>
<tr>
<td>summary.json</td>
<td>Summary</td>
</tr>
<tr>
<td>warnings.json</td>
<td>Summary</td>
</tr>
</tbody>
</table>
You can read the following .json files without a special parser:

- area.json
- area_src.json
- loops.json
- quartus.json
- summary.json

For example, if you want to identify all of the values and bottlenecks for the initiation interval (II) of a loop, you can find the information in the `children` section in the `loops.json` file, as shown below:

```json
"name":"<block name|Component: component name>  # Find the loops which does not begin with "Component:"

  "data": [<Yes|No>, <#|n/a>, <II|n/a>]  # The data field corresponds to "Pipelined", "II", "Bottleneck"
```

A. Reviewing the High Level Design Reports (report.html)

UG-20266 | 2019.12.18
B. Limitations of the Intel HLS Compiler Standard Edition

When creating your IP using the HLS compiler, be aware of the current set of software and programming limitations.

Compiler support

- **Linux compiler support**
  - The HLS compiler does not support GCC 4.7.0 or newer. The compiler requires GCC compiler and C++ Libraries version 4.4.7.

- **Windows compiler support**
  - The HLS compiler for Windows is compatible with Microsoft Visual Studio 2010 only.

C++ Language Restrictions

The Intel HLS Compiler accepts C++ code.

For the best results when you synthesize your component, code your component function with C99.

- A component cannot include virtual functions, function pointers, or bit fields.
- Function-scoped static variables that are a part of the component cannot use function arguments for initialization.

**C++ restrictions**

- The HLS compiler does not support certain C++ features such as initializer lists and lambda functions.

**Class membership**

- HLS component functions cannot be a C++ class member. However, you can declare your component function as a wrapper function. This wrapper function can call a member function of a class or a part of a namespace.

**Exception handling**

- A component cannot contain exception handling.

**Library calls**

- The HLS compiler does not currently support calls to C++ runtime libraries on Windows, including calls from the testbench code.
**Library functions**
- A component cannot contain standard C or C++ library functions, unless they are explicitly supported by header files provided with the Intel HLS Compiler.

A component that contains `printf()` or `cout` calls works in its x86 implementation. However, the generated RTL does not include the `printf()` or `cout` function calls if you include the HLS/stdio.h library or the HLS/iostream standard C library functions provided with the Intel HLS Compiler. If you try to generate RTL with the regular `stdio.h` or `iostream` headers you will likely experience compiler errors.

**Multiple inheritance**
- The HLS compiler does not support classes with multiple inheritance used as parameters. You may use classes as parameters provided that each class inherits from, at most, one class directly.

**Namespaces**
- HLS component functions cannot be a part of a declared namespace. However, you can declare your component function as a global wrapper function. This wrapper function can call a member function of a class or a part of a namespace.

**Overloading/Templates**
- Templated functions or overloaded functions cannot be components. If you need a templated or overloaded function in your component, create a wrapper component and call the templated or overloaded function from the wrapper component.

**Parameters**
- The HLS compiler does not support classes with multiple inheritance used as parameters. You may use classes as parameters as long as each class inherits from, at most, one class directly.

**Recursion**
- The HLS compiler does not support the synthesis of components that use recursion; however, tail recursion is supported.

If a component has an algorithm that uses recursion, and it is identified for FPGA acceleration, modify the algorithm to use tail recursion, if possible.
# C. Intel HLS Compiler Standard Edition User Guide Archives

<table>
<thead>
<tr>
<th>Intel HLS Compiler Version</th>
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<tr>
<td>18.1.1</td>
<td>Intel HLS Compiler User Guide</td>
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<tr>
<td>18.1</td>
<td>Intel HLS Compiler User Guide</td>
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<tr>
<td>18.0</td>
<td>Intel HLS Compiler User Guide</td>
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<tr>
<td>17.1.1</td>
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### Document Revision History for Intel HLS Compiler User Guide


<table>
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<th>Document Version</th>
<th>Intel Quartus Prime Version</th>
<th>Changes</th>
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</table>
| 2019.09.30       | 19.3                       | • **PRO** Added Graph Viewer (Beta).  
• Split information about viewing your component design into separate sections for Intel HLS Compiler Pro Edition and Intel HLS Compiler Standard Edition:  
  − **PRO** Viewing Component Design  
  − **STD** Viewing Component Design on page 30  
• In Verifying the Functionality of Your Design on page 10, removed information about using MSVC to debug a design compiled with the `i++` command. You cannot use MSVC to debug a design compiled with the `i++` command.  
  On Linux, you can use GDB to debug a design compiled with the `i++` command. |
| 2019.07.01       | 19.2                       | • **PRO** Updated Reviewing the High Level Design Report (report.html) to reflect the merging of various viewers into the Graph Viewer (beta). Some images in the section do not reflect the new reporting interface. The images will be updated in a future release of this document. |

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</table>
| 2019.04.01       | 19.1                       | • **PRO** Updated Reviewing the High Level Design Report (report.html) section as follows:  
  — The Function Viewer report is the new name for what previously called the Component Viewer report.  
  — Added Function Memory Viewer.  
  The Function Memory Viewer report replaces the Component Memory Viewer report.  
  — Added Reviewing System Information  
  — Added Reviewing Block Information  
  — Added Reviewing Cluster Information  
  • Updated to Synthesize your Component with Intel Quartus Prime Standard Edition on page 17 to indicate that compiling your component with Intel Quartus Prime is not intended to close timing for your component.  
  • **PRO** Revised the Limitations of the Intel HLS Compiler Pro Edition as follows:  
  — Revised C++ 14 restriction  
  — Removed Overloading/Templates limitation  
  • **PRO** Added Reviewing fMAX II Information |
  • Corrected typos in High-Throughput Simulation (Asynchronous Component Calls) Using Enqueue Function Calls on page 14 and Comparison of Explicit and Enqueued Function Calls on page 15:  
  — `ihs_hls_component_run_all` is now `ihc_hls_component_run_all`.  
  — `ihs_hls_enqueue` is now `ihc_hls_enqueue`. |
| 2018.09.24       | 18.1                       | • **PRO** The Intel HLS Compiler has a new front end. For a summary of the changes introduced by this new front end, see Improved Intel HLS Compiler Front End in the Intel High Level Synthesis Compiler Version 18.1 Release Notes.  
  • In Debugging during Verification on page 14, added a reminder to run the executable compiled with the `--ghdl` option before viewing the waveform in ModelSim.  
  • **PRO** Added information to Overview of the Intel HLS Compiler Pro Edition topic to indicate that the Intel HLS Compiler treats all input files as C++14-compliant code. While you can compile code compliant with other standards by using the `--std` compile option, not all Intel HLS Compiler features are supported for other C++ standards. |
| 2018.07.02       | 18.0                       | • Added information about viewing the high level design report data in JSON files. See Accessing HLD FPGA Reports in JSON Format on page 47 for details.  
  • Added related links to Simulating Your Design on page 13 for Mentor Graphics ModelSim prerequisites. |

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<tbody>
<tr>
<td>2018.05.07</td>
<td>18.0</td>
<td>• Starting with Intel Quartus Prime Version 18.0, the features and devices supported by the Intel HLS Compiler depend on what edition of Intel Quartus Prime you have. Intel HLS Compiler publications now use icons to indicate content and features that apply only to a specific edition as follows:</td>
</tr>
<tr>
<td></td>
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<td>PRO Indicates that a feature or content applies only to the Intel HLS Compiler provided with Intel Quartus Prime Pro Edition.</td>
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<tr>
<td></td>
<td></td>
<td>STD Indicates that a feature or content applies only to the Intel HLS Compiler provided with Intel Quartus Prime Standard Edition.</td>
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<tr>
<td></td>
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<td>• STD Added important prerequisite for Intel MAX 10 users to Synthesize your Component with Intel Quartus Prime Standard Edition on page 17.</td>
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<tr>
<td></td>
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<td>• Revised Debugging during Verification on page 14 to clarify how to view the waveform in ModelSim after simulation.</td>
</tr>
<tr>
<td>2017.12.22</td>
<td>17.1.1</td>
<td>• Corrected typos in Execution Model on page 15:</td>
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<td></td>
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<td>— ihs_hls_component_run_all is now ihc_hls_component_run_all.</td>
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<tr>
<td></td>
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<td>— ihs_hls_run_all_enqueued is now ihc_hls_component_run_all.</td>
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<td>2017.11.06</td>
<td>17.1</td>
<td>• Moved the following content to Intel High Level Synthesis Compiler Best Practices Guide:</td>
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<tr>
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<td>— Moved compiler best practice content from &quot;Creating a High-Level Synthesis Component and Testbench on page 8&quot; to &quot;Best Practices for Coding and Compiling Your Component&quot;.</td>
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<td>• Moved the following content to Intel High Level Synthesis Compiler Reference Manual:</td>
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<tr>
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<td>— Moved &quot;High Level Synthesis Component Interface Definition&quot; to Component Interface Definition.</td>
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<td>— Moved Reset Behavior section to &quot;Reset Behavior&quot;.</td>
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<td>Added new chapter &quot;Optimizing and Refining Your Component&quot; on page 11 to provide a brief introduction to the high-level design report (report.html).</td>
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<tr>
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<td>• Added new chapter &quot;Verifying the Functionality of Your Design&quot; on page 10 to provide some details about how to perform functional verification on your HLS component.</td>
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<td>• Rearranged the order of sections to better reflect the user flow of using the compiler.</td>
</tr>
<tr>
<td>2017.06.23</td>
<td>—</td>
<td>• Minor changes and corrections.</td>
</tr>
<tr>
<td>2017.06.09</td>
<td>—</td>
<td>• Updated Limitations of the Intel HLS Compiler Standard Edition on page 49 to add, remove, and change compiler limitations found in this release.</td>
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<td>• Rebranding <strong>ALERTA_COMPILER</strong> and <strong>ALTERA_TYPE</strong> to <strong>INTEL_FPGA_COMPILER</strong> and <strong>INTEL_FPGA_TYPE</strong>.</td>
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<td>• Changed references for the compiler option -march=fpga to -march=&quot;&lt;FPGA_family_or_part_number&gt;&quot;. For details about changes to the -march compiler option, see Command Options that Customize Compilation in the Intel HLS Compiler Standard Edition Reference Manual.</td>
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<td>• Added recommendation to compile components with -Wconversion to Creating a High-Level Synthesis Component and Testbench on page 8.</td>
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<td>• Added information about HLS component reset behavior in Reset Behavior.</td>
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</table>
| 2017.02.03        | —                          | • Added note about what functions have components synthesized for them when you run the i++ command.  
• Under Reviewing Your Component’s report.html File, added Component memory viewer section to introduce the Component memory viewer report.  
• Under Reviewing Your Component’s report.html File, updated examples and screen captures to reflect examples and tutorials provided with the Intel HLS Compiler.  
• Updated the values for the __ALTERA_COMPILER__ HLS compiler-defined preprocessor macro. |
| 2016.11.30        | —                          | • Under Reviewing Your Component’s report.html File, added the Information on Component Verification Results section to introduce the Verification Statistics report.  
• In Verifying Your HLS IP, noted that information on the supported versions of the ModelSim software is available in the Intel Quartus Prime Software and Device Support Release Notes.  
• Removed the Latency Measurement during Verification section because the APIs described within have been removed.  
• In Adding the Compiler-Generated IP into a Intel Quartus Prime Project and Adding the Compiler-Generated IP into a Qsys System, specified that for the Intel Quartus Prime Standard Edition software, the file in question is the .qsys file. For the Intel Quartus Prime Pro Edition software, the file in question is the .ip file.  
• Updated the Limitations of the HLS Compiler section:  
  — Removed the limitation on ModelSim software version support.  
  — Added the limitation that C++ library calls are not supported on Windows. |
| 2016.09.12        | —                          | • Initial release. |