

Introduction

This chapter provides guidelines on using the IEEE Std. 1149.1 boundary-scan test (BST) circuitry in Cyclone® III family devices (Cyclone III and Cyclone III LS devices). BST architecture tests pin connections without using physical test probes, and captures functional data while a device is operating normally. Boundary-scan cells (BSCs) in a device can force signals onto pins or capture data from pin or logic array signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared to expected results.

This chapter contains the following sections:

- “IEEE Std. 1149.1 BST Architecture” on page 12–1
- “IEEE Std. 1149.1 BST Operation Control” on page 12–2
- “I/O Voltage Support in a JTAG Chain” on page 12–5
- “Guidelines for IEEE Std. 1149.1 BST” on page 12–6
- “Boundary-Scan Description Language Support” on page 12–7

IEEE Std. 1149.1 BST Architecture

Cyclone III family devices operating in the IEEE Std. 1149.1 BST mode use four required pins:

- TDI
- TDO
- TMS
- TCK

The TCK pin has an internal weak pull-down resistor, while the TDI and TMS pins have weak internal pull-up resistors. The TDO output pin and all the JTAG input pins are powered by the 2.5-V or 3.0-V V_{CCIO} supply. All user I/O pins are tri-stated during JTAG configuration.



For recommendations on how to connect a JTAG chain with multiple voltages across the devices in the chain, refer to [“I/O Voltage Support in a JTAG Chain” on page 12–5](#).



For more information on the description and functionality of all JTAG pins, registers used by the IEEE Std. 1149.1 BST circuitry, and the test access port (TAP) controller, refer to [AN39: IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices](#).

IEEE Std. 1149.1 BST Operation Control

Table 12-1 shows the boundary-scan register length for devices in Cyclone III family devices.

Table 12-1. Boundary-Scan Register Length for Cyclone III Family Devices

Family	Device	Boundary-Scan Register Length
Cyclone III	EP3C5	603
	EP3C10	603
	EP3C16	1,080
	EP3C25	732
	EP3C40	1,632
	EP3C55	1,164
	EP3C80	1,314
	EP3C120	1,620
Cyclone III LS	EP3CLS70	1,314
	EP3CLS100	1,314
	EP3CLS150	1,314
	EP3CLS200	1,314

Table 12-2 shows the IDCODE information for devices in Cyclone III family devices.

Table 12-2. Device IDCODE for Cyclone III Family Devices

Family	Device	IDCODE (32 Bits) <i>(Note 1)</i>			
		Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) <i>(2)</i>
Cyclone III	EP3C5	0000	0010 0000 1111 0001	000 0110 1110	1
	EP3C10	0000	0010 0000 1111 0001	000 0110 1110	1
	EP3C16	0000	0010 0000 1111 0010	000 0110 1110	1
	EP3C25	0000	0010 0000 1111 0011	000 0110 1110	1
	EP3C40	0000	0010 0000 1111 0100	000 0110 1110	1
	EP3C55	0000	0010 0000 1111 0101	000 0110 1110	1
	EP3C80	0000	0010 0000 1111 0110	000 0110 1110	1
	EP3C120	0000	0010 0000 1111 0111	000 0110 1110	1
Cyclone III LS	EP3CLS70	0000	0010 0111 0000 0001	000 0110 1110	1
	EP3CLS100	0000	0010 0111 0000 0000	000 0110 1110	1
	EP3CLS150	0000	0010 0111 0000 0011	000 0110 1110	1
	EP3CLS200	0000	0010 0111 0000 0010	000 0110 1110	1

Notes to Table 12-2:

- (1) The MSB is on the left.
- (2) The LSB of the IDCODE is always 1.

Cyclone III family devices support the IEEE Std. 1149.1 (JTAG) instructions as shown in Table 12-3.

Table 12-3. IEEE Std. 1149.1 (JTAG) Instructions Supported by Cyclone III Family Devices (Part 1 of 2)

JTAG Instruction	Instruction Code	Description
SAMPLE/PRELOAD	00 0000 0101	Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap® II embedded logic analyzer.
EXTEST (1)	00 0000 1111	Allows the external circuitry and board-level interconnects to be tested by forcing a test pattern at the output pins and capturing test results at the input pins.
BYPASS	11 1111 1111	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation.
USERCODE	00 0000 0111	Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO.
IDCODE	00 0000 0110	Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. IDCODE is the default instruction at power up and in TAP RESET state.
HIGHZ	00 0000 1011	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation, while tri-stating all of the I/O pins.
CLAMP	00 0000 1010	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary scan register.
ICR Instructions	—	Used when configuring Cyclone III family devices via the JTAG port with a USB-Blaster™ ByteBlaster™ II, MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File, or JBC File via an embedded processor.
PULSE_NCONFIG	00 0000 0001	Emulates pulsing the nCONFIG pin low to trigger reconfiguration even though the physical pin is unaffected.
CONFIG_IO (2)	00 0000 1101	Allows I/O reconfiguration through JTAG ports using the IOCSR for JTAG testing. This is executed after or during configurations. nSTATUS pin must go high before you can issue the CONFIG_IO instruction.
EN_ACTIVE_CLK (2)	01 1110 1110	Allows CLKUSR pin signal to replace the internal oscillator as the configuration clock source.
DIS_ACTIVE_CLK (2)	10 1110 1110	Allows you to revert the configuration clock source from CLKUSR pin signal set by EN_ACTIVE_CLK back to the internal oscillator.
ACTIVE_DISENGAGE (2)	10 1101 0000	Places the active configuration mode controllers into idle state prior to CONFIG_IO to configure the IOCSR or perform board level testing.
ACTIVE_ENGAGE (2)	10 1011 0000	This instruction might be used in AS and AP configuration schemes to re-engage the active controller.

Table 12-3. IEEE Std. 1149.1 (JTAG) Instructions Supported by Cyclone III Family Devices (Part 2 of 2)

JTAG Instruction	Instruction Code	Description
APFC_BOOT_ADDR (2), (3)	10 0111 0000	Places the 22-bit active boot address register between the TDI and TDO pins, allowing a new active boot address to be serially shifted into TDI and into the active parallel (AP) flash controller. In remote system upgrade, the PFC_BOOT_ADDR instruction sets the boot address for the factory configuration.
FACTORY (4)	10 1000 0001	Enables access to all other JTAG instructions (other than BYPASS, SAMPLE/PRELOAD and EXTEST instructions, which are supported upon power up). This instruction also clears the device configuration data and advanced encryption standard (AES) volatile key.
KEY_PROG_VOL (4)	01 1010 1101	Used to enter and store the security key into volatile registers. When this instruction is executed, TDI is connected to a 512-bit volatile key scan chain. TDO is not connected to the end of this scan chain.
KEY_CLR_VREG (4)	00 0010 1001	Clears the volatile verify register which signifies the validity of the volatile keys stored in the registers. You must clear the volatile verify register by issuing this command whenever you attempt to program a new volatile key. This instruction must be asserted for at least 10 TCK cycles.

Notes to Table 12-3:


- (1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.
- (2) For more information on how to use CONFIG_IO, EN_ACTIVE_CLK, DIS_ACTIVE_CLK, ACTIVE_DISENGAGE, ACTIVE_ENGAGE and APFC_BOOT_ADDR instructions for Cyclone III family devices, refer to the *Configuration, Design Security, and Remote System Upgrades in Cyclone III Devices* chapter of the *Cyclone III Device Handbook*.
- (3) APFC_BOOT_ADDR instruction is not supported in Cyclone III LS devices.
- (4) For Cyclone III LS devices only. For more information on how to program the security key into the volatile registers, refer to the *Configuration, Design Security, and Remote System Upgrades in Cyclone III Devices* chapter of the *Cyclone III Device Handbook*.

The IEEE Std. 1149.1 BST circuitry is enabled upon device power-up. You can perform BST on Cyclone III family devices before, after, and during configuration. Cyclone III family devices support the BYPASS, IDCODE and SAMPLE instructions during configuration without interrupting configuration. To send all other JTAG instructions, interrupt the configuration using the CONFIG_IO instruction except for active configuration schemes in which the ACTIVE_DISENGAGE instruction is used instead.

The CONFIG_IO instruction allows you to configure I/O buffers via the JTAG port, and when issued, interrupts configuration. This instruction allows you to perform board-level testing prior to configuring Cyclone III family devices. Alternatively, you can wait for the configuration device to complete configuration. After configuration is interrupted and JTAG BST is complete, you must reconfigure the part via JTAG (PULSE_NCONFIG instruction) or by pulsing nCONFIG low.



When you perform JTAG boundary-scan testing before configuration, the nCONFIG pin must be held low.

 For more information on the following topics, refer to [AN39: IEEE 1149.1 \(JTAG\) Boundary-Scan Testing in Altera Devices](#):

- TAP controller state-machine
- Timing requirements for IEEE Std. 1149.1 signals
- Instruction mode
- Mandatory JTAG instructions (SAMPLE/PRELOAD, EXTEST and BYPASS)
- Optional JTAG instructions (IDCODE, USERCODE, CLAMP and HIGHZ)


The following information is only applicable to Cyclone III LS devices:

- Only the three mandatory JTAG 1149.1 JTAG instructions (BYPASS, SAMPLE/PRELOAD, EXTEST) and the FACTORY private instruction are supported from the JTAG pins upon power up. The FACTORY instruction (instruction code: 10 1000 0001) must be issued before the device starts loading the core configuration data to enable access to all other JTAG instructions. This instruction also clears the device configuration data and AES volatile key.
- IDCODE instruction is not supported upon power-up, prior to issuing the FACTORY instruction. However, it is the default instruction when the TAP controller is in the reset state. Without loading any instructions, you can go to the Shift_DR state and shift out the JTAG Device ID.
- IDCODE, CONFIG_IO, ACTIVE_DISENGAGE, HIGHZ, CLAMP, USERCODE and PULSE_NCONFIG instructions are supported, provided that the FACTORY instruction is executed.

I/O Voltage Support in a JTAG Chain

A JTAG chain can contain several different devices. However, you must be cautious if the chain contains devices that have different V_{CCIO} levels. The output voltage level of the TDO pin must meet the specifications of the TDI pin it drives. For Cyclone III family devices, the TDO pin is powered by the V_{CCIO} power supply. Because the V_{CCIO} supply is 3.3 V, the TDO pin drives out 3.3 V.

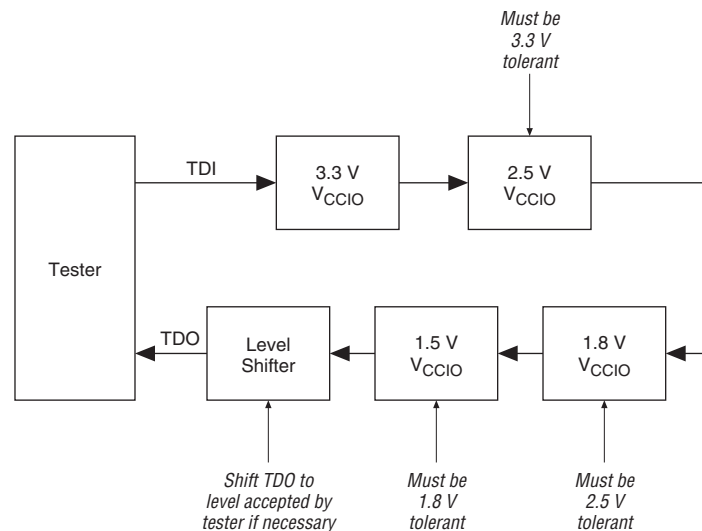
Devices can interface with each other although they might have different V_{CCIO} levels. For example, a device with a 3.3-V TDO pin can drive to a device with a 5.0-V TDI pin because 3.3 V meets the minimum TTL-level V_{IH} for the 5.0-V TDI pin. JTAG pins on Cyclone III family devices can support 2.5-V or 3.3-V input levels.

 For multiple devices in a JTAG chain with 3.0-V or 3.3-V I/O standard, you must connect a 25- Ω series resistor on a TDO pin driving a TDI pin.

You can also interface the TDI and TDO lines of the devices that have different V_{CCIO} levels by inserting a level shifter between the devices. If possible, the JTAG chain must be built in such a way that a device with a higher V_{CCIO} level drives to a device with an equal or lower V_{CCIO} level. This way, a level shifter may be required only to shift the TDO level to a level acceptable to the JTAG tester.

Figure 12-1 shows the JTAG chain of mixed voltages and how a level shifter is inserted in the chain.

Figure 12-1. JTAG Chain of Mixed Voltages



Guidelines for IEEE Std. 1149.1 BST

Use the following guidelines when performing BST with IEEE Std. 1149.1 devices:

- If the 10 bit checkerboard pattern (1010101010) does not shift out of the instruction register via the TDO pin during the first clock cycle of the SHIFT_IR state, the TAP controller did not reach the proper state. To solve this problem, try one of the following procedures:
 - Verify that the TAP controller has reached the SHIFT_IR state correctly. To advance the TAP controller to the SHIFT_IR state, return to the RESET state and send the code 01100 to the TMS pin.
 - Check the connections to the VCC, GND, JTAG, and dedicated configuration pins on the device.
- Perform a SAMPLE/PRELOAD test cycle prior to the first EXTEST test cycle to ensure that known data is present at the device pins when you enter the EXTEST mode. If the OEJ update register contains a 0, the data in the OUTJ update register is driven out. The state must be known and correct to avoid contention with other devices in the system.
- Do not perform EXTEST testing during ICR. This instruction is supported before or after ICR, but not during ICR. Use the CONFIG_IO instruction to interrupt configuration and then perform testing, or wait for configuration to complete.
- If testing is performed before configuration, hold the nCONFIG pin low.

- The following private instructions must not be used as they might render the device inoperable:
1000010000
1001000000
1011100000
You should take precautions not to invoke these instructions at any time.


Boundary-Scan Description Language Support

The boundary-scan description language (BSDL), a subset of VHDL, provides a syntax that allows you to describe the features of an IEEE Std. 1149.1 BST-capable device that can be tested. To download BSDL files for IEEE Std. 1149.1-compliant Cyclone III family devices, visit the [Altera Download Center](#).

-  BSDL files for IEEE std. 1149.1-compliant Cyclone III LS devices can also be generated using version 9.0 and later of the Quartus II software.

To perform BST on a configured device, a post configuration BSDL file that is customized to your design is required. Post configuration BSDL file generation with BSDL Customizer script (available on the [Altera Download Center](#)) is for Cyclone III devices only.

Use version 9.0 and later of the Quartus II software to create a post configuration BSDL file for Cyclone III LS devices.

-  For information on the procedures to generate the generic and post configuration BSDL files with Quartus II software, visit the [Altera Download Center](#).

Chapter Revision History

Table 12-4 shows the revision history for this chapter.

Table 12-4. Chapter Revision History

Date and Document Version	Changes Made	Summary of Changes
June 2009 v2.0	<ul style="list-style-type: none"> ■ Updated “Introduction” on page 12-1, “IEEE Std. 1149.1 BST Architecture” on page 12-1, “IEEE Std. 1149.1 BST Operation Control” on page 12-2, “Guidelines for IEEE Std. 1149.1 BST” on page 12-6, and “Boundary-Scan Description Language Support” on page 12-7 ■ Updated Table 12-1 on page 12-2, Table 12-2 on page 12-2, and Table 12-3 on page 12-3 	<ul style="list-style-type: none"> ■ Updated to include Cyclone III LS information
October 2008 v1.3	<ul style="list-style-type: none"> ■ Updated chapter to new template 	—
May 2008 v1.2	<ul style="list-style-type: none"> ■ Minor textual changes 	—

Table 12-4. Chapter Revision History

Date and Document Version	Changes Made	Summary of Changes
July 2007 v1.1	<ul style="list-style-type: none"> ■ Updated “IEEE Std.1149.1 Boundary-Scan Register” section ■ Updated IDCODE information and removed SignalTap II instructions in Table 12-4 ■ Updated “BST for Configured Devices” section ■ Added a guideline to “Guidelines for IEEE Std. 1149.1 Boundary-Scan Testing” section ■ Added chapter TOC and “Referenced Documents” section 	—
March 2007 v1.0	Initial release	—



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