

This chapter describes the high-speed differential I/O features and resources in the Cyclone III device family.

High-speed differential I/O standards have become popular in high-speed interfaces because of their significant advantages over single-ended I/O standards. The Altera® Cyclone® III device family (Cyclone III and Cyclone III LS devices) supports LVDS, BLVDS, reduced swing differential signaling (RSDS), mini-LVDS, and point-to-point differential signaling (PPDS).

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- “True Output Buffer Feature” on page 7-15
- “High-Speed I/O Timing” on page 7-16
- “Design Guidelines” on page 7-17
- “Software Overview” on page 7-18

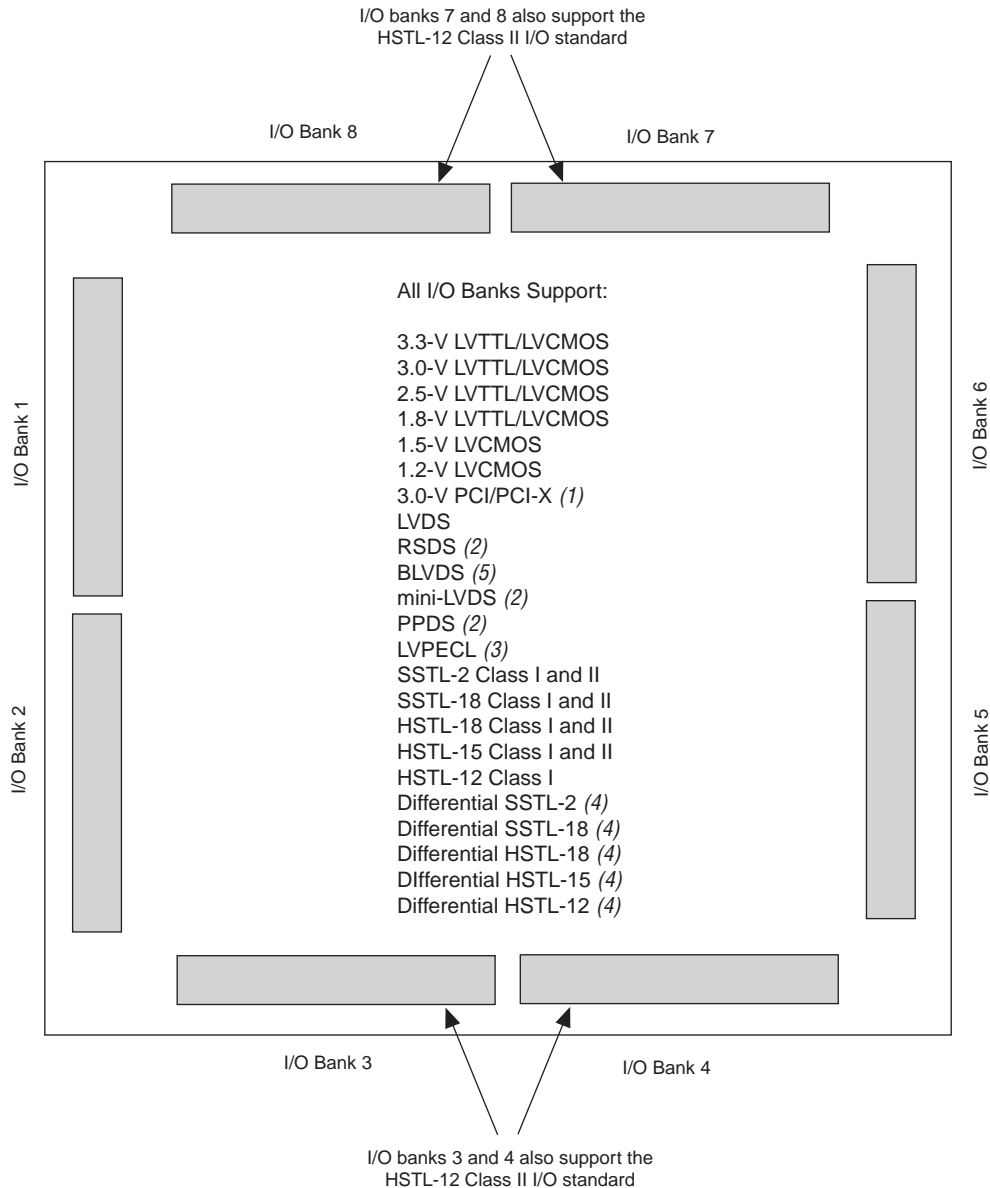
High-Speed I/O Interface

Cyclone III device family I/Os are separated into eight I/O banks, as shown in [Figure 7-1](#). Each bank has an independent power supply. True output drivers for LVDS, RSDS, mini-LVDS, and PPDS are on the left and right I/O banks. These I/O standards are also supported on the top and bottom I/O banks using external resistors. On the left and right I/O banks, some of the differential pin pairs (p and n pins) of the true output drivers are not located on adjacent pins. In these cases, a power pin is located between the p and n pins. These I/O standards are also supported on all I/O banks using two single-ended output with the second output programmed as inverted, and an external resistor network. True input buffers for these I/O standards are supported on all I/O banks.

 For more information about the location of Cyclone III device family true differential pins, refer to the [Pin-Out Files for Altera Devices](#) webpage on the Altera website.

Figure 7-1 shows the I/O banks of the Cyclone III device family.

Figure 7-1. Cyclone III Device Family I/O Banks



Notes to Figure 7-1:

- (1) The PCI-X I/O standard does not meet the IV curve requirement at the linear region.
- (2) The RSDS, mini-LVDS, and PPDS I/O standards are only supported on output pins. These I/O standards are not supported on input pins.
- (3) The LVPECL I/O standard is only supported on dedicated clock input pins. This I/O standard is not supported on output pins.
- (4) The differential SSTL-2, SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards are only supported on dedicated clock input pins and PLL output clock pins. PLL output clock pins do not support Class II interface type of differential SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards.
- (5) BLVDS output uses two single-ended outputs with the second output programmed as inverted. BLVDS input uses LVDS input buffer.

Table 7-1 lists which I/O bank supports these I/O standards in the Cyclone III device family.

Table 7-1. Differential I/O Standards Supported in Cyclone III Device Family I/O Banks

Differential I/O Standards	I/O Bank Location	External Resistor Network at Transmitter	Transmitter (TX)	Receiver (RX)
LVDS	1,2,5,6	Not Required	Yes	Yes
	All	Three Resistors		
RSDS	1,2,5,6	Not Required	Yes	Not Supported
	3, 4, 7, 8	Three Resistors		
	All	Single Resistor		
mini-LVDS	1,2,5,6	Not Required	Yes	Not Supported
	All	Three Resistors		
PPDS	1,2,5,6	Not Required	Yes	Not Supported
	All	Three Resistors		
BLVDS ⁽¹⁾	All	Single Resistor	Yes	Yes
LVPECL ⁽²⁾	All	NA	Not Supported	Yes
Differential SSTL-2 ⁽³⁾	All	NA	Yes	Yes
Differential SSTL-18 ⁽³⁾	All	NA	Yes	Yes
Differential HSTL-18 ⁽³⁾	All	NA	Yes	Yes
Differential HSTL-15 ⁽³⁾	All	NA	Yes	Yes
Differential HSTL-12 ⁽³⁾	All	NA	Yes	Yes

Notes to Table 7-1:

- (1) Transmitter and Receiver F_{MAX} depend on system topology and performance requirement.
- (2) The LVPECL I/O standard is only supported on dedicated clock input pins.
- (3) The differential SSTL-2, SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards are only supported on clock input pins and PLL output clock pins. PLL output clock pins do not support Class II interface type of differential SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards.

You can use I/O pins and internal logic to implement a high-speed differential interface in the Cyclone III device family. The Cyclone III device family does not contain dedicated serialization or deserialization circuitry. Therefore, shift registers, internal phase-locked loops (PLLs), and I/O cells are used to perform serial-to-parallel conversions on incoming data and parallel-to-serial conversion on outgoing data. The differential interface data serializers and deserializers (SERDES) are automatically constructed in the core logic elements (LEs) with the Quartus® II software ALTLVDS megafunction.

Table 7-2 lists the total number of supported row and column differential channels in the Cyclone III device family.

Table 7-2. Cyclone III Device Family Differential Channels (Part 1 of 2)

Cyclone III Device Family	Device	Package	Number of Differential Channels ^{(1), (2)}			
			User I/O	Clock Input	Clock Output	Total
Cyclone III Devices	EP3C5	E144	16	4	2	22
		F256	62	4	2	68
		M164	22	4	2	28
		U256	62	4	2	68
	EP3C10	E144	16	4	2	22
		F256	62	4	2	68
		M164	22	4	2	28
		U256	62	4	2	68
	EP3C16	E144	7	8	4	19
		E240	35	8	4	47
		F256	43	8	4	55
		F484	128	8	4	140
		M164	11	8	4	23
		U256	43	8	4	55
	EP3C25	U484	128	8	4	140
		E144	6	8	4	18
		E240	31	8	4	43
		F256	42	8	4	54
		F324	71	8	4	83
	EP3C40	U256	42	8	4	54
		E240	14	8	4	26
		F324	49	8	4	61
		F484	115	8	4	127
		F780	215	8	4	227
	EP3C55	U484	115	8	4	127
		F484	123	8	4	135
		F780	151	8	4	163
	EP3C80	U484	123	8	4	135
		F484	101	8	4	113
		F780	169	8	4	181
	EP3C120	U484	101	8	4	113
		F484	94	8	4	106
		F780	221	8	4	233

Table 7-2. Cyclone III Device Family Differential Channels (Part 2 of 2)

Cyclone III Device Family	Device	Package	Number of Differential Channels ^{(1), (2)}			
			User I/O	Clock Input	Clock Output	Total
Cyclone III LS Devices	EP3CLS70	U484	101	8	4	113
		F484	101	8	4	113
		F780	169	8	4	181
	EP3CLS100	U484	101	8	4	113
		F484	101	8	4	113
		F780	169	8	4	181
	EP3CLS150	F484	75	8	4	87
		F780	169	8	4	181
	EP3CLS200	F484	75	8	4	87
		F780	169	8	4	181

Notes to Table 7-2:

- (1) User I/O pins are used as inputs or outputs; clock input pins are used as inputs only; clock output pins are used as output only.
- (2) For differential pad placement guidelines, refer to the *I/O Features in the Cyclone III Device Family* chapter.

Table 7-3 lists the numbers of differential channels that can be migrated in Cyclone III devices.

Table 7-3. Cyclone III Devices Migratable Differential Channels ⁽¹⁾ (Part 1 of 2)

Package Type	Migration Between Devices	Migratable Channels		
		User I/O	CLK	Total
E144	EP3C5 and EP3C10	16	4	20
	EP3C5 and EP3C16	5	4	9
	EP3C5 and EP3C25	6	4	10
	EP3C10 and EP3C16	5	4	9
	EP3C10 and EP3C25	6	4	10
	EP3C16 and EP3C25	5	8	13
M164	EP3C5 and EP3C10	22	4	26
	EP3C5 and EP3C16	11	4	15
	EP3C10 and EP3C16	19	4	14
Q240	EP3C16 and EP3C25	23	8	31
	EP3C16 and EP3C40	11	8	19
	EP3C25 and EP3C40	12	8	20
F256	EP3C5 and EP3C10	62	4	66
	EP3C5 and EP3C16	39	4	43
	EP3C5 and EP3C25	40	4	44
	EP3C10 and EP3C16	39	4	43
	EP3C10 and EP3C25	40	4	44
	EP3C16 and EP3C25	33	8	41

Table 7-3. Cyclone III Devices Migratable Differential Channels ⁽¹⁾ (Part 2 of 2)

Package Type	Migration Between Devices	Migratable Channels		
		User I/O	CLK	Total
U256	EP3C5 and EP3C10	62	4	66
	EP3C5 and EP3C16	39	4	43
	EP3C5 and EP3C25	40	4	44
	EP3C10 and EP3C16	39	4	43
	EP3C10 and EP3C25	40	4	44
	EP3C16 and EP3C25	33	8	41
F324	EP3C25 and EP3C40	47	8	55
F484	EP3C16 and EP3C40	102	8	110
	EP3C16 and EP3C55	98	8	106
	EP3C16 and EP3C80	79	8	87
	EP3C16 and EP3C120	72	8	80
	EP3C40 and EP3C55	102	8	110
	EP3C40 and EP3C80	84	8	92
	EP3C40 and EP3C120	74	8	82
	EP3C55 and EP3C80	98	8	106
	EP3C55 and EP3C120	85	8	93
	EP3C80 and EP3C120	88	8	96
U484	EP3C16 and EP3C40	102	8	110
	EP3C16 and EP3C55	98	8	106
	EP3C16 and EP3C80	79	8	87
	EP3C40 and EP3C55	102	8	110
	EP3C40 and EP3C80	84	8	92
	EP3C55 and EP3C80	98	8	106
F780	EP3C40 and EP3C55	46	8	54
	EP3C40 and EP3C80	51	8	59
	EP3C40 and EP3C120	54	8	62
	EP3C55 and EP3C80	144	8	152
	EP3C55 and EP3C120	142	8	150
	EP3C80 and EP3C120	160	8	168

Note to Table 7-3:

- (1) The migratable differential channels for Cyclone III devices are not directly migratable to Cyclone III LS devices and vice versa.

Table 7-4 lists the numbers of differential channels that can be migrated in Cyclone III LS devices.

Table 7-4. Cyclone III LS Devices Migratable Differential Channels ⁽¹⁾

Package Type	Migration between Devices	Migratable Channels			
		User I/O	Clock Input	Clock Output	Total
U484	EP3CLS70 and EP3CLS100	101	8	4	113
F484	EP3CLS70 and EP3CLS100	101	8	4	113
	EP3CLS70 and EP3CLS150	71	8	4	83
	EP3CLS70 and EP3CLS200	71	8	4	83
	EP3CLS100 and EP3CLS150	71	8	4	83
	EP3CLS100 and EP3CLS200	71	8	4	83
	EP3CLS150 and EP3CLS200	75	8	4	87
F780	EP3CLS70 and EP3CLS100	169	8	4	181
	EP3CLS70 and EP3CLS150	169	8	4	181
	EP3CLS70 and EP3CLS200	169	8	4	181
	EP3CLS100 and EP3CLS150	169	8	4	181
	EP3CLS100 and EP3CLS200	169	8	4	181
	EP3CLS150 and EP3CLS200	169	8	4	181

Note to Table 7-4:

- (1) The migratable differential channels for Cyclone III devices are not directly migratable to Cyclone III LS devices and vice versa.

High-Speed I/O Standards Support

This section provides information about the high-speed I/O standards supported in the Cyclone III device family.

LVDS I/O Standard Support in the Cyclone III Device Family

The LVDS I/O standard is a high-speed, low-voltage swing, low power, and general purpose I/O interface standard. The Cyclone III device family meets the ANSI/TIA/EIA-644 standard with the following exceptions:

- The maximum differential output voltage (V_{OD}) is increased to 600 mV. The maximum V_{OD} for ANSI specification is 450 mV.
- The input voltage range is reduced to the range of 1.0 V to 1.6 V, 0.5 V to 1.85 V, or 0 V to 1.8 V based on different frequency ranges. The ANSI/TIA/EIA-644 specification supports an input voltage range of 0 V to 2.4 V.



For more information about the LVDS I/O standard electrical specifications in the Cyclone III device family, refer to the *Cyclone III Device Data Sheet* and *Cyclone III LS Device Data Sheet* chapters.

Designing with LVDS

Cyclone III device family I/O banks support LVDS I/O standard. The left and right I/O banks support true LVDS transmitters. On the top and bottom I/O banks, the emulated LVDS transmitters are supported using two single-ended output buffers with external resistors. One of the single-ended output buffers is programmed to have opposite polarity. The LVDS receiver requires an external 100- Ω termination resistor between the two signals at the input buffer.

Figure 7-2 shows a point-to-point LVDS interface using Cyclone III device family true LVDS output and input buffers.

Figure 7-2. Cyclone III Device Family LVDS Interface with True Output Buffer on the Left and Right I/O Banks

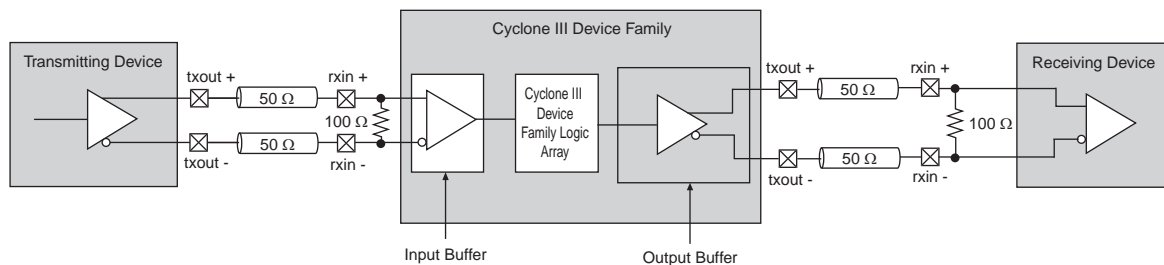
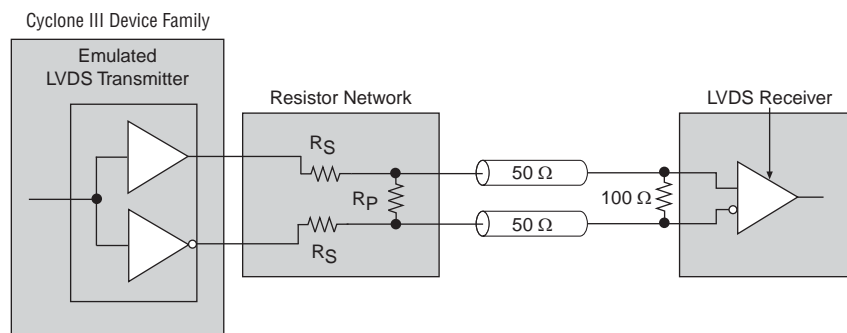


Figure 7-3 shows a point-to-point LVDS interface with Cyclone III device family LVDS using two single-ended output buffers and external resistors.

Figure 7-3. LVDS Interface with External Resistor Network on the Top and Bottom I/O Banks ⁽¹⁾



Note to Figure 7-3:

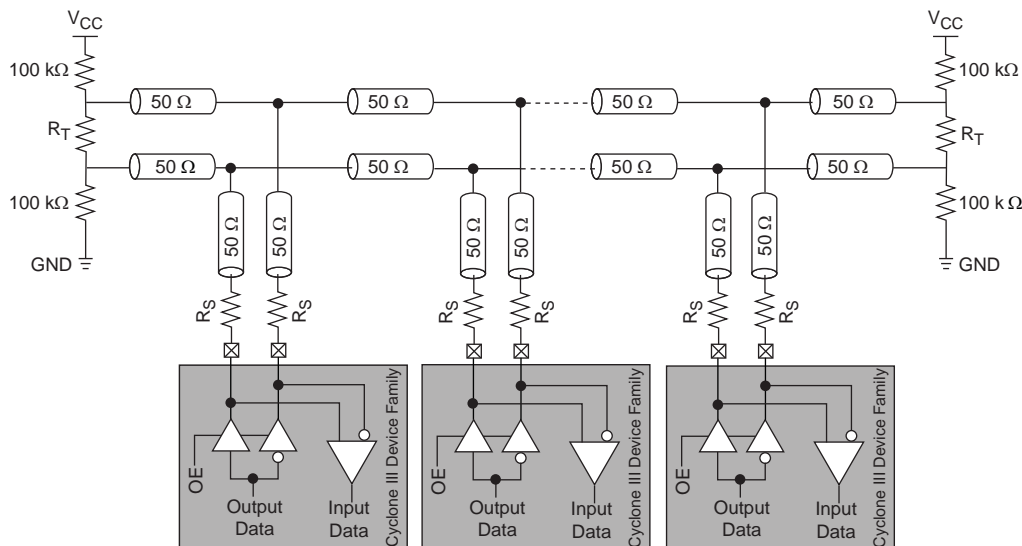
(1) $R_S = 120 \Omega$; $R_P = 170 \Omega$

BLVDS I/O Standard Support in the Cyclone III Device Family


The BLVDS I/O standard is a high-speed differential data transmission technology that extends the benefits of standard point-to-point LVDS to multipoint configuration that supports bidirectional half-duplex communication. BLVDS differs from standard LVDS by providing a higher drive to achieve similar signal swings at the receiver while loaded with two terminations at both ends of the bus.


Figure 7-4 shows a typical BLVDS topology with multiple transmitter and receiver pairs.

Figure 7-4. BLVDS Topology with Cyclone III Device Family Transmitters and Receivers



The BLVDS I/O standard is supported on all I/O banks of the Cyclone III device family. The BLVDS transmitter uses two single-ended output buffers with the second output buffer programmed as inverted, while the BLVDS receiver uses a true LVDS input buffer. The transmitter and receiver share the same pins. An output-enabled (OE) signal is required to tristate the output buffers when the LVDS input buffer receives a signal.


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For more information about BLVDS I/O features and electrical specifications, refer to the *I/O Features in the Cyclone III Device Family* chapter in volume 1 of the *Cyclone III Device Handbook* and the *Cyclone III Device Data Sheet* and *Cyclone III LS Device Data Sheet* chapters.
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For more information and design examples about implementing the BLVDS interfaces in the Cyclone III device family, refer to *AN 522: Implementing Bus LVDS Interface in Supported Altera Device Families*.

Designing with BLVDS

The BLVDS bidirectional communication requires termination at both ends of the bus in BLVDS. The termination resistor (R_T) must match the bus differential impedance, which in turn depends on the loading on the bus. Increasing the load decreases the bus differential impedance. With termination at both ends of the bus, termination is not required between the two signals at the input buffer. A single series resistor (R_S) is required at the output buffer to match the output buffer impedance to the transmission line impedance. However, this series resistor affects the voltage swing at the input buffer. The maximum data rate achievable depends on many factors.

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Altera recommends that you perform simulation using the IBIS model while considering factors such as bus loading, termination values, and output and input buffer location on the bus to ensure that the required performance is achieved.

RSDS, Mini-LVDS, and PPDS I/O Standard Support in the Cyclone III Device Family

The RSDS, mini-LVDS, and PPDS I/O standards are used in chip-to-chip applications between the timing controller and the column drivers on the display panels such as LCD monitor panels and LCD televisions. The Cyclone III device family meets the National Semiconductor Corporation RSDS Interface Specification, Texas Instruments mini-LVDS Interface Specification, and National Semiconductor Corporation PPDS Interface Specification to support RSDS, mini-LVDS and PPDS output standards, respectively.

- For more information about the Cyclone III device family RSDS, mini-LVDS, and PPDS output electrical specifications, refer to the *Cyclone III Device Data Sheet* and *Cyclone III LS Device Data Sheet* chapters.
- For more information about the RSDS I/O standard, refer to the RSDS specification from the National Semiconductor website (www.national.com).

Designing with RSDS, Mini-LVDS, and PPDS

Cyclone III device family I/O banks support RSDS, mini-LVDS, and PPDS output standards. The left and right I/O banks support true RSDS, mini-LVDS, and PPDS transmitters. On the top and bottom I/O banks, RSDS, mini-LVDS, and PPDS transmitters are supported using two single-ended output buffers with external resistors. The two-single ended output buffers are programmed to have opposite polarity.

Figure 7-5 shows a RSDS, mini-LVDS, or PPDS interface with a true output buffer.

Figure 7-5. Cyclone III Device Family RSDS, Mini-LVDS, or PPDS Interface with True Output Buffer on the Left and Right I/O Banks

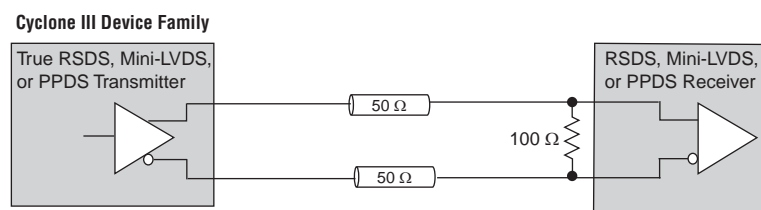
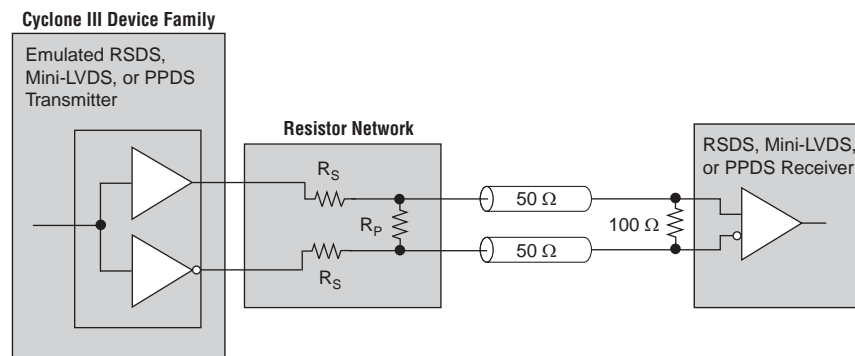


Figure 7-6 shows a RSDS, mini-LVDS, or PPDS interface with two singled-ended output buffers and external resistors.

Figure 7-6. RSDS, Mini-LVDS, or PPDS Interface with External Resistor Network on the Top and Bottom I/O Banks (1)



Note to Figure 7-6:

(1) $R_S = 120 \Omega$; $R_P = 170 \Omega$

A resistor network is required to attenuate the output voltage swing to meet RSDS, mini-LVDS, and PPDS specifications when using emulated transmitters. You can modify the resistor network values to reduce power or improve the noise margin.

The resistor values chosen must satisfy Equation 7-1.

Equation 7-1.

$$\frac{R_S \times \frac{R_P}{2}}{R_S + \frac{R_P}{2}} = 50 \Omega$$

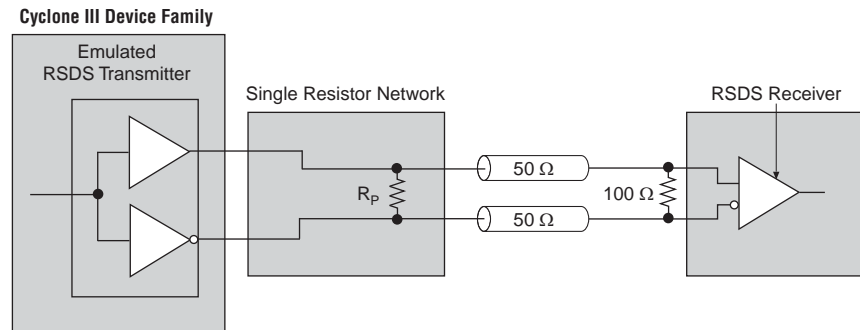


Altera recommends that you perform simulations using Cyclone III device family IBIS models to validate that custom resistor values meet the RSDS, mini-LVDS, or PPDS requirements.

You can use a single external resistor instead of using three resistors in the resistor network for an RSDS interface, as shown in Figure 7-7. The external single-resistor solution reduces the external resistor count while still achieving the required signaling level for RSDS. However, the performance of the single-resistor solution is lower than the performance with the three-resistor network.

Figure 7-7 shows the RSDS interface with a single resistor network on the top and bottom I/O banks.

Figure 7-7. RSDS Interface with Single Resistor Network on the Top and Bottom I/O Banks



Note to Figure 7-7:

(1) $R_p = 100 \Omega$

LVPECL I/O Support in the Cyclone III Device Family

The LVPECL I/O standard is a differential interface standard that requires a 2.5-V V_{CCIO} . This standard is used in applications involving video graphics, telecommunications, data communications, and clock distribution. The Cyclone III device family supports the LVPECL input standard at the dedicated clock input pins only. The LVPECL receiver requires an external 100- Ω termination resistor between the two signals at the input buffer.

For more information about the LVPECL I/O standard electrical specification, refer to the *Cyclone III Device Data Sheet* and *Cyclone III LS Device Data Sheet* chapters.

AC coupling is required when the LVPECL common mode voltage of the output buffer is higher than the Cyclone III device family LVPECL input common mode voltage.

Figure 7-8 shows the AC-coupled termination scheme. The 50- Ω resistors used at the receiver are external to the device. DC-coupled LVPECL is supported if the LVPECL output common mode voltage is in the Cyclone III device family LVPECL input buffer specification (Figure 7-9).

Figure 7-8. LVPECL AC-Coupled Termination

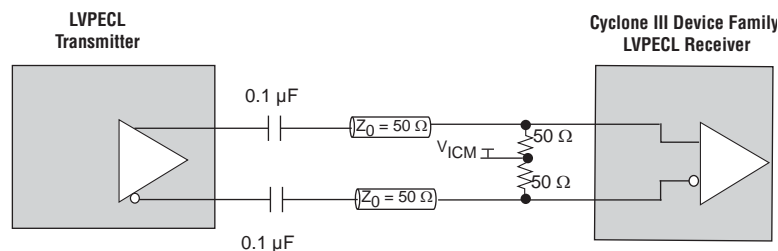
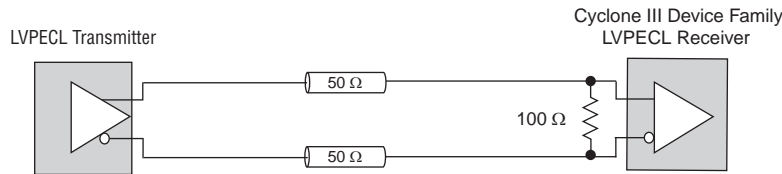


Figure 7-9 shows the LVPECL DC-coupled termination.

Figure 7-9. LVPECL DC-Coupled Termination



Differential SSTL I/O Standard Support in the Cyclone III Device Family

The differential SSTL I/O standard is a memory-bus standard used for applications such as high-speed DDR SDRAM interfaces. The Cyclone III device family supports differential SSTL-2 and SSTL-18 I/O standards. The differential SSTL output standard is only supported at PLL#_CLKOUT pins using two single-ended SSTL output buffers (PLL#_CLKOUTp and PLL#_CLKOUTn), with the second output programmed to have opposite polarity. The differential SSTL input standard is supported on the GCLK pins only, treating differential inputs as two single-ended SSTL and only decoding one of them.

The differential SSTL I/O standard requires two differential inputs with an external reference voltage (V_{REF}) as well as an external termination voltage (V_{TT}) of $0.5 \times V_{CCIO}$ to which termination resistors are connected.


 For more information about the differential SSTL electrical specifications, refer to the *I/O Features in the Cyclone III Device Family* chapter and the *Cyclone III Device Data Sheet* and *Cyclone III LS Device Data Sheet* chapters.

Figure 7-10 shows the differential SSTL Class I interface.

Figure 7-10. Differential SSTL Class I Interface

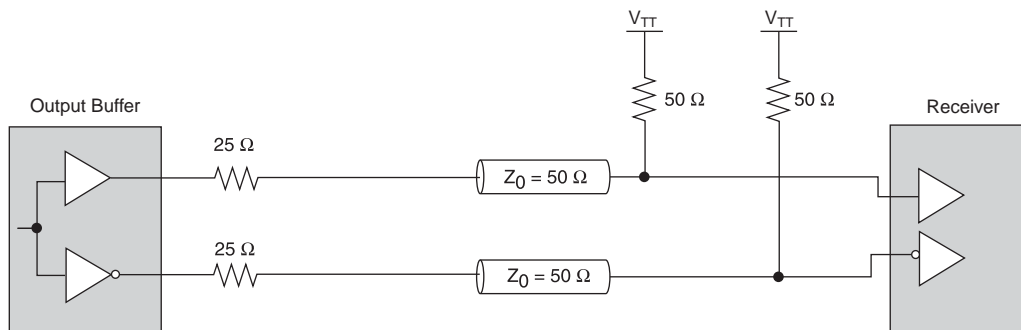
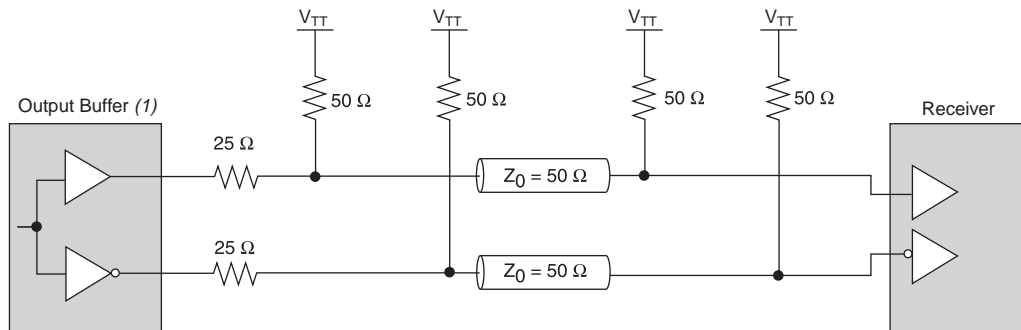


Figure 7-11 shows the differential SSTL Class II interface.

Figure 7-11. Differential SSTL Class II Interface



Note to Figure 7-11:

(1) PLL output clock pins do not support differential SSTL-18 Class II I/O standard.

Differential HSTL I/O Standard Support in the Cyclone III Device Family

The differential HSTL I/O standard is used for the applications designed to operate in 0 V to 1.2 V, 0 V to 1.5 V, or 0 V to 1.8 V HSTL logic switching range. The Cyclone III device family supports differential HSTL-18, HSTL-15, and HSTL-12 I/O standards. The differential HSTL input standard is available on GCLK pins only, treating the differential inputs as two single-ended HSTL and only decoding one of them. The differential HSTL output standard is only supported at the PLL#_CLKOUT pins using two single-ended HSTL output buffers (PLL#_CLKOUT p and PLL#_CLKOUT n), with the second output programmed to have opposite polarity.

The differential HSTL I/O standard requires two differential inputs with an external reference voltage (V_{REF}), as well as an external termination voltage (V_{TT}) of $0.5 \times V_{CCIO}$ to which termination resistors are connected.


 For more information about the differential HSTL signaling characteristics, refer to the *I/O Features in the Cyclone III Device Family*, *Cyclone III Device Data Sheet*, and *Cyclone III LS Device Data Sheet* chapters.

Figure 7-12 shows the differential HSTL Class I interface.

Figure 7-12. Differential HSTL Class I Interface

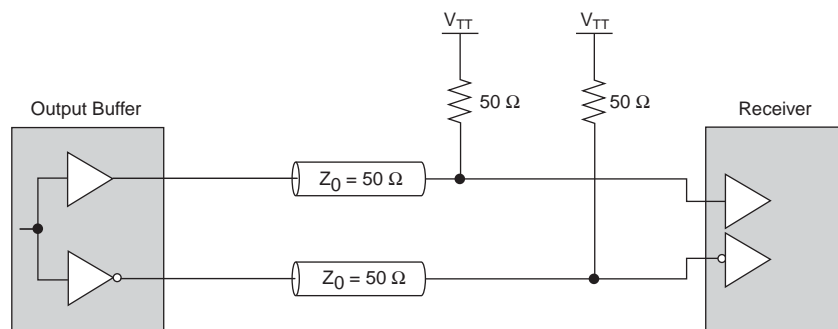
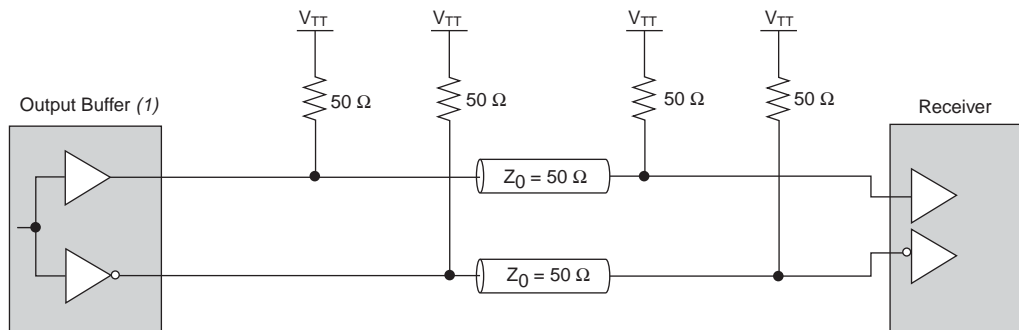


Figure 7-13 shows the differential HSTL Class II interface.

Figure 7-13. Differential HSTL Class II Interface



Note to Figure 7-13:

(1) PLL output clock pins do not support differential HSTL Class II I/O standard.

True Output Buffer Feature

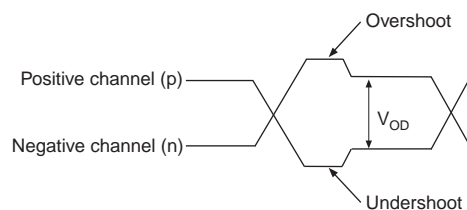
Cyclone III device family true differential transmitters offer programmable pre-emphasis—you can choose to turn it on or off. The default setting is on.

Programmable Pre-Emphasis

The programmable pre-emphasis boosts the high frequencies of the output signal to compensate the frequency-dependent attenuation of the transmission line to maximize the data eye opening at the far-end receiver. Without pre-emphasis, the output current is limited by the V_{OD} specification and the output impedance of the transmitter. At high frequency, the slew rate may not be fast enough to reach full V_{OD} before the next edge; this may lead to pattern dependent jitter. With pre-emphasis, the output current is momentarily boosted during switching to increase the output slew rate. The overshoot produced by this extra switching current is different from the overshoot caused by signal reflection. This overshoot happens only during switching, and does not produce ringing.

Figure 7-14 shows the differential output signal with pre-emphasis.

Figure 7-14. The Output Signal with Pre-Emphasis



High-Speed I/O Timing

This section discusses the timing budget, waveforms, and specifications for source-synchronous signaling in the Cyclone III device family. Timing for source-synchronous signaling is based on skew between the data and clock signals.

High-speed differential data transmission requires timing parameters provided by IC vendors and requires you to consider the board skew, cable skew, and clock jitter. This section provides information about high-speed I/O standards timing parameters in the Cyclone III device family.

Table 7-5 lists the parameters of the timing diagram as shown in Figure 7-15.

Table 7-5. High-Speed I/O Timing Definitions

Parameter	Symbol	Description
Transmitter channel-to-channel skew ⁽¹⁾	TCCS	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window	SW	The period of time during which the data must be valid in order for you to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window. $T_{SW} = T_{SU} + T_{hd} + \text{PLL jitter}$.
Receiver input skew margin	RSKM	RSKM is defined by the total margin left after accounting for the sampling window and TCCS. The RSKM equation is: $RSKM = \frac{(TUI - SW - TCCS)}{2}$
Input jitter tolerance (peak-to-peak)	—	Allowed input jitter on the input clock to the PLL that is tolerable while maintaining PLL lock.
Output jitter (peak-to-peak)	—	Peak-to-peak output jitter from the PLL.

Note to Table 7-5:

- (1) The TCCS specification applies to the entire bank of differential I/O as long as the SERDES logic is placed in the logic array block (LAB) adjacent to the output pins.

Figure 7-15. High-Speed I/O Timing Diagram

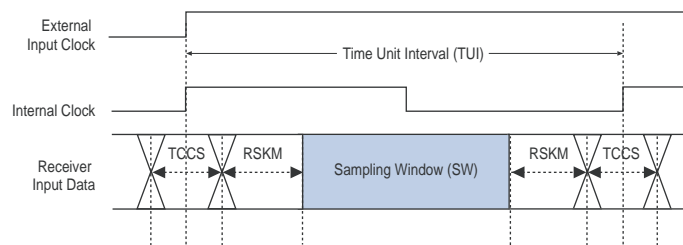
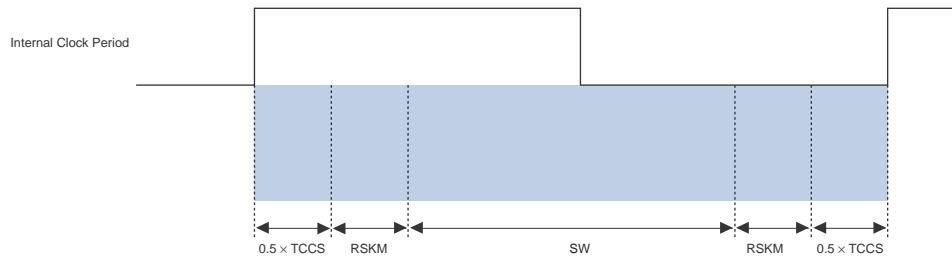


Figure 7-16 shows the Cyclone III device family high-speed I/O timing budget.

Figure 7-16. Cyclone III Device Family High-Speed I/O Timing Budget (1)



Note to Figure 7-16:

(1) The equation for the high-speed I/O timing budget is:

$$\text{period} = 0.5 \times TCCS + RSKM + SW + RSKM + 0.5 \times TCCS$$

For more information, refer to the *Cyclone III Device Data Sheet* and *Cyclone III LS Device Data Sheet* chapters in volume 2 of the *Cyclone III Device Handbook*.

Design Guidelines

This section provides guidelines for designing with the Cyclone III device family.

Differential Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply, you must observe some restrictions on the placement of single-ended I/O pins in relation to differential pads.

Altera recommends that you create a Quartus II design, enter your device I/O assignments, and compile your design to validate your pin placement. The Quartus II software checks your pin connections with respect to the I/O assignment and placement rules to ensure proper device operation.

For more information about how the Quartus II software checks I/O restrictions, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

Board Design Considerations

This section explains how to achieve the optimal performance from the Cyclone III device family I/O interface and ensure first-time success in implementing a functional design with optimal signal quality. You must consider the critical issues of controlled impedance of traces and connectors, differential routing, and termination techniques to get the best performance from the Cyclone III device family.

Use the following general guidelines for improved signal quality:


- Base board designs on controlled differential impedance. Calculate and compare all parameters, such as trace width, trace thickness, and the distance between two differential traces.
- Maintain equal distance between traces in differential I/O standard pairs as much as possible. Routing the pair of traces close to each other maximizes the common-mode rejection ratio (CMRR).


- Longer traces have more inductance and capacitance. These traces must be as short as possible to limit signal integrity issues.
- Place termination resistors as close to receiver input pins as possible.
- Use surface mount components.
- Avoid 90° corners on board traces.
- Use high-performance connectors.
- Design backplane and card traces so that trace impedance matches the impedance of the connector and termination.
- Keep an equal number of vias for both signal traces.
- Create equal trace lengths to avoid skew between signals. Unequal trace lengths result in misplaced crossing points and decrease system margins as the transmitter-channel-to-channel skew (TCCS) value increases.
- Limit vias because they cause discontinuities.
- Keep switching transistor-to-transistor logic (TTL) signals away from differential signals to avoid possible noise coupling.
- Do not route TTL clock signals to areas under or above the differential signals.
- Analyze system-level signals.

 For more information about PCB layout guidelines, refer to the *High-Speed Board Layout Guidelines* and *Guidelines for Designing High-Speed FPGA PCBs* application notes.

Software Overview

Cyclone III device family high-speed I/O system interfaces are created in core logic by a Quartus II software megafunction because they do not have a dedicated circuit for the SERDES. The Cyclone III device family uses the I/O registers and LE registers to improve the timing performance and support the SERDES. Altera Quartus II software allows you to design your high-speed interfaces using the ALTLVDS megafunction. This megafunction implements either a high-speed deserializer receiver or a high-speed serializer transmitter. There is a list of parameters in the ALTLVDS megafunction that you can set to customize your SERDES based on your design requirements. The megafunction is optimized to use Cyclone III device family resources to create high-speed I/O interfaces in the most effective manner.

 When you are using the Cyclone III device family with the ALTLVDS megafunction, the interface always sends the MSB of your parallel data first.

 For more information about designing your high-speed I/O systems interfaces using the ALTLVDS megafunction, refer to the *LVDS SERDES Transmitter/Receiver (ALTLVDS_TX and ALTLVDS_RX) Megafunction User Guide* and the *Quartus II Handbook*.

Document Revision History

Table 7-6 lists the revision history for this document.

Table 7-6. Document Revision History (Part 1 of 2)

Date	Version	Changes
December 2011	4.0	<ul style="list-style-type: none"> ■ Updated Table 7-2. ■ Updated “Differential SSTL I/O Standard Support in the Cyclone III Device Family” on page 7-13, “Differential HSTL I/O Standard Support in the Cyclone III Device Family” on page 7-14, and “Differential Pad Placement Guidelines” on page 7-17. ■ Updated hyperlinks. ■ Minor text edits.
December 2009	3.2	Minor changes to the text.
July 2009	3.1	Made minor correction to the part number.
June 2009	3.0	<p>Updated to include Cyclone III LS information</p> <ul style="list-style-type: none"> ■ Updated chapter part number. ■ Updated “Introduction” on page 7-1, “High-Speed I/O Interface” on page 7-1, “High-Speed I/O Standards Support” on page 7-7, “LVDS I/O Standard Support in Cyclone III Family Devices” on page 7-7, “Designing with LVDS” on page 7-8, “BLVDS I/O Standard Support in Cyclone III Family Devices” on page 7-8, “RSDS, Mini-LVDS, and PPDS I/O Standard Support in Cyclone III Family Devices” on page 7-10, “LVPECL I/O Support in Cyclone III Family Devices” on page 7-12, “Differential SSTL I/O Standard Support in Cyclone III Family Devices” on page 7-13, and “Differential HSTL I/O Standard Support in Cyclone III Family Devices” on page 7-14. ■ Updated Figure 7-1 on page 7-2, Figure 7-4 on page 7-9, and Figure 7-5 on page 7-10. ■ Updated Table 7-1 on page 7-3, Table 7-2 on page 7-4, Table 7-3 on page 7-5, and Table 7-4 on page 7-7.
October 2008	1.3	<ul style="list-style-type: none"> ■ Updated Table 7-2. ■ Updated Table 7-1. ■ Updated “BLVDS I/O Standard Support in Cyclone III Devices”. ■ Updated “Software Overview”. ■ Removed registered trademark symbols for RSDS and PPDS. ■ Removed any mention of “RSDS and PPDS are registered trademarks of National Semiconductor” in this chapter. ■ Updated chapter to new template.

Table 7-6. Document Revision History (Part 2 of 2)

Date	Version	Changes
May 2008	1.2	Changes include addition of BLVD information <ul style="list-style-type: none"> ■ Updated “Introduction” section with BLVDS information. ■ Updated Figure 7-1 with BLVDS information and added Note 5. ■ Updated Table 7-1 and added BLVDS information. ■ Updated “Cyclone III High-Speed I/O Banks” section with BLVDS information. ■ Updated Table 7-2 and 7-6. ■ Added new section “BLVDS I/O Standard Support in Cyclone III Devices”. ■ Updated Note 4 to Figure 7-4. ■ Updated Note 1 to Figure 7-10. ■ Updated Note 1 to Figure 7-11. ■ Updated Note 1 to Figure 7-14. ■ Updated “Mini-LVDS I/O Standard Support in Cyclone III Devices” section. ■ Updated Note 1 to Figure 7-17. ■ Updated “LVPECL I/O Support in Cyclone III Devices” section. ■ Added new Figure 7-18.
July 2007	1.1	<ul style="list-style-type: none"> ■ Added note that PLL output clock pins do not support Class II type of selected differential I/O standards. ■ Added Table 8-3 that lists the number of differential channels which are migratable across densities and packages. ■ Updated (<i>Note 4</i>) to Figure 7-1. ■ Updated (<i>Note 3</i>) to Table 7-1. ■ Added new Table 7-3. ■ Added (<i>Note 1</i>) to Figure 7-21. ■ Added (<i>Note 1</i>) to Figure 7-23. ■ Added chapter TOC and “Referenced Documents” section.
March 2007	1.0	Initial release.