

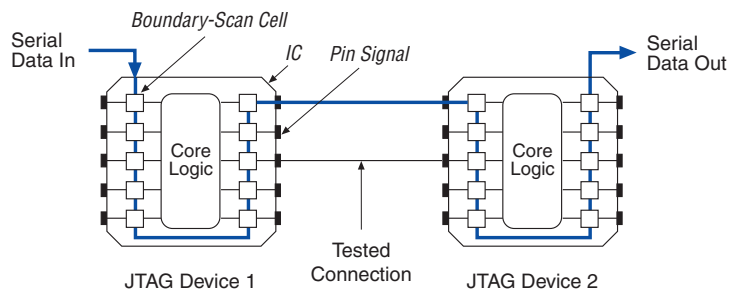
Introduction

As printed circuit boards (PCBs) become more complex, the need for thorough testing becomes increasingly important. Advances in surface-mount packaging and PCB manufacturing have resulted in smaller boards, making traditional test methods (e.g., external test probes and “bed-of-nails” test fixtures) harder to implement. As a result, cost savings from PCB space reductions are sometimes offset by cost increases in traditional testing methods.

In the 1980s, the Joint Test Action Group (JTAG) developed a specification for boundary-scan testing that was later standardized as the IEEE Std. 1149.1 specification. This boundary-scan test (BST) architecture offers the capability to efficiently test components on PCBs with tight lead spacing.

This BST architecture tests pin connections without using physical test probes and captures functional data while a device is operating normally. Boundary-scan cells in a device force signals onto pins or capture data from pin or logic array signals. Forced test data is serially shifted into the boundary-scan cells. Captured data is serially shifted out and externally compared with expected results. [Figure 14-1](#) shows the concept of boundary-scan testing.

Figure 14-1. IEEE Std. 1149.1 Boundary-Scan Testing



This chapter discusses how to use the IEEE Std. 1149.1 BST circuitry in Cyclone™ II devices, including:

- IEEE Std. 1149.1 BST architecture
- IEEE Std. 1149.1 boundary-scan register
- IEEE Std. 1149.1 BST operation control
- I/O voltage support in JTAG chain
- Using IEEE Std. 1149.1 BST circuitry
- Disabling IEEE Std. 1149.1 BST circuitry
- Guidelines for IEEE Std. 1149.1 boundary-scan testing
- Boundary-Scan Description Language (BSDL) support

In addition to BST, you can use the IEEE Std. 1149.1 controller for Cyclone II device in-circuit reconfiguration (ICR). However, this chapter only discusses the BST feature of the IEEE Std. 1149.1 circuitry.



For information on configuring Cyclone II devices via the IEEE Std. 1149.1 circuitry, see the *Configuring Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook*.

IEEE Std. 1149.1 BST Architecture

A Cyclone II device operating in IEEE Std. 1149.1 BST mode uses four required pins, TDI, TDO, TMS and TCK. The optional TRST pin is not available in Cyclone II devices. TDI and TMS pins have weak internal pull-up resistors while TCK has weak internal pull-down resistors. All user I/O pins are tri-stated during JTAG configuration. Table 14–1 summarizes the functions of each of these pins.

Table 14–1. IEEE Std. 1149.1 Pin Descriptions

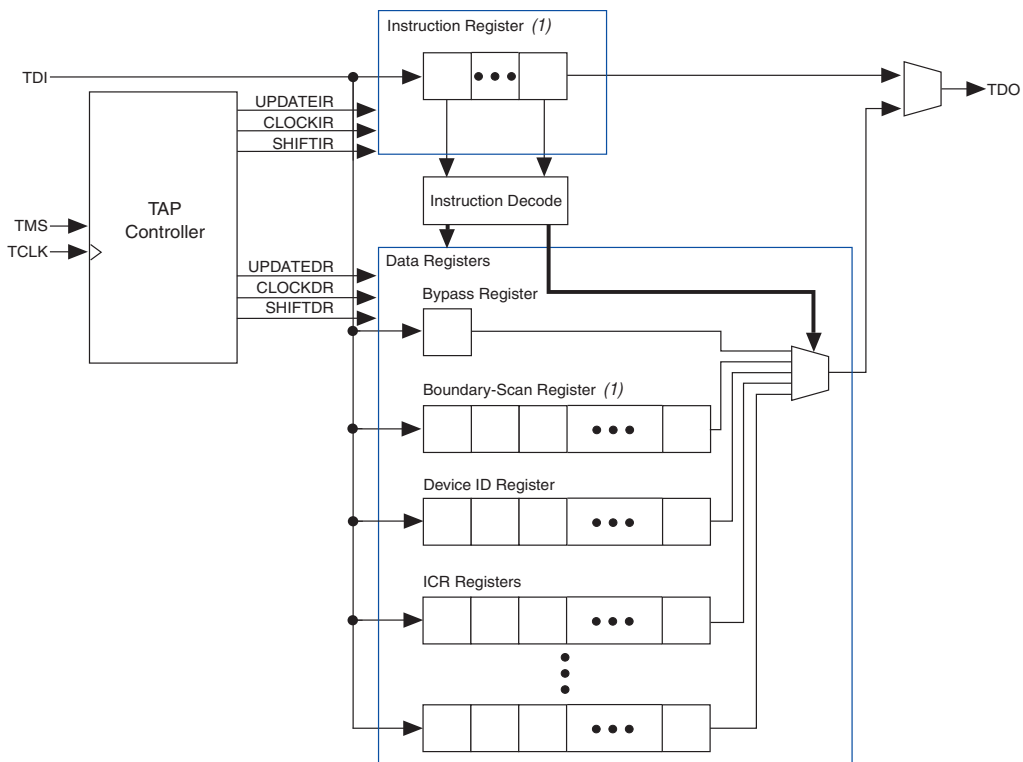
Pin	Description	Function
TDI	Test data input	Serial input pin for instructions as well as test and programming data. Signal applied to TDI is expected to change state at the falling edge of TCK. Data is shifted in on the rising edge of TCK.
TDO	Test data output	Serial data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of TCK. The pin is tri-stated if data is not being shifted out of the device.
TMS	Test mode select	Input pin that provides the control signal to determine the transitions of the TAP controller state machine. Transitions within the state machine occur at the rising edge of TCK. Therefore, TMS must be set up before the rising edge of TCK. TMS is evaluated on the rising edge of TCK. During non-JTAG operation, TMS is recommended to be driven high.
TCK	Test clock input	The clock input to the BST circuitry. Some operations occur at the rising edge, while others occur at the falling edge. The clock input waveform should have a 50% duty cycle.

The IEEE Std. 1149.1 BST circuitry requires the following registers:

- The instruction register determines the action to be performed and the data register to be accessed.
- The bypass register is a 1-bit-long data register that provides a minimum-length serial path between TDI and TDO.
- The boundary-scan register is a shift register composed of all the boundary-scan cells of the device.

Figure 14–2 shows a functional model of the IEEE Std. 1149.1 circuitry.

Figure 14–2. IEEE Std. 1149.1 Circuitry



Note to Figure 14–2:

- (1) For register lengths, see the device data sheet in the *Configuration & Testing* chapter in Volume 1 of the *Cyclone II Device Handbook*.

IEEE Std. 1149.1 boundary-scan testing is controlled by a test access port (TAP) controller. For more information on the TAP controller, see “IEEE Std. 1149.1 BST Operation Control” on page 14–6. The TMS and TCK pins

operate the TAP controller, and the TDI and TDO pins provide the serial path for the data registers. The TDI pin also provides data to the instruction register, which then generates control logic for the data registers.

IEEE Std. 1149.1 Boundary-Scan Register

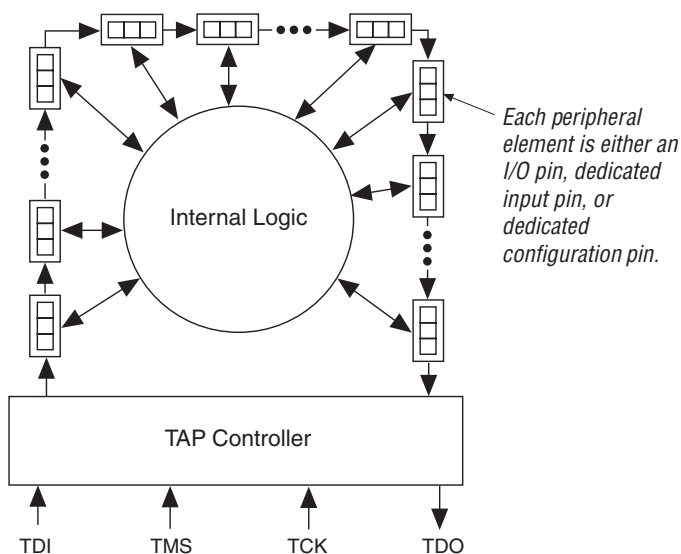
The boundary-scan register is a large serial shift register that uses the TDI pin as an input and the TDO pin as an output. The boundary-scan register consists of 3-bit peripheral elements that are associated with Cyclone II I/O pins. You can use the boundary-scan register to test external pin connections or to capture internal data.



See the *Configuration & Testing* chapter in Volume 1 of the *Cyclone II Device Handbook* for the Cyclone II device boundary-scan register lengths.

Figure 14-3 shows how test data is serially shifted around the periphery of the IEEE Std. 1149.1 device.

Figure 14-3. Boundary-Scan Register



Boundary-Scan Cells of a Cyclone II Device I/O Pin

The Cyclone II device 3-bit boundary-scan cell (BSC) consists of a set of capture registers and a set of update registers. The capture registers can connect to internal device data via the $OUTJ$ and OEJ signals, and connect

to external device data via the `PIN_IN` signal, while the update registers connect to external data through the `PIN_OUT` and `PIN_OE` signals. The global control signals for the IEEE Std. 1149.1 BST registers (for example, shift, clock, and update) are generated internally by the TAP controller. The `MODE` signal is generated by a decode of the instruction register. The data signal path for the boundary-scan register runs from the serial data in (`SDI`) signal to the serial data out (`SDO`) signal. The scan register begins at the `TDI` pin and ends at the `TDO` pin of the device.

Figure 14–4 shows the Cyclone II device's user I/O boundary-scan cell.

Figure 14–4. Cyclone II Device's User I/O BSC with IEEE Std. 1149.1 BST Circuitry

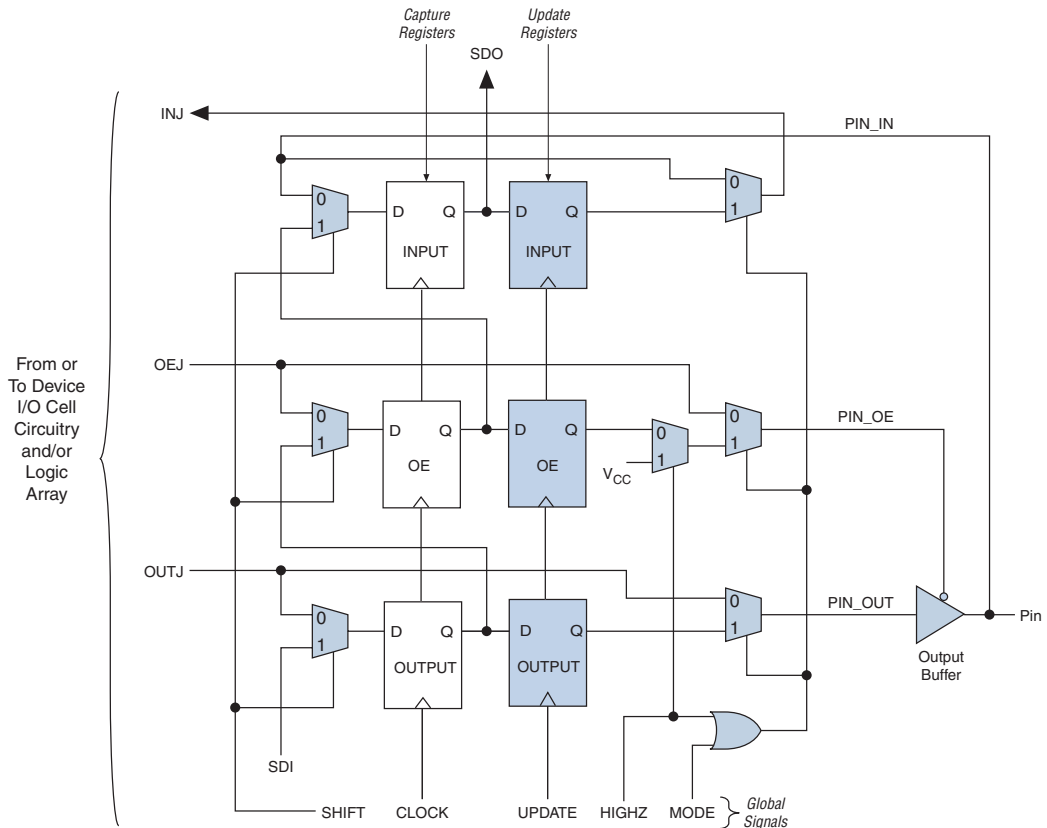


Table 14–2 describes the capture and update register capabilities of all types of boundary-scan cells within Cyclone II devices.

Table 14–2. Cyclone II Device Boundary Scan Cell Descriptions *Note (1)*

Pin Type	Captures			Drives			Comments
	Output Capture Register	OE Capture Register	Input Capture Register	Output Update Register	OE Update Register	Input Update Register	
User I/O pins	OUTJ	OEJ	PIN_IN	PIN_OUT	PIN_OE	INJ	
Dedicated clock input	0	1	PIN_IN	N.C. (2)	N.C. (2)	N.C. (2)	PIN_IN drives to clock network or logic array
Dedicated input (3)	0	1	PIN_IN	N.C. (2)	N.C. (2)	N.C. (2)	PIN_IN drives to control logic
Dedicated bidirectional (open drain) (4)	0	OEJ	PIN_IN	N.C. (2)	N.C. (2)	N.C. (2)	PIN_IN drives to configuration control
Dedicated bidirectional (5)	OUTJ	OEJ	PIN_IN	N.C. (2)	N.C. (2)	N.C. (2)	OUTJ drives to output buffer

Notes to Table 14–2:

- (1) TDI, TDO, TMS, TCK, all V_{CC} and GND pin types do not have BSCs.
- (2) N.C.: no connect.
- (3) This includes nCONFIG, MSEL0, MSEL1, DATA0, and nCE pins and DCLK (when not used in Active Serial mode).
- (4) This includes CONF_DONE and nSTATUS pins.
- (5) This includes DCLK (when not used in Active Serial mode).

IEEE Std. 1149.1 BST Operation Control

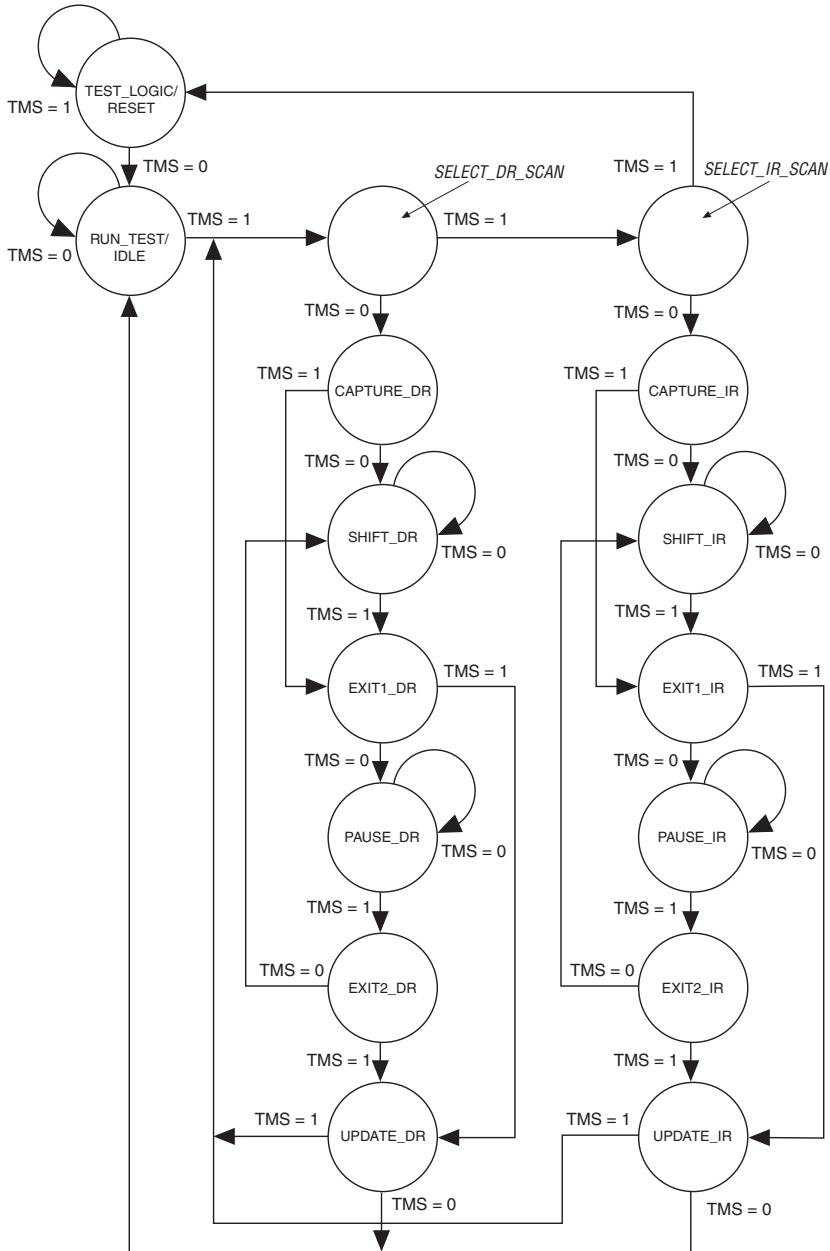
Cyclone II devices implement the following IEEE Std. 1149.1 BST instructions: SAMPLE/PRELOAD, EXTEST, BYPASS, IDCODE, USERCODE, CLAMP, and HIGHZ. The BST instruction length is 10 bits. These instructions are described later in this chapter.



For summaries of the BST instructions and their instruction codes, see the *Configuration & Testing* chapter in Volume 1 of the *Cyclone II Device Handbook*.

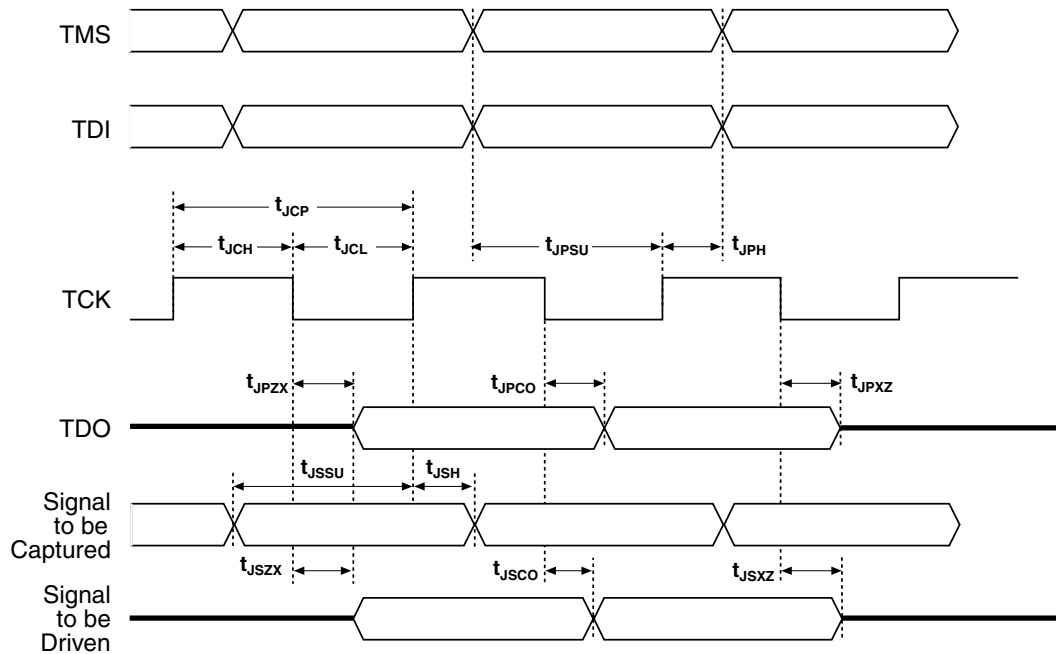
The IEEE Std. 1149.1 test access port (TAP) controller, a 16-state state machine clocked on the rising edge of TCK, uses the TMS pin to control IEEE Std. 1149.1 operation in the device. Figure 14–5 shows the TAP controller state machine.

Figure 14-5. IEEE Std. 1149.1 TAP Controller State Machine

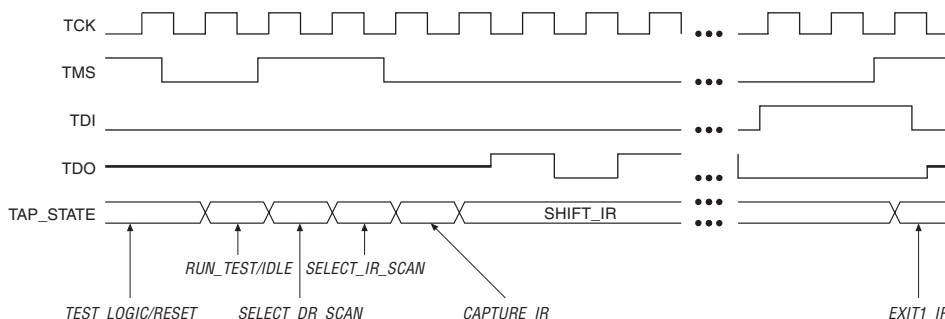


When the TAP controller is in the `TEST_LOGIC/RESET` state, the BST circuitry is disabled, the device is in normal operation, and the instruction register is initialized with `IDCODE` as the initial instruction. At device power-up, the TAP controller starts in this `TEST_LOGIC/RESET` state. In addition, forcing the TAP controller to the `TEST_LOGIC/RESET` state is done by holding `TMS` high for five `TCK` clock cycles. Once in the `TEST_LOGIC/RESET` state, the TAP controller remains in this state as long as `TMS` is held high (while `TCK` is clocked). Figure 14–6 shows the timing requirements for the IEEE Std. 1149.1 signals.

Figure 14–6. IEEE Std. 1149.1 Timing Waveforms



To start IEEE Std. 1149.1 operation, select an instruction mode by advancing the TAP controller to the shift instruction register (`SHIFT_IR`) state and shift in the appropriate instruction code on the `TDI` pin. The waveform diagram in Figure 14–7 represents the entry of the instruction code into the instruction register. It shows the values of `TCK`, `TMS`, `TDI`, `TDO`, and the states of the TAP controller. From the `RESET` state, `TMS` is clocked with the pattern `01100` to advance the TAP controller to `SHIFT_IR`.

Figure 14–7. Selecting the Instruction Mode

The TDO pin is tri-stated in all states except in the `SHIFT_IR` and `SHIFT_DR` states. The TDO pin is activated at the first falling edge of TCK after entering either of the shift states and is tri-stated at the first falling edge of TCK after leaving either of the shift states.

When the `SHIFT_IR` state is activated, TDO is no longer tri-stated, and the initial state of the instruction register is shifted out on the falling edge of TCK. TDO continues to shift out the contents of the instruction register as long as the `SHIFT_IR` state is active. The TAP controller remains in the `SHIFT_IR` state as long as TMS remains low.

During the `SHIFT_IR` state, an instruction code is entered by shifting data on the TDI pin on the rising edge of TCK. The last bit of the instruction code must be clocked at the same time that the next state, `EXIT1_IR`, is activated. Set TMS high to activate the `EXIT1_IR` state. Once in the `EXIT1_IR` state, TDO becomes tri-stated again. TDO is always tri-stated except in the `SHIFT_IR` and `SHIFT_DR` states. After an instruction code is entered correctly, the TAP controller advances to serially shift test data in one of seven modes (`SAMPLE/PRELOAD`, `EXTEST`, `BYPASS`, `IDCODE`, `USERCODE`, `CLAMP`, or `HIGHZ`) that are described below.

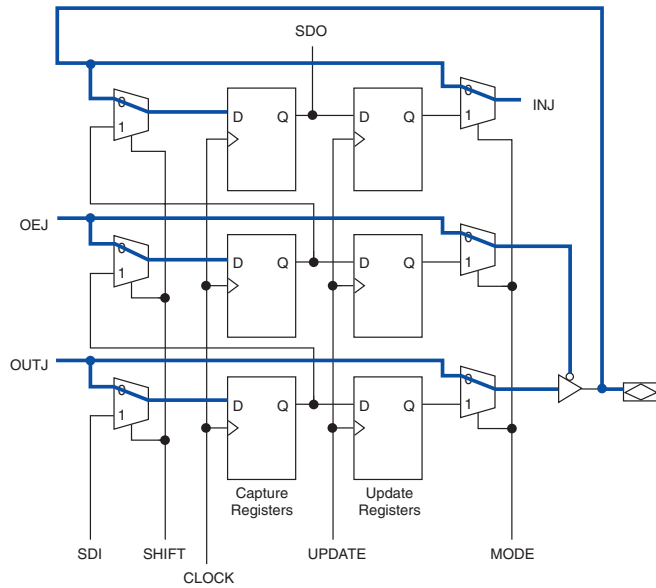
SAMPLE/PRELOAD Instruction Mode

The `SAMPLE/PRELOAD` instruction mode allows you to take a snapshot of device data without interrupting normal device operation. You can also use this instruction to preload the test data into the update registers prior to loading the `EXTEST` instruction. [Figure 14–8](#) shows the capture, shift, and update phases of the `SAMPLE/PRELOAD` mode.

Figure 14–8. IEEE Std. 1149.1 BST SAMPLE/PRELOAD Mode

Capture Phase

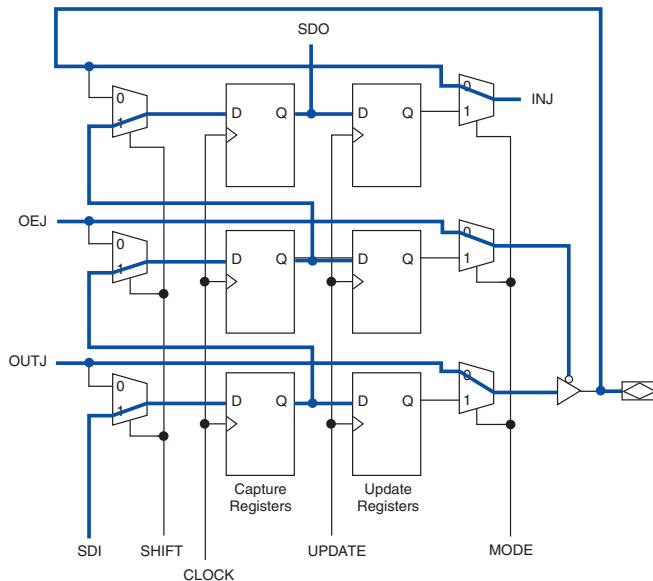
In the capture phase, the signals at the pin, OEJ and OUTJ, are loaded into the capture registers. The CLOCK signals are supplied by the TAP controller's CLOCKDR output. The data retained in these registers consists of signals from normal device operation.



Shift & Update Phases

In the shift phase, the previously captured signals at the pin, OEJ and OUTJ, are shifted out of the boundary-scan register via the TDO pin using CLOCK. As data is shifted out, the patterns for the next test can be shifted in via the TDI pin.

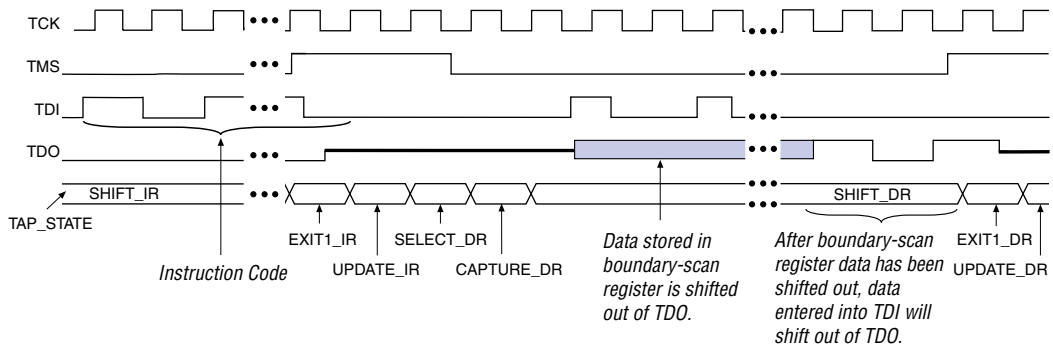
In the update phase, data is transferred from the capture to the UPDATE registers using the UPDATE clock. The data stored in the UPDATE registers can be used for the EXTEST instruction.



During the capture phase, multiplexers preceding the capture registers select the active device data signals. This data is then clocked into the capture registers. The multiplexers at the outputs of the update registers also select active device data to prevent functional interruptions to the device. During the shift phase, the boundary-scan shift register is formed by clocking data through capture registers around the device periphery, then out of the TDO pin. The device can simultaneously shift new test data into TDI and replace the contents of the capture registers. During the update phase, data in the capture registers is transferred to the update registers. This data can then be used in the EXTEST instruction mode. See “EXTEST Instruction Mode” on page 14–11 for more information.

Figure 14–9 shows the SAMPLE/PRELOAD waveforms. The SAMPLE/PRELOAD instruction code is shifted in through the TDI pin. The TAP controller advances to the CAPTURE_DR state, then to the SHIFT_DR state, where it remains if TMS is held low. The data that was present in the capture registers after the capture phase is shifted out of the TDO pin. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register. Figure 14–9 shows that the instruction code at TDI does not appear at the TDO pin until after the capture register data is shifted out. If TMS is held high on two consecutive TCK clock cycles, the TAP controller advances to the UPDATE_DR state for the update phase.

Figure 14–9. SAMPLE/PRELOAD Shift Data Register Waveforms



EXTEST Instruction Mode

The EXTEST instruction mode is used to check external pin connections between devices. Unlike the SAMPLE/PRELOAD mode, EXTEST allows test data to be forced onto the pin signals. By forcing known logic high and low levels on output pins, opens and shorts can be detected at pins of any device in the scan chain.

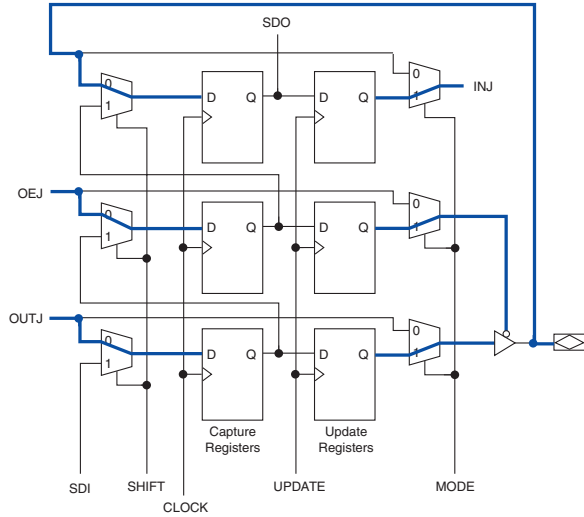
Figure 14–10 shows the capture, shift, and update phases of the EXTEST mode.

Figure 14–10. IEEE Std. 1149.1 BST EXTEST Mode

Capture Phase

In the capture phase, the signals at the pin, OEJ and OUTJ, are loaded into the capture registers. The CLOCK signals are supplied by the TAP controller's CLOCKDR output. Previously retained data in the update registers drive the PIN_IN, INJ, and allows the I/O pin to tri-state or drive a signal out.

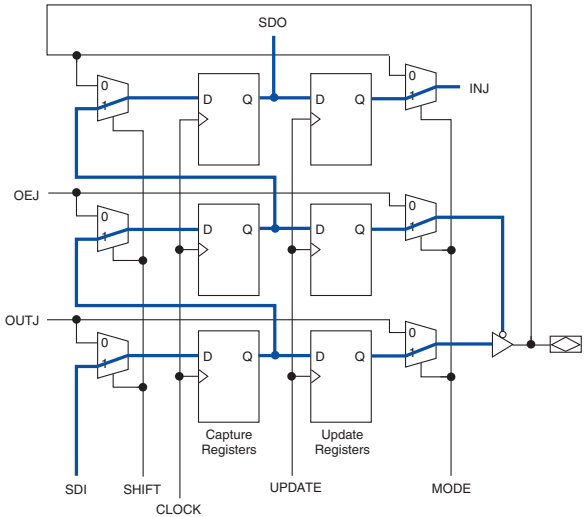
A “1” in the OEJ update register tri-states the output buffer.



Shift & Update Phases

In the shift phase, the previously captured signals at the pin, OEJ and OUTJ, are shifted out of the boundary-scan register via the TDO pin using CLOCK. As data is shifted out, the patterns for the next test can be shifted in via the TDI pin.

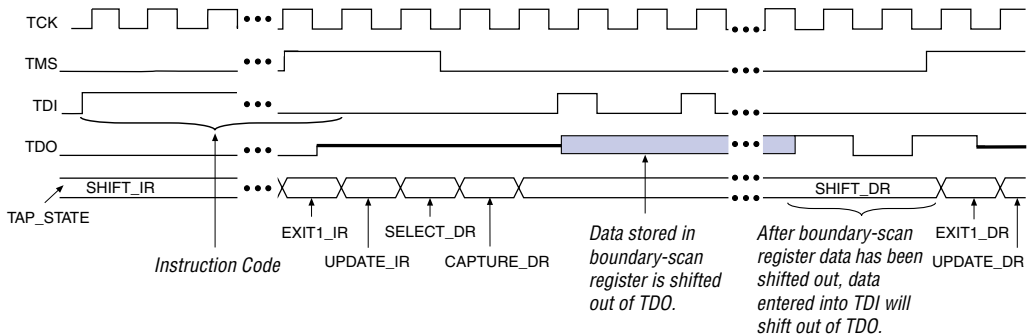
In the update phase, data is transferred from the capture registers to the update registers using the UPDATE clock. The update registers then drive the PIN_IN, INJ, and allow the I/O pin to tri-state or drive a signal out.



EXTEST selects data differently than SAMPLE/PRELOAD. EXTEST chooses data from the update registers as the source of the output and output enable signals. Once the EXTEST instruction code is entered, the multiplexers select the update register data. Thus, data stored in these registers from a previous EXTEST or SAMPLE/PRELOAD test cycle can be forced onto the pin signals. In the capture phase, the results of this test data are stored in the capture registers, then shifted out of TDO during the shift phase. New test data can then be stored in the update registers during the update phase.

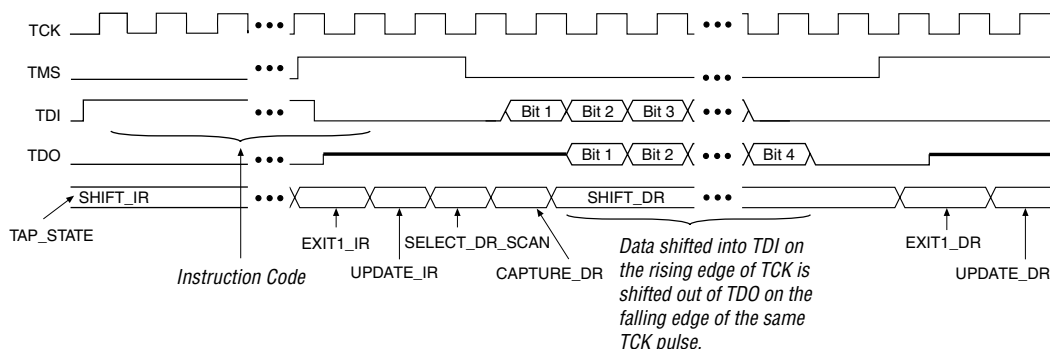
The EXTEST waveform diagram in Figure 14–11 resembles the SAMPLE/PRELOAD waveform diagram, except for the instruction code. The data shifted out of TDO consists of the data that was present in the capture registers after the capture phase. New test data shifted into the TDI pin appears at the TDO pin after being clocked through the entire boundary-scan register.

Figure 14–11. EXTEST Shift Data Register Waveforms



BYPASS Instruction Mode

The BYPASS mode is activated when an instruction code of all 1's is loaded in the instruction register. The waveforms in Figure 14–12 show how scan data passes through a device once the TAP controller is in the SHIFT_DR state. In this state, data signals are clocked into the bypass register from TDI on the rising edge of TCK and out of TDO on the falling edge of the same clock pulse.

Figure 14–12. BYPASS Shift Data Register Waveforms

IDCODE Instruction Mode

The `IDCODE` instruction mode is used to identify the devices in an IEEE Std. 1149.1 chain. When `IDCODE` is selected, the device identification register is loaded with the 32-bit vendor-defined identification code. The device ID register is connected between the `TDI` and `TDO` ports, and the device `IDCODE` is shifted out. The `IDCODE` for Cyclone II devices are listed in the *Configuration & Testing* chapter in Volume 1 of the *Cyclone II Device Handbook*.

USERCODE Instruction Mode

The `USERCODE` instruction mode is used to examine the user electronic signature (UES) within the devices along an IEEE Std. 1149.1 chain. When this instruction is selected, the device identification register is connected between the `TDI` and `TDO` ports. The user-defined UES is shifted into the device ID register in parallel from the 32-bit `USERCODE` register. The UES is then shifted out through the device ID register. The UES value is not user defined until after the device has been configured. Before configuration, the UES value is set to the default value.

CLAMP Instruction Mode

The `CLAMP` instruction mode is used to allow the boundary-scan register to determine the state of the signals driven from the pins. In `CLAMP` instruction mode, the bypass register is selected as the serial path between the `TDI` and `TDO` ports.

If you are testing the device after configuring it, the programmable weak pull-up resistor or the bus hold feature overrides the `CLAMP` value (the value stored in the update register of the boundary-scan cell) at the pin.

HIGHZ Instruction Mode

The `HIGHZ` instruction mode is used to set all of the user I/O pins to an inactive drive state. These pins are tri-stated until a new JTAG instruction is executed. When this instruction is loaded into the instruction register, the bypass register is connected between the `TDI` and `TDO` ports.

If you are testing the device after configuring it, the programmable weak pull-up resistor or the bus hold feature overrides the `HIGHZ` value at the pin.

I/O Voltage Support in JTAG Chain

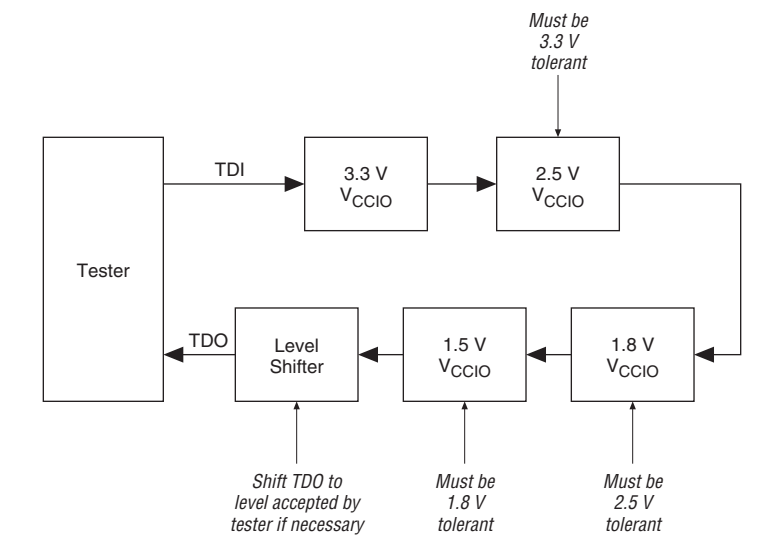
A JTAG chain can contain several different devices. However, you should be cautious if the chain contains devices that have different V_{CCIO} levels. The output voltage level of the `TDO` pin must meet the specifications of the `TDI` pin it drives. For Cyclone II devices, the `TDO` pin is powered by the V_{CCIO} power supply. Since the V_{CCIO} supply is 3.3 V, the `TDO` pin drives out 3.3 V.

Devices can interface with each other although they might have different V_{CCIO} levels. For example, a device with a 3.3-V `TDO` pin can drive to a device with a 5.0-V `TDI` pin because 3.3 V meets the minimum TTL-level V_{IH} for the 5.0-V `TDI` pin. JTAG pins on Cyclone II devices can support 2.5- or 3.3-V input levels.



For more information on MultiVolt I/O support, see the *Cyclone II Architecture* chapter in Volume 1 of the *Cyclone II Device Handbook*.

You can also interface the `TDI` and `TDO` lines of the devices that have different V_{CCIO} levels by inserting a level shifter between the devices. If possible, the JTAG chain should be built such that a device with a higher V_{CCIO} level drives to a device with an equal or lower V_{CCIO} level. This way, a level shifter may be required only to shift the `TDO` level to a level acceptable to the JTAG tester. [Figure 14-13](#) shows the JTAG chain of mixed voltages and how a level shifter is inserted in the chain.

Figure 14–13. JTAG Chain of Mixed Voltages

Using IEEE Std. 1149.1 BST Circuitry

Cyclone II devices have dedicated JTAG pins, and the IEEE Std. 1149.1 BST circuitry is enabled upon device power-up. You can perform BST on Cyclone II FPGAs not only before and after configuration, but also during configuration. Cyclone II FPGAs support the `BYPASS`, `IDCODE`, and `SAMPLE` instructions during configuration without interrupting configuration. To send all other JTAG instructions, you must interrupt configuration using the `CONFIG_IO` instruction.

The `CONFIG_IO` instruction allows you to configure I/O buffers via the JTAG port, and when issued, interrupts configuration. This instruction allows you to perform board-level testing prior to configuring the Cyclone II FPGA or waiting for a configuration device to complete configuration. Once configuration has been interrupted and JTAG BST is complete, the part must be reconfigured via JTAG (`PULSE_CONFIG` instruction) or by pulsing `nCONFIG` low.

When you perform JTAG boundary-scan testing before configuration, the `nCONFIG` pin must be held low.

The device-wide reset (`DEV_CLRn`) and device-wide output enable (`DEV_OE`) pins on Cyclone II devices do not affect JTAG boundary-scan or configuration operations. Toggling these pins does not disrupt BST operation any more than usual.

When designing a board for JTAG configuration of Cyclone II devices, the connections for the dedicated configuration pins need to be considered.



For more information on using the IEEE Std.1149.1 circuitry for device configuration, see the *Configuring Cyclone II Devices* chapter in Volume 1 of the *Cyclone II Device Handbook*.

BST for Configured Devices

For a configured device, the input buffers are turned off by default for I/O pins that are set as output only in the design file. Nevertheless, executing the SAMPLE instruction will turn on the input buffers for the output pins. You can set the Quartus II software to always enable the input buffers on a configured device so it behaves the same as an unconfigured device for boundary-scan testing, allowing sample function on output pins in the design. This aspect can cause slight increase in standby current because the unused input buffer is always on. In the Quartus II software, do the following:

1. Choose **Settings** (Assignment menu).
2. Click **Assembler**.
3. Turn on **Always Enable Input Buffers**.
4. If you use the default setting with input disabled, you need to convert the default BSDL file to the design-specific BSDL file using the BSDLCustomizer script. For more information regarding BSDL file, refer to ["Boundary-Scan Description Language \(BSDL\) Support"](#).

Disabling IEEE Std. 1149.1 BST Circuitry

The IEEE Std. 1149.1 BST circuitry for Cyclone II devices is enabled upon device power-up. Because this circuitry may be used for BST or in-circuit reconfiguration, this circuitry must be enabled only at specific times as mentioned in “Using IEEE Std. 1149.1 BST Circuitry” on page 14–16.

If the IEEE Std. 1149.1 circuitry will not be utilized at any time, the circuitry should be permanently disabled. Table 14–3 shows the pin connections necessary for disabling the IEEE Std. 1149.1 circuitry in Cyclone II devices to ensure that the circuitry is not inadvertently enabled when it is not needed.

Table 14–3. Disabling IEEE Std. 1149.1 Circuitry

JTAG Pins (1)	Connection for Disabling
TMS	V _{CC}
TCK	GND
TDI	V _{CC}
TDO	Leave open

Note to Table 14–3:

- (1) There is no software option to disable JTAG in Cyclone II devices. The JTAG pins are dedicated.

Guidelines for IEEE Std. 1149.1 Boundary-Scan Testing

Use the following guidelines when performing boundary-scan testing with IEEE Std. 1149.1 devices:

- If the 10-bit checkerboard pattern “1010101010” does not shift out of the instruction register via the TDO pin during the first clock cycle of the SHIFT_IR state, the TAP controller has not reached the proper state. To solve this problem, try one of the following procedures:
 - Verify that the TAP controller has reached the SHIFT_IR state correctly. To advance the TAP controller to the SHIFT_IR state, return to the RESET state and send the code 01100 to the TMS pin.
 - Check the connections to the V_{CC}, GND, JTAG, and dedicated configuration pins on the device.

- Perform a `SAMPLE/PRELOAD` test cycle prior to the first `EXTEST` test cycle to ensure that known data is present at the device pins when the `EXTEST` mode is entered. If the `OEJ` update register contains a 0, the data in the `OUTJ` update register is driven out. The state must be known and correct to avoid contention with other devices in the system.
- Do not perform `EXTEST` testing during `ICR`. This instruction is supported before or after `ICR`, but not during `ICR`. Use the `CONFIG_IO` instruction to interrupt configuration, then perform testing, or wait for configuration to complete.
- If performing testing before configuration, hold the `nCONFIG` pin low.
- After configuration, any pins in a differential pin pair cannot be tested. Therefore, performing `BST` after configuration requires editing `BSC` group definitions that correspond to these differential pin pairs. The `BSC` group should be redefined as an internal cell. See the `BSDL` file for more information on editing.

For more information on boundary scan testing, contact Altera Applications.

Boundary-Scan Description Language (BSDL) Support

The Boundary-Scan Description Language (BSDL), a subset of VHDL, provides a syntax that allows you to describe the features of an IEEE Std. 1149.1 BST-capable device that can be tested. Test software development systems then use the `BSDL` files for test generation, analysis, and failure diagnostics. For more information, or to receive `BSDL` files for IEEE Std. 1149.1-compliant Cyclone II devices, visit the Altera web site at www.altera.com.

Conclusion

The IEEE Std. 1149.1 BST circuitry available in Cyclone II devices provides a cost-effective and efficient way to test systems that contain devices with tight lead spacing. Circuit boards with Altera and other IEEE Std. 1149.1-compliant devices can use the `EXTEST`, `SAMPLE/PRELOAD`, `BYPASS`, `IDCODE`, `USERCODE`, `CLAMP`, and `HIGHZ` modes to create serial patterns that internally test the pin connections between devices and check device operation.

References

Bleeker, H., P. van den Eijnden, and F. de Jong. *Boundary-Scan Test: A Practical Approach*. Eindhoven, The Netherlands: Kluwer Academic Publishers, 1993.

Institute of Electrical and Electronics Engineers, Inc. *IEEE Standard Test Access Port and Boundary-Scan Architecture* (IEEE Std 1149.1-2001). New York: Institute of Electrical and Electronics Engineers, Inc., 2001.

Maunder, C. M., and R. E. Tulloss. *The Test Access Port and Boundary-Scan Architecture*. Los Alamitos: IEEE Computer Society Press, 1990.

Document Revision History

Table 14–4 shows the revision history for this document.

<i>Table 14–4. Document Revision History</i>		
Date & Document Version	Changes Made	Summary of Changes
February 2007 v2.1	<ul style="list-style-type: none">• Added document revision history.• Added new section “BST for Configured Devices”.	<ul style="list-style-type: none">• Added information about ‘Always Enable Input Buffer’ option.
July 2005 v2.0	Moved the “JTAG Timing Specifications” section to the <i>DC Characteristics & Timing Specifications</i> chapter.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	