7. PLLs in Cyclone II Devices

CII51007-3.1

Introduction

Cyclone® II devices have up to four phase-locked loops (PLLs) that provide robust clock management and synthesis for device clock management, external system clock management, and I/O interfaces. Cyclone II PLLs are versatile and can be used as a zero delay buffer, a jitter attenuator, a low skew fan out buffer, or a frequency synthesizer.

Each Cyclone II device has up to four PLLs, supporting advanced capabilities such as clock switchover and programmable switchover. These PLLs offer clock multiplication and division, phase shifting, and programmable duty cycle and can be used to minimize clock delay and clock skew, and to reduce or adjust clock-to-out (t_{CO}) and set-up (t_{SU}) times.

Cyclone II devices also support a power-down mode where unused clock networks can be turned off. The Altera® Quartus® II software enables the PLLs and their features without requiring any external devices.

Cyclone II PLLs have been characterized to operate in the commercial junction temperature range (0° to 85° C), the industrial junction temperature range (-40° to 100° C) and the extended temperature range (-40° to 125° C).

Table 7–1 shows the PLLs available in each Cyclone II device.

Table 7–1. Cyclone II Device PLL Availability

Device	PLL1	PLL2	PLL3	PLL4
EP2C5	✓	✓		
EP2C8	✓	✓		
EP2C15	✓	✓	✓	✓
EP2C20	✓	✓	✓	✓
EP2C35	✓	✓	✓	✓
EP2C50	✓	✓	✓	✓
EP2C70	✓	✓	✓	✓

Table 7–2 provides an overview of the Cyclone II PLL features.

Table 7–2. Cyclone II PLL Features

Feature	Description
Clock multiplication and division	*m* / (*n* × post-scale counter) *(1)*
Phase shift	Down to 125-ps increments *(2)*, *(3)*
Programmable duty cycle	✓
Number of internal clock outputs	Up to three per PLL *(4)*
Number of external clock outputs	One per PLL *(4)*
Locked port can feed logic array	✓
PLL clock outputs can feed logic array	✓
Manual clock switchover	✓
Gated lock	✓

Notes to Table 7–2:

(1) *m* and post-scale counter values range from 1 to 32. *n* ranges from 1 to 4.

(2) The smallest phase shift is determined by the voltage control oscillator (VCO) period divided by 8.

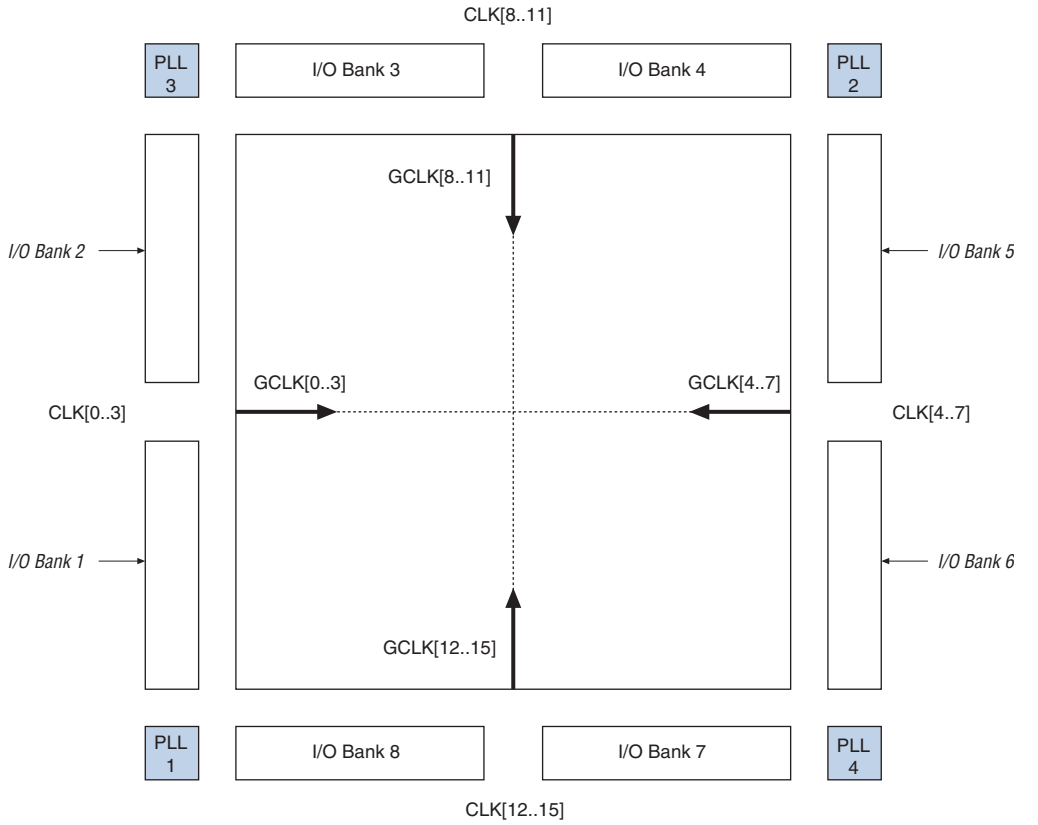
(3) For degree increments, Cyclone II devices can shift output frequencies in increments of at least 45°. Smaller degree increments are possible depending on the VCO frequency.

(4) The Cyclone II PLL has three output counters that drive the global clock network. One of these output counters (c2) can also drive a dedicated external I/O pin (single ended or differential). This counter output can also drive the external clock output (`PLL<#>_OUT`) and internal global clock network at the same time.

Cyclone II PLL Hardware Overview

Cyclone II devices contain up to four PLLs that are arranged in the four corners of the Cyclone II device as shown in Figure 7–1, which shows a top-level diagram of the Cyclone II device and the PLL locations.

Figure 7–1. Cyclone II Device PLL Locations *Note (1)*



Note to Figure 7–1:

(1) This figure shows the PLL and clock inputs in the EP2C15 through EP2C70 devices. The EP2C5 and EP2C8 devices only have eight global clocks (`CLK[0..3]` and `CLK[4..7]`) and PLLs 1 and 2.

The main purpose of a PLL is to synchronize the phase and frequency of the VCO to an input reference clock. There are a number of components that comprise a PLL to achieve this phase alignment.

The PLL compares the rising edge of the reference input clock to a feedback clock using a phase-frequency detector (PFD). The PFD produces an up or down signal that determines whether the VCO needs to operate at a higher or lower frequency. The PFD output is applied to the charge pump and loop filter, which produces a control voltage for setting the frequency of the VCO. If the PFD transitions the up signal high, then the VCO frequency increases. If the PFD transitions the down signal high, then the VCO frequency decreases.

The loop filter converts these up and down signals to a voltage that is used to bias the VCO. If the charge pump receives a logic high on the up signal, current is driven into the loop filter. If the charge pump receives a logic high on the down signal, current is drawn from the loop filter. The loop filter filters out glitches from the charge pump and prevents voltage over-shoot, which minimizes the jitter on the VCO.

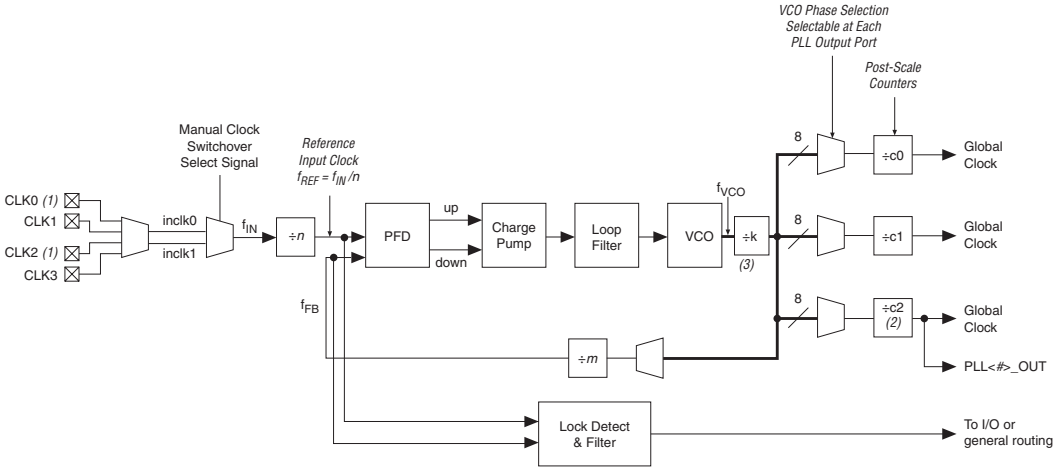
The voltage from the charge pump determines how fast the VCO operates. The VCO is implemented as an four-stage differential ring oscillator. A divide counter, *m*, is inserted in the feedback loop to increase the VCO frequency above the input reference frequency, making the VCO frequency $f_{VCO} = m \times f_{REF}$. Therefore, the feedback clock, f_{FB}, applied to one input of the PFD, is locked to the input reference clock, f_{REF} (f_{IN}/n), applied to the other input of the PFD.

The VCO output can feed up to three post-scale counters (c0, c1, and c2). These post-scale counters allow a number of harmonically related frequencies to be produced by the PLL.

Additionally, Cyclone II PLLs have internal delay elements to compensate for routing on the global clock networks and I/O buffers. These internal delays are fixed and not accessible to the user.

Figure 7–2 shows a simplified block diagram of the major components of a Cyclone II device PLL.

Figure 7–2. Cyclone II PLL Block Diagram



Notes to Figure 7–2:

(1) This input can be single-ended or differential. If you are using a differential I/O standard, then the design uses two clock pins. LVDS input is supported via the secondary function of the dedicated clock pins. For example, the `CLK0` pin's secondary function is `LVDSCLK1p` and the `CLK1` pin's secondary function is `LVDSCLK1n`. Figure 7–2 shows the possible clock input connections to PLL 1.

(2) This counter output is shared between a dedicated external clock output (`PLL<#>_OUT`) and the global clock network.

(3) If the VCO post scale counter = 2, a 300- to 500-MHz internal VCO frequency is available.

The Cyclone II PLL supports up to three global clock outputs and one dedicated external clock output. The output frequency to the global clock network or dedicated external clock output is determined by using the following equation:

$$f_{global/external} = f_{IN} \frac{m}{n \times C}$$

f_{IN} is the clock input to the PLL and C is the setting on the c0, c1, or c2 counter.

The VCO frequency is determined in all cases by using the following equation:

$$f_{VCO} = f_{IN} \frac{m}{n}$$

The VCO frequency is a critical parameter that must be between 300 and 1,000 MHz to ensure proper operation of the PLL. The Quartus II software automatically sets the VCO frequency within the recommended range based on the clock output and phase-shift requirements in your design.

PLL Reference Clock Generation

In Cyclone II devices, up to four clock pins can drive the PLL, as shown in Figure 7–11 on page 7–26. The multiplexer output feeds the PLL reference clock input. The PLL has internal delay elements that compensate for the clock delay from the input pin to the clock input port of the PLL.

Table 7–3 shows the clock input pin connections to the PLLs in the Cyclone II device.

Table 7–3. PLL Clock Input Pin Connections

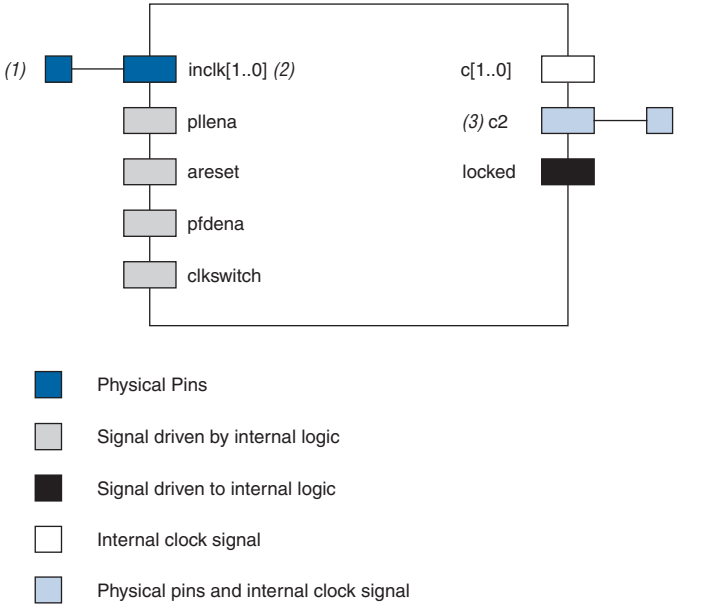
Device	PLL 1		PLL 2		PLL 3		PLL 4	
	CLK0 CLK1	CLK2 CLK3	CLK4 CLK5	CLK6 CLK7	CLK8 CLK9	CLK10 CLK11	CLK12 CLK13	CLK14 CLK15
EP2C5	✓	✓	✓	✓				
EP2C8	✓	✓	✓	✓				
EP2C15	✓	✓	✓	✓	✓	✓	✓	✓
EP2C20	✓	✓	✓	✓	✓	✓	✓	✓
EP2C35	✓	✓	✓	✓	✓	✓	✓	✓
EP2C50	✓	✓	✓	✓	✓	✓	✓	✓
EP2C70	✓	✓	✓	✓	✓	✓	✓	✓

Each PLL can be fed by one of four single-ended or two differential clock input pins. For example, PLL 1 can be fed by `CLK[3..0]` when using a single-ended I/O standard. When your design uses a differential I/O standard, these same clock pins have a secondary function as `LVDSCLK[2..1]p` and `LVDSCLK[2..1]n` pins. When using differential clocks, the `CLK0` pin's secondary function is `LVDSCLK1p`, the `CLK1` pin's secondary function is `LVDSCLK1n`, etc.

Software Overview

You can use the altpll megafunction in the Quartus II software to enable Cyclone II PLLs. Figure 7–3 shows the available ports in Cyclone II PLLs and their sources and destinations. The c0 and c1 counters feed the internal global clock networks and the c2 counter can feed the global clock network and a dedicated external clock output pin (PLL<#>_OUT) at the same time.

Figure 7–3. Cyclone II PLL Signals



Notes to Figure 7–3:

(1) These signals can be assigned to either a single-ended or differential I/O standard.
(2) The inclk must be driven by one of two dedicated clock input pins.
(3) This counter output can drive both a dedicated external clock output (PLL<#>_OUT) and the global clock network.

Tables 7–4 and 7–5 describe the Cyclone II PLL input and output ports.

Table 7–4. PLL Input Signals

Port	Description	Source	Destination
inclk[1..0]	Primary and secondary clock inputs to the PLL.	Dedicated clock input pins	*n* counter
pllena	pllena is an active high signal that acts as an enable and reset signal for the PLL. It can be used for enabling or disabling each PLL. When pllena transitions low, the PLL clock output ports are driven to GND and the PLL loses lock. Once pllena transitions high again, the lock process begins and the PLL re-synchronizes to its input reference clock. The pllena port can be driven by an LE output or any general-purpose I/O pin.	Logic array or input pin	PLL control signal
areset	areset is an active high signal that resets all PLL counters to their initial values. When this signal is driven high the PLL resets its counters, clears the PLL outputs and loses lock. Once this signal is driven low again, the lock process begins and the PLL re-synchronizes to its input reference clock. The areset port can be driven by an LE output or any general-purpose I/O pin.	Logic array or input pin	PLL control signal
pfdena	pfdena is an active high signal that enables or disables the up/down output signals from the PFD. When pfdena is driven low, the PFD is disabled, while the VCO continues to operate. The PLL clock outputs continue to toggle regardless of the input clock, but may experience some long-term drift. Because the output clock frequency does not change for some time, you can use the pfdena port as a shutdown or cleanup function when a reliable input clock is no longer available. The pfdena port can be driven by an LE output or any general-purpose I/O pin.	Logic array or input pin	PFD
clkswitch	clkswitch is an active high switchover signal used to initiate manual clock switchover.	Logic array or input pin	PLL control signal

Table 7–5. PLL Output signals

Port	Description	Source	Destination
c[2..0]	PLL clock outputs driving the internal global clock network or external clock output pin (PLL<#>_OUT)	PLL post-scale counter	Global clock network or external I/O pin
Locked	Gives the status of the PLL lock. When the PLL is locked, this port drives V_{CC}. When the PLL is out of lock, this port drives GND. The locked port may pulse high and low during the PLL lock process.	PLL lock detect circuit	Logic array or output pin

Table 7–6 shows a list of I/O standards supported in Cyclone II device PLLs.

Table 7–6. I/O Standards Supported for Cyclone II PLLs (Part 1 of 2)

I/O Standard	Input	Output	
	inclk	lock	pll_out
LVTTL (3.3, 2.5, and 1.8 V)	✓	✓	✓
LVCMOS (3.3, 2.5, 1.8, and 1.5 V)	✓	✓	✓
3.3-V PCI	✓	✓	✓
3.3-V PCI-X *(1)*	✓	✓	✓
LVPECL	✓		
LVDS	✓	✓	✓
1.5 and 1.8 V differential HSTL class I and class II	✓		✓ *(2)*
1.8 and 2.5 V differential SSTL class I and class II	✓		✓ *(2)*
1.5-V HSTL class I	✓	✓	✓
1.5-V HSTL class II *(3)*	✓	✓	✓
1.8-V HSTL class I	✓	✓	✓
1.8-V HSTL class II *(3)*	✓	✓	✓
SSTL-18 class I	✓	✓	✓
SSTL-18 class II *(3)*	✓	✓	✓
SSTL-25 class I	✓	✓	✓

Table 7–6. I/O Standards Supported for Cyclone II PLLs (Part 2 of 2)

I/O Standard	Input	Output	
	inclk	lock	pll_out
SSTL-25 class II	✓	✓	✓
RSDS/mini-LVDS *(4)*		✓	✓

Notes to Table 7–6:
(1) The PCI-X I/O standard is supported only on side I/O pins.
(2) Differential SSTL and HSTL outputs are only supported on the PLL<#>_OUT pins.
(3) These I/O standards are only supported on top and bottom I/O pins.
(4) The RSDS and mini-LVDS pins are only supported on output pins.

Clock Feedback Modes

Cyclone II PLLs support four clock feedback modes: normal mode, zero delay buffer mode, no compensation mode, and source synchronous mode. Cyclone II PLLs do not have support for external feedback mode. All the supported clock feedback modes allow for multiplication and division, phase shifting, and programmable duty cycle. The phase relationships shown in the waveforms in Figures 7–4 through 7–6 are for the default (zero degree) phase shift setting. Changing the phase-shift setting changes the relationships between the output clocks from the PLL.

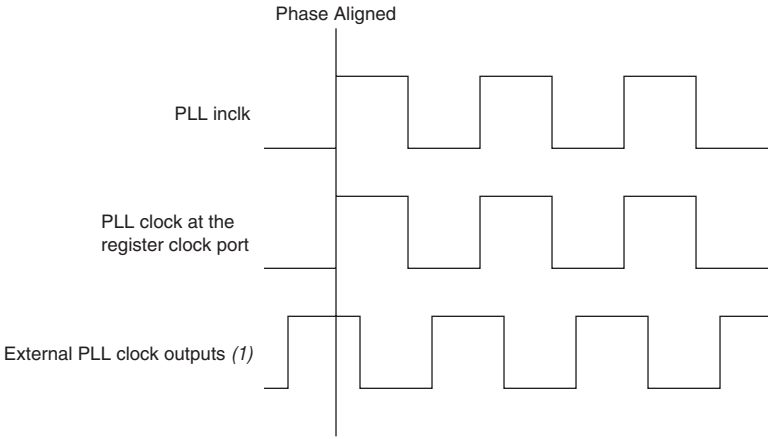
Normal Mode

In normal mode, the PLL phase-aligns the input reference clock with the clock signal at the ports of the registers in the logic array I/O registers to compensate for the internal global clock network delay. Use the `altpll` megafunction in the Quartus II software to define which internal clock output from the PLL (c0, c1, or c2) to compensate for.

If an external clock output pin (PLL<#>_OUT) is used in this mode, there is a phase shift with respect to the clock input pin. Similarly, if the internal PLL clock outputs are used to drive general-purpose I/O pins, there is be phase shift with respect to the clock input pin.

Figure 7–4 shows an example waveform of the PLL clocks' phase relationship in this mode.

Figure 7–4. Phase Relationship between Cyclone II PLL Clocks in Normal Mode

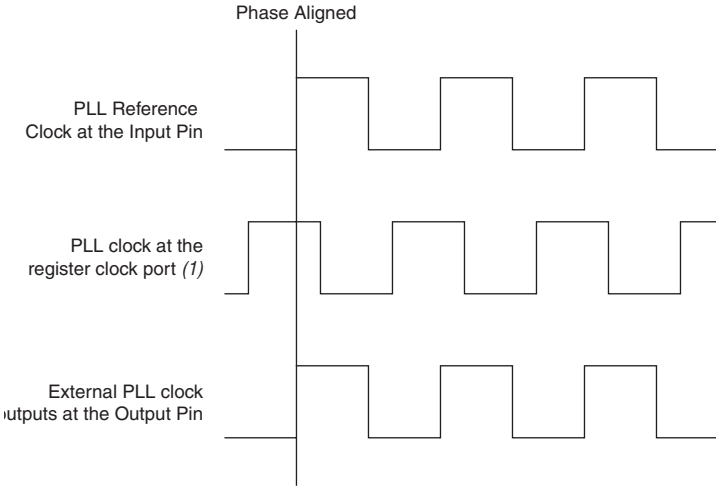


Note to Figure 7–4:
(1) The external clock output can lead or lag the PLL clock signals.

Zero Delay Buffer Mode

In zero delay buffer mode, the clock signal on the PLL external clock output pin (PLL<#>_OUT), fed by the c2 counter, is phase-aligned with the PLL input clock pin for zero delay. If the c[1..0] ports drive internal clock ports, there is a phase shift with respect to the input clock pin. Figure 7–5 shows an example waveform of the PLL clocks' phase relationship in this mode.

Figure 7–5. Phase Relationship between Cyclone II PLL Clocks in Zero Delay Buffer Mode



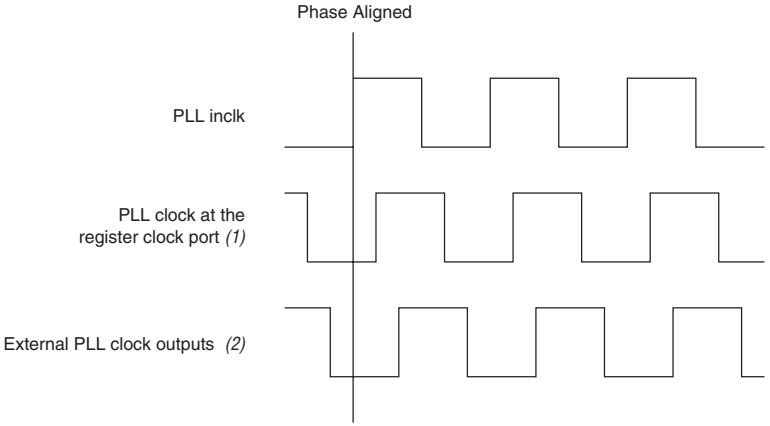
Note to Figure 7–5:
(1) The internal clock output(s) can lead or lag the external PLL clock output (PLL<#>_OUT) signals.

Altera recommends using the same I/O standard on the input and output clocks when using the Cyclone II PLL in zero delay buffer mode.

No Compensation Mode

In no compensation mode, the PLL does not compensate for any clock networks, which leads to better jitter performance. Because the clock feedback into the PFD does not pass through as much circuitry, both the PLL internal clock outputs and external clock outputs are phase shifted with respect to the PLL clock input. Figure 7–6 shows an example waveform of the PLL clocks' phase relationship in this mode.

Figure 7–6. Phase Relationship between Cyclone II PLL Clocks in No Compensation Mode

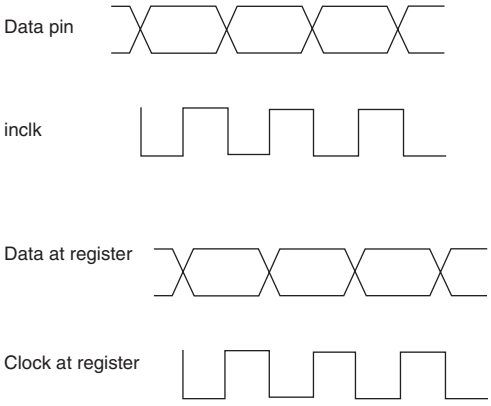


Notes to Figure 7–6:
(1) Internal clocks fed by the PLL are in phase with each other.
(2) The external clock outputs can lead or lag the PLL internal clocks.

Source-Synchronous Mode

If data and clock arrive at the same time at the input pins, they are guaranteed to keep the same phase relationship at the clock and data ports of any IOE input register. Figure 7–7 shows an example waveform of the clock and data in this mode. This mode is recommended for source-synchronous data transfer. Data and clock signals at the IOE experience similar buffer delays as long as the same I/O standard is used.

Figure 7–7. Phase Relationship between Cyclone II PLL Clocks in Source-Synchronous Compensation Mode



Set the input pin to the register delay chain within the IOE to zero in the Quartus II software for all data pins clocked by a source-synchronous mode PLL.

Hardware Features

Cyclone II device PLLs support a number of features for general-purpose clock management. This section discusses clock multiplication and division implementation, phase-shifting implementation and PLL lock circuits.

Clock Multiplication & Division

Cyclone II device PLLs provide clock synthesis for PLL output ports using $m/(n \times \text{post-scale})$ scaling factors. Every PLL has one pre-scale divider, n, with a range of 1 to 4 and one multiply counter, m, with a range of 1 to 32. The input clock, f_{IN}, is divided by a pre-scale counter, n, to produce the input reference clock, f_{REF}, to the PFD. This input reference clock, f_{REF}, is then multiplied by the m feedback factor. The control loop drives the VCO frequency to match $f_{IN} \times (m/n)$. The equations for these frequencies are:

$$f_{REF} = \frac{f_{IN}}{n}$$

$$f_{VCO} = f_{REF} \times m = f_{IN} \frac{m}{n}$$

Each output port has a unique post-scale counter to divide down the high-frequency VCO. There are three post-scale counters (c0, c1, and c2), which range from 1 to 32. The following equations show the frequencies for the three post-scale counters:

$$f_{C0} = \frac{f_{VCO}}{C0} = f_{IN} \frac{m}{n \times C0}$$

$$f_{C1} = \frac{f_{VCO}}{C1} = f_{IN} \frac{m}{n \times C1}$$

$$f_{C2} = \frac{f_{VCO}}{C2} = f_{IN} \frac{m}{n \times C2}$$

All three output counters can drive the global clock network. The c2 output counter can also drive a dedicated external I/O pin (single ended or differential). This counter output can drive a dedicated external clock output pin (`PLL<#>_OUT`) and the global clock network at the same time.

For multiple PLL outputs with different frequencies, the VCO is set to the least common multiple of the output frequencies that meets the VCO frequency specifications. Then, the post-scale counters scale down the VCO frequency for each PLL clock output port. For example, if clock output frequencies required from one PLL are 33 and 66 MHz, the VCO is set to 330 MHz (the least common multiple in the VCO's range).

Programmable Duty Cycle

The programmable duty cycle feature allows you to set the PLL clock output duty cycles. The duty cycle is the ratio of the clock output high and low time to the total clock cycle time, expressed as a percentage of high time. This feature is supported on all three PLL post-scale counters, c0, c1, and c2, and when using all clock feedback modes.

The duty cycle is set by using a low- and high-time count setting for the post-scale counters. The Quartus II software uses the input frequency and target multiply/divide ratio to select the post-scale counter. The granularity of the duty cycle is determined by the post-scale counter value chosen on a PLL clock output and is defined as 50% ÷ post-scale counter value. For example, if the post-scale counter value is 3, then the allowable duty cycle precision would be 50% ÷ 3 = 16.67%. Because the `altpll` megafunction does not accept non-integer values for the duty cycle values, the allowable duty cycles are 17% 33% 50% and 67%. For example, if the c0 counter is 10, then steps of 5% are possible for duty cycle choices between 5 to 90%.

Phase-Shifting Implementation

Cyclone II devices use fine or coarse phase shifts for clock delays because they are more efficient than delay elements and are independent of process, voltage, and temperature.

Phase shift is implemented by using a combination of the VCO phase output and the counter starting time. The VCO phase taps and counter starting time are independent of process, voltage, and temperature. The VCO phase taps allow you to phase shift the Cyclone II PLL output clocks with fine resolution. The counter starting time allows you to phase shift the Cyclone II PLL output clocks with coarse resolution.

Fine-resolution phase shifting is implemented using any of the eight VCO phases for the output counters (`c[2..0]`) or the feedback counter (*m*) reference clock. This provides the finest resolution for phase shift. The minimum delay time that may be inserted using this method is defined by the equation:

$$\Delta t_{FINE} = \frac{1}{8} t_{VCO} = \frac{1}{8 \times f_{VCO}} = \frac{n}{8 \times m \times f_{IN}}$$

f_{IN} is input reference clock frequency.

For example, if f_{IN} is 100 MHz, *n* is 1 and *m* is 8, then f_{VCO} is 800 MHz and Δt is 156.25 ps. This delay time is defined by the PLL operating frequency which is governed by the reference clock and the counter settings.

The second way to implement phase shifts is by delaying the start of the *m* and post-scale counters for a predetermined number of counter clocks. This delay time may be expressed as:

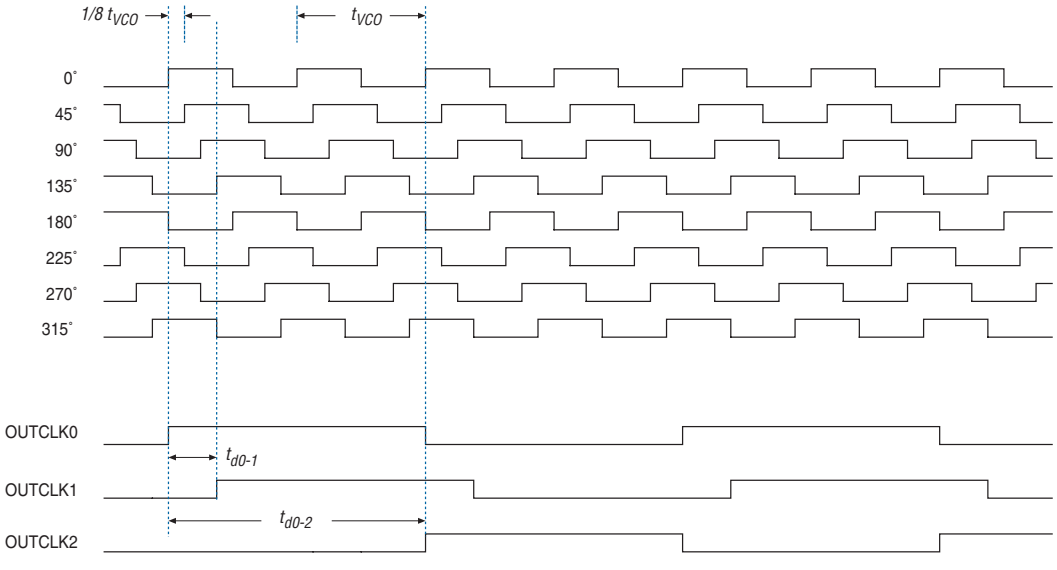
$$\Delta t_{COARSE} = \frac{S - 1}{f_{VCO}} = \frac{(S - 1) \times n}{m \times f_{IN}}$$

where S is the value set for the counter starting time. The counter starting time is called the **Initial** setting in the PLL Usage section of the compilation report in the Quartus II software.

Figure 7–8 shows an example of delay insertion using these two methods. The eight phases from the VCO are shown and labeled for reference. For this example, `OUTCLK0` is based off the 0° phase from the VCO and has the S value for the counter set to 1. It is divided by 4 (two VCO clocks for high time and two VCO clocks for low time). `OUTCLK1` is based off the 135° phase tap from the VCO and also has the S value for the counter set to 1. It is also divided by 4. In this case, the two clocks are offset by three

Δt_{FINE} periods. OUTCLK2 is based off the 0° phase from the VCO but has the S value for the counter set to 3. This creates a delay of two Δt_{COARSE} periods.

Figure 7–8. Cyclone II PLL Phase Shifting using VCO Phase Output & Counter Delay Time



Control Signals

The four control signals in Cyclone II PLLs (pllena, areset, pfdena, and locked) control PLL operation.

pllena

The PLL enable signal, pllena, enables and disables the PLL. You can either enable/disable a single PLL (by connecting pllena port independently) or multiple PLLs (by connecting pllena ports together). The pllena signal is an active-high signal. When pllena is low, the PLL clock output ports are driven by GND and the PLL loses lock. All PLL counters, including gated lock counter return to default state. When pllena transitions high, the PLL relocks and resynchronizes to the input clock. In Cyclone II devices, the pllena port can be fed by an LE output or any general-purpose I/O pin. There is no dedicated pllena pin. This increases flexibility since each PLL can have its own pllena control circuitry or all PLLs can share the same pllena circuitry. The pllena signal is optional. When it is not enabled in the Quartus II software, the port is internally tied to V_{CC}.

areset

The PLL areset signal is the reset and resynchronization input for each PLL. The areset signal should be asserted every time the PLL loses lock to guarantee correct phase relationship between the PLL input and output clocks. You should include the areset signal in designs if any of the following conditions are true:

- Manual clock switchover is enabled in the design
- Phase relationships between input and output clocks need to be maintained after a loss of lock condition
- If the input clock to the PLL is not toggling or is unstable upon powerup, assert the areset signal after the input clock is toggling, staying within the input jitter specification

Altera recommends using the areset and locked signals in your designs to control and observe the status of your PLL.

The areset signal is an active high signal and, when driven high, the PLL counters reset, clearing the PLL output and causing the PLL to lose lock. The VCO is also set back to its nominal frequency. The clock outputs from the PLL are driven to ground as long as areset is active. When areset transitions low, the PLL resynchronizes to its input clock as the PLL relocks. If the target VCO frequency is below this nominal frequency, then the PLL clock output frequency starts at a higher value than desired during the lock process. In this case, Altera recommends monitoring the gated locked signal to ensure the PLL is fully in lock before enabling the clock outputs from the PLL. The Cyclone II device can drive this PLL input signal from LEs or any general-purpose I/O pin. The areset signal is optional. When it is not enabled in the Quartus II software, the port is internally tied to GND.

pfdena

The pfdena signal is an active high signal that controls the PFD output in the PLL with a programmable gate. If you disable the PFD by transitioning pfdena low, the VCO operates at its last set control voltage and frequency value with some long-term drift to a lower frequency. Even though the PLL clock outputs continue to toggle regardless of the input clock, the PLL could lose lock. The system continues running when the PLL goes out of lock or if the input clock is disabled. By maintaining the current frequency, the system has time to store its current settings before shutting down. If the pfdena signal transitions high, the PLL relocks and resynchronizes to the input clock. The pfdena input signal can be driven by any general-purpose I/O pin or from LEs. This signal is optional. When it is not enabled in the Quartus II software, the port is internally tied to V_{CC}.

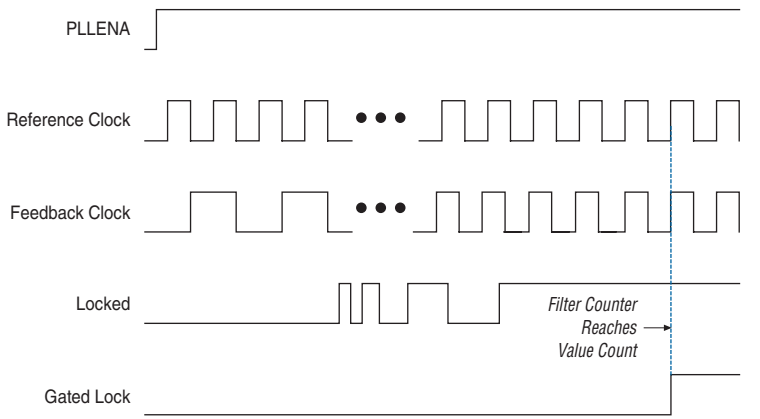
locked

When the `locked` port output is a logic high level, this indicates a stable PLL clock output in phase with the PLL reference input clock. The `locked` port may toggle as the PLL begins tracking the reference clock. The `locked` port of the PLL can feed any general-purpose I/O pin or LEs. The `locked` signal is optional, but is useful in monitoring the PLL lock process.

The `locked` output indicates that the PLL has locked onto the reference clock. You may need to gate the locked signal for use as a system-control signal. Either a gated `locked` signal or an ungated `locked` signal from the `locked` port can drive the logic array or an output pin. Cyclone II PLLs include a programmable counter that holds the `locked` signal low for a user-selected number of input clock transitions. This allows the PLL to lock before transitioning the `locked` signal high. You can use the Quartus II software to set the 20-bit counter value. The device resets and enables both the counter and the PLL simultaneously upon power-up and/or the assertion of the `pllenable` signal. To ensure correct lock circuit operation, and to ensure that the output clocks have the correct phase relationship with respect to the input clock, Altera recommends that the input clock be running before the Cyclone II device is configured.

Figure 7–9 shows the timing waveform for LOCKED and gated LOCKED signals.

Figure 7–9. Timing Waveform for LOCKED & Gated LOCKED Signals

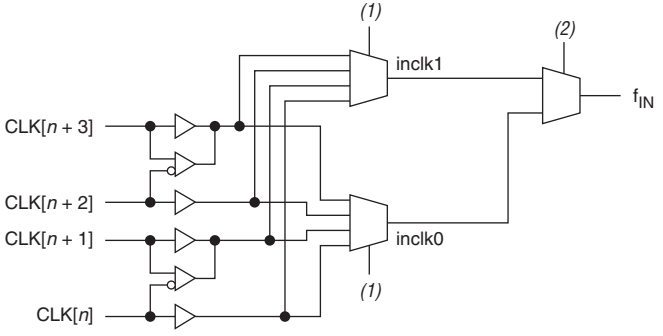


Manual Clock Switchover

The Cyclone II PLLs support manual switchover of the reference clock through internal logic. This enables you to switch between two reference input clocks. Use this feature for a dual clock domain application such as in a system that turns on the redundant clock if the primary clock stops running.

Figure 7–10 shows how the PLL input clock (f_{IN}) is generated from one of four possible clock sources. The first stage multiplexing consists of two dedicated multiplexers that generate two single-ended or two differential clocks from four dedicated clock pins. These clock signals are then multiplexed to generate f_{IN} by using another dedicated 2-to-1 multiplexer. The first stage multiplexers are controlled by configuration bit settings in the configuration file generated by the Quartus II software, while the second stage multiplexer is either controlled by the configuration bit settings or logic array signal to allow the f_{IN} to be controlled dynamically. This allows the implementation of a manual clock switchover circuit where the PLL reference clock can be switched during user mode for applications that requires clock redundancy.

Figure 7–10. Cyclone II PLL Input Clock Generation



Notes to Figure 7–10:

(1) This select line is set through the configuration file.

(2) This select line can either be set through the configuration file or it can be dynamically set in user mode when using the manual switchover feature.

PLL Specifications

See the *DC & Switching Characteristics* chapter in Volume 1 of the *Cyclone II Device Handbook* for information on PLL timing specifications.

Clocking

Cyclone II devices provide up to 16 dedicated clock pins (`CLK[15..0]`) that can drive the global clock networks. The smaller Cyclone II devices (EP2C5 and EP2C8 devices) support four dedicated clock pins on each side (left and right) capable of driving a total of eight global clock networks, while the larger devices (EP2C15 devices and larger) support four clock pins on all four sides of the device. These clock pins can drive a total of 16 global clock networks.

Table 7–7 shows the number of global clocks available across the Cyclone II family members.

Table 7–7. Number of Global Clocks Available in Cyclone II Devices

Device	Number of Global Clocks
EP2C5	8
EP2C8	8
EP2C15	16
EP2C20	16
EP2C35	16
EP2C50	16
EP2C70	16

Global Clock Network

Global clocks drive throughout the entire device, feeding all device quadrants. All resources within the device (IOEs, logic array blocks (LABs), dedicated multiplier blocks, and M4K memory blocks) can use the global clock networks as clock sources. These clock network resources can also be used for control signals, such as clock enables and synchronous or asynchronous clears fed by an external pin. Internal logic can also drive the global clock networks for internally generated global clocks and asynchronous clears, clock enables, or other control signals with high fan-out.

Table 7–8 shows the clock sources connectivity to the global clock networks.

Table 7–8. Global Clock Network Connections (Part 1 of 3)

Global Clock Network Clock Sources	Global Clock Networks															
	All Cyclone II Devices								EP2C15 through EP2C70 Devices Only							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
CLK0/LVDSCLK0p	✓		✓													
CLK1/LVDSCLK0n		✓	✓													
CLK2/LVDSCLK1p	✓			✓												
CLK3/LVDSCLK1n		✓		✓												
CLK4/LVDSCLK2p					✓		✓									
CLK5/LVDSCLK2n						✓	✓									
CLK6/LVDSCLK3p					✓			✓								
CLK7/LVDSCLK3n						✓		✓								
CLK8/LVDSCLK4n									✓		✓					
CLK9/LVDSCLK4p										✓	✓					
CLK10/LVDSCLK5n									✓			✓				
CLK11/LVDSCLK5p										✓		✓				
CLK12/LVDSCLK6n													✓		✓	
CLK13/LVDSCLK6p														✓	✓	
CLK14/LVDSCLK7n													✓			✓
CLK15/LVDSCLK7p														✓		✓
PLL1_c0	✓	✓		✓												
PLL1_c1	✓		✓	✓												
PLL1_c2		✓	✓													
PLL2_c0					✓	✓		✓								
PLL2_c1					✓		✓	✓								
PLL2_c2						✓	✓									
PLL3_c0									✓	✓		✓				
PLL3_c1									✓		✓	✓				
PLL3_c2										✓	✓					

Table 7–8. Global Clock Network Connections (Part 2 of 3)

Global Clock Network Clock Sources	Global Clock Networks															
	All Cyclone II Devices								EP2C15 through EP2C70 Devices Only							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
PLL4_c0													✓	✓		✓
PLL4_c1													✓		✓	✓
PLL4_c2														✓	✓	
DPCLK0 *(1)*	✓															
DPCLK1 *(1)*		✓														
DPCLK10 *(1)*, *(2)* CDPCLK0 or CDPCLK7 *(3)*			✓													
DPCLK2 *(1)*, *(2)* CDPCLK1 or CDPCLK2 *(3)*				✓												
DPCLK7 *(1)*					✓											
DPCLK6 *(1)*						✓										
DPCLK8 *(1)*, *(2)* CDPCLK5 or CDPCLK6 *(3)*							✓									
DPCLK4 *(1)*, *(2)* CDPCLK4 or CDPCLK3 *(3)*								✓								
DPCLK8 *(1)*									✓							
DPCLK11 *(1)*										✓						
DPCLK9 *(1)*											✓					
DPCLK10 *(1)*												✓				
DPCLK5 *(1)*													✓			
DPCLK2 *(1)*														✓		
DPCLK4 *(1)*															✓	

Table 7–8. Global Clock Network Connections (Part 3 of 3)

Global Clock Network Clock Sources	Global Clock Networks															
	All Cyclone II Devices								EP2C15 through EP2C70 Devices Only							
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
DPCLK3 *(1)*																✓

Notes to Table 7–8:
(1) See the *Cyclone II Architecture* chapter in Volume 1 of the *Cyclone II Device Handbook* for more information on DPCLK pins.
(2) This pin only applies to EP2C5 and EP2C8 devices.
(3) These pins only apply to EP2C15 devices and larger. Only one of the two CDPCLK pins can feed the clock control block. The other pin can be used as a regular I/O pin.

If the dedicated clock pins are not used to feed the global clock networks, they can be used as general-purpose input pins to feed the logic array using the MultiTrack interconnect. However, if they are used as general-purpose input pins, they do not have support for an I/O register and must use LE-based registers in place of an I/O register.

Clock Control Block

Every global clock network is driven by a clock control block residing either on the top, bottom, left, or right side of the Cyclone II device. The global clock network has been optimized for minimum clock skew and delay.

Table 7–9 lists the sources that can feed the clock control block, which in turn feeds the global clock networks.

Table 7–9. Clock Control Block Inputs (Part 1 of 2)

Input	Description
Dedicated clock inputs	Dedicated clock input pins can drive clocks or global signals, such as asynchronous clears, presets, or clock enables onto a given global clock network.
Dual-purpose clock (DPCLK and CDPCLK) I/O inputs	DPCLK and CDPCLK I/O pins are bidirectional dual function pins that can be used for high fan-out control signals, such as protocol signals, TRDY and IRDY signals for PCI, or DQS for DDR, via the global clock network.

Table 7–9. Clock Control Block Inputs (Part 2 of 2)

Input	Description
PLL outputs	The PLL counter outputs can drive the global clock network.
Internal logic	The global clock network can also be driven through the logic array routing to enable internal logic (LEs) to drive a high fan-out, low skew signal path.

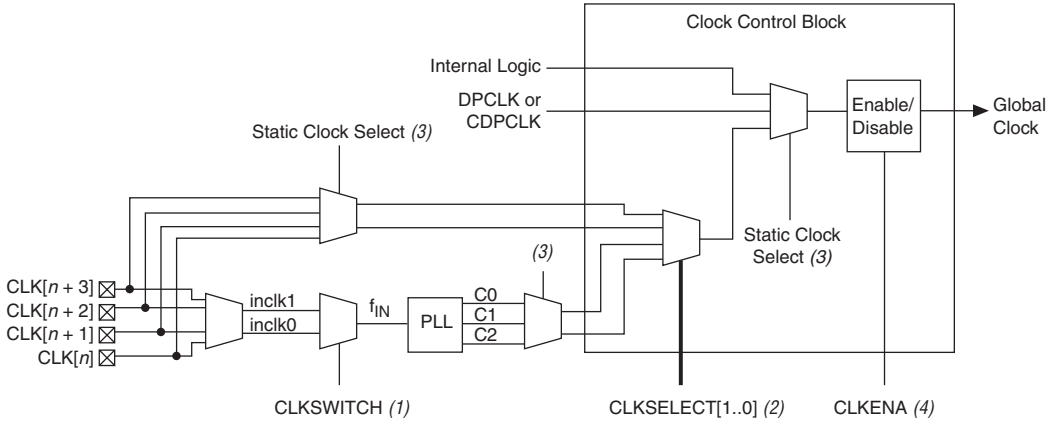
In Cyclone II devices, the dedicated clock input pins, PLL counter outputs, dual-purpose clock I/O inputs, and internal logic can all feed the clock control block for each global clock network. The output from the clock control block in turn feeds the corresponding global clock network. The clock control blocks are arranged on the device periphery and there are a maximum of 16 clock control blocks available per Cyclone II device.

The control block has two functions:

- Dynamic global clock network clock source selection
- Global clock network power-down (dynamic enable and disable)

Figure 7–11 shows the clock control block.

Figure 7–11. Clock Control Block



Notes to Figure 7–11:

(1) The CLKSWITCH signal can either be set through the configuration file or dynamically set when using the manual PLL switchover feature. The output of the multiplexer is the input reference clock (f_{IN}) for the PLL.

(2) The CLKSELECT[1..0] signals are fed by internal logic and can be used to dynamically select the clock source for the global clock network when the device is in user mode.

(3) The static clock select signals are set in the configuration file and cannot be dynamically controlled when the device is in user mode.

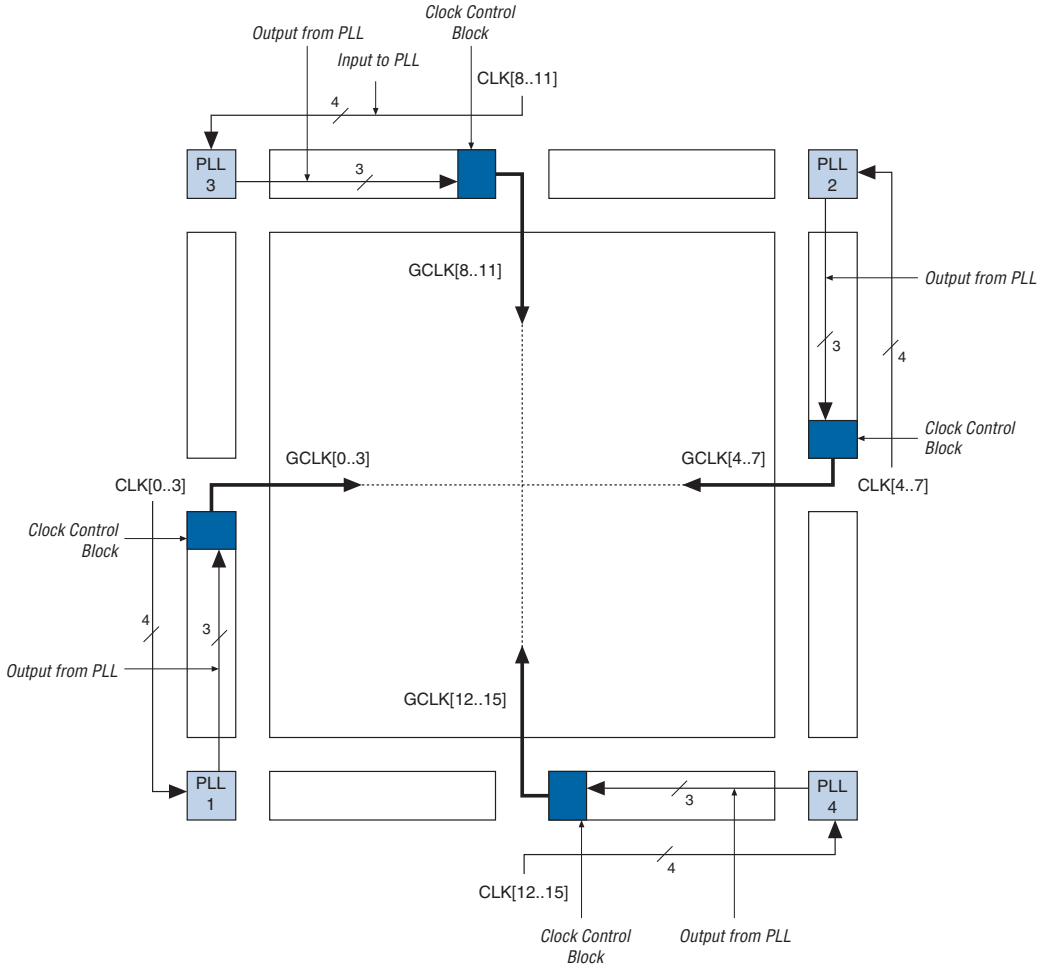
(4) Internal logic can be used to enable or disable the global clock network in user mode.

Each PLL generates three clock outputs through the c[1..0] and c2 counters. Two of these clocks can drive the global clock network through the clock control block.

Global Clock Network Clock Source Generation

There are a total of 8 clock control blocks on the smaller Cyclone II devices (EP2C5 and EP2C8 devices) and a total of 16 clock control blocks on the larger Cyclone II devices (EP2C15 devices and larger). Figure 7–12 shows the Cyclone II clock inputs and the clock control blocks placement.

Figure 7–12. Cyclone II Clock Control Blocks Placement



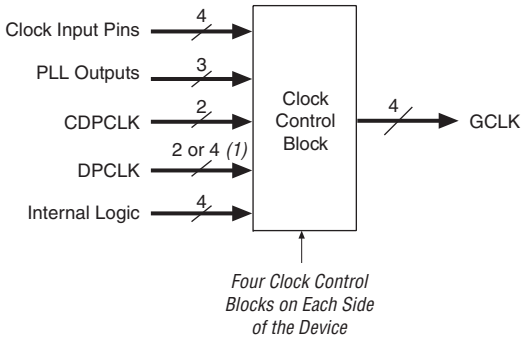
The inputs to the four clock control blocks on each side are chosen from among the following clock sources:

- Four clock input pins
- Three PLL counter outputs
- Two DPCLK pins and two CDPCLK pins from both the left and right sides and four DPCLK pins and two CDPCLK pins from both the top and bottom
- Four signals from internal logic

From the clock sources listed above, only two clock input pins, two PLL clock outputs, one DPCLK or CDPCLK pin, and one source from internal logic can drive into any given clock control blocks, as shown in Figure 7–11. Out of these six inputs to any clock control block, the two clock input pins and two PLL outputs can be dynamic selected to feed a global clock network. The clock control block supports static selection of the DPCLK or CDPCLK pin and the signal from internal logic.

Figure 7–13 shows the simplified version of the four clock control blocks on each side of the Cyclone II device periphery. The Cyclone II devices support up to 16 of these clock control blocks and this allows for up to a maximum of 16 global clocks in Cyclone II devices.

Figure 7–13. Clock Control Blocks on Each Side of the Cyclone II Device



Note to Figure 7–13:

(1) The left and right sides of the device have two DPCLK pins, and the top and bottom of the device have four DPCLK pins.

Global Clock Network Power Down

The Cyclone II global clock network can be disabled (powered down) by both static and dynamic approaches. When a clock network is powered down, all the logic fed by the clock network is in an off-state, thereby reducing the overall power consumption of the device.

The global clock networks that are not used are automatically powered down through configuration bit settings in the configuration file generated by the Quartus II software.

The dynamic clock enable or disable feature allows internal logic to synchronously control power up or down on the global clock networks in the Cyclone II device. This function is independent of the PLL and is applied directly on the clock network, as shown in Figure 7–11. The input

clock sources and the clkena signals for the global clock network multiplexers can be set through the Quartus II software using the altclkctrl megafunction.

clkena signals

In Cyclone II devices, the clkena signals are supported at the clock network level. Figure 7–14 shows how the clkena is implemented. This allows you to gate off the clock even when a PLL is not being used. Upon re-enabling the output clock, the PLL does not need a resynchronization or relock period because the clock is gated off at the clock network level. Also, the PLL can remain locked independent of the clkena signals since the loop-related counters are not affected.

Figure 7–14. clkena Implementation

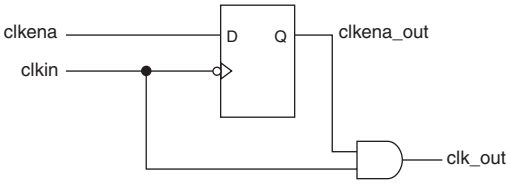
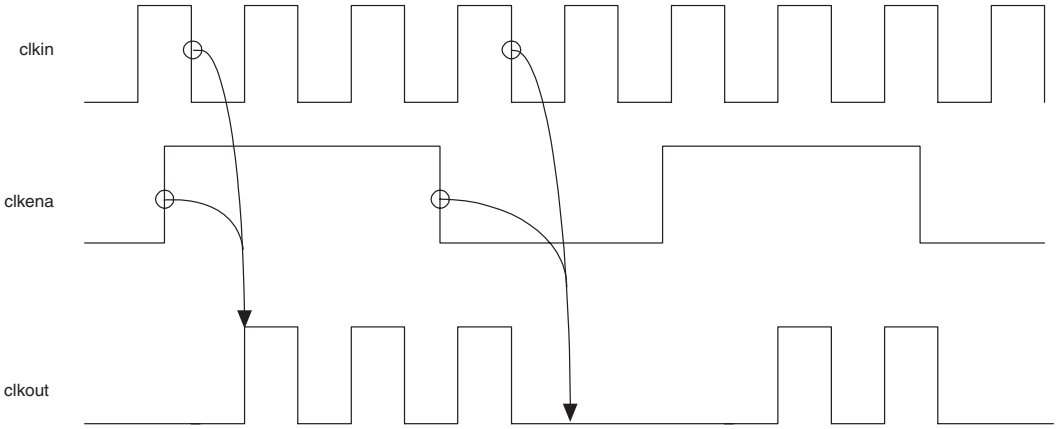


Figure 7–15 shows the waveform example for a clock output enable. clkena is synchronous to the falling edge of the clock (clkin).

This feature is useful for applications that require a low power or sleep mode. The exact amount of power saved when using this feature is pending device characterization.

Figure 7–15. clkena Implementation



The clkena signal can also disable clock outputs if the system is not tolerant to frequency overshoot during PLL resynchronization.

Altera recommends using the clkena signals when switching the clock source to the PLLs or the global clock network. The recommended sequence to be followed is:

1. Disable the primary output clock by de-asserting the clkena signal.
2. Switch to the secondary clock using the dynamic select signals of the clock control block.
3. Allow some clock cycles of the secondary clock to pass before re-asserting the clkena signal. The exact number of clock cycles you need to wait before enabling the secondary clock is design dependent. You can build custom logic to ensure glitch-free transition when switching between different clock sources.

Board Layout

The PLL circuits in Cyclone II devices contain analog components embedded in a digital device. These analog components have separate power and ground pins to minimize noise generated by the digital components.

VCCA & GNDA

Each Cyclone II PLL uses separate VCC and ground pin pairs for their analog circuitry. The analog circuit power and ground pin for each PLL is called VCCA_PLL<*PLL number*> and GNDA_ PLL<*PLL number*>. Connect

the VCCA power pin to a 1.2-V power supply, even if you do not use the PLL. Isolate the power connected to VCCA from the power to the rest of the Cyclone II device or any other digital device on the board. You can use one of three different methods of isolating the VCCA pin:

- Use separate VCCA power planes
- Use a partitioned VCCA island within the VCCINT plane
- Use thick VCCA traces

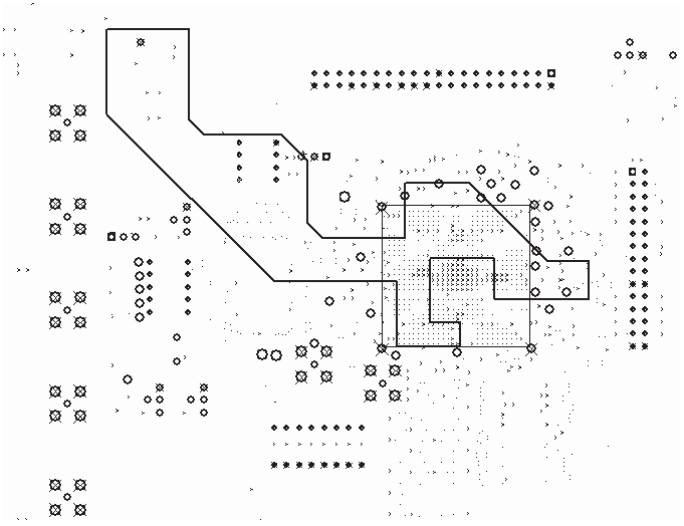
Separate VCCA Power Plane

A mixed signal system is already partitioned into analog and digital sections, each with its own power planes on the board. To isolate the VCCA pin using a separate VCCA power plane, connect the VCCA pin to the analog 1.2-V power plane.

Partitioned VCCA Island Within the VCCINT Plane

Fully digital systems do not have a separate analog power plane on the board. Since it is expensive to add new planes to the board, you can create islands for VCCA_PLL. Figure 7–16 shows an example board layout with an analog power island. The dielectric boundary that creates the island should be 25 mils thick. Figure 7–16 shows a partitioned plane within V_{CCINT} for VCCA.

Figure 7–16. V_{CCINT} Plane Partitioned for VCCA Island

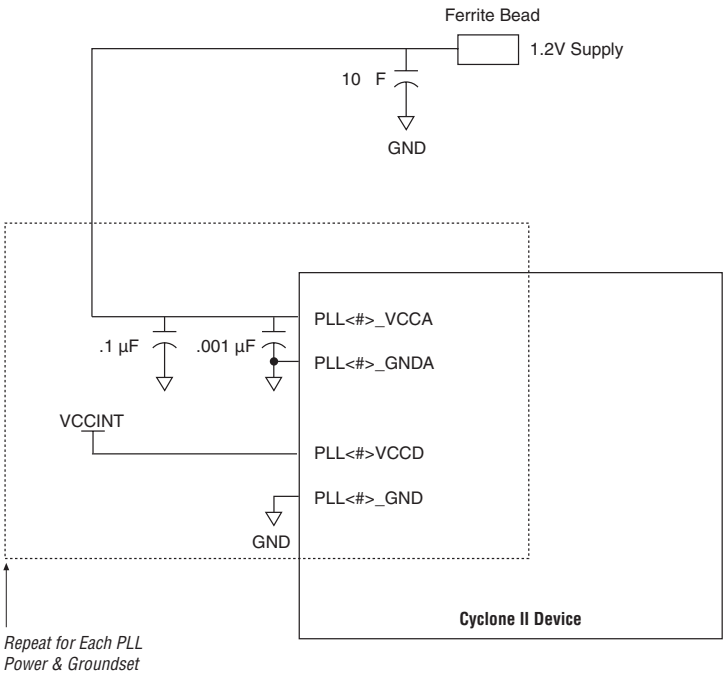


Thick VCCA Trace

Because of board constraints, you may not be able to partition a VCCA island. Instead, run a thick trace from the power supply to each VCCA pin. The traces should be at least 20 mils thick.

In each of these three cases, you should filter each VCCA pin with a decoupling circuit shown in Figure 7–17. Place a ferrite bead that exhibits high impedance at frequencies of 50 MHz or higher and a 10 µF tantalum parallel capacitor where the power enters the board. Decouple each VCCA pin with a 0.1 µF and 0.001 µF parallel combination of ceramic capacitors located as close as possible to the Cyclone II device. You can connect the GNDA pins directly to the same ground plane as the device's digital ground.

Figure 7–17. PLL Power Schematic for Cyclone II PLLs



Note to Figure 7–17:
(1) Applies to PLLs 1 through 4.

VCCD & GND

The digital power and ground pins are labeled VCCD_ PLL<*PLL number*> and GND_PLL<*PLL number*>. The VCCD pin supplies the power for the digital circuitry in the PLL. Connect these VCCD pins to the quietest digital supply on the board. In most systems, this is the digital 1.2-V supply supplied to the device's V_{CCINT} pins. Connect the VCCD pins to a power supply even if you do not use the PLL. When connecting the V_{CCD} pins to V_{CCINT}, you do not need any filtering or isolation. You can connect the GND pins directly to the same ground plane as the device's digital ground. See Figure 7–17.

Conclusion

Cyclone II device PLLs provide you with complete control of device clocks and system timing. These PLLs support clock multiplication/division, phase shift, and programmable duty cycle for your cost-sensitive clock synthesis applications.

In addition, the clock networks in the Cyclone II device support dynamic selection of the clock source and also support a power-down mode where clock networks that are not being used can easily be turned off, reducing the overall power consumption of the device.

Document Revision History

Table 7–10 shows the revision history for this document.

Table 7–10. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2007 v3.1	• Added document revision history. • Updated handpara note in "Introduction". • Updated *Note (3)* in Table 7–2. • Updated Figure 7–5. • Updated "Control Signals" section. • Updated "Thick VCCA Trace" section.	• Updated chapter with extended temperature information. • Updated `pllena` information in "Control Signals" section. • Corrected capacitor unit from10-F to 10 µF.
December 2005 v2.2	Updated industrial temperature range	
November 2005 v2.1	• Updated Figure 7–12. • Updated Figure 7–17.	
July 2005 v2.0	• Updated Table 7–6. • Updated "Hardware Features" section. • Updated "areset" section. • Updated Table 7–8. • Added "Board Layout" section.	
February 2005 v1.2	Updated information concerning signals. Added a note to Figures 7-9 through 7-13 regarding violating the setup or hold time on address registers.	
November, 2004 v1.1	Updated "Introduction" section.	
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	