Arria 10 Migration Guide
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Altera GPIO Megafuction
Altera OCT Megafuction
Altera LVDS SERDES Megafuction
ALTASMI_PARALLEL Megafuction
PFL Megafuction
SFL Megafuction

Document Revision History
This document describes the known issues only with the Altera Complete Design Suite (ACDS) version 13.1 Arria 10 edition. For the latest Altera IP migration information and exceptions, refer to the Introduction to Altera IP Cores and the Altera IP Release Notes, respectively.

**Note:** The directory structure, file names, module/entity naming conventions, and saved parameterization format for all IP variants in Arria 10 IP are preliminary and will change in Quartus® II software version 14.0. Altera recommends that you minimize hard-coded file paths, directory structure assumptions, or node entity/module names in Synopsys Design Constraints files (.sdc), scripts, and other infrastructure. Altera also recommends that you rely on the contents of generated report files and that you avoid editing generated IP files.

**Related Information**
- Introduction to Altera IP Cores
- Altera IP Release Notes

**Device Support for Arria 10 Devices**

The core speed grades shown in Arria 10 part names in the software are different from the device ordering codes. Refer to the Arria 10 device family documentation for the correct ordering codes and speed grades. When you migrate your design to Quartus II software Arria 10 Edition v13.1, change the device part number selection in the software.

The ACDS 13.1 Arria 10 software includes advance timing models. An advance model has the following characteristics:

- It is based on an advance version of silicon building blocks, before detailed block completion
- It is based on pre-silicon layout information with estimated routing locations and clocking structures
- It includes paths with no advance information, and Altera IP cores include false path assignments for some of the key affected paths
- It does not serve as an accurate predictor of absolute timing performance due to advance clock skew and timing delay information
- It is useful to understand the floor planning and pipelining needs of the design architecture
- It is scheduled to be replaced by a preliminary timing model in the following production release

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Because timing models for DSP, MLAB, & M20K blocks are based on advance information, the following false timing violations and incorrect timing reports are expected:

- **Digital Signal Processing (DSP)** — Timing violations within a single DSP instance or cascaded DSP configurations may be reported. These can be ignored.
- **M20K** — Not all paths in the M20K in ECC mode will be reported.
- **MLAB** — Timing violations within a single MLAB instance can be seen in some configurations. These violations should be ignored.

**Related Information**

IP Core Migration to Arria 10 Devices on page 1-3

For more information about support for specific Arria 10 IP cores

**Transceiver High-Speed Serial Interface Support**

Transceiver high-speed serial interface (HSSI) support has the following known issues:

- The Quartus II settings file (QSF) settings for $V_{CCR\_GXB}/V_{CCT\_GXB}$ transceiver voltages might create incorrect voltage settings in the pin report. The auto voltage assignment works correctly.
- Unused HSSI AUX block might not be powered down if all transceivers in that HSSI strip are powered down.
- If the data rate is less than 6 Gbps, mixed voltages are possible when a master CGB drives slave CGBs in different tiles. Mixed voltages are not supported for data rates less than 6 Gbps.
- If the QSF settings for $V_{CCR\_GXB}/V_{CCT\_GXB}$ voltages for transceiver channels results in invalid voltage settings for channels using xN routing (because these channels require a common voltage setting across the tiles connected by the xN routing), the placer incorrectly allows compilation to proceed instead of giving an error.
- The HSSI placer currently incorrectly places the `pin_perst` input for the upper left hard IP (HIP) at the pin labeled for the lower right HIP in the pin-out and vice versa.

**Related Information**

IP Core Migration to Arria 10 Devices on page 1-3

For more information about support for specific Arria 10 IP cores

**Clock Support**

Clock networks have a different structure in Arria 10 devices, compared to earlier Arria or Stratix® families. Arria 10 regional clocks drive the entire width of the chip, instead of half the width. Therefore, Dual-Regional clocks are no longer needed or supported. If a global signal assignment is made to route a signal on a Dual-Regional network, this beta software generates an internal error.

Arria 10 devices also include an additional clock network type, called a large periphery clock. However, those clock networks are not supported in the beta software. The option to target a large periphery clock is present in the Clock Control Block MegaWizard™, and in the assignment editor as an option for global signal assignments. Selecting this clock type results in an internal error in this release.

Some regional clocks are able to reach too many device blocks in this beta software. In the beta software, the regional clocks that physically reach the top quarter of the device are incorrectly connected to blocks in the entire top half of the chip. The regional clocks that physically reach the bottom quarter of the device are incorrectly connected to blocks in the entire bottom half of the device.
Device Support for Other Device Families

No device families other than Arria 10 FPGAs are supported in the Quartus II software Arria 10 Edition v13.1.

Quartus II Software Incremental Compilation

If the netlist type of a parent partition is Empty, registers in its child partition might not be timing analyzed if they feed only paths in the parent partition. Therefore, timing paths fully contained within the child partition might not have timing slacks reported if the paths terminate at a register that feeds only the parent partition. For core registers, you can work around this issue by adding another register as a branch of the child’s destination register. As long as the new register is preserved through compilation, the child’s destination register feeds a register within the child partition and the path is analyzed by TimeQuest.

TimeQuest Timing Analyzer

Timing analysis is not supported for the Arria 10 fPLL used as a core PLL. No paths, slacks, or constraints are reported in TimeQuest for fPLL usage in the core. Timing is analyzed for fPLLs used with the transceiver PHY (the primary usage for fPLLs) and for IOPLLs (Altera PLL) that feed the core.

If your design’s clock routing connectivity changes between compilations, the names of output clocks in the Altera PLL and Arria 10 FPLL megafuntion instances can change due to output clock rotation during the Fitter. Avoid making manual create_clock or create_generated_clock Synopsis Design Constraints Files (.sdc) constraints for PLL output clocks in the beta software. The derive_pll_clocks command ensures clocks are created successfully for any compile. However, variation in PLL names can cause other clock constraints like set_false_path, set_multicycle, and set_clock_groups to be missed or incorrectly applied to the wrong clock when recompiling in the beta software.

Timing paths to and from hard IP blocks, such as the HSSI, can have incorrect source or register destination names in timing reports. The endpoint in the hard IP block is reported with the name of the clock driving the register. In the detailed path report, the correct name of the source or destination endpoint is displayed as the register pin name immediately after or before the misnamed register.

Related Information
IP Core Migration to Arria 10 Devices on page 1-3
For simulation-related issues related to specific IP cores

IP Core Migration to Arria 10 Devices

To migrate a design to an Arria 10 device, some IP cores must be removed and replaced with a new variant for the Arria 10 device family. All IP cores which are incompatible with Arria 10 will be indicated in the IP-Upgrade display within the Quartus II software. You cannot compile your design with an invalid IP core.
Upgrading your IP core to a compatible version varies depending on the IP core. Some IP cores allow you to regenerate the existing parameterization for Arria 10, while others indicate that they must be removed and replaced with an appropriate IP core.

**Note:** This document applies only to migration in the Quartus II software version 13.1a. For the latest Altera IP migration information and exceptions, refer to the *Introduction to Altera IP Cores* and the *Altera IP Release Notes*, respectively.

**Related Information**
- *Introduction to Altera IP Cores*
- *Altera IP Release Notes*

**External Memory Interface (EMIF) IP Core**

The EMIF core has the following restrictions:
- The Cadence NCSIM and Aldec Riviera simulators are currently not supported for the EMIF example design simulation in this release.
- Simulation of multi-rank or multiple-CS memory interfaces is not supported in this release.
- Simulation of interfaces slower than 400 MHz is not supported in this release.
- RDIMM and LRDIMM configurations are not supported in this release.
- The I/O assignments that come with the IP in the .QIP file are not optimal and are preliminary.
- Arria 10 memory interfaces use a clock phase alignment circuitry to generate the core clock signals. However, this circuitry is not supported in this release, and core clocks are generated using PLL outputs.
- This release does not include all of the controller features that will be available in a future release.

**Altera PHYLite for Memory IP Core**

The Altera PHYLite for memory IP has the following restrictions:
- The Aldec RivieraPRO simulator is not supported for Altera PHYLite example design simulation in this release.
  - The ModelSim® SE simulator must compile the IP with the -novopt flag when the IP is generated in VHDL in this release. If using the example design, the provided `ld_debug` function can be used instead of `ld` in the `msim_setup.tcl` script.
- VHDL post-fit and post-map simulations are not supported in this release.
- The example design QSF is missing the following line required for the Fitter to pass in most configurations:
  ```
  set_instance_assignment -name IO_STANDARD "SSTL-15 CLASS I" -to ref_clk_clock_sink_clk
  ```
- Because Arria 10 device timing is based on advance information, you should remove non-optimized periphery paths from timing analysis. An example `.sdc` file is generated as part of the example design.

**Transceiver Native PHY IP Core**

Native PHY includes an extra `.sdc` file called `altera_xcvr_native_a10_b2.sdc` along with `altera_xcvr_native_a10_false_paths.sdc`. This `.sdc` is included to remove unintentional timing arcs inside the HSSI for this beta software.
You might observe HSSI-to-core timing violations on certain HSSI designs. Altera recommends waiving such timing violations in the beta software.

**PCI Express (PCIe) Hard IP Core**

Compiling a design with PCIe IP might result in the following Fitter error:


To avoid this error in the beta software, create a **quartus.ini** file in your project directory that includes the following line:

```
ipsta_disable_create_clock_NIGHTFURY_HSSI_GEN3_X8_PCIE_HIP_CORE_CLK_OUT=on
```

PCIe IP generates TimeQuest hold timing violations on the HIP.DFF to Core.LUTRAM path in the beta software. You can ignore these violations in the beta software.

There is a missing timing arc when instantiating global clock primitive. The PCIe design example uses the global clock primitive in `altpcied_sv_hwtcl.sv`, and this results in a missing timing path in the PCIe application. As a workaround, remove the instantiated global primitive and directly assign `pld_clk_hip` to `coreclkout_hip`.

To migrate a Stratix V design to an Arria 10 device, re-create the PCIe HIP with the new Arria 10 PCIe user interface and re-enter all of the HIP parameters. A Stratix V PCIe HIP project will NOT compile for Arria 10 if you do not create a new Arria 10 PCIe HIP variant.

**Altera LVDS SERDES IP Core**

Because Arria 10 device timing is based on advance information, you should remove non-optimized periphery paths from timing analysis. An example **.sdc** file is generated as part of the example design.

**Arria 10 1G/10GbE and 10GBASE-KR PHY IP Core**

You might observe timing violations in the PHY IP. Many of these violations are masked in the **beta2_131a10_ip.sdc** file delivered with the PHY-only design example, but not all of the paths are masked for all variants and fitter seeds.

**Triple Speed Ethernet IP Core**

The LVDS variants have the following issues:

- The link might not function correctly due to different LVDS bit ordering as compared to other device families. To work around this issue in the beta software, you can hand edit the generated file to reverse the bit ordering. The production version is scheduled to reverse the bit ordering to match earlier device families.
- The IP might generate a recovery timing failure in the altera_lvds instance due to an LVDS clocking issue.
- The `rx_divfwd_clk` clock pin is not constrained automatically, causing an error in timing analysis. To work around the issue, create a clock constraint for this pin.

For GXB variants, there is a missing clock constraint for the `ref_clk` that drives core logic and Native PHY IP. To work around the issue, create a clock constraint for this pin.
Interlaken 100G IP Core

The 12 lane 12G configurations might generate setup timing violations from the M20K ECC status signal to registers. You can ignore these violations in the beta software.

The 12 lane 12G configurations might generate setup timing violations between `pld_10g_tx_pempty` and `loose_ready_r`. You can ignore these violations in the beta software.

Qsys

When you open a Qsys system that targets a non-Arria 10 device, in rare circumstances, the Qsys user interface could become unresponsive upon loading Qsys systems. If this issue occurs, open the Qsys system `.qsys` file in a text editor and change the device family to Arria 10.

SoC Embedded Design Suite (EDS)

SoC EDS is not included in the beta release.

Nios® II EDS

No issues reported.

DSP Builder

No issues reported.

ModelSim-Altera

No issues reported.

Related Information

IP Core Migration to Arria 10 Devices on page 1-3
For simulation-related issues related to specific IP cores
These guidelines aid only in cross-family migration of existing Stratix V and Arria V designs to Arria 10 in Quartus II software Arria 10 Edition v13.1.

**Note:** For the latest Altera IP migration information and exceptions, refer to the *Introduction to Altera IP Cores* and the *Altera IP Release Notes*, respectively.

### Copying the Project for Arria 10

Copy your Stratix V or Arria V project into a new directory. This can be accomplished in one of the following ways:

- Using the archive feature in Quartus II
- Copying the project directory directly

If your Quartus II project references a central register transfer level (RTL), IP library, or other files outside of the project directory, the Quartus II archive feature should be used. Otherwise, you can copy and paste the directory.

**Note:** This step is optional; however, Altera recommends this as a best practice because referencing the Stratix V or Arria V project may be necessary.

### Archiving and Restoring your Stratix V or Arria V Project in Quartus II

1. Open your Stratix V or Arria V project in the latest Quartus II version in which the project was last updated.
2. Click **Project > Archive Project**.
3. Enter the project archive name and Click **Archive**.
   
   Note that the archive file appears in the current project directory.
4. Open the Quartus II software Arria 10 Edition v13.1, and click **Project > Restore Archived Projects**.
5. Select the Stratix V or Arria V project with the Quartus II Archive File (.qar) extension that you archived above.
6. Change the project destination folder to the Quartus II project directory, then click **OK** to restore.

**Caution:** Unarchiving projects created by previous Quartus II versions using Quartus II software Arria 10 Edition v13.1 can result in Quartus project database corruption. To avoid database corruption, you must immediately close and reopen the unarchived project before taking any further action.

### Copying your Stratix V or Arria V Project to a New Directory

You can copy and paste your project in either Windows or Linux.

**Table 2-1: Windows and Linux Copying and Pasting Procedure**

<table>
<thead>
<tr>
<th>Platform</th>
<th>Steps</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linux</td>
<td>At the command line, type <code>cp -R &lt;source_dir&gt;&lt;destination_dir&gt;</code> then press Enter.</td>
</tr>
<tr>
<td>Windows</td>
<td>1. Select the project folder.</td>
</tr>
<tr>
<td></td>
<td>2. Right-click on the folder and select <strong>Copy</strong>.</td>
</tr>
<tr>
<td></td>
<td>3. Right-click on the Arria 10 project directory, then click <strong>Paste</strong>.</td>
</tr>
</tbody>
</table>
Opening the Stratix V or Arria V Project in Quartus II Software Arria 10 Edition v13.1

After restoring the archived file or copying the directory, you can open up the project in Quartus II software Arria 10 Edition v13.1.

**Tip:** Do not unarchive projects created by a previous Quartus II release using Quartus II software Arria 10 Edition v13.1. This can result in Quartus project database corruption. If you must unarchive a project archived in a previous version of the Quartus II software, you must immediately close and reopen the unarchived project before taking any other action.

1. Click **File > Open Project**.
2. Select the Quartus project file (.qpf) from the Arria 10 project directory you created.
   When opening the restored or copied project for the first time, the system may generate the following message.

**Figure 2-3: Overwrite Database Warning**

![Picture of Overwrite Database Warning dialog box]

This message occurs if you copied over the entire directory with the /db (database) and /incremental_db (incremental database) directories. You do not need the old database files, and they should be overwritten. Click **Yes** to proceed.

Quartus II generates another warning that the family of devices your project is designed for is not available in Quartus II software Arria 10 Edition v13.1. The system uses the default Arria 10 family because older families are not supported.

**Figure 2-4: Remove All Location Assignments Warning**

![Picture of Remove All Location Assignments Warning dialog box]

You must remove all location assignments because the core, general purpose input/output (GPIO), and other IP components pin placement are different. You must also delete any non-pin location assignments. Click **Yes** to proceed.

3. Click **Close** on the **Upgrade IP Components** window.
Figure 2-5: Upgrade IP Components Window

This window displays the list of all IP components that need to be upgraded or regenerated. This process will be covered in a later section.

After you close this window, Quartus II displays a confirmation dialog box.

Figure 2-6: Closing the IP Components Upgrade Window Dialog Box

Click Yes to proceed.

4. Click Assignments > Device if you know the specific Arria 10 device you plan to use.
   If you need help determining which Arria 10 device to use, refer to the Arria 10 FPGAs Overview before proceeding to the next step.
5. Select the target device for your project, then click OK.
Removing Stratix V or Arria V IP Components from the Quartus II Project

Stratix V or Arria V IP components-related files are not needed in the Arria 10 project.

1. Click Project > Add/Remove Files in Project.
2. Select the Files category, then highlight all Quartus II IP Files (.qip) and Quartus II Simulation IP Files (.sip) from the file list of the associated IP to select them.
3. Click Remove.

Figure 2-7: Device Window

Figure 2-8: Add/Remove Files in Project Window
Note: This does not remove or delete files from the directory. It only removes them from being part of the project.

Leaving the Stratix V or Arria V IP files or directories does not affect the Arria 10 project. The newly generated IP has its own .qip and .sip files added to the project, which directs Quartus II to the proper files.

If you choose to delete the old IP files, you can remove the `<variant_name>`.* file and the following directories from the folder in which those IPs reside:

- `<variant_name>`
- `<variant_name>_sim`

Table 2-2: Windows and Linux Removing IP Files Procedure

<table>
<thead>
<tr>
<th>Platform</th>
<th>Steps</th>
</tr>
</thead>
<tbody>
<tr>
<td>Linux</td>
<td>At the command line, type <code>rm -R &lt;variant_name&gt;*</code> then press Enter.(^{(1)})</td>
</tr>
</tbody>
</table>
| Windows  | 1. Open Windows Explorer and navigate to the IP variation file location.  
2. Delete the `<variation_name>` (all file extensions).  
3. Delete the `<variation_name>` directory.  
4. Delete the `<variation_name>_sim` directory.  
5. Repeat the deletion for each Stratix V or Arria V series IP. |

Selecting and Configuring the Arria 10 IP Components that Require Manual Recreation

Some Arria 10 IP components are not compatible with the Stratix V or Arria V series IP components. To open or edit any of the Stratix V or Arria V series IP components, you need to use the Quartus II version that supports the older IP, or use Quartus II software version 13.1.

1. Open the MegaWizard Plug-In Manager in Quartus II software Arria 10 Edition v13.1 to select the IP component that best corresponds to the Stratix V or Arria V components you removed previously. For example, if the design had the **Stratix V Transceiver PLL v12.1** IP component, you must replace it with the **Arria10 Transceiver ATX PLL v13.1** and **Arria10 Transceiver CMU PLL v13.1** IP components.

\(^{(1)}\) Ensure that other files not associated with the IP do not begin with `<variant_name>`, otherwise they will be deleted as well.
2. Click **Next** to view the parameters and leave this window open.

3. Open the MegaWizard Plug-In Manager in Quartus II version 13.1 or earlier to open the Stratix V or Arria V IP instance.

4. Select **Edit an existing custom megafuction variation**, then click **Next**.
5. Navigate to the directory containing your Stratix V or Arria V design and select your Stratix V or Arria V IP component.
6. Click **Next** to view the Stratix V or Arria V parameters in parallel with the Arria 10 parameters.

7. Follow the IP-specific guidelines for the selected IP component in your Arria 10 design to replicate the parameters that best match your requirements and the corresponding Stratix V or Arria V design.

8. Click **Finish** to instantiate the Arria 10 IP component.

9. Repeat step 1 through step 8 for each IP in your design.
10. Verify that the instantiation of IP, its new name, and its port list is matched and properly connected to the rest of the RTL after regenerating all of the Arria 10 IP components.

11. Close any open Stratix V- or Arria V-compatible versions of the Quartus II software. You should only have Quartus II software Arria 10 Edition v13.1 open.

12. Click **Processing > Start Compilation** to recompile your design for the Arria 10 device.
This document provides guidelines for Qsys and MegaWizard™ designs that use Altera External Memory Interfaces IP from the Stratix V to Arria 10 device family using the Quartus II software.

**Stratix V Directly to Arria 10**

Do not attempt to compile a design targeted to a previous family.

The primitives used for UniPHY and earlier IPs are no longer supported in the Arria 10 device.

**Migrating to the Arria 10 External Memory IP**

1. Refer to the Arria 10 External Memory Interfaces (EMIF) IP documentation prior to regeneration because the Arria 10 EMIF IP is significantly different from the UniPHY IP.
2. Save a copy of the configuration you used in the previous IP as a baseline to generate the new Arria 10 EMIF IP.
3. Remove the Stratix V/Arria V UniPHY IP component related files before generating the new Arria 10 EMIF IP.
4. Follow either the MegaWizard steps or the Qsys steps to generate the new Arria 10 EMIF IP.
5. Modify your HDL to align with the IP port changes (MegaWizard flow).
6. Make the appropriate Qsys conduit connections to align with the IP port changes (Qsys flow).
7. Remove all previous Quartus Settings File (.qsf) assignments such as pins, termination, and so on.
8. Make the appropriate pinouts for the Arria 10 device.

**External Memory Interfaces IP User Interface**

Many of the planned features that are available in existing families are not yet offered in this initial release of Arria 10 External Memory Interfaces IP. They will be available in a future release of the IP.
Table 3-1: New Arria 10 External Memory Interfaces IP User Interface Elements

<table>
<thead>
<tr>
<th>User Interface Tab</th>
<th>Section</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>General</td>
<td>Configuration</td>
<td>Hard PHY and Hard Controller</td>
</tr>
<tr>
<td></td>
<td>Clocks</td>
<td>If needed, change your PLL reference clock frequency to one from the approved list of frequencies based upon your memory data rate.</td>
</tr>
<tr>
<td></td>
<td>I/O</td>
<td>I/O Standard and Input Termination (Rt)/Output Termination (Rs) values must match your board layout.</td>
</tr>
<tr>
<td>Memory Topology</td>
<td>Topology and Mode</td>
<td>Make sure the settings match the memory configuration.</td>
</tr>
<tr>
<td></td>
<td>Register Settings</td>
<td></td>
</tr>
<tr>
<td>Memory Timing</td>
<td>All</td>
<td>Consult with your memory manufacturer’s datasheet to determine new and required timing parameters such as, AC/DC levels, $t_{WLS}$, $t_{WLH}$, and so on.</td>
</tr>
<tr>
<td>Board Timing</td>
<td>Board and Package</td>
<td>Maximum delay difference between DIMMs/devices—the largest propagation delay on DQ signals between ranks. For example, in a two-rank configuration where DIMMs are placed in different slots, there is an extra propagation delay for DQ signals going to and coming back from the furthest DIMM compared to the nearest DIMM. This is a new parameter for Arria 10.</td>
</tr>
<tr>
<td></td>
<td>Skews</td>
<td></td>
</tr>
<tr>
<td>Controller</td>
<td>Efficiency</td>
<td>The following options were included in the previous EMIF IP:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Address Ordering</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Enable Reordering</td>
</tr>
<tr>
<td></td>
<td></td>
<td>• Starvation limit for each command</td>
</tr>
</tbody>
</table>

Generating the New Arria 10 EMIF IP Using the MegaWizard

1. If the Upgrade IP Cores dialog box is displayed, you can ignore and close it.
2. Save a copy of the configuration you used in the previous IP as a baseline to generate the new Arria 10 EMIF IP.
   This is either your variation file (.v) or you can open the variation file in a separate MegaWizard window as a visual aid for migration.
3. Click Project > Add/Remove Files in Project.
4. Remove the Stratix V/Arria V UniPHY IP components from the Files section by highlighting the .qip and .sip files from the file list of the associated IP and clicking Remove.
Generating the New Arria 10 EMIF IP Using Qsys

1. If the Upgrade IP Cores dialog box is displayed, you can ignore and close it.
2. Save a copy of the configuration you used in the previous IP as a baseline to generate the new Arria 10 EMIF IP.
   1. Open a separate Qsys window.
   2. Double-click on the instance of the UniPHY IP instance that you wish to migrate.
   3. Use this as your baseline.
3. Delete all files in your synthesized Qsys directory.
4. Click Tools > Qsys.
5. Click File > Open and select your .qsys file to open your Qsys system.
   If the Upgrade IPCores window opens, ignore and close it.
6. Click the Project Settings tab and set the Device family to Arria 10.
7. Right-click the External Memory Interfaces IP instance in Qsys and click Remove.
8. Under the Library tree, select Memories and Memory Controllers > External Memory Interfaces (Arria 10) > Arria 10 External Memory Interfaces, then click Add.
9. Set your configuration using your baseline and following External Memory Interfaces IP User Interface on page 3-1.
10. Click Finish to add this IP to your Qsys system.
11. Make the appropriate conduit connections in Qsys.
12. Click Generate > Generate.
13. In the Generation window, click Generate to generate your Qsys design.
14. Set the correct device, remove termination .qsf assignments and make the appropriate pinout changes to support your Arria 10 device.

Arria 10 EMIF IP Example Design

After IP generation is complete, the <variation_name>_example_design directory is created in your project directory. The example design includes a driver connected to a generated Arria 10 EMIF IP. The driver generates random traffic and internally checks the validity of the outgoing data.

Synthesizing the Arria 10 EMIF IP Example Design

1. Open the Nios II command shell and browse to the <variation_name>_example_design directory.
2. Type quartus_sh -t make_qii_design.tcl then press Enter to run the Quartus II design script.
3. Open the ed_synth.qpf example design project file.
4. Click Processing > Start Compilation.

Simulating the Arria 10 EMIF IP Example Design

1. Open the Nios II command shell and browse to the <variation_name>_example_design directory.
2. Type quartus_sh -t make_sim_design.tcl then press Enter to run the simulation design script.
   The script creates a simulation directory containing a subdirectory and corresponding script for each Altera-supported simulation tool.

Recompiling Your Arria 10 EMIF IP Design

To recompile your design for the Arria 10 device, click Processing > Start Compilation.

Stratix V to Arria 10 EMIF IP Migration Checklist

Table 3-2: Stratix V to Arria 10 EMIF IP Migration Checklist

<table>
<thead>
<tr>
<th>Item</th>
<th>Completed?</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td>Review External Memory Interfaces IP User Interface on page 3-1 prior to regeneration.</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>Save a copy of the old configuration as a baseline for the new IP.</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>Remove all files related to the previous IP in the project directory, or Delete all files in the synthesized directory of Qsys.</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>Follow either the MegaWizard or Qsys steps for migration.</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>Modify your HDL(MegaWizard) or Qsys conduit connections (Qsys) to align with the IP port changes.</td>
</tr>
<tr>
<td>Item</td>
<td>Completed?</td>
<td>Description</td>
</tr>
<tr>
<td>------</td>
<td>------------</td>
<td>-------------</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>Remove all previous <code>.qsf</code> assignments.</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>Make your new pin placements using the pin planner.</td>
</tr>
</tbody>
</table>
This document aids in migrating existing Stratix V and Arria V transceiver PHY IP designs to Arria 10 in Quartus II software Arria 10 Edition v13.1. In addition to migration instructions, this document also describes the design flow changes between Stratix V or Arria V transceiver PHY IPs and the Arria 10 family transceiver PHY IPs.

The 11 separate Stratix V and Arria V PHY IPs were consolidated into the following Arria 10 PHY IPs:

- Native PHY
- 1G/10GbE and 10GBASE-KR PHY
- XAUI PHY

Migration not covered in this document includes the following:

- Stratix V and Arria V GZ 1G/10GbE and 10GBASE-KR to Arria 10 1G/10GbE and 10GBASE-KR PHY IP
- Stratix V and Arria V XAUI PHY IP to Arria 10 XAUI PHY IP—Quartus II software Arria 10 Edition v13.1 does not support it

**Related Information**

- *Transceiver Architecture in Stratix V Devices*
- *Transceiver Architecture in Arria V Devices*
- *Arria 10 Transceiver PHY User Guide*

**Arria 10 and Stratix V / Arria V PHY IP Connection Differences**

The IP blocks show the separate MegaWizard-generated IPs that you connect together. The light green blocks indicate the connectivity change. The yellow block indicates where the PHY calibration is handled.
The TX PLL is now external to the PHY IP (this is an option in the V-series family). The Reconfiguration Controller IP for Stratix V and Arria V is no longer required because the calibration block is now a hard IP in the PHY.

Selecting the Corresponding Arria 10 PHY IP

When migrating to Arria 10, refer to this table to decide which PHY IP to select. If you select the Native PHY IP, this table helps you determine which transceiver configuration rule must be applied for your protocol or design.

Table 4-1: Map of Equivalent PHY IPs Between Stratix V, Arria V and Arria 10

Transceiver configuration rules were previously referred to as Protocol Modes in V-series IP.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>1G/10GbE and 10GBASE-KR PHY</td>
<td>Stratix V and Arria V GZ</td>
<td>Ethernet</td>
<td>• 1G/10GbE</td>
<td>N/A</td>
<td>Ethernet</td>
<td>• Backplane</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>• 10GBASE-KR PHY</td>
<td></td>
<td></td>
<td>• LineSide</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>• LineSide with 1588</td>
</tr>
</tbody>
</table>

\(^{(2)}\) The location in the MegaWizard is under the Interfaces category.
## Transferring the Main Transceiver Parameters

Arria 10 IP components are not compatible with the Stratix V or Arria V series IP components.

<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>XAUI PHY</td>
<td>Stratix V and Arria V (all variants)</td>
<td>Ethernet</td>
<td>XAUI PHY(3)</td>
<td>N/A</td>
<td>Ethernet</td>
<td>N/A</td>
</tr>
<tr>
<td>10GBASE-R</td>
<td>Stratix V and Arria V GZ/GT/ST</td>
<td>Ethernet</td>
<td>10G BASE-R</td>
<td>10G BASE-R 1588</td>
<td>10GBASE-R w/FEC</td>
<td>10G BASE-R 1588 10GBASE-R w/FEC</td>
</tr>
<tr>
<td>Interlaken PHY</td>
<td>Stratix V and Arria V GZ</td>
<td>Interlaken</td>
<td>Interlaken</td>
<td>Gen1 PIPE</td>
<td>PCle PIPE Gen2x1</td>
<td>Interlaken 10x12.5 Gbps 10x6.25 6x10.3 Gbps</td>
</tr>
<tr>
<td>PHY IP Core for PCI Express (PIPE)</td>
<td>Stratix V and Arria V (all variants)</td>
<td>PCI Express</td>
<td>Gen2 PIPE</td>
<td>Gen3 PIPE</td>
<td>PCle PIPE Gen2x8</td>
<td>PCIle PIPE Gen3x1 PCIle PIPE Gen3x8</td>
</tr>
<tr>
<td>Custom PHY</td>
<td>Stratix V and Arria V (all variants)</td>
<td>Transceiver PHY</td>
<td>Basic/Custom</td>
<td>GbE/GbE 1588</td>
<td>GIGE 1.25 Gbps</td>
<td>GIGE 1.25 Gbps w/ 1588</td>
</tr>
<tr>
<td>Low Latency PHY</td>
<td>Stratix V and Arria V GZ</td>
<td>Transceiver PHY</td>
<td>Basic/Custom</td>
<td>CPRI (Standard PCS)</td>
<td>Low Latency Standard PCS</td>
<td>Low Latency Enhanced PCS</td>
</tr>
<tr>
<td>Stratix V Transceiver Native PHY</td>
<td>Stratix V</td>
<td>Transceiver PHY</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Arria V GZ Transceiver Native PHY</td>
<td>Arria V GZ</td>
<td>Transceiver PHY</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>Arria V Transceiver Native PHY (5)</td>
<td>Arria V GX/GT/SX/ST</td>
<td>Transceiver PHY</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

---

### Notes:

1. **The location in the MegaWizard is under the Interfaces category.**
2. **The Arria 10 XAUI PHY IP will be released in a future version of the Quartus II software.**
3. **In Arria VGT, you implement 9.8304 Gbps CPRI using the Arria V Transceiver Native PHY (PMA direct) with soft PCS by user logic. When migrated to Arria 10, you can select the presets available for CPRI 9.8 Gbps for this implementation.**
4. **Use the Transceiver Reconfiguration Rules to configure CPRI applications from 1228.8 Mbps up to 6144 Mbps. For 9.8304 Gbps applications, you can select the presets.**

---

**Migrating Stratix V and Arria V Transceiver PHY IP to Arria 10**

Altera Corporation
To open or edit any of the Stratix V or Arria V series IP components, you need to use the Quartus II version that supports the older IP, or use Quartus II software version 13.1.

Transferring parameters from Stratix V or Arria V designs to Arria 10 designs is accomplished by opening Quartus II software Arria 10 Edition v13.1 in parallel with a Stratix V or Arria V-compatible version of the Quartus II software and matching the parameter values manually.

The main transceiver parameters are to transfer are:

- Lane data rate
- Input PLL reference clock frequency (for clock data recover (CDR) and Transmit PLL)
- The number of data channels or transceiver lanes
- Transmit PLL type
- Channel bonding

2. Click Tools > MegaWizard Plug-In Manager.
3. Select Create a new custom megafunciton variation, then click Next.
4. Select Arria 10 device family.
5. Select Interfaces > Transceiver PHY > Arria 10 Native PHY IP in the Installed Plug-Ins tree.
6. Under Which type of output file do you want to create?, select Verilog or VHDL as the hardware description language.
7. In What name do you want for the output file?, browse to the location where you want to save your design, and enter a filename.
8. Click Next.
9. Set the values for the main transceiver parameters to match your Stratix V or Arria V design.

Figure 4-3: Location of the Main Transceiver Parameters in Arria 10
Related Information

For complete descriptions of the ports and parameters, refer to the Implementing Protocols in Arria 10 Transceivers chapter of the Arria 10 Transceiver PHY User Guide

Protocol Presets

Protocol presets are a powerful design tool component that give you a valid transceiver design and helps you learn the legal settings for creating your own transceiver design. Altera recommends that you take advantage of this feature in the Arria 10 transceiver PHY IPs. The protocol presets are located in the right pane of the Arria 10 Transceiver Native PHY MegaWizard window.

To set the Arria 10 Transceiver Native PHY parameters, select a preset which automatically sets all the valid configurations for the Native PHY and selects the appropriate transceiver configuration rule.

Datapath Options (Transceiver Configuration Rules and Main Parameters Transfer)

If you choose not use a protocol preset, then you must select the appropriate transceiver configuration rules under Datapath Options of the Arria 10 Transceiver Native PHY. Refer to Table 4-1 to select the appropriate transceiver configuration rules for your design. Once you select a transceiver configuration rule option, either the Standard PCS or Enhanced PCS tab appears. In Quartus II software Arria 10 Edition v13.1, the enhanced PCS replaces the 10G PCS in Stratix V and Arria V GZ designs. Arria V GT/ST devices do not support Enhanced PCS, and 10G applications are implemented using soft PCS, for example, 9.8304 Gbps CPRI applications.

The transceiver configuration rules do not automatically set the Arria 10 Native PHY IP parameters for that protocol mode. By default, the Message level rule for violations is set to error. Any invalid setting that violates the transceiver configuration rules causes an error message to appear in the message box at the bottom of the Arria 10 Transceiver Native PHY window. Errors prevent you from instantiating the IP. The error messages describe what action is needed to correct the error and permit instantiation of the IP.

Match the Transceiver mode settings in the Arria 10 Transceiver Native PHY with the Duplex/Simplex mode setting in your Stratix V or Arria V PHY IP. Match the Number of data channels and the Data rate settings in the Arria 10 Transceiver Native PHY with the Transceiver lanes and Transceiver lane datarate in Mbps settings in your Stratix V or Arria V PHY IP.

PCS Reconfiguration and Simplified Data Interface

If you are planning to perform PCS reconfiguration, select the Enable reconfiguration between Standard and Enhanced PCS datapaths option. Leave the Enable simplified data interface unselected. You must also determine the precise parallel data path interface mapping. You must to refer to the Transceiver Native PHY section of the Arria 10 Transceiver PHY User Guide for the precise parallel data path interface mapping, and remap the Stratix V and Arria V GZ PHY IP parallel data interface ports. Enhanced PCS datapath is not supported in Arria V GX/GT/SX/ST, so the Enable reconfiguration between Standard and Enhanced PCS datapaths option is not applicable.

If you are not planning to perform PCS reconfiguration, Altera recommends that you select the Enable simplified data interface option. This limits the number of transmit and receive parallel data paths to only the specific data paths required for the transceiver configuration rule selected. Unnecessary data paths appear as unused transmit and receive parallel data. You must tie all unused transmit parallel data input ports to Logic 0. The unused receive parallel data output ports can be left unconnected. If you do not use the simplified data interface, then you must determine the precise parallel data path interface mapping
The Arria 10 Transceiver Native PHY transmit and receive parallel data path interface does not have the identical mapping as the Stratix V and Arria V Transceiver Native PHY IP. If you are migrating from a Stratix V or Arria V Transceiver Native PHY, you must determine the parallel data path interface mapping.

**Related Information**
Refer to the Transceiver Native PHY IP Overview section of the *Arria 10 Transceiver PHY User Guide* for precise parallel data path interface mapping.

### Setting the TX PMA Tab Options

1. Select **Not bonded** if you are using the non-bonded configurations using the x1 clock network or xN clock network (xN non-bonded).
2. Select **PMA bonding** for Arria 10 designs because this matches the Stratix V and Arria V usage. Arria V GX/GT/SX/ST support x6 and xN bonding modes only while Stratix V and Arria V GZ use x6, xN, and feedback compensation transmit bonding.
3. Select **PMA/PCS bonding** if you are bonding both the PMA and the PCS.
   - This type of PMA and PCS bonding is required for the SFI-S, 40GBASE-KR, and PCIe transceiver configuration rules, which use the PCS control plane bonding to align the TX FIFOs. This type of PMA and PCS bonding is optional for the Interlaken, CPRI, and Basic transceiver configuration rules. You must also specify the type of PMA bonding employed in the Transceiver Transmit PLL IP.

### Figure 4-4: Transmit Channel Bonding Options

<table>
<thead>
<tr>
<th>TX PMA</th>
<th>RX PMA</th>
<th>Standard PCS</th>
<th>Dynamic Reconfiguration</th>
<th>Generation Options</th>
</tr>
</thead>
<tbody>
<tr>
<td>TX Bonding Options</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TX channel bonding mode:</td>
<td>Not bonded</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PCS TX channel bonding master:</td>
<td>Not bonded</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Actual PCS TX channel bonding master:</td>
<td>PMA/PCS bonding</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

The **PMA/PCS bonding** option allows you to automatically or manually select a transmit PCS channel bonding master. The **Auto** option selects the center channel of your bonded channel group. Use the **Manual** option to select a different PCS channel bonding master because the channel generating your tx_clkout / rx_clkout source to your IP from your bonded channel group may not be the channel selected by the **Auto** option.

4. Copy and enter the **TX PLL Options** from your Stratix V or Arria V design into your Arria 10 design. This sets up the local clock generation block (CGB) on the transceiver channels.

### Setting the RX PMA Tab Options

Copy and enter the **RX PMA** options from your Stratix V or Arria V design into your Arria 10 design.

### Setting the Standard PCS, Enhanced PCS, Dynamic Reconfiguration, and General Options

You should copy and enter most of the options from the **Standard PCS**, **Enhanced PCS** (10G PCS in Stratix V or Arria V GZ Native PHY), **Dynamic Reconfiguration**, and **General Options** tabs of your Stratix V or Arria V design into your Arria 10 design.
**Arria 10 Transmit PLL IP**

The transmit PLL use models in Stratix V and Arria V PHY IPs are:

- Internal Transmit PLL (Inside the PHY IP)—All PHY IPs
- External Transmit PLL (Outside the PHY IP)—Option for Transceiver Native PHY Only

Arria 10 PHY IPs use external transmit PLLs exclusively. The transceiver transmit PLLs are:

- ATX PLL
- fPLL
- CMU PLL

---

**Figure 4-5: Arria 10 Transceiver Transmit PLLs and Associated Megafunctions**

These Megafunctions are located in the **PLL** section of the MegaWizard Plug-In Manager.

---

**Recommended PLL Migration Guideline**

Whether you are using internal or external transmit PLLs in your Stratix V and Arria V PHY IPs, the following table helps you determine the recommended transmit PLL migration selections to the Arria 10 family.
The largest Arria 10 device has 32 ATX PLLs. If you require more than 32, priority for ATX PLL usage should be given to the designs with the highest data rates. For Stratix V and Arria V designs using the CMU PLL or fPLL as transmit PLL where an Arria 10 ATX PLL is not available or have been maximized, you should use the Arria 10 fPLL. The Arria 10 fPLL has enhanced capabilities and is functionally equivalent to the Stratix V and Arria V GZ CMU PLL.

For all bonded clocking designs up to 12.5 Gbps or xN non-bonded clocking configurations, the Arria 10 fPLL is the only viable alternative to the Arria 10 ATX PLL.

### Configuring the Transmit PLL

2. Click **Tools > MegaWizard Plug-In Manager**.
3. Select **Create a new custom megafuntion variation**, then click **Next**.
4. Select **Arria 10 device family**.
5. Select **PLL > Arria 10 Transceiver ATX PLL** in the **Installed Plug-Ins** tree.
6. Under **Which type of output file do you want to create?**, select Verilog or VHDL as the hardware description language.
7. In **What name do you want for the output file?**, browse to the location where you want to save your design, and enter a filename.
8. Click **Next**.
9. Select the appropriate setting in the **Protocol mode** list in the **General** section of the **PLL** tab (ATX and CMU PLL only).
   - If you are migrating a PCIe design, select the appropriate **PCle Gen 1**, **PCie Gen 2**, or **PCie Gen 3** option. Select **Basic** for all other designs.

---

(8) Only the Channel PLL from Channel 1 or Channel 4 of the transceiver bank can be reconfigured as a CMU PLL. The maximum number of non-bonded channels is limited to 5, and they must all be co-located in the same transceiver bank.

(7) The Arria 10 fPLL supports a maximum data rate of 12.5 Gpbs. The CMU PLL supports a maximum data rate of 17.4 Gbps.

(6) Not supported in Arria V GX/GT/SX/ST devices.
The CMU PLL can only be used in Basic protocol mode.

**Note:** The CMU PLL can only be used in Basic protocol mode.

**Figure 4-6: PLL General Options**

<table>
<thead>
<tr>
<th>PLL</th>
<th>Master Clock Generation Block</th>
<th>Dynamic Reconfiguration</th>
<th>PLL Options</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>General</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Message level for rate variations:</td>
<td>High</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Device speed grade:</td>
<td>High Speed</td>
<td>Low Speed</td>
<td></td>
</tr>
<tr>
<td>Protocol mode:</td>
<td>Basic</td>
<td>High Speed</td>
<td></td>
</tr>
<tr>
<td>Bandwidth:</td>
<td>Low</td>
<td>High</td>
<td></td>
</tr>
<tr>
<td>Number of PLL reference clocks:</td>
<td>1</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>Selected reference clock source:</td>
<td>1</td>
<td>2</td>
<td></td>
</tr>
</tbody>
</table>

10. Select **low** from the **Bandwidth** list.
   This is the default setting and should be used unless you require higher bandwidth.

11. For ATX PLL only with data rates above 17.4 Gbps, select **GT clock output buffer** from the **Primary PLL clock output buffer** list and select the **Enable PLL GT clock output port** option. For all other data rates, select the **GX clock output buffer**. Enabled PLL GX clock output port is selected by default.

   For ATX and fPLL only, if you are migrating a PCIe design, you must select the **Enable PCIe clock output port** option. For rate switching purposes, the Arria 10 fPLL generating Gen1 and Gen2 data rates needs to output the **pll_pcie_clk** port for the clock.

12. Set the **PLL output frequency** to half the desired data rate.
   For example, a 5 Gbps data rate requires a PLL output frequency of 2500 MHz.

   **Note:** The Arria 10 fPLL output frequency can only be used as either a transceiver PLL or a core PLL, but not both at the same time.

13. Select the lane or channel data rate of your transceiver design from the **PLL reference clock frequency** list. The PLLs internal counters are automatically configured and updated.

14. Click the **Master Clock Generation Block** (MCGB) tab.
15. Configure the MCGB if you are migrating transceiver channel designs that are bonded or are non-bonded using the xN clock network.
   a. Select the **Include Master Clock Generation Block** option to enable the MCGB.
   b. Select the appropriate **Clock division factor** for your MCGB output data rate.
   c. Select the **Enable x6/xN non-bonded high-speed clock output port** option for xN non-bonded configurations or deselect it for xN bonded configurations.
   d. For PCIe Gen2 and Gen3, enable the clock switch input port, `pcie_sw[1:0]`, by selecting the **Enable PCIe clock switch interface** option.

16. Configure the Bonding options.
   a. Select the **Enable bonding clock output ports** option for designs using the x6/xN and feedback compensation bonding.
   b. Select the **Enable feedback compensation bonding** option for designs using feedback compensation bonding. This enables the bonded clock output group `tx_bonding_clocks[5:0]` that the transceiver PHY requires.
   c. Select the appropriate PMA interface width setting for your design that matches the Standard PCS/Enhanced PCS-PMA interface width on the Arria 10 Transceiver PHY IP.
Reusing and Regenerating the Transceiver Reset Controller

Arria 10 devices do not use the embedded reset controller or the Avalon Memory Mapped (Avalon-MM) interface for the reset registers, so the designs that use them must be modified. The Arria 10 transceiver reset sequence is currently the same as Stratix V and Arria V reset sequences. There is currently no change to the reset logic, whether it is using the Altera Transceiver PHY Reset Controller IP, or your own reset logic.

The Altera Transceiver Reset Controller IP or any custom user reset sequence logic from Stratix V and Arria V transceiver designs that use the **Standard Transceiver Reset Ports** can be re-used for Arria 10 designs. If the Altera Transceiver Reset Controller IP is used, ensure it is regenerated in Quartus II software Arria 10 Edition v13.1 so that the latest code updates are generated.

Table 4-2: Stratix V and Arria V Transceiver PHY IP Reset Controller Types, Registers, and Ports

<table>
<thead>
<tr>
<th>Stratix V and Arria V Transceiver PHY IP</th>
<th>Embedded Reset Controller</th>
<th>Avalon-MM Reset Register</th>
<th>Standard Transceiver Reset Ports (tx_analogreset, rx_analogreset, tx_digitalreset, rx_digitalreset)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Transceiver Native PHY</td>
<td>N/A</td>
<td>N/A</td>
<td>Yes</td>
</tr>
<tr>
<td>Custom PHY</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Deterministic Latency PHY</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Low Latency PHY(9)</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>PHY IP Core for PCI Express (PIPE)</td>
<td>Yes</td>
<td>Yes</td>
<td>N/A</td>
</tr>
</tbody>
</table>

(9) Stratix V and Arria V GZ variant only.
Related Information

For details about the reset controller, refer to the Resetting Transceiver Channels chapter of the *Arria 10 Transceiver PHY User Guide*

### Instantiating a New Reset Controller

If you are using the embedded reset controller or the Avalon-MM interface to the reset registers in the Stratix V and Arria V PHY IPs, you must instantiate a new Altera Transceiver PHY Reset Controller IP.

If you are using the embedded reset controller, create an instance of the Altera Transceiver PHY Reset Controller IP to replace it. The same functionality can be maintained with the use of the Altera Transceiver PHY Reset Controller IP.

2. Click *Tools > MegaWizard Plug-In Manager*.
3. Select *Create a new custom megafunction variation*, then click *Next*.
4. Select *Arria 10* device family.
5. Select *Interfaces > Transceiver PHY > Transceiver PHY Reset Controller* in the *Installed Plug-Ins* tree.
6. Under *Which type of output file do you want to create?*, select Verilog or VHDL as the hardware description language.
7. In *What name do you want for the output file?*, browse to the location where you want to save your design, and enter a filename.
8. Click *Next*.

### Table 4-3: Reset Controller Port Mapping from Stratix V and Arria V to Arria 10

<table>
<thead>
<tr>
<th>Stratix V and Arria V PHY IP</th>
<th>Embedded Reset Controller</th>
<th>Avalon-MM Reset Register</th>
<th>Standard Transceiver Reset Ports (tx_analogreset, rx_analogreset, tx_digitalreset, rx_digitalreset)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interlaken PHY (9)</td>
<td>Yes</td>
<td>Yes</td>
<td>N/A</td>
</tr>
<tr>
<td>10GBASE-R PHY (10)</td>
<td>Yes</td>
<td>Yes</td>
<td>N/A</td>
</tr>
<tr>
<td>XAUI PHY</td>
<td>Yes</td>
<td>Yes</td>
<td>N/A</td>
</tr>
</tbody>
</table>

---

(10) Stratix V and Arria V GZ/GT/ST variants only.
You can use the same source used for `phy_mgmt_clk` for the Transceiver PHY Reset Controller clock input when migrating from the Embedded Reset Controller.

9. Duplicate the settings from your Stratix V or Arria V design to the Arria 10 Transceiver PHY Reset Controller, then click **Finish** to instantiate the new IP.

**Related Information**

For details about resetting transceiver channels, refer to the Resetting Transceiver Channels chapter of the *Arria 10 Transceiver PHY User Guide*.

### Arria 10 Transceiver Dynamic Reconfiguration Flow

The transceiver reconfiguration controller is no longer a requirement in Arria 10 designs. In Stratix V and Arria V families, the reconfiguration controller performs the calibration of the transceiver analog circuitry and provides an Avalon-MM interface for the reconfiguration of the transceiver PCS and PMA blocks. Arria 10 includes a hardened calibration logic as well as individual Avalon-MM interfaces to the PLL and each transceiver channel to perform PLL and channel PCS and PMA reconfiguration. If you have dynamic PLL reconfiguration requirements, channel reconfiguration requirements, or both, you must create an Avalon Master that is compliant to the Avalon Interface to perform dynamic reconfiguration. Use the Avalon Master to execute the reconfiguration files generated under the **Dynamic Reconfiguration** tab of the transceiver PHY IP, the transceiver PLL IP, or both to perform the reconfiguration.

**Related Information**

Refer to the Reconfiguration Interface and Dynamic Reconfiguration chapter of the *Arria 10 Transceiver PHY User Guide* for more information.
Completing the Migration Design

1. Connect the Arria 10 transceiver PHY, the transceiver transmit PLL, and the reset controller (transceiver reset controller IP or user reset controller logic) instances together. A new Avalon Master block is needed if you want to use PMA/PCS and PLL dynamic reconfiguration.

2. Connect the Data Generator and Data Analyzer IP blocks to the Transceiver PHY IP and Transceiver PHY Reset Controller IP instances.

   **Note:** The Data Generator and Analyzer block are generic terms and can be any user logic or IP, such as the MAC, Frame, or Packet Generators.

3. Compile the design and verify correct functionality once you have connected all of the fundamental building blocks.

**Figure 4-10: Arria 10 Transceiver PHY IP Design Flow**

<table>
<thead>
<tr>
<th>Instantiate the Transceiver PHY Reset Controller IP</th>
<th>Instantiate the Transceiver PHY IP</th>
<th>Instantiate Transmit PLL IP</th>
<th>Create an Avalon Master (optional)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Configure the Reset Sequence</td>
<td>Configure the transceiver</td>
<td>Select clocking options and configure the Master CGB</td>
<td></td>
</tr>
<tr>
<td>Generate Reset Controller Instance</td>
<td>Generate the PHY Instance</td>
<td>Generate Transmit PLL Instance</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Connect the IPs together</td>
<td>Compile and Verify Functionality</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Arria 10 Top Level Transceiver Design**

Your migrated Arria 10 transceiver design should look similar to the diagram below, which includes the high level port connections between PHY IP and component blocks that comprise the Arria 10 transceiver design.
Figure 4-11: Arria 10 Transceiver Design Flow and Basic Building Blocks

Blocks in blue shading are Altera MegaWizard-generated IP blocks.
This document describes how to migrate a 100G Interlaken design from Stratix V devices on Quartus II software version 13.0 to the Arria 10 device family on Quartus II software Arria 10 edition v13.1.

Removing the Stratix V Transceiver Reconfiguration Controller

The 100G Interlaken IP core for Stratix V devices requires an external transceiver reconfiguration controller. However, the 100G Interlaken IP core in an Arria 10 device includes a reconfiguration controller block and does not require an external transceiver reconfiguration controller. In Arria 10 devices, any of the PMA/PCS DPRIO registers can be configured flexibly through an Avalon-MM Arria 10 transceiver reconfiguration interface.

1. Open your existing Stratix V 100G Interlaken project with the Quartus II software Arria 10 Edition v13.1.
2. Click the IP Components tab in the Project Navigator pane and remove the Reconfiguration Controller.

Generating an Arria 10 PLL

The transceiver PLL is included in the 100G Interlaken IP core for Stratix V devices. The 100G Interlaken IP core in Arria 10 devices requires an external PLL to drive the transceiver channels.

2. Click Tools > MegaWizard Plug-In Manager.
3. Select Create a new custom megafunction variation, then click Next.
4. Select Arria 10 device family.
5. Select PLL > Arria 10 Transceiver ATX PLL in the Installed Plug-Ins tree.
6. Under Which type of output file do you want to create?, select Verilog or VHDL as the hardware description language.
7. In What name do you want for the output file?, browse to the location where you want to save your design, and enter a filename.
8. Click Next.
9. Set the PLL output frequency to one half the per-lane data rate of the 100G Interlaken IP core.
Set the PLL reference clock frequency to the value of the 100G Interlaken MegaCore function PLL Transceiver reference clock frequency parameter.

Upgrading the 100G Interlaken MegaCore Function to the Arria 10 Version

2. Click Tools > MegaWizard Plug-In Manager.
3. Select Edit an existing custom megafuction variation, then click Next.
4. Select the existing megafuction variation file (.v/.vhdl/.vhd) for the 100G Interlaken IP core, then click Next.
5. Set the parameters for the Arria 10 100G Interlaken IP core.
Table 5-1: New Arria 10 100G Interlaken MegaCore Function Parameters

<table>
<thead>
<tr>
<th>Arria 10 100G Interlaken Options</th>
<th>Description</th>
</tr>
</thead>
</table>
| Transceiver reference clock frequency | This is the reference frequency for the Clock Recovery Unit (CRU).  
**Note:** In most designs, this reference frequency has the same source as the one driving the external PLL reference clock. |
| Include advanced error reporting and handling | Enables advanced error checking and reporting. If enabled, the following errors are reported on the irx_err:
  - CRC24 errors
  - Loss of lane alignment
  - Illegal control word
  - Illegal framing pattern
  - Missing SOP or EOP indicator |
| Enable M20K ECC support | Specifies whether the 100G Interlaken MegaCore function variation supports the ECC feature in the M20K memory blocks that are configured as part of the IP core. |
The Arria 10 Interlaken IP core provides the following Avalon-MM Interface used to access all of the Native PHY Transceiver DPRIO registers:

- reconfig_clk
- reconfig_reset
- reconfig_read
- reconfig_write
- reconfig_address
- reconfig_readdata
- reconfig_waitrequest
- reconfig_writedata

Related Information

- For more information about how to use this interface, refer to the 100G Interlaken MegaCore Function User Guide
- Avalon Interface Specifications

Connecting the Arria 10 PLL to the New Arria 10 100G Interlaken IP Core

Instantiate and connect the PLL as shown below.

Figure 5-3: Arria 10 PLL to Arria 10 100G Interlaken MegaCore Function Connection Diagram
Assigning New I/O Standard Values to Interlaken Serial I/Os

Update the following I/O standard for 100G Interlaken-related pins for the Arria 10 device:

- serial rx_pin(s): High Speed Differential I/O
- serial tx_pin(s): High Speed Differential I/O
Migrating PCIe Hard IP Qsys Design to Arria 10

This document provides guidelines in cross-family migration for a Qsys design that uses Altera PCIe Hard IP to Arria® 10 device family using the Quartus II software Arria 10 Edition v13.1. Stratix V is used as a reference device for this document, but the migration guidelines are applicable to all 28nm Altera devices. To migrate your Stratix V PCIe design to an Arria 10 device, start with up-front planning by considering the differences in the Hard IP.

Differences in Arria 10 and Stratix V PCIe Hard IP

Graphical User Interface (GUI) Differences

The Arria 10 PCIe Hard IP uses a common graphical user interface (GUI) for Avalon-Memory Mapped (Avalon-MM) and Avalon Streaming (Avalon-ST) interfaces. To select between Avalon-MM and Avalon-ST interfaces, use the Interface type pull down menu.
Figure 6-1: Stratix V Hard IP for PCI Express

Figure 6-2: Arria 10 Hard IP for PCI Express
Table 6-1: System Setting Differences Between Stratix V and Arria 10 PCIe Hard IP GUI

<table>
<thead>
<tr>
<th>Settings</th>
<th>Stratix V</th>
<th>Arria 10</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCIe Modes</td>
<td>Gen1 x1: 62.5 MHz</td>
<td>For Gen1 x1 use 125 MHz&lt;sup&gt;(11)&lt;/sup&gt;</td>
</tr>
<tr>
<td></td>
<td>Gen3 x2: 125 MHz, 128 bits</td>
<td>For Gen3 x2 use 250 MHz, 64 bits&lt;sup&gt;(11)&lt;/sup&gt;</td>
</tr>
<tr>
<td>PCIe Base Specification Version</td>
<td>2.1, 3.0</td>
<td>3.0</td>
</tr>
<tr>
<td>Interface</td>
<td>Application Interface</td>
<td>Interface Type</td>
</tr>
<tr>
<td>Reference Clock</td>
<td>100 MHz or 125 MHz</td>
<td>100 MHz</td>
</tr>
<tr>
<td>Deprecated RX ST Byte Enable</td>
<td>Yes</td>
<td>Not supported</td>
</tr>
</tbody>
</table>

Table 6-2: Device Identification Register Values and PHY Characteristics Setting Differences Between Stratix V and Arria 10 PCIe Hard IP GUI

<table>
<thead>
<tr>
<th>Settings</th>
<th>Stratix V</th>
<th>Arria 10</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device identification register default values</td>
<td>Altera default values</td>
<td>0</td>
</tr>
<tr>
<td>PHY Characteristics</td>
<td>ATX or CMU PLL for Gen1/Gen2</td>
<td>ATX PLL or CMU PLL for Gen1/Gen2</td>
</tr>
<tr>
<td></td>
<td>ATX and CMU PLL for Gen3</td>
<td>ATX and CMU PLL for Gen3</td>
</tr>
<tr>
<td></td>
<td>Low latency mode (Common clock configuration) supported</td>
<td>Low latency mode (No common clock configuration) not supported</td>
</tr>
</tbody>
</table>

Note: There are no differences for Base Address Register settings, Base and Limit Register for Root Port settings, and PCI Express / PCI Capabilities settings between Stratix V and Arria PCIe Hard IP.

Pinout Differences

Transceiver Reconfiguration Controller IP

Because the Arria 10 PCIe Hard IP does not use the Transceiver Reconfiguration Controller IP, the reconfig_from_xcvr and reconfig_to_xcvr ports are not present in the generated variation of the IP. These ports are present in the generated variation of the PCIe Hard IP for Stratix V.

Local Management Interface

For Arria 10 PCIe Hard IP, the local management interface data in / data out ports are 8 bits. For Stratix V PCIe Hard IP, these ports are 32 bits.

tx_cred Interface

For Arria 10 PCIe Hard IP, the tx_cred interface is time division multiplexed.

<sup>(11)</sup> Only in Quartus II Software Arria 10 Edition v13.1
### Table 6-3: tx_cred Interface Differences between Arria 10 and Stratix PCIe Hard IP

<table>
<thead>
<tr>
<th>Direction</th>
<th>Name</th>
<th>Width</th>
<th>Arria 10</th>
<th>Name</th>
<th>Width</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output</td>
<td>tx_cred_data_fc</td>
<td>12</td>
<td>Output</td>
<td>tx_cred_data_fc</td>
<td>12</td>
</tr>
<tr>
<td>Output</td>
<td>tx_cred_data_fcp</td>
<td>12</td>
<td>Output</td>
<td>tx_cred_hdr_fc</td>
<td>8</td>
</tr>
<tr>
<td>Output</td>
<td>tx_cred_data_fcnp</td>
<td>12</td>
<td>Output</td>
<td>tx_cred_fc_hip_cons</td>
<td>6</td>
</tr>
<tr>
<td>Output</td>
<td>tx_cred_hdr_fc</td>
<td>12</td>
<td>Output</td>
<td>tx_cred_fc_infinite</td>
<td>6</td>
</tr>
<tr>
<td>Output</td>
<td>tx_cred_fc_infinite</td>
<td>8</td>
<td>Input</td>
<td>tx_cred_fc_sel</td>
<td>2</td>
</tr>
</tbody>
</table>

### Channel Alignment Differences

For Arria 10 PCIe Hard IP, the PCIe lane 0 always aligns with the channel 4 of transceiver bank as shown in the diagrams below.

**Figure 6-3: PCIe Hard IP x1 and x2 Configuration Channel Alignment**

The diagrams illustrate the channel alignment for PCIe Hard IP configurations x1 and x2. The alignment is as follows:

**x1 Configuration**
- PLL1
- ATX PLL1
- PLL0
- ATX PLL0
- Gen1/2
- PLL1
- ATX PLL1

**x2 Configuration**
- PLL1
- ATX PLL1
- PLL0
- ATX PLL0
- PLL0
- ATX PLL0

These configurations show the PMA and PCS channel mapping for PCIe Hard IP, with highlighting for required or used channels and ATX PLL used as a clock source for the channels.
Device Pin Compatibility

There is no device package pin compatibility between Altera® 28-nm devices and Arria 10 devices.

Device Migration Flow in Quartus II

This section describes how to migrate the Qsys PCIe example design to an Arria 10 device. The migration flow consists of the following steps:

1. Open the design in Quartus II software Arria 10 Edition v13.1.
2. Update the Qsys sub-system to Arria 10.
3. Simulate the Arria 10 Design.
4. Compile the design for the an Arria 10 device.

Open the Design in Quartus II Software Arria 10 Edition v13.1

1. In the File menu, select Open Project.
2. Click Yes in the pop-up window for overwriting the database with Arria 10 version of Quartus II software.
3. Click Yes in the pop-up window for removing all location assignments.
4. In the Upgrade IP Component window, select the IP component entity to be upgraded.
5. Click Upgrade to launch Qsys.

Update the Qsys Sub-System to Arria 10

1. Remove the Transceiver Reconfiguration Controller IP.
   a. On the Tools menu, select Qsys
   b. Browse to the .qsys file and open it.
   c. Ignore the error message related to device_family_hw.tcl and port difference.
   d. In the System Contents pane, click on the following instances and then click Remove to delete them:
2. Upgrade PCIe Hard IP to the Arria 10 version
   b. Configure the Arria 10 Hard IP for PCI Express instance to match the Stratix V instance.
      Note: You can start another Qsys session to open the Stratix V instantiation to refer to the configuration settings for comparison.

3. Connect the Arria 10 PCIe Hard IP to your design
   a. In the Export column, note the Stratix V exported ports and their names. Select each exported name to remove it.
   b. In the Export column, select each Arria 10 port that has the same name as the previously exported Stratix V port. Type in the same exported name as in the above step.
   c. Right click on the APPS instance and select Edit.
      • Select Arria 10 as the Targeted Device Family.
      • Uncheck Use deprecated RX Avalon-ST data byte port.
      Note: If your application design uses the Local Management interface and/or tx_cred interface, update your design to match the port changes in Arria 10 PCIe Hard IP. If your application design includes other blocks that target Stratix V, retarget them to Arria 10.
   d. Right click on each conduit / IO of the Arria 10 PCIe Hard IP and select the target conduit / IO from the pop-up connection menu.
   e. Click on the Stratix V instance and select Remove.

4. Regenerate for synthesis and simulation.
   a. Click on Generate to build the testbench and the synthesis file for the design.
   b. In the Generate menu window, select Standard BFMs for Qsys interfaces to create testbench Qsys system.
   c. Select Verilog or VHDL for Create testbench simulation model option.
   d. Select Verilog or VHDL for Create HDL design files for synthesis option.
      Note: Altera recommends to use the same output directory structure and synthesis file as the Stratix V design to avoid manipulation of the project files.
   e. Click Generate.
   f. Click Save in the Save Changes dialog box.

Simulate your Arria 10 Design

1. Start your simulation tool. This example uses the ModelSim software.
2. From the ModelSim transcript window, in the generated testbench directory, enter the following commands:
• do msim_setup.tcl
• ld_debug
• run -all

Compile the Arria 10 Design

1. On the Assignment menu, click Device.
2. Under the Available devices list, select the necessary Arria 10 device in the package, pin count and speed grade that you intend to migrate to.
3. On the Assignment menu, click Pin Planner to make IO location assignments specific to your targeted Arria 10 device.
4. On the Processing menu, click Start Compilation.

Arria 10 PCIe Hard IP Migration Checklist

<table>
<thead>
<tr>
<th>Item</th>
<th>Done</th>
<th>N/A</th>
<th>Arria 10 PCIe Hard IP Migration Check List</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td></td>
<td></td>
<td>Review the Hard IP configuration to ensure that all intended features are configured and implemented.</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td></td>
<td>Review all the sub-blocks to ensure that the targeted family is Arria 10.</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td></td>
<td>Review if the Local Management Interface is used and revise user the application logic to account for difference in width.</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td></td>
<td>Review if tx_cred interface is used and revise the user application logic to account for the port change.</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td></td>
<td>Review if deprecated RX ST byte enable is used to revise the user application logic.</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td></td>
<td>Remove the Transceiver Reconfiguration Controller IP and associated logic from your design.</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td></td>
<td>If CvP Update is used, replace it with Partial Configuration.</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td></td>
<td>Review the PCIe serial pinout. <strong>Note:</strong> PCIe lane 0 must align the channel 4 of the transceiver bank.</td>
</tr>
<tr>
<td>9</td>
<td></td>
<td></td>
<td>Review the reset sequence.</td>
</tr>
<tr>
<td>10</td>
<td></td>
<td></td>
<td>Review the timing constraints.</td>
</tr>
</tbody>
</table>
This IP migration flow configures the Altera Triple-Speed Ethernet MegaCore function to match the settings of the existing design and allow you to regenerate the MegaCore function.

**Note:** The Triple-Speed Ethernet MegaCore function design generated in the Qsys system requires manual parameterization as no automated upgrade mechanism is available.

**Before you begin**

- Restore the archived file or copy your project into a new directory as described in the Copying the Project for Arria 10 on page 2-1 section.
- Open your project in the Quartus II software Arria 10 Edition v13.1 as described in the Opening the Stratix V or Arria V Project in Quartus II Software Arria 10 Edition v13.1 on page 2-3 section.

To migrate the MegaCore function in the Qsys system, follow these steps:

1. On the Tools menu, click Qsys.
2. On the File menu, click Open and select the Qsys file.
   For Triple-Speed Ethernet MegaCore function prior to 13.0 version, the System Contents tab highlights that the triple_speed_ethernet IP is not found or could not be instantiated.
3. Delete the old Triple-Speed Ethernet MegaCore function (triple_speed_ethernet) and instantiate a new 13.1 version of the Triple-Speed Ethernet MegaCore function (altera_eth_tse). Redo all the IP connectivity.
4. On the Generate menu, click Generate to generate the synthesis files for the design.

For Triple-Speed Ethernet MegaCore function 13.0 version that was previously generated using the MegaWizard Plug-In Manager, you can use the Upgrade IP Components function to migrate your MegaCore function.

**Note:** For Triple-Speed Ethernet MegaCore function prior to 13.0 version, a Failed status is shown when you use the Upgrade IP Components function. You must manually open the MegaWizard Plug-In Manager to generate a new 13.1 version and then delete the old version.
To migrate the MegaCore function using the Upgrade IP Components function, follow these steps:

1. On the File menu, click **Open Project**.
2. Select the Quartus II project file (.qpf) from the Arria 10 project directory you created.
3. Click **Yes** to proceed when a warning message to remove all location assignments appears.
4. On the Project menu, click **Upgrade IP Components**. This window displays the list of all IP components that need to be upgraded or regenerated. To open the parameter editor and edit the IP settings before upgrading, double-click on the entity. Click **Finish** to close the parameter editor.
5. Click **Upgrade**. The Status column indicates a successful or failed upgrade.

**Related Information**

*Altera Triple-Speed Ethernet User Guide*

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**Change in the Triple-Speed Ethernet MegaCore Function for Arria 10 Devices**

The implementation of the Altera Triple-Speed Ethernet MegaCore function for Arria 10 devices is different from the Arria V and Stratix V devices.

For TSE 1000BASE-X/SGMII PCS only with GXB transceiver variant, the reset controller and TX PLL are no longer inside the TSE IP block. You must manually instantiate and connect the reset controller and TX PLL to the Altera Native PHY IP Core (GXB transceiver) interface in system level. The following figure shows the implementation.

*Figure 7-1: TSE 1000BASE-X/SGMII PCS Only with GXB Transceiver*

The Native PHY IP Core terminator block functions to terminate and adapt the hw_tcl interface from and to the Native PHY IP Core.
This chapter describes how to migrate the following megafunctions from Arria V and Stratix V devices to Arria 10 devices.

- Altera GPIO Megafunction
- Altera OCT Megafunction
- Altera LVDS SERDES Megafunction
- Active Serial Memory Interface (ALTASMI_PARALLEL) Megafunction
- Parallel Flash Loader (PFL) Megafunction
- Serial Flash Loader (SFL) Megafunction

### Altera GPIO Megafunction

The IP migration flow configures the Altera GPIO megafunction to match the settings of the ALTDDIO_IN, ALTDDIO_OUT, ALTDDIO_BIDIR, or ALTIOBUF megafunction, allowing you to regenerate the megafunction.

#### Before you begin

- Restore the archived file or copy your project into a new directory as described in the Copying the Project for Arria 10 on page 2-1.
- Open your project in the Quartus II software Arria 10 Edition v13.1 as described in the Opening the Stratix V or Arria V Project in Quartus II Software Arria 10 Edition v13.1 on page 2-3.

To migrate the megafunction, follow these steps:

1. In the Quartus II software version 13.1 or earlier, on the Tools menu, click MegaWizard Plug-In Manager.
2. Select Edit an existing custom megafuction variation, then click Next.
3. Navigate to the directory containing your Stratix V or Arria V design and select your Stratix V or Arria V megafunction component that you want to edit or migrate.

   **Note:** This section uses the ALTDDIO_BIDIR megafunction as an example.

4. Click Next. The ALTDDIO_BIDIR parameter editor appears.
5. Turn off the Match project/default option. Then, in the Currently selected device family, select Arria 10.
6. Click Finish to open the Altera GPIO parameter editor. The Quartus II software will configure the Altera GPIO megafun
c tion similar to the old settings.
7. Turn on the Show signals option to view the port names.
8. Click Finish to regenerate the megafunction. The Generation dialog box appears. In the dialog box, turn on the Generate Example Design option if you want to generate a design example, in addition to generating the megafunction component files.
9. Click Exit.
10. Replace the ALTDDIO_BIDIR megafunction instantiation in the RTL with the Altera GPIO megafunction.
11. To edit or migrate another megafunction such as the ALTDDIO_IN, ALTDDIO_OUT or ALTIIOBUF megafunc
tion, repeat step 1 to step 10.
12. After regenerating all the Arria 10 megafunction components for your design, make sure that the Quartus II software successfully generates the new name and the ports are matched and connected correctly to the rest of the RTL.
13. To recompile your design for the Arria 10 device, on the Processing menu, click Start Compilation.

Related Information
- Altera GPIO Megafunction User Guide

Altera OCT Megafunction

This IP migration flow configures the Altera OCT megafunction to match the settings of the ALTOCT megafunction, allowing you to regenerate the megafunction.

Before you begin
- Restore the archived file or copy your project into a new directory as described in the Copying the Project for Arria 10 on page 2-1.
- Open your project in the Quartus II software Arria 10 Edition v13.1 as described in the Opening the Stratix V or Arria V Project in Quartus II Software Arria 10 Edition v13.1 on page 2-3.

To migrate the megafunction, follow these steps:
1. In the Quartus II software version 13.1 or earlier, on the Tools menu, click MegaWizard Plug-In Manager.
2. Select Edit an existing megafunction variation, then click Next.
3. Navigate to the directory containing your Stratix V or Arria V design and select your Stratix V or Arria V ALTOCT megafunction component that you want to edit or migrate.
4. Click Next. The ALTOCT parameter editor appears.
5. Turn off the Match project/default option. Then, in the Currently selected device family, select Arria 10.
6. Click Finish to open the Altera OCT parameter editor. The Quartus II software will configure the Altera OCT megafunction similar to the old settings.
7. Turn on the Show signals option to view the port names.
8. Click Finish to regenerate the megafunction. The Generation dialog box appears. In the dialog box, turn on the Generate Example Design option if you want to generate a design example, in addition to generating the megafunction component files.
9. Click Exit.
10. Replace the ALTOCT megafunction instantiation in the RTL with the Altera OCT megafunction.
11. After regenerating all the Arria 10 megafunction components for your design, make sure that the Quartus II software successfully generates the new name and the ports are matched and connected correctly to the rest of the RTL.

12. To recompile your design for the Arria 10 device, on the Processing menu, click Start Compilation.

Related Information
- Altera OCT Megafunction User Guide

Altera LVDS SERDES Megafuion

The IP migration flow configures the Altera LVDS SERDES IP to match the settings of the ALTLVDS_RX or ALTLVDS_TX, allowing you to regenerate the IP.

Before you begin
- Restore the archived file or copy your project into a new directory as described in the Copying the Project for Arria 10 on page 2-1.
- Open your project in the Quartus II software Arria 10 Edition v13.1 as described in the Opening the Stratix V or Arria V Project in Quartus II Software Arria 10 Edition v13.1 on page 2-3.

To migrate the megafuion, follow these steps:

1. In the Quartus II software version 13.1 or earlier, on the Tools menu, click MegaWizard Plug-In Manager.
2. Select Edit an existing custom megafuion variation, then click Next.
3. Navigate to the directory containing your Stratix V or Arria V design and select your ALTLVDS_RX or ALTLVDS_TX megafuion component that you want to edit or migrate.
4. Click Next. The ALTLVDS_RX or ALTLVDS_TX parameter editor appears.
5. Turn off the Match project/default option. Then, in the Currently selected device family, select Arria 10.
6. In the Frequency/PLL settings tab, turn on the Use 'pll_areset' input port parameter. The PLL reset pin is required in Arria 10 devices to reset the PLL.
7. Click Finish to open the Altera LVDS SERDES parameter editor. The Quartus II software will configure the Altera LVDS SERDES megafuion similar to the old settings.

For Altera LVDS SERDES in RX-DPA mode, you need more reset ports such as the dpa_reset, fifo_reset, and bitslip_reset. Therefore, if you are using ALTLVDS RX-DPA mode, ensure that you enable these ports accordingly. Refer to the following table for more details on the supported reset ports.

Table 8-1: Supported Reset Pin

<table>
<thead>
<tr>
<th>Port</th>
<th>Function</th>
<th>ALTLVDS_RX</th>
<th>Altera LVDS SERDES in RX Mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>rx_reset</td>
<td>Resets the DPA circuitry.</td>
<td>Supported</td>
<td>Not supported. For LVDS master reset, reset all individual reset pin at the same time to complete a master reset.</td>
</tr>
<tr>
<td>pll_reset</td>
<td>Resets the PLL circuitry.</td>
<td>Supported</td>
<td>Supported</td>
</tr>
<tr>
<td>dpa_reset</td>
<td>Resets the DPA circuitry.</td>
<td>Not supported</td>
<td>Supported</td>
</tr>
</tbody>
</table>
8. Turn on the Show signals option to view the port names.
9. Click Finish to regenerate the megafunction. The Generation dialog box appears. In the dialog box, turn on the Generate Example Design option if you want to generate a design example, in addition to generating the megafunction component files.
10. Click Exit.
11. The Quartus II dialog box appears. Click Yes.
12. The Update Symbol or Block dialog box appears. Select Selected symbol(s) or block(s) and then click OK.
13. Double-click the megafunction in your design to view the megafunction in the Altera LVDS SERDES parameter editor. The Quartus II software will configure the Altera LVDS SERDES megafunction similar to the old settings.
14. After regenerating all the Arria 10 megafunction components for your design, make sure that the Quartus II software successfully generates the new name and the ports are matched and connected correctly to the rest of the RTL.
15. To recompile your design for the Arria 10 device, on the Processing menu, click Start Compilation.

Note: The tx_outclock division factor 1, which is supported in the ALTLVDS_TX megafunction, is no longer supported in the Altera LVDS SERDES megafunction.

Note: The core clock resource type is selectable in the ALTLVDS_RX and ALTLLVDS_TX megafunctions. The Altera LVDS SERDES megafunction supports only AUTO mode. The core clock can still be assigned to a different clock network using QSF assignments.

Note: The Altera LVDS SERDES megafunction does not support the external PLL mode.

Related Information
- Altera LVDS SERDES Megafuction User Guide

ALTASMI_PARALLEL Megafuction

This IP migration flow configures the active serial memory interface (ALTASMI_PARALLEL) to match the settings of the ALTASMI_PARALLEL megafunction for Arria 10 devices, allowing you to regenerate the megafuction.

Before you begin
- Restore the archived file or copy your project into a new directory as described in the Copying the Project for Arria 10 on page 2-1.
- Open your project in the Quartus II software Arria 10 Edition v13.1 as described in the Opening the Stratix V or Arria V Project in Quartus II Software Arria 10 Edition v13.1 on page 2-3.
To migrate the megafunction, follow these steps:

1. In the Quartus II software version 13.1 or earlier, on the Tools menu, click MegaWizard Plug-In Manager.
2. Select Edit an existing custom megafunction variation, then click Next.
3. Navigate to the directory containing your Arria V or Stratix V design and select your Arria V or Stratix V ALTASMI_PARALLEL megafunction component that you want to edit or migrate.
4. Click Next. The ALTASMI_PARALLEL parameter editor appears.
5. Turn off the Match project/default option. Then, in the Currently selected device family, select Arria 10.
6. Click Finish to complete the ALTASMI_PARALLEL reinstantiation for Arria 10 devices.
7. The sce[2..0] input pin is added after the ALTASMI_PARALLEL reinstantiation. Connect the sce[2..0] pin to GND.
8. To recompile your design for the Arria 10 device, on the Processing menu, click Start Compilation.

Related Information
- Active Serial Memory Interface (ALTASMI_PARALLEL) Megafunction User Guide

PFL Megafuction

This IP migration flow configures the parallel flash loader (PFL) megafunction to match the settings of the PFL megafunction for Arria 10 devices, allowing you to regenerate the megafunction.

Before you begin
- Restore the archived file or copy your project into a new directory as described in the Copying the Project for Arria 10 on page 2-1.
- Open your project in the Quartus II software Arria 10 Edition v13.1 as described in the Opening the Stratix V or Arria V Project in Quartus II Software Arria 10 Edition v13.1 on page 2-3.

To migrate the megafunction, follow these steps:

1. In the Quartus II software version 13.1 or earlier, on the Tools menu, click MegaWizard Plug-In Manager.
2. Select Edit an existing custom megafunction variation, then click Next.
3. Navigate to the directory containing your Arria V or Stratix V design and select your Arria V or Stratix V PFL megafunction component that you want to edit or migrate.
4. Click Next. The PFL parameter editor appears.
5. Turn off the Match project/default option. Then, in the Currently selected device family, select Arria 10.
6. Click Finish to complete the PFL reinstantiation for Arria 10 devices.
7. To recompile your design for the Arria 10 device, on the Processing menu, click Start Compilation.

Related Information
- Parallel Flash Loader Megafunction User Guide

SFL Megafuction

This IP migration flow configures the serial flash loader (SFL) megafunction to match the settings of the SFL megafunction for Arria 10 devices, allowing you to regenerate the megafunction.
Before you begin

- Restore the archived file or copy your project into a new directory as described in the Copying the Project for Arria 10 on page 2-1.
- Open your project in the Quartus II software Arria 10 Edition v13.1 as described in the Opening the Stratix V or Arria V Project in Quartus II Software Arria 10 Edition v13.1 on page 2-3.

To migrate the megafunction, follow these steps:

1. In the Quartus II software version 13.1 or earlier, on the Tools menu, click MegaWizard Plug-In Manager.
2. Select Edit an existing custom megafunction variation, then click Next.
3. Navigate to the directory containing your Arria V or Stratix V design and select your Arria V or Stratix V SFL megafunction component that you want to edit or migrate.
4. Click Next. The SFL parameter editor appears.
5. Turn off the Match project/default option. Then, in the Currently selected device family, select Arria 10.
6. Click Finish to complete the SFL reinstatement for Arria 10 devices.
7. To recompile your design for the Arria 10 device, on the Processing menu, click Start Compilation.

Related Information

- AN 370: Using the Serial Flash Loader with the Quartus II Software
## Document Revision History

<table>
<thead>
<tr>
<th>Date</th>
<th>Version</th>
<th>Changes</th>
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<tbody>
<tr>
<td>August 2014</td>
<td>2014.08.18</td>
<td>Added links to current migration information in <em>Introduction to Altera IP Cores</em> and <em>Altera IP Release Notes.</em></td>
</tr>
<tr>
<td>December 2013</td>
<td>2013.12.02</td>
<td>Initial release</td>
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