



# Intel<sup>®</sup> Agilex<sup>™</sup> General Purpose I/O and LVDS SERDES User Guide



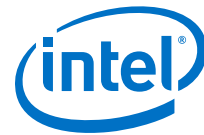
# Contents

---

- 1. Intel® Agilex™ General Purpose I/O and LVDS SERDES Overview..... 4**
  - 1.1. Intel Agilex I/O and Differential I/O Buffers..... 4
  - 1.2. Package Selection and I/O Vertical Migration Support..... 5
  - 1.3. I/O Banks..... 5
- 2. Intel Agilex I/O Features and Usage..... 8**
  - 2.1. GPIO Features..... 8
    - 2.1.1. Supported I/O Standards..... 8
    - 2.1.2. Intel Agilex I/O Buffer Behavior..... 10
    - 2.1.3. I/O Standards Restrictions and Implementation Guidelines..... 10
  - 2.2. Programmable I/O Element (IOE) Features in Intel Agilex Devices..... 11
    - 2.2.1. Programmable Output Slew Rate Control..... 15
    - 2.2.2. Programmable IOE Delay..... 15
    - 2.2.3. Programmable Open-Drain Output..... 15
    - 2.2.4. Programmable Bus Hold..... 16
    - 2.2.5. Programmable Pull-Up Resistor..... 16
    - 2.2.6. Programmable Pre-Emphasis..... 16
    - 2.2.7. Programmable De-Emphasis..... 17
    - 2.2.8. Programmable Differential Output Voltage..... 18
- 3. Intel Agilex I/O Termination..... 19**
  - 3.1. 1.5 V True Differential Signaling I/O Termination..... 19
    - 3.1.1. External I/O Termination..... 20
    - 3.1.2. 1.5 V True Differential Signaling I/O Standard OCT Termination..... 20
  - 3.2. Single-Ended I/O Termination in Intel Agilex Devices..... 21
    - 3.2.1. Single-Ended I/O Standard OCT Termination..... 21
    - 3.2.2. OCT Calibration Block..... 25
    - 3.2.3. Single-Ended I/O Standards External Termination ..... 26
- 4. Intel Agilex I/O Design Guidelines..... 29**
  - 4.1. Placement Requirements..... 29
  - 4.2. Special Pins Requirement..... 29
  - 4.3. External Memory Interface Pin Placement Requirements..... 30
  - 4.4. HPS Shared I/O Requirements..... 31
  - 4.5. SDM Shared I/O Requirements..... 31
  - 4.6. Configuration Pins..... 31
  - 4.7. Unused Pins..... 31
  - 4.8. Guidelines for GPIO Pins During Power Sequencing..... 32
  - 4.9. Maximum DC Current Restrictions..... 32
  - 4.10. 1.2 V I/O Interface Voltage Level Compatibility..... 32
  - 4.11. I/O Simulation..... 34
    - 4.11.1. HSPICE Models..... 34
- 5. Intel Agilex High-Speed SERDES I/O Architecture..... 35**
  - 5.1. Intel Agilex High-Speed SERDES I/O Overview..... 35
    - 5.1.1. High-Speed SERDES Architecture..... 35
    - 5.1.2. Intel Agilex GPIO Banks, SERDES, and DPA Locations..... 38
  - 5.2. Intel Agilex LVDS SERDES Transmitter..... 39



- 5.2.1. LVDS SERDES Transmitter Blocks..... 39
- 5.2.2. Serializer Bypass for DDR and SDR Operations..... 39
- 5.2.3. Serializer..... 40
- 5.2.4. Differential I/O Bit Position..... 41
- 5.2.5. Clocking Differential Transmitters..... 42
- 5.3. Intel Agilex LVDS SERDES Receiver..... 42
  - 5.3.1. LVDS SERDES Receiver Blocks..... 42
  - 5.3.2. Clocking LVDS SERDES Receivers..... 47
  - 5.3.3. LVDS SERDES Receiver Modes ..... 47
- 5.4. Intel Agilex LVDS SERDES Source-Synchronous Timing Budget..... 50
  - 5.4.1. Transmitter Channel-to-Channel Skew..... 50
  - 5.4.2. Receiver Skew Margin ..... 51
- 5.5. Intel Agilex LVDS SERDES Timing..... 52
  - 5.5.1. I/O Timing Analysis..... 53
- 5.6. Intel Agilex LVDS SERDES Design Guidelines..... 53
  - 5.6.1. Use High-Speed Clock from PLL to Clock SERDES Only..... 53
  - 5.6.2. Pin Placement for Differential Channels..... 54
  - 5.6.3. SERDES Pin Pairs for Soft-CDR Mode..... 54
- 6. Documentation Related to the Intel Agilex General Purpose I/O and LVDS SERDES User Guide..... 55**
- 7. Document Revision History for the Intel Agilex General Purpose I/O and LVDS SERDES User Guide..... 56**



## 1. Intel® Agilex™ General Purpose I/O and LVDS SERDES Overview

---

The Intel® Agilex™ I/O system includes a general purpose I/O (GPIO) interface, a Secure Device Manager (SDM) I/O interface and a Hard Processor System (HPS) I/O interface. Each I/O interface is designed to meet different interfacing requirements.

The General Purpose I/O interface system can support:

- 1.2 V single-ended non-voltage referenced Joint Electron Device Engineering Council (JEDEC) compliant I/O standards.
- 1.2 V single-ended and differential voltage referenced JEDEC compliant I/O standards.
- 1.5 V true differential I/O compatible with LVDS, RSDS, Mini-LVDS, and LVPECL I/O standards.
- DDR4 memory interface up to 1600 MHz with a Hard Memory Controller (HMC).
- LVDS serializer/deserializer (SERDES) interface up to 1.6 Gbps.

The SDM and HPS I/O interfaces can support 1.8 V single-ended non-voltage referenced I/O standard for SDM and HPS interfacing.

### Related Information

[Intel Agilex Data Sheet](#)

### 1.1. Intel Agilex I/O and Differential I/O Buffers

The I/O bank within the GPIO interface supports differential and single-ended I/O standards. The GPIO bank has true differential I/O buffers using the 1.5 V True Differential Signaling I/O standard, which is compatible with the LVDS, RSDS, Mini-LVDS, and LVPECL I/O standards. The true differential buffer forms a pair of unidirectional true differential channels. Half of the true differential channels support dedicated transmitter pins and the other half support dedicated true receiver pins. Refer to the device pin-out files for locations of dedicated receiver and transmitter channels.

Differential voltage referenced output pins are not true differential output pins. The differential voltage referenced I/O standards use two single-ended output pins where one of the output pins is inverted.

The I/O bank within the HPS and SDM interfaces supports single-ended IO standard.

Different power supplies power the Intel Agilex I/O buffer:



- VCCIO\_PIO and VCCPT power the I/O buffers located in the I/O bank within the GPIO interface.
- VCCIO\_SDM powers the I/O buffers located in the I/O bank within the SDM I/O interface.
- VCCIO\_HPS powers the I/O buffers located in the HPS I/O bank within the HPS I/O interface.

Each I/O bank within the interface has its own VCCIO power supply and supports only one VCCIO voltage. The supported I/O standards vary between interfaces. Refer to *Supported I/O Standards* for the list of I/O standards supported by each I/O interface.

## 1.2. Package Selection and I/O Vertical Migration Support

**Figure 1. Migration Capability Across Intel Agilex Product Lines—Preliminary**

- The arrows indicate the migration paths. The shades represent the devices included in each vertical migration path.
- To achieve full I/O migration across product lines in the same migration path, restrict I/Os and transceivers utilization to match the product line with the lowest I/O and transceiver counts.
- Different device packages have a different number of I/O banks. Refer to the device pin-out files for the total number of I/O banks available for each device package.

Variant	Product Line	Package									
		F894A	R1681A	R1957A	R2068A	R2280A	R2486A	R2486B	R2979A	R3343A	R3803A
F-Series	AGF 004	↑	↑	↑							
	AGF 006	↓									
	AGF 008		↓								
	AGF 012			↑	↑	↑	↑	↑			
	AGF 014			↓	↓	↓	↓	↓			
	AGF 022							↑			
	AGF 027							↓			
I-Series	AGI 022								↑	↑	↑
	AGI 027								↓	↓	↓

## 1.3. I/O Banks

There are three types of I/O banks available in the Intel Agilex I/O interface system:

- GPIO banks
- HPS I/O bank
- SDM I/O bank

In each GPIO bank, there are two sub-banks. The top sub-bank is placed near the edge of the die, and the bottom sub-bank is placed near the FPGA core.



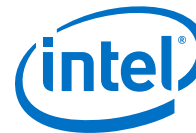
In each sub-bank, there are four I/O lanes with 12 I/O pins in each lane that make up a total of 48 single-ended I/O pins or 24 true differential I/O pairs per sub-bank. Each I/O lane supports three differential receiver input buffer pairs with SERDES and dynamic phase alignment (DPA) channels and three differential transmitter output buffer pairs with SERDES channels.

Other than the I/O lanes, SERDES and DPA, each I/O sub-bank also contains dedicated circuitries including I/O PLL, hard memory controller and OCT calibration blocks.

The total bank count in a GPIO bank varies across different device packages. Certain GPIO banks are shared with the SDM and HPS function blocks. Refer to the device pin-out files for available GPIO banks, GPIO and SDM shared I/O banks, and GPIO and HPS shared I/O banks per package.

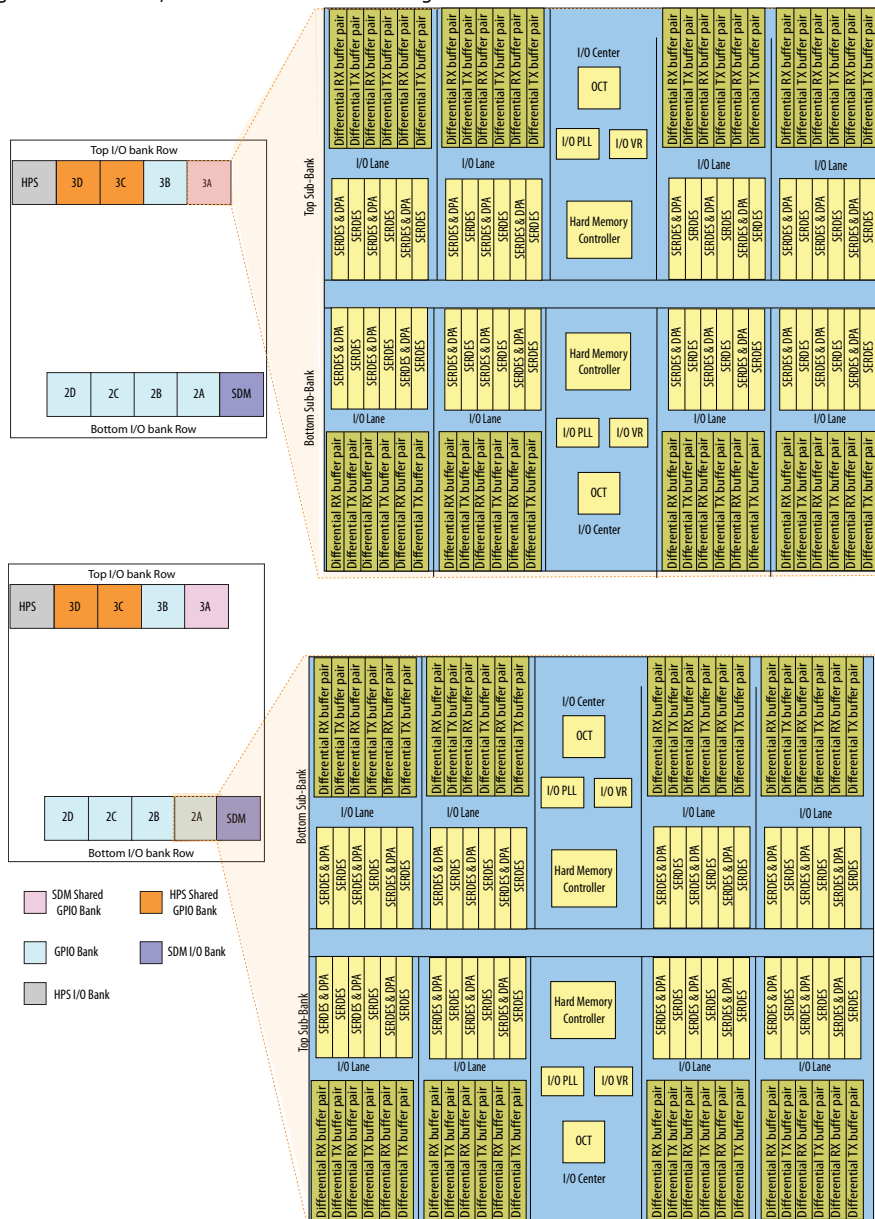
The HPS I/O bank consists of 48 I/O pins. These pins are used for HPS clocks, peripherals, mass storage flash and JTAG.

The SDM I/O bank consists of 24 dedicated pins for device configuration purposes. Refer to the device pin-out files for the dedicated function of each pin in the SDM I/O bank.



**Figure 2. Intel Agilix I/O Bank Structure (Bottom View)**

This diagram shows the I/O bank structure of Intel Agilix AGF 012 and AGF 014 devices.



Different device packages have a different number of I/O banks. Refer to the device pin-out files for available bank location for each device package.

## 2. Intel Agilex I/O Features and Usage

---

The I/O buffers in Intel Agilex devices provide the following features:

- Single-ended non-voltage referenced and voltage referenced I/O standards
- Differential voltage-referenced I/O standards
- True differential transmitters and receivers
- Serializer/deserializer (SERDES)
- Programmable slew rate
- Programmable bus-hold
- Programmable weak pull-up resistor
- Programmable differential output voltage ( $V_{OD}$ )
- Programmable open-drain output
- On-chip series termination ( $R_S$  OCT) with and without calibration
- On-chip parallel termination ( $R_T$  OCT)
- On-chip differential termination ( $R_D$  OCT)
- Dynamic on-chip parallel termination
- Internally generated  $V_{REF}$  with DDR4 calibration
- Programmable pre-emphasis for true differential output buffer
- Programmable de-emphasis for voltage-referenced /O standards

### 2.1. GPIO Features

#### 2.1.1. Supported I/O Standards

$VCCIO\_PIO$ ,  $VCCPT$ , and  $VCC$  power supplies power the Intel Agilex GPIO buffers. The  $VCCIO\_SDM$  power supply powers the SDM I/O buffer and the  $VCCIO\_HPS$  power supply powers the HPS I/O buffer. Each I/O bank has its own power supply and supports only one I/O voltage.

The following table shows the supported I/O standards for GPIO, HPS, and SDM I/O banks:



**Table 1. Intel Agilex I/O Standards Support per I/O Bank Type**

The 1.5 V True Differential Signaling I/O standard is compatible with the LVDS, RSDS, Mini-LVDS, and LVPECL standards at lower signal swing. Refer to *Intel Agilex Device Data Sheet for the electrical specifications of the 1.5 V True Differential Signaling I/O standard*.

I/O Standard	GPIO Bank	HPS I/O Bank	SDM I/O Bank
1.8 V LVCMOS	No	Yes	Yes
1.2 V LVCMOS	Yes	No	No
SSTL-12	Yes	No	No
HSTL-12	Yes	No	No
POD12	Yes	No	No
Differential SSTL-12	Yes	No	No
Differential HSTL-12	Yes	No	No
Differential HSUL-12	Yes	No	No
Differential POD12	Yes	No	No
1.5 V True Differential Signaling	Yes	No	No

**Table 2. Intel Agilex GPIO Bank Supported I/O Standards**

I/O Standard	VCCIO_PIO (V)	VCCPT (V)	Vref (V)	VTT (V)	Application	JEDEC Standard
1.2 V LVCMOS	1.2	1.8	-	-	General purpose	JESD-12A.01
SSTL-12	1.2	1.8	0.6	0.6	DDR4, RLDRAM3, QDR-IV	JESD79-4B
HSTL-12	1.2	1.8	0.6	0.6	QDR-IV	JESD-16A
HSUL-12	1.2	1.8	0.6	-	LPDDR3	JESD209-3C
POD12	1.2	1.8	Internally calibrated	1.2	DDR4, QDR-IV	JESD79-4B
Differential SSTL-12 <sup>(1)</sup>	1.2	1.8	-	0.6	RLDRAM3	JESD79-4B
Differential HSTL-12 <sup>(1)</sup>	1.2	1.8	-	0.6	General purpose	JESD8-16A
Differential HSUL-12 <sup>(1)</sup>	1.2	1.8	-	-	LPDDR3	JESD209-3C
Differential POD-12 <sup>(1)</sup>	1.2	1.8	Internally calibrated	1.2	DDR4	JESD79-4B
1.5 V True Differential Signaling	1.5	1.8	-	-	SGMII, SFI, SPI	-

### Related Information

[Special Pins Requirement](#) on page 29

(1) Uses two single-ended outputs with second output programmed as inverted.

### 2.1.2. Intel Agilex I/O Buffer Behavior

All I/O pins in the GPIO bank are configured as tri-stated with weak pull-up enabled during device power up and device configuration. During device power down, all I/O pins are in undetermined state and pin signal is measured between GND to VCCIO\_PIO level.

Input signals of an I/O pin at any point should not exceed the maximum DC input voltage specification as specified in the *Intel Agilex Device Data Sheet*.

### 2.1.3. I/O Standards Restrictions and Implementation Guidelines

Observe the following I/O standard restrictions and implementation guidelines to ensure the success of your design. Unless noted otherwise, these guidelines apply to all variants of the Intel Agilex device family.

#### 2.1.3.1. Guidelines: V<sub>REF</sub> Sources and V<sub>REF</sub> Pins

Consider the following V<sub>REF</sub> pins guidelines:

- Intel Agilex devices support internal and external V<sub>REF</sub> sources.
  - There is an external V<sub>REF</sub> pin for every I/O bank, providing one external V<sub>REF</sub> source for all I/Os in the same bank.
  - Each I/O lane in the bank also has its own internal V<sub>REF</sub> generator. You can configure each I/O lane independently to use its internal V<sub>REF</sub> or the I/O bank's external V<sub>REF</sub> source. All I/O pins in the same I/O lane use the same V<sub>REF</sub> source.
- You can use the internal V<sub>REF</sub> with calibration to support DDR4 using the POD12 I/O standard.
- You can place any combination of input, output, or bidirectional pins near V<sub>REF</sub> pins. There is no V<sub>REF</sub> pin placement restriction.
- The V<sub>REF</sub> pins are dedicated for voltage-referenced single-ended I/O standards. You cannot use the V<sub>REF</sub> pins as user I/Os.
- Connect unused V<sub>REF</sub> pins to GND.

The V<sub>REF</sub> pin leakage current is typically 0.15 uA, and can go up to 4.1 uA.

#### 2.1.3.2. Guidelines: I/O Standards Implementation based on VCCIO\_PIO Voltages

The following guidelines apply to I/O standards based on the VCCIO\_PIO voltages.

##### 1.2 V VCCIO\_PIO

When using 1.2 V VCCIO\_PIO, you can implement singled-ended non-voltage-referenced and voltage-referenced I/O standards. This buffer also supports differential voltage-referenced I/O standards with this voltage. You can implement a mix of both voltage-referenced and non-voltage-referenced I/O standards within the I/O bank.



### 1.5 V VCCIO\_PIO

When using 1.5 V VCCIO\_PIO voltage, you can only implement true differential I/O standards. The buffer can interface with upstream or downstream devices that are compatible with the electrical specification of Intel Agilex devices, specified in the *Intel Agilex Device Data Sheet*. Analyze the electrical specification requirement to implement your true differential receiver. Implement DC coupling when the signal swing and offset voltage requirement is bounded within the Intel Agilex 1.5 V True Differential Signaling standard specification. Otherwise, implement AC coupling and external bias circuitry.

#### Related Information

[Intel Agilex Data Sheet](#)

## 2.2. Programmable I/O Element (IOE) Features in Intel Agilex Devices

The SDM and HPS I/O buffers in the Intel Agilex devices support different I/O standards and programmable I/O features than the general purpose I/O buffers. The following tables list the supported I/O standards and features by each I/O bank.

**Table 3. Programmable IOE Feature Settings for Intel Agilex GPIO Bank**

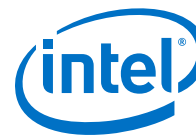
I/O Standard	Programmable IOE Feature							
	Slew Rate Control	I/O Delay	Open-Drain Output	Bus-Hold	Weak Pull-up Resistor	Pre-Emphasis	De-Emphasis	Differential Output Voltage
1.2 V LVCMOS	<ul style="list-style-type: none"> <li>Fast (Default)</li> <li>Medium</li> <li>Slow</li> </ul>	Refer to data sheet	<ul style="list-style-type: none"> <li>Off (Default)</li> <li>On</li> </ul>	<ul style="list-style-type: none"> <li>Off (Default)</li> <li>On</li> </ul>	<ul style="list-style-type: none"> <li>Off (Default)</li> <li>On</li> </ul>	—	—	—
SSTL-12	<ul style="list-style-type: none"> <li>Fast (Default)</li> <li>Medium</li> <li>Slow</li> </ul>	Refer to data sheet	—	—	—	—	<ul style="list-style-type: none"> <li>Off (Default)</li> <li>Low</li> <li>Medium</li> <li>High</li> <li>Low constant impedance</li> <li>Medium constant impedance</li> <li>High constant impedance</li> </ul>	—
HSTL-12	<ul style="list-style-type: none"> <li>Fast (Default)</li> <li>Medium</li> <li>Slow</li> </ul>	Refer to device data sheet	—	—	—	—	<ul style="list-style-type: none"> <li>Off (Default)</li> <li>Low</li> <li>Medium</li> <li>High</li> </ul>	—

*continued...*



I/O Standard	Programmable IOE Feature							
	Slew Rate Control	I/O Delay	Open-Drain Output	Bus-Hold	Weak Pull-up Resistor	Pre-Emphasis	De-Emphasis	Differential Output Voltage
							<ul style="list-style-type: none"> <li>Low constant impedance</li> <li>Medium constant impedance</li> <li>High constant impedance</li> </ul>	
HSUL-12	<ul style="list-style-type: none"> <li>Fast (Default)</li> <li>Medium</li> <li>Slow</li> </ul>	Refer to device data sheet	—	—	—	—	<ul style="list-style-type: none"> <li>Off (Default)</li> <li>Low</li> <li>Medium</li> <li>High</li> <li>Low constant impedance</li> <li>Medium constant impedance</li> <li>High constant impedance</li> </ul>	—
POD-12	<ul style="list-style-type: none"> <li>Fast (Default)</li> <li>Medium</li> <li>Slow</li> </ul>	Refer to device data sheet	—	—	—	—	<ul style="list-style-type: none"> <li>Off</li> <li>Low</li> <li>Medium</li> <li>High (Default)</li> </ul>	—
Differential SSTL-12	<ul style="list-style-type: none"> <li>Fast (Default)</li> <li>Medium</li> <li>Slow</li> </ul>	Refer to device data sheet	—	—	—	—	<ul style="list-style-type: none"> <li>Off (Default)</li> <li>Low</li> <li>Medium</li> <li>High</li> <li>Low constant impedance</li> <li>Medium constant impedance</li> <li>High constant impedance</li> </ul>	—
Differential HSTL-12	<ul style="list-style-type: none"> <li>Fast (Default)</li> <li>Medium</li> <li>Slow</li> </ul>	Refer to device data sheet	—	—	—	—	<ul style="list-style-type: none"> <li>Off (Default)</li> <li>Low</li> <li>Medium</li> <li>High</li> </ul>	—

*continued...*



I/O Standard	Programmable IOE Feature							
	Slew Rate Control	I/O Delay	Open-Drain Output	Bus-Hold	Weak Pull-up Resistor	Pre-Emphasis	De-Emphasis	Differential Output Voltage
							<ul style="list-style-type: none"> <li>Low constant impedance</li> <li>Medium constant impedance</li> <li>High constant impedance</li> </ul>	
Differential HSUL-12	<ul style="list-style-type: none"> <li>Fast (Default)</li> <li>Medium</li> <li>Slow</li> </ul>	Refer to device data sheet	—	—	—	—	<ul style="list-style-type: none"> <li>Off (Default)</li> <li>Low</li> <li>Medium</li> <li>High</li> <li>Low constant impedance</li> <li>Medium constant impedance</li> <li>High constant impedance</li> </ul>	—
Differential POD12	<ul style="list-style-type: none"> <li>Fast (Default)</li> <li>Medium</li> <li>Slow</li> </ul>	Refer to device data sheet	—	—	—	—	<ul style="list-style-type: none"> <li>Off</li> <li>Low</li> <li>Medium</li> <li>High (Default)</li> </ul>	—
1.5 True Differential Signaling	—	Refer to device data sheet	—	—	—	Off, Low power (Default), Constant impedance	—	<ul style="list-style-type: none"> <li>Low</li> <li>Medium low</li> <li>Medium high (Default)</li> <li>High</li> </ul>

**Table 4. Programmable IOE Feature Settings for Intel Agilex HPS I/O Bank**

I/O Standard	Programmable IOE Feature				
	Current Strength	Slew Rate	Weak Pull-up/Pull-down	Schmitt Trigger/TTL Input	Open Drain
1.8 V LVCMOS	<ul style="list-style-type: none"> <li>2 mA</li> <li>4 mA</li> <li>6 mA</li> <li>8 mA (Default)</li> </ul>	<ul style="list-style-type: none"> <li>Slow</li> <li>Fast (Default)</li> </ul>	<ul style="list-style-type: none"> <li>Disable</li> <li>Weak pull-up with 20 kOhm resistor (Default)</li> <li>Weak pull-up with 50 kOhm resistor</li> <li>Weak pull-up with 80 kOhm resistor</li> </ul>	<ul style="list-style-type: none"> <li>Schmitt Trigger (Default)</li> <li>TTL</li> </ul>	<ul style="list-style-type: none"> <li>Enable</li> <li>Disable (Default)</li> </ul>



I/O Standard	Programmable IOE Feature				
	Current Strength	Slew Rate	Weak Pull-up/ Pull-down	Schmitt Trigger/TTL Input	Open Drain
			<ul style="list-style-type: none"> <li>Weak pull-down with 20 kOhm resistor</li> <li>Weak pull-down with 50 kOhm resistor</li> <li>Weak pull-down with 80 kOhm resistor</li> </ul>		

**Table 5. Intel Agilex Configuration Pin I/O Standards and Features**

Configuration Pin Function	Location	Direction	I/O Standard	Drive Strength (mA)	Weak Pull-Up/Pull-Down
TDO	SDM I/O bank	Output	1.8 V LVCMOS	8	Weak pull-up
TMS	SDM I/O bank	Input	Schmitt Trigger Input	—	Weak pull-up
TCK	SDM I/O bank	Input	Schmitt Trigger Input	—	Weak pull-down
TDI	SDM I/O bank	Input	Schmitt Trigger Input	—	Weak pull-up
nSTATUS	SDM I/O bank	Output	1.8V LVCMOS	8	Weak pull-up
OSC_CLK_1	SDM I/O bank	Input	Schmitt Trigger Input	—	Weak pull-down
nCONFIG	SDM I/O bank	Input	Schmitt Trigger Input	—	Weak pull-up
SDM_IO[0],SDM_IO[8], SDM_IO[16]	SDM I/O bank	I/O	Schmitt Trigger Input or 1.8 V LVCMOS	8	Weak pull-down
SDM_IO[7:1],SDM_IO[15:9]	SDM I/O bank	I/O	Schmitt Trigger Input or 1.8 V LVCMOS	—	Weak pull-up
AVST_CLK	SDM Shared GPIO bank	Input	1.2 V LVCMOS	—	—
AVST_READY	SDM Shared GPIO bank	Output	1.2 V LVCMOS	Series 34 ohm on-chip termination (OCT)	—

*continued...*



Configuration Pin Function	Location	Direction	I/O Standard	Drive Strength (mA)	Weak Pull-Up/Pull-Down
				without calibration <sup>(2)</sup>	
AVST_VALID	SDM Shared GPIO bank	Input	1.2 V LVCMOS	—	—
AVST_DATA	SDM Shared GPIO bank	Input	1.2 V LVCMOS	—	—

### 2.2.1. Programmable Output Slew Rate Control

Each I/O pin contains a slew rate control, allowing you to specify the slew rate on a pin-by-pin basis. The slew rate control affects both the rising and falling edges of the signal.

You can select between three slew rate settings: Fast, Medium, and Slow.

- The Fast slew rate provides high-speed transitions for high-performance systems. This is the default setting.
- The Slow slew rate reduces system noise and crosstalk but adds a nominal delay to the rising and falling edges.
- Enable the DQS DLL in the same lane when you use a medium or slow slew rate for voltage referenced I/O standards

### 2.2.2. Programmable IOE Delay

You can activate the programmable IOE delays to ensure zero hold time, minimize setup time, or increase clock-to-output time. This feature helps read and write timing margins because it minimizes the uncertainties between signals in the bus.

Each pin can have a different input delay from pin-to-input register or a delay from output register-to-output pin values. This is to ensure that the signals within a bus have the same delay going into or out of the device.

For more information about the programmable IOE delay specifications, refer to the device data sheet.

#### Related Information

[Intel Agilex Data Sheet](#)

### 2.2.3. Programmable Open-Drain Output

Intel Agilex devices support open drain output on 1.2 V LVCMOS I/O standard. The programmable open-drain output provides a high-impedance state on output when logic to the output buffer is high. If logic to the output buffer is low, output is low.

---

(2) Slow slew rate signal



You can attach several open-drain outputs to a wire. This connection type is like a logical OR function, and is commonly called an active-low wired-OR circuit. If at least one of the outputs is in logic 0 state (active), the circuit sinks the current and brings the line to low voltage.

You can use open-drain output if you are connecting multiple devices to a bus. For example, you can use the open-drain output for system-level control signals that can be asserted by any device or as an interrupt.

Do not pull the output voltage higher than the  $V_{\text{I}}$  (DC) level. Intel recommends that you perform HSPICE simulation to verify the output voltage in your selected topology. Ensure the output voltage meets the  $V_{\text{IH}}$  and  $V_{\text{IL}}$  requirements of the receiving device.

#### 2.2.4. Programmable Bus Hold

Intel Agilex devices support the programmable bus hold feature on 1.2 V LVCMOS output. Each I/O pin provides an optional bus-hold feature that is active only after configuration. When the device enters user mode, the bus-hold circuit captures the value that is present on the pin by the end of the configuration.

The bus-hold circuitry uses a resistor to weakly pull the signal level to the last-driven state of the pin. The bus-hold circuitry holds this pin state until the next input signal is present. Therefore, you do not require an external pull-up or pull-down resistor to hold a signal level when the bus is tri-stated.

For each I/O pin, you can individually specify that the bus-hold circuitry pulls non-driven pins away from the input threshold voltage—where noise can cause unintended high-frequency switching. To prevent over-driving signals, the bus-hold circuitry drives the voltage level of the I/O pin lower than the  $V_{\text{CCIO\_PIO}}$  level.

If you enable the bus-hold feature, you cannot use the programmable pull-up option.

#### 2.2.5. Programmable Pull-Up Resistor

Intel Agilex devices support programmable pull up resistor on 1.2 V LVCMOS I/O. Each I/O pin provides an optional programmable pull-up resistor during user mode.

The programmable pull-up resistor feature is enabled by default on unused I/O for both 1.2 V and 1.5 V  $V_{\text{CCIO\_PIO}}$ . The pull-up resistor weakly holds the I/O to the  $V_{\text{CCIO\_PIO}}$  level.

If you enable the weak pull-up resistor, you cannot use the bus-hold feature.

#### 2.2.6. Programmable Pre-Emphasis

The  $V_{\text{OD}}$  setting and the output impedance of the driver set the output current limit of a high-speed transmission signal. At a high frequency, the slew rate may not be fast enough to reach the full  $V_{\text{OD}}$  level before the next edge, producing pattern-dependent jitter. With pre-emphasis, the output current is boosted momentarily during switching to increase the output slew rate.

Pre-emphasis increases the amplitude of the high-frequency component of the output signal, and thus helps to compensate for the frequency-dependent attenuation along the transmission line. The overshoot introduced by the extra current happens only during a change of state switching to increase the output slew rate, and does not ring,

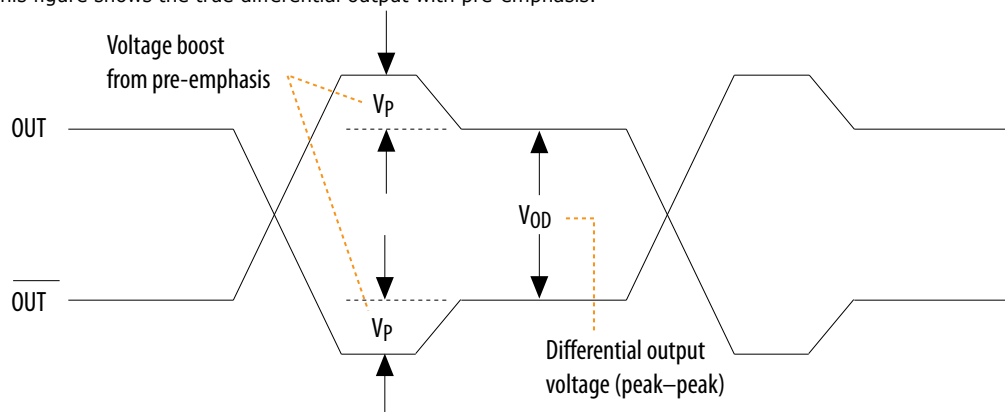




unlike the overshoot caused by signal reflection. The amount of pre-emphasis required depends on the attenuation of the high-frequency component along the transmission line.

**Figure 3. Programmable Pre-Emphasis**

This figure shows the true differential output with pre-emphasis.



### 2.2.7. Programmable De-Emphasis

The programmable de-emphasis feature is supported for all voltage-reference I/O standards. This feature supports a two-taps de-emphasis implementation, which consists of a main tap and a 1-UI delayed post tap.

When using this feature, the height of the I/O signal is attenuated whenever a symbol is longer than one UI. This feature supports two types of de-emphasis:

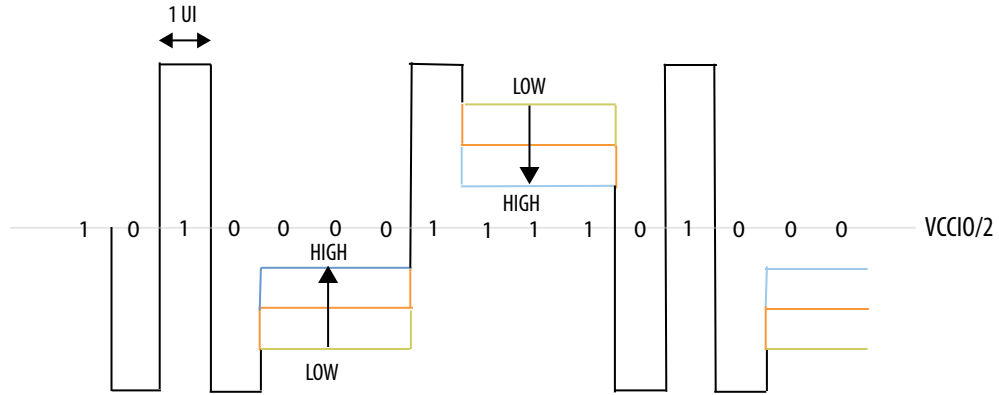
- Constant impedance—available for single-ended and differential SSTL-12, HSTL-12, and HSUL-12 I/O standards.
- Low power (non-constant impedance)—available for single-ended and differential SSTL-12, HSTL-12, HSUL-12, and POD12 I/O standards.

Each of the de-emphasis has three equalization settings - low, medium, and high.

Constant impedance de-emphasis has double effective equalization level of the low power de-emphasis.

**Figure 4. Programmable De-emphasis**

This figure shows the SSTL and HSTL standards with de-emphasis enabled.



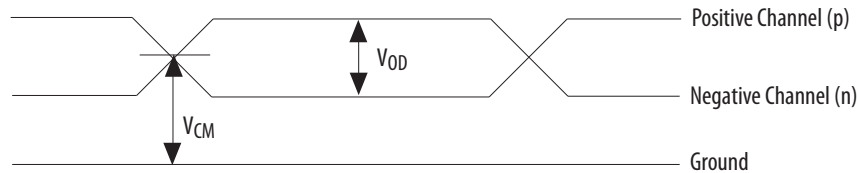
### 2.2.8. Programmable Differential Output Voltage

The programmable  $V_{OD}$  settings allow you to adjust the output eye opening to optimize the trace length and power consumption. A higher  $V_{OD}$  swing improves voltage margins at the receiver end, and a smaller  $V_{OD}$  reduces power consumption. You can statically adjust the  $V_{OD}$  of the differential signal by changing the  $V_{OD}$  settings in the software Assignment Editor.

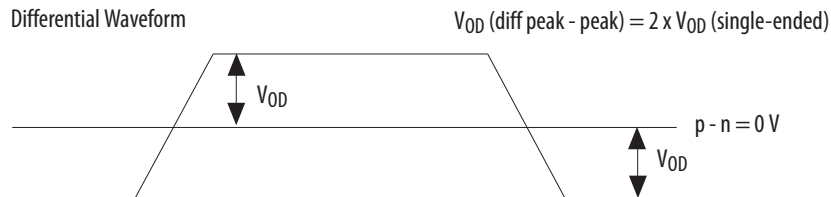
**Figure 5. Differential  $V_{OD}$**

This figure shows the  $V_{OD}$  of the true differential output.

Single-Ended Waveform



Differential Waveform

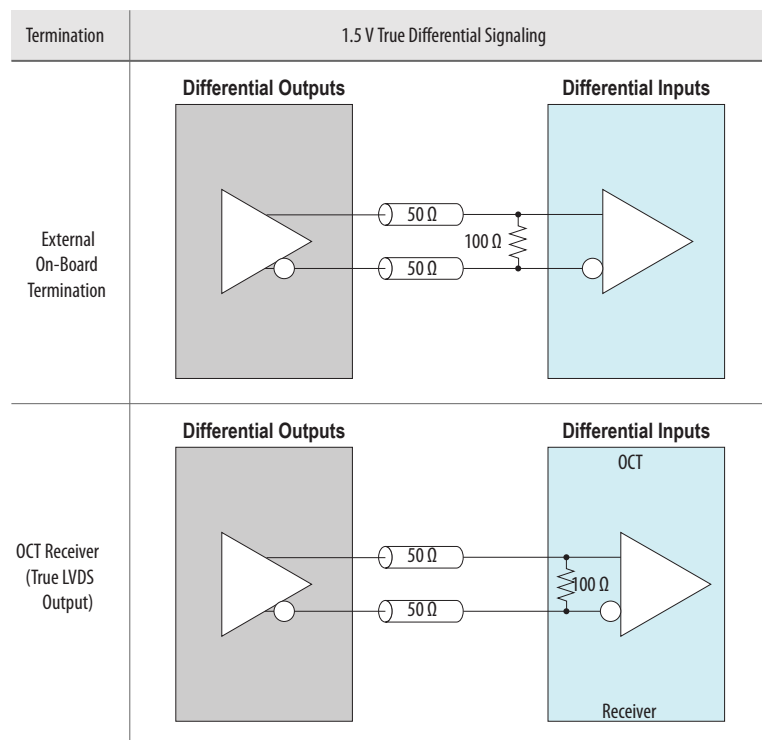


## 3. Intel Agilex I/O Termination

### 3.1. 1.5 V True Differential Signaling I/O Termination

All GPIO banks have dedicated circuitry to support true differential I/O standards by using the 1.5 V True Differential Signaling differential buffers without resistor networks. The 1.5 V True Differential Signaling buffer is compatible with the LVDS, RSDS, Mini-LVDS, and LVPECL standards, and supports 100  $\Omega$  differential on-chip termination (RD OCT).

**Figure 6. 1.5 V True Differential Signaling I/O Standard Termination**



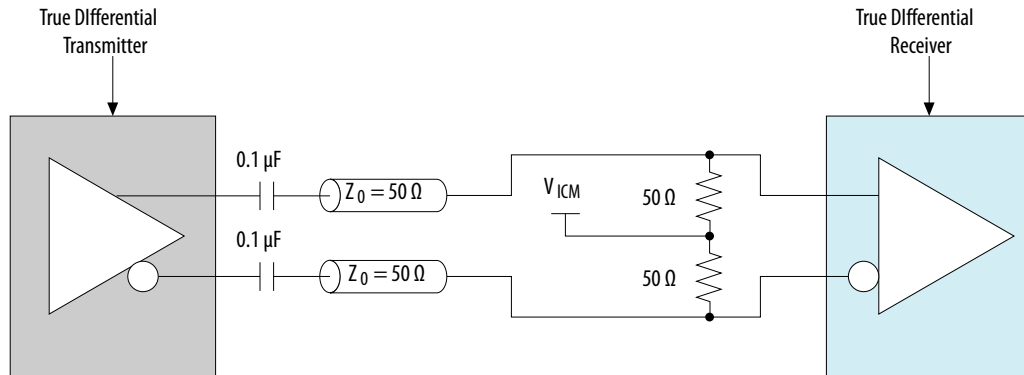
Use OCT with these I/O standards to save board space and cost. OCT reduces the number of external termination resistors usage. Refer to Intel Agilex device pin-out files for more information on the dedicated differential transmitter and receiver pins.

### 3.1.1.1. External I/O Termination

Use AC coupling and external voltage bias circuitry if the common-mode voltage of the output buffer does not match the differential receiver input common-mode voltage. For information about the  $V_{ICM}$  specification, refer to the device data sheet.

*Note:* Intel recommends that you use SPICE models to verify your AC/DC-coupled termination.

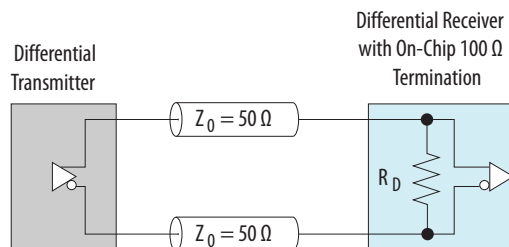
**Figure 7. AC-Coupled External Termination**



### 3.1.2. 1.5 V True Differential Signaling I/O Standard OCT Termination

All I/O pins and dedicated clock input pins in Intel Agilex devices support on-chip differential termination,  $R_D$  OCT. The Intel Agilex devices provide a  $100 \pm 40 \Omega$ , on-chip differential termination option on each differential receiver channel for 1.5 V True Differential Signaling I/O standards.

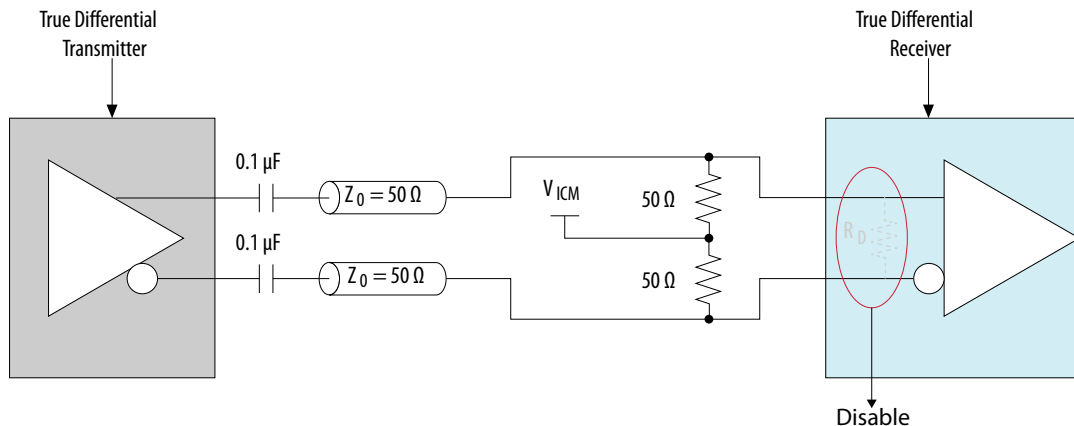
**Figure 8. OCT for Differential I/O Termination**



#### 3.1.2.1. Differential Input $R_D$ OCT Restrictions and Guidelines

For interfaces which require external voltage bias circuitry near the Intel Agilex device's true differential receiver, you must disable the OCT  $R_D$ .

**Figure 9. External Voltage Bias Circuitry with  $R_D$  Disabled**

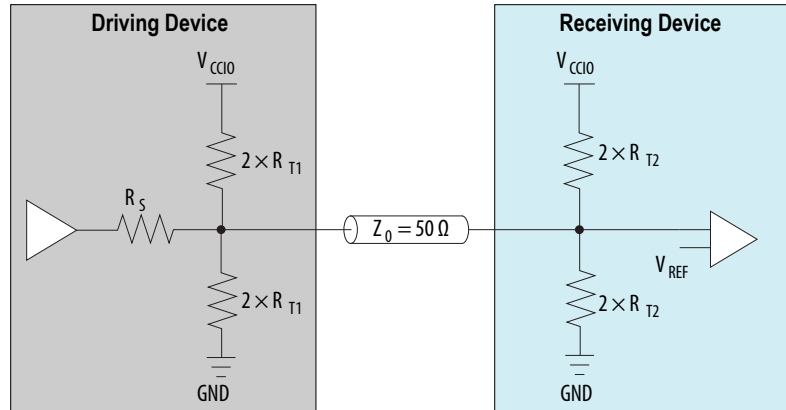


### 3.2. Single-Ended I/O Termination in Intel Agilex Devices

The Intel Agilex devices support on-chip termination for single-ended I/O standards. OCT maintains signal quality, saves board space, and reduces external component costs.

**Figure 10.  $R_S$  and  $R_T$  OCT**

This figure shows the single-ended termination schemes supported in Intel Agilex devices.  $R_{T1}$  and  $R_{T2}$  are dynamic parallel terminations and are enabled only if the device is receiving. In bidirectional applications,  $R_{T1}$  and  $R_{T2}$  are automatically switched on when the device is receiving and switched off when the device is driving.



#### 3.2.1. Single-Ended I/O Standard OCT Termination

Serial ( $R_S$ ) and parallel ( $R_T$ ) OCT provides I/O impedance matching and termination capabilities. OCT maintains signal quality, saves board space, and reduces external component costs.

The OCT calibration circuit uses the impedance of the external resistor that is connected to the RZQ pin as reference. The impedance of the I/O buffer is continuously altered until the target impedance is achieved during OCT calibration. The targeted impedance is achieved when the impedance of I/O buffer reaches a predetermined ratio to the reference resistance.

**Table 6. OCT Schemes Supported in Intel Agilex Devices**

Direction	OCT Schemes
Output	$R_S$ OCT with calibration
	$R_S$ OCT without calibration
Input	$R_T$ OCT with calibration
Bidirectional	Dynamic $R_S$ and $R_T$ OCT

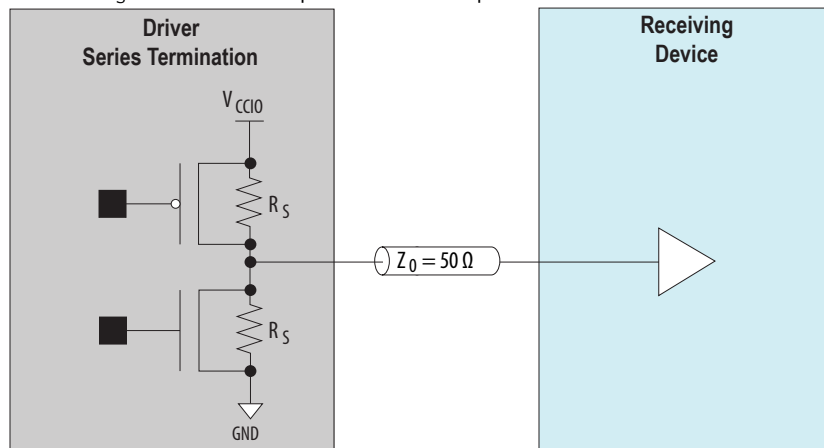
### $R_S$ OCT

The Intel Agilex devices support  $R_S$  OCT with and without calibration for single-ended and voltage-referenced I/O standards.

OCT Scheme	Description
$R_S$ without calibration	<ul style="list-style-type: none"> <li>Only supported on output buffer.</li> <li>Driver-impedance matching provides the I/O driver with controlled output impedance that closely matches the impedance of the transmission line.</li> </ul>
$R_S$ with calibration	<ul style="list-style-type: none"> <li>The OCT calibration circuit uses the impedance of the external resistor that is connected to the RZQ pin as reference. The impedance of the I/O buffer is continuously altered until the target impedance is achieved during OCT calibration. The targeted impedance is achieved when the impedance of I/O buffer reaches a predetermined ratio to the reference resistance.</li> <li>Calibration occurs at the end of device configuration. When the calibration circuit finds the correct impedance, the circuit powers down and stops changing the characteristics of the drivers.</li> <li>You may trigger re-calibration during user-mode.</li> </ul>

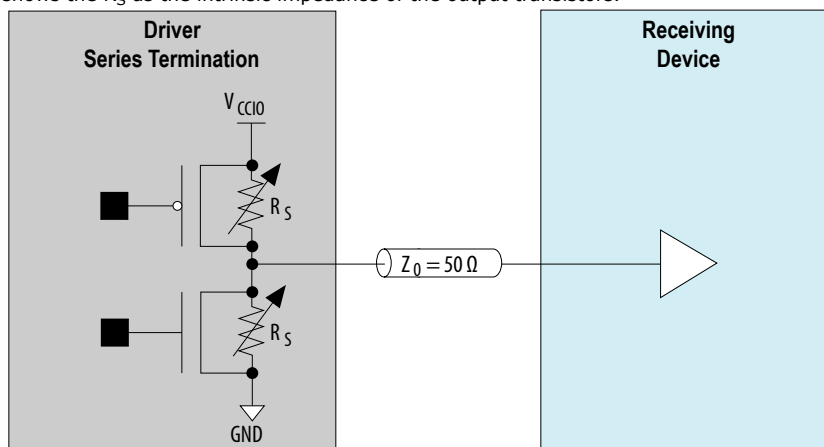
**Figure 11.  $R_S$  OCT Without Calibration**

This figure shows the  $R_S$  as the intrinsic impedance of the output transistors.



**Figure 12.  $R_S$  OCT with Calibration**

This figure shows the  $R_S$  as the intrinsic impedance of the output transistors.



**Table 7. Selectable I/O Standards for  $R_S$  OCT**

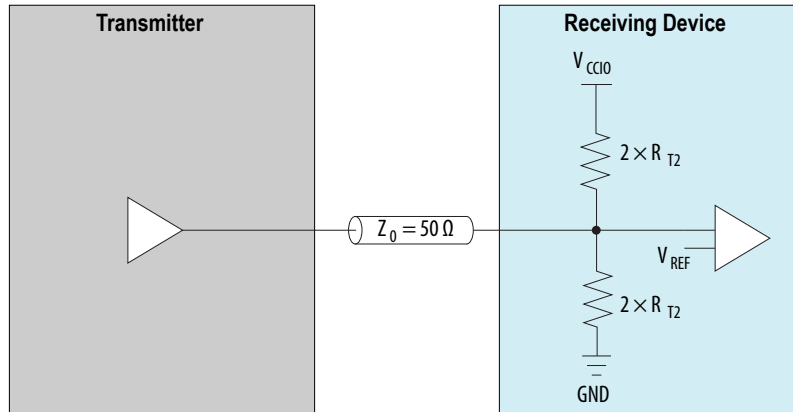
I/O Standard	$R_S$ OCT without Calibration ( $\Omega$ )	$R_S$ OCT with Calibration ( $\Omega$ )
1.2 V LVCMOS	34, 40 (Default)	34, 40
SSTL-12	34, 40 (Default)	34, 40
POD12	34 (Default), 40	34, 40
HSTL-12	34, 40 (Default)	34, 40
HSUL-12	34, 40 (Default)	34, 40
Differential SSTL-12	34, 40 (Default)	34, 40
Differential POD12	34 (Default), 40	34, 40
Differential HSTL-12	34, 40 (Default)	34, 40
Differential HSUL-12	34, 40 (Default)	34, 40

### $R_T$ OCT

$R_T$  OCT with calibration is available only for configuration of input and bidirectional pins. Output pin configurations do not support  $R_T$  OCT with calibration.

The  $R_T$  OCT calibration circuit compares the total impedance of the I/O buffer to the external resistor connected to the  $RZQ$  pin. The impedance of the I/O buffer is continuously altered until the target impedance is achieved during OCT calibration. The targeted impedance is achieved when the impedance of I/O buffer reaches a predetermined ratio to the reference resistance.

Calibration occurs at the end of the device configuration. When the calibration circuit finds the correct impedance, the circuit powers down and stops changing the characteristics of the drivers. You may trigger re-calibration during user-mode.



**Table 8. Selectable I/O Standards for  $R_T$  OCT With Calibration**

This table lists the output termination settings for calibrated OCT on different I/O standards.

I/O Standard	$R_T$ OCT with Calibration ( $\Omega$ )
SSTL-12	50, 60 $\Omega$
POD12	50, 60 $\Omega$
HSTL-12	50, 60 $\Omega$
Differential SSTL-12	50, 60 $\Omega$
Differential POD12	50, 60 $\Omega$
Differential HSTL-12	50, 60 $\Omega$

### Dynamic OCT

Dynamic OCT is useful for terminating a high-performance bidirectional path by optimizing the signal integrity depending on the direction of the data. Dynamic OCT also helps save power because termination switches on only during input operation and thus draw less static power.

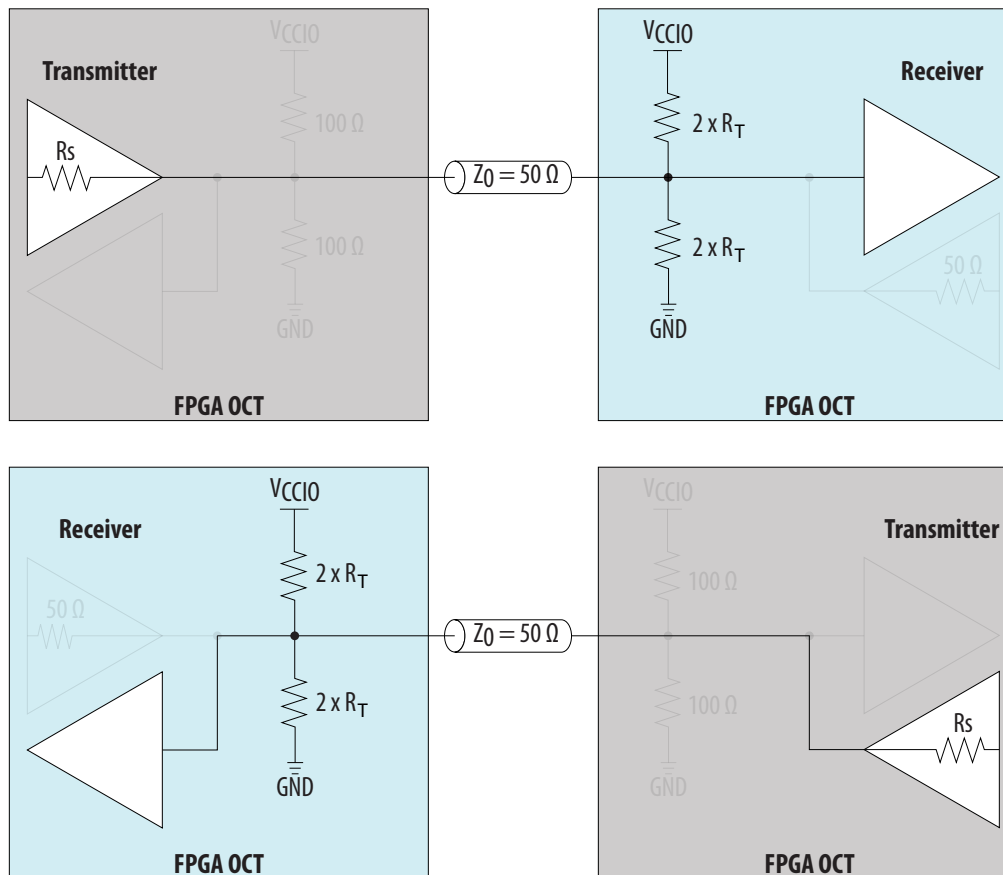
**Table 9. Dynamic OCT Based on Bidirectional I/O**

Dynamic  $R_T$  OCT or  $R_S$  OCT is enabled or disabled based on whether the bidirectional I/O acts as a receiver or driver.

Dynamic OCT	Bidirectional I/O	State
Dynamic $R_T$ OCT	Acts as a receiver	Enabled
	Acts as a driver	Disabled
Dynamic $R_S$ OCT	Acts as a receiver	Disabled
	Acts as a driver	Enabled



Figure 13. Dynamic  $R_T$  OCT in Intel Agilex Devices



### 3.2.2. OCT Calibration Block

You can calibrate the OCT using the OCT calibration block available in each I/O bank.

There is two OCT calibration block for each GPIO bank. Every OCT calibration block can calibrate the I/O buffer located in the same row but not the I/O of different row. Example, OCT calibration block in bank 2A can be used to calibrate I/O from bank 2A, 2B, 2C, and 2D but not the I/O from bank 3A, 3B, 3C, and 3D.

The OCT calibration process uses the  $RZQ$  pin that is available in every calibration block in a given I/O bank for series- and parallel-calibrated termination:

- Each OCT calibration block has an external  $240\ \Omega$  reference resistor associated with it through the  $RZQ$  pin.
- Connect the  $RZQ$  pin to GND through an external  $240\ \Omega$  resistor.
- The  $RZQ$  pin shares the same  $VCCIO\_PIO$  supply voltage with the I/O bank where the pin is located.
- The  $RZQ$  pin is a dual-purpose I/O pin and functions as a general purpose I/O pin if you do not use the calibration circuit.
- Only the 1.2 V  $VCCIO\_PIO$  bank can use the OCT calibration block.



### 3.2.3. Single-Ended I/O Standards External Termination

SSTL-12, HSTL-12, POD12 I/O standards require an input VREF and a termination voltage (VTT). The reference voltage of the receiving device tracks the termination voltage of the transmitting device.

Intel recommends that you use OCT with these I/O standards to save board space and cost. OCT reduces the number of external termination resistors used.

**Note:** You cannot use RS and RT OCT simultaneously. For more information, refer to the related information.

**Table 10. I/O Standards Required External Termination**

I/O Standard	External Termination Scheme
1.2 V LVCMOS	No on-board termination required
SSTL-12	Single-ended SSTL I/O standard termination
HSTL-12	Single-ended SSTL I/O standard termination
HSUL-12	No on-board termination required
POD12	Differential POD I/O standard termination
Differential SSTL-12	Differential SSTL I/O standard termination
Differential HSTL-12	Differential HSTL I/O standard termination
Differential HSUL-12	No on-board termination required
Differential POD12	Differential POD I/O standard termination



Figure 14. SSTL and HSTL I/O Standards External Termination

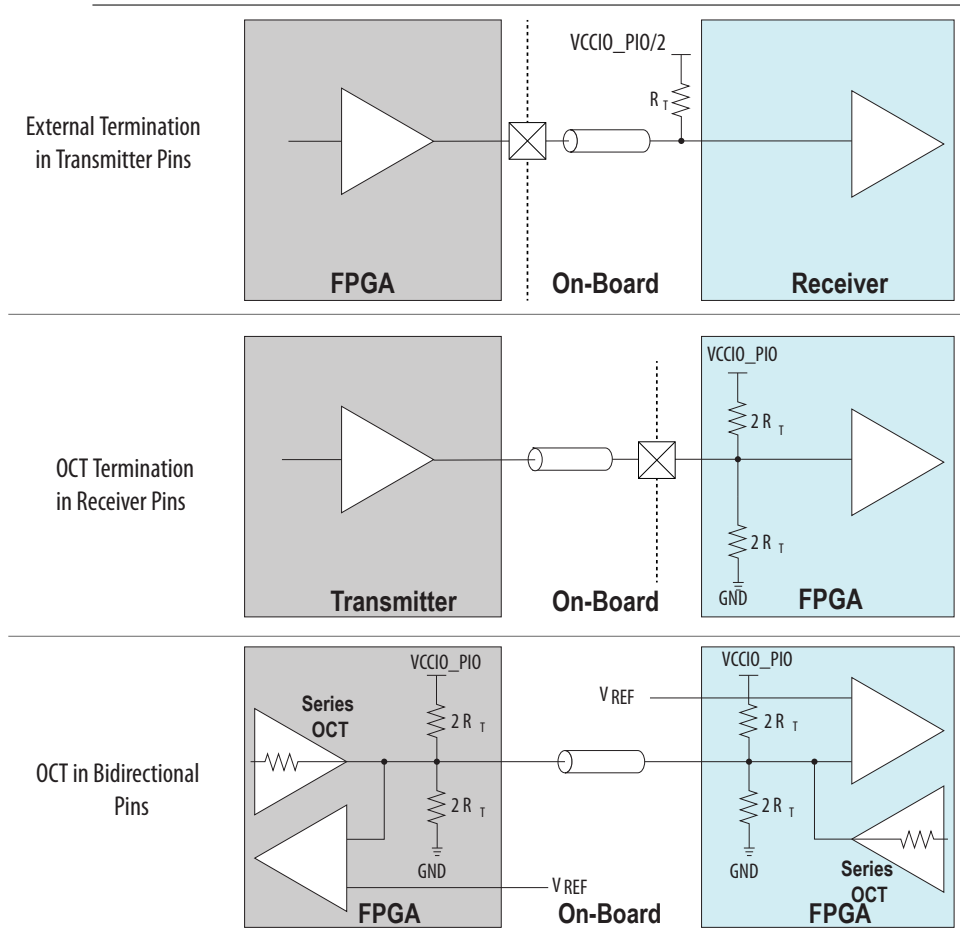
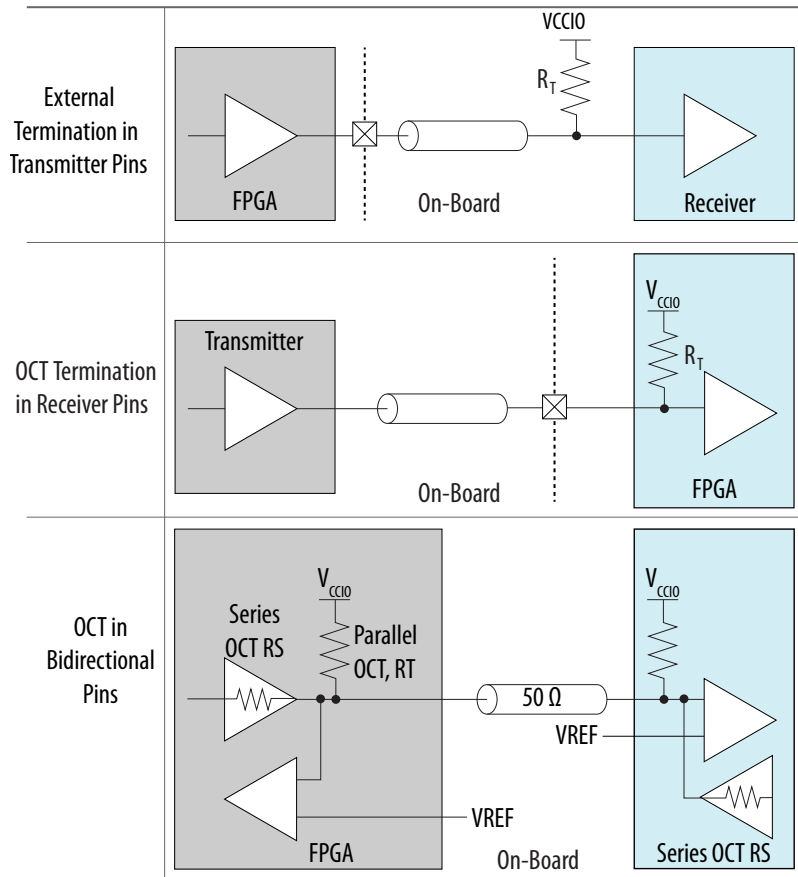
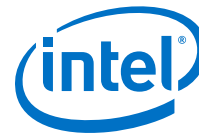


Figure 15. POD12 I/O Standard External Termination





## 4. Intel Agilex I/O Design Guidelines

---

This chapter provides the restrictions and guidelines on placement, connection requirements and clocking requirements for different functions of the GPIO pins. For more information on the each pin function, refer to the *Intel Agilex Pin Connection Guidelines*.

### Related Information

[Intel Agilex Device Family Pin Connection Guidelines](#)

### 4.1. Placement Requirements

#### I/O Pins Placement Restrictions

The following are the pin placement requirements for Intel Agilex devices:

- Only DQS pins support differential voltage referenced input standard.
- All x4 DQ group shared the same OE, Reset, and clock enable signals, therefore you cannot split the OE or Reset signals within a x4 DQ group. Refer to the Intel Agilex device pin-out files for more information on DQ groups.

#### I/O Pins Placement Guidelines

The following are guidelines for I/O standard selection and I/O bank supply compatibility check:

- Select a suitable signaling type and I/O standard for each I/O pin. The I/O banks are located in rows along the top and bottom periphery of the device. Each I/O sub-bank contains its own PLL, DPA and SERDES circuitry.
- Ensure that the selected I/O standard is supported in the targeted I/O bank.
- Place I/O pins that share voltage levels in the same I/O bank.
- Verify that all output signals in each I/O bank are intended to drive out at the bank's I/O voltage level.
- Verify that all voltage referenced signals in each I/O bank are intended to use the bank's VREF voltage level

### 4.2. Special Pins Requirement

#### RZQ Pins

There are two RZQ pins per I/O bank. When used for OCT calibration, connect a precision resistor with a  $\pm 1\%$  tolerance to this pin. The RZQ pin is a dual purpose pin, and can be used as general purpose I/O when OCT calibration is not used.

### V<sub>REF</sub> Pins

A V<sub>REF</sub> voltage is required for all voltage referenced I/O standards. Intel Agilex GPIO bank supports internal and external V<sub>REF</sub> types. The external V<sub>REF</sub> pin is a dedicated pin and, it cannot be used as a general purpose I/O pin. You must tie the pin to ground when it is not in used. Each I/O lane must share the same V<sub>REF</sub> type (internal or external V<sub>REF</sub>), and when external VREF is used, it must share the identical V<sub>REF</sub> voltage.

### Related Information

Supported I/O Standards on page 8

For more information on supported I/O standards.

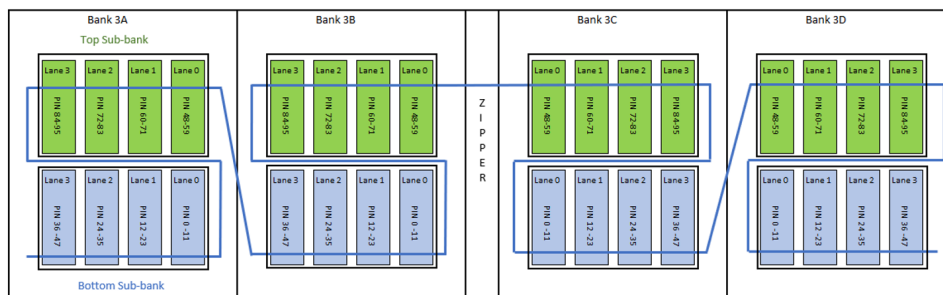
## 4.3. External Memory Interface Pin Placement Requirements

When selecting pins in the External Memory Interface grouping, all pins within the same group must be located in adjacent sub-banks.

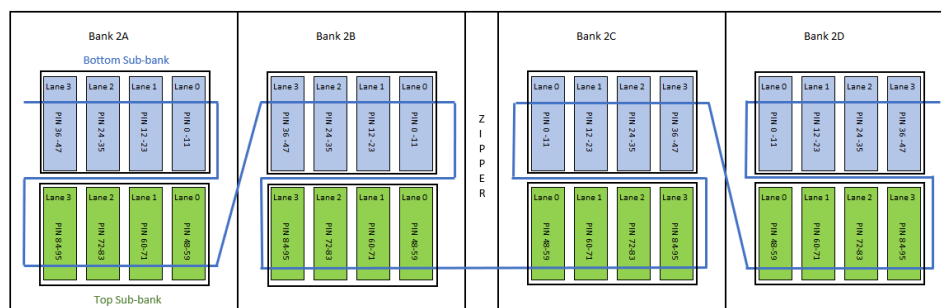
Within an I/O bank, the top sub-bank is placed near the edge of the die, and the bottom sub-bank is placed near the FPGA core.

There are interconnects between the sub-banks which chain the sub-banks into a row. The following figures show how I/O lanes in various sub-banks are chained together to form the top and bottom I/O rows in Intel Agilex AGF 012 and AGF 014 device variants, respectively. These figures represent the top view of the silicon die that corresponds to a reverse view of the device package.

**Figure 16. Sub-Bank Ordering in Top I/O Row in Intel Agilex AGF 012 and AGF 014 devices**



**Figure 17. Sub-Bank Ordering in Bottom I/O Row in Intel Agilex AGF 012 and AGF 014 devices**





The two sub-banks within an I/O bank are adjacent to each other, unless any of the sub-banks is not bonded out or partially bonded out. The blue line in the above figures shows the connectivity between the sub-banks.

For example, in the top row in Intel Agilex AGF 012 and AGF 014 devices:

- The top sub-bank in 3A is adjacent to the bottom sub-bank in 3A and the bottom sub-bank in 3B.
- The top sub-bank in 3B is adjacent to the bottom sub-bank in 3B and the top sub-bank in 3C.
  - The top sub-bank in 3B is adjacent to the top sub-bank in 3C even though there is a zipper block between the two sub-banks.
- The top sub-bank in 3B is not adjacent to the bottom sub-bank in 3A.

You can identify where a pin is located within an I/O bank based on its `Index within I/O Bank` value in the device pinout file.

#### Related Information

[Pin Placement for Differential Channels](#) on page 54

## 4.4. HPS Shared I/O Requirements

The HPS EMIF uses I/O pins located in the GPIO bank instead of HPS I/O bank. The 1.2 V `VCCIO_PIO` powers the GPIO bank instead of the 1.8 V `VCCIO_HPS`. Refer to Intel Agilex device pin-out for the location of the HPS shared GPIO pins.

## 4.5. SDM Shared I/O Requirements

AvSTx16 and AvSTx32 configuration modes use the configuration pins located in a general purpose I/O bank for device configuration instead of SDM I/O bank. The general purpose I/O bank is powered by 1.2 V `VCCIO_PIO` instead of 1.8 V `VCCIO_SDM` required by the SDM I/O bank. Refer to the *Intel Agilex Configuration User Guide* for more details on the I/O setting of the pins during device configuration.

#### Related Information

[Intel Agilex Configuration User Guide](#)

## 4.6. Configuration Pins

You must adhere to configuration pin connections requirement and ensure that the pull-up and pull-down resistors are set correctly for your configuration schemes. Refer to *Intel Agilex Pin Connection Guidelines* for detailed pin connection of each configuration pin.

## 4.7. Unused Pins

There are specific guidelines for unused pins connections and reserved state settings. Intel Agilex devices support several options of reserved state settings, to allow flexibility in the board design.



### No Connect (NC) Pins

For vertical device migration, where the device package is the same but contains different density, you can leave the NC pins floating or connect to  $V_{CCIO}$  or to ground. You can refer to the device pin-out files for a list of NC pins.

### Do Not Use (DNU) Pins

Do not connect these pins to power, ground, or any other signal. DNU pins must be left floating.

### Related Information

[Intel Agilex Device Pin Connection Guidelines](#)

## 4.8. Guidelines for GPIO Pins During Power Sequencing

Intel Agilex devices do not support hot-socketing and require a specific power-up sequence. Design your power supply solution to properly control the complete power sequence. Refer to the *Intel Agilex Power Management User Guide* for more information on power sequence requirement for Intel Agilex devices.

Adhere to the following guidelines to prevent unnecessary current draw on the GPIO pins:

- During device power-up, the GPIO pins can tolerate a tri-state, drive to ground or drive to  $V_{CCIO\_PIO}$  condition.
- During device power-down and without power condition, the GPIO pins can tolerate a maximum of 10 mA per pin and a total of 100 mA per GPIO bank. The voltage level must not exceed 1.2 V.

## 4.9. Maximum DC Current Restrictions

There are no restrictions on the maximum DC current of any 10 consecutive I/O pins for Intel Agilex devices.

Intel Agilex devices conform to the  $V_{CCIO}$  Electro-Migration (EM) rule and IR drop targets for all I/O standard drive strength settings—ensuring reliability over the lifetime of the devices.

## 4.10. 1.2 V I/O Interface Voltage Level Compatibility

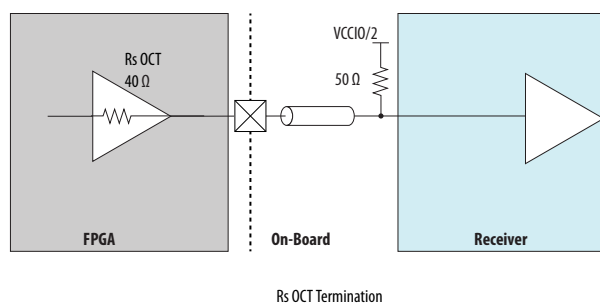
Evaluate the electrical signal level compatibility between Intel Agilex 1.2 V output and the downstream device to ensure the 1.2 V output buffer  $V_{oh}$  and  $V_{ol}$  voltages are within the downstream's receiving buffer's  $V_{ih}$  and  $V_{il}$  specifications.

The following examples showcase Intel Agilex 1.2 V output voltage swing calculations:



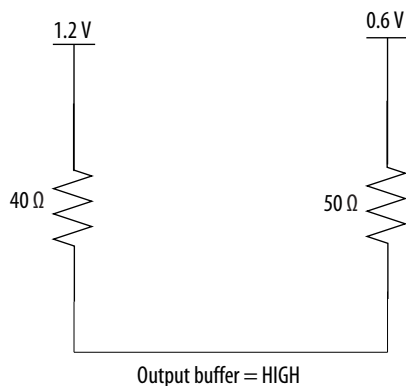
- Example 1:
  - When using 1.2 V LVCMOS, the output signal swings from 0 V to 1.2 V on a lossless transmission line with no external pull-up or pull-down component. You must ensure the  $V_{IH}$  or  $V_{IL}$  tolerance of the downstream connecting device is able to meet those conditions.
- Example 2:
  - When using 1.2V voltage referenced I/O standards, the output signal swing has a dependency on the external board termination or the receiver's internal termination. The following diagram shows an example termination setup and its equivalent circuit.

**Figure 18. Termination Setup using 40 Ω RS OCT Driver with On-Board 50 Ω Pull-Up Resistor to VCCIO/2**



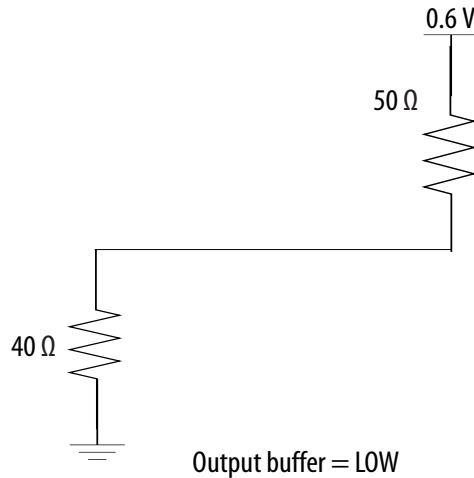
When output buffer is driving HIGH, pin voltage is 0.93 V based on voltage divider rule.

**Figure 19. Equivalent Circuit of Example 2 with Output Buffer Driving HIGH**



When output buffer is driving LOW, pin voltage is 0.27 V based on voltage divider rule.

**Figure 20. Equivalent Circuit of Example 2 with Output Buffer Driving LOW**



## 4.11. I/O Simulation

### 4.11.1. HSPICE Models

Intel Agilex devices provide a SPICE model which you can use to perform system-level simulations for various configurations.

The SPICE kits provide models that support a wide variety of I/O features across process, voltage, and temperature (PVT). Each SPICE kit contains the following information:

- Encrypted transistor and logic cell library models
- Encrypted input or output buffer circuit models for single-ended and differential I/O
- Single-ended and differential sample SPICE decks
- User guide describing the model usage

The HSPICE models provide options to simulate buffer behavior for following I/O feature:

- RS OCT with and without calibration
- RT OCT with calibration
- Internal weak pull-up
- Open drain
- Bus-hold

## 5. Intel Agilex High-Speed SERDES I/O Architecture

### 5.1. Intel Agilex High-Speed SERDES I/O Overview

Intel Agilex devices support LVDS serializer/deserializer (SERDES) through the 1.5 V True Differential Signaling I/O banks.

These devices support SERDES on all 1.5 V True Differential Signaling I/O banks with the following features :

- Differential 100-ohm OCT  $R_D$
- Differential I/O reference clock for the I/O PLL that drives the SERDES
- Dedicated transmitter and dedicated receiver differential pin pairs in each I/O bank
- 24 receiver channels with SERDES and DPA, and 24 transmitter channels with SERDES in each I/O bank

The total of SERDES channel count vary among Intel Agilex devices depending on the total pins available in the package.

**Table 11. Usage Modes Summary of the Intel Agilex High-Speed SERDES**

All usage modes in this table support SERDES factors of 3 to 10.

Usage Mode	Quick Guideline
Transmitter	In this mode, the SERDES block acts as a serializer.
DPA Receiver	<ul style="list-style-type: none"> <li>• The dynamic phase alignment block (DPA) automatically adjusts the clock phase to achieve optimal data-to-clock skew.</li> </ul>
Non-DPA Receiver	<ul style="list-style-type: none"> <li>• This mode is useful for source-synchronous clocking applications.</li> <li>• You must manage the data-to-clock skew.</li> </ul>
Soft-CDR Receiver	<ul style="list-style-type: none"> <li>• The soft clock data recovery (soft-CDR) mode is useful for asynchronous clocking applications.</li> <li>• An asynchronous clock drives the LVDS SERDES IP core. The IP core outputs a recovered clock from the received data.</li> </ul>
Bypass the SERDES	<p>You can bypass the serializer to use SERDES factor of 2 by using the GPIO IP core:</p> <ul style="list-style-type: none"> <li>• Single data rate (SDR) mode—you do not require clocks.</li> <li>• Double data rate (DDR) mode—useful for slow source-synchronous clocking applications.</li> </ul>

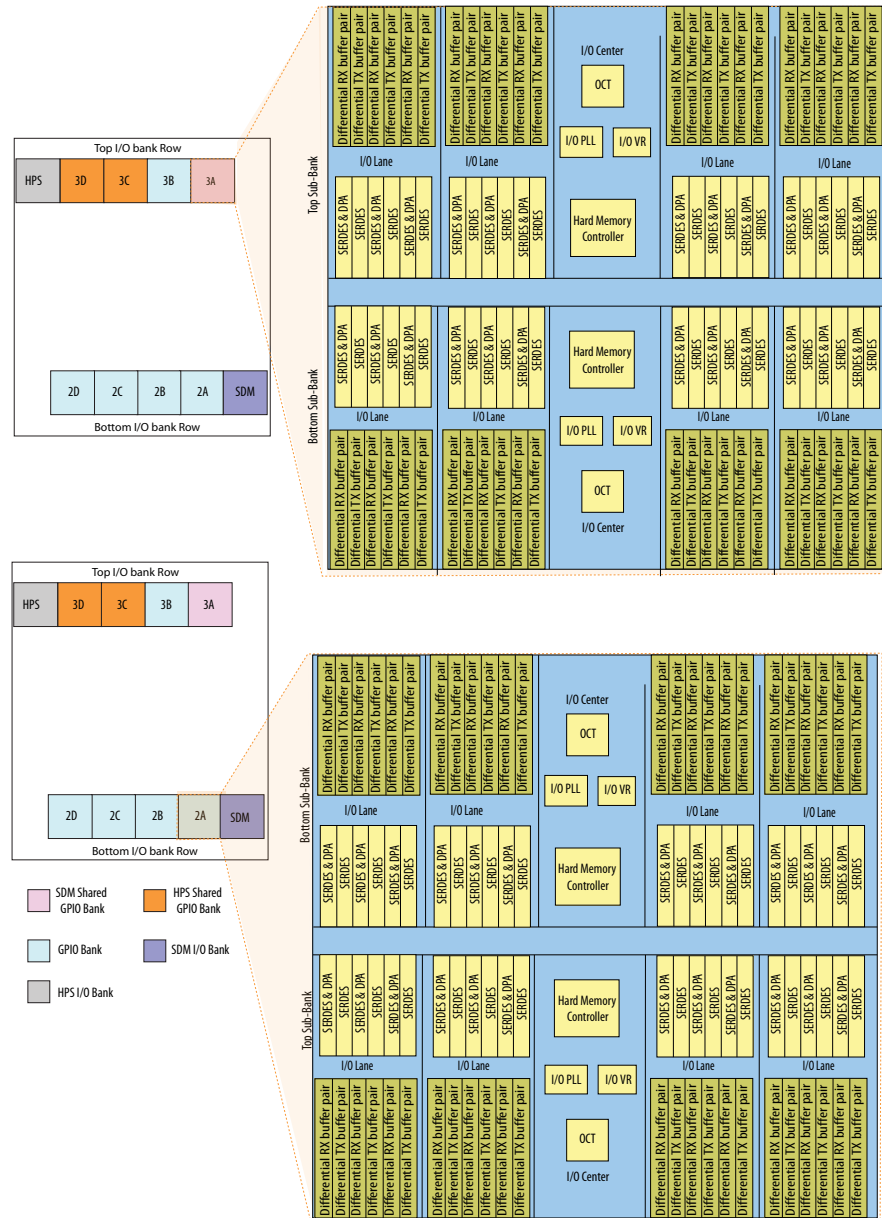
#### 5.1.1. High-Speed SERDES Architecture

Each GPIO bank in Intel Agilex devices consists of two I/O sub-banks. Each I/O sub-bank consists of the following components:

- 12 pairs of dedicated SERDES transmitter channels.
- 12 pairs of dedicated SERDES receiver channels that support DPA and non-DPA modes. Four pairs from the top sub-bank and eight pairs from the bottom sub-bank dedicated SERDES receiver channels support Soft-CDR mode. Refer to the Intel Agilex device pin-out files for the exact location of the Soft-CDR pins.

The SERDES transmitter and receiver channels are adjacent to each other. Refer to the Intel Agilex device pin-out files for the exact location of the SERDES pins.

Figure 21. Intel Agilex I/O Subsystem (Bottom View)

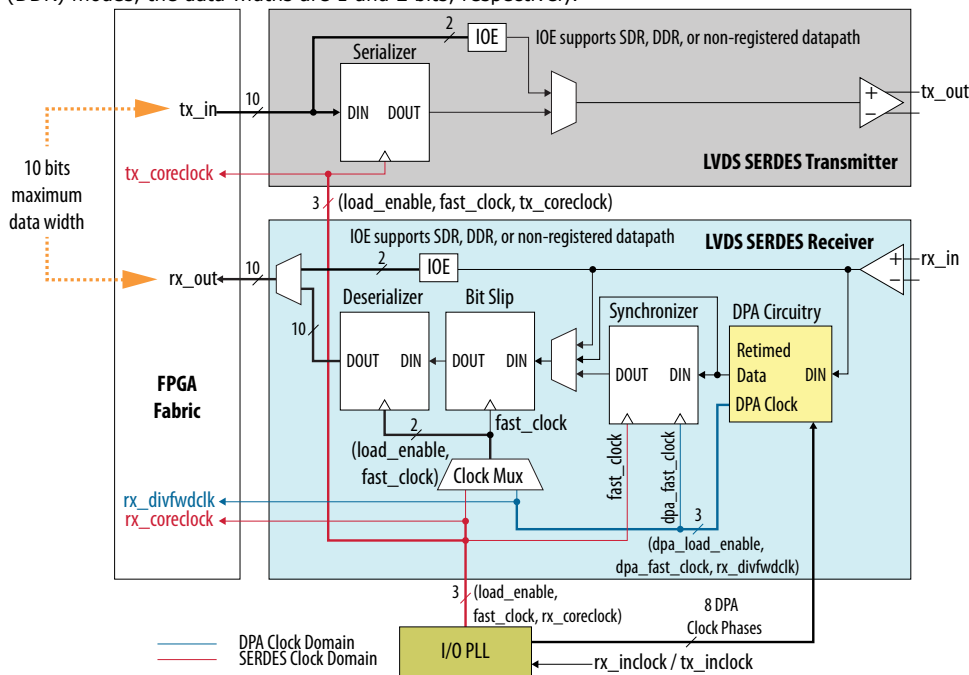


Different device package has different I/O banks offering. Refer device pin-out files for available bank location for each device package.



**Figure 22. SERDES Circuitry**

This figure shows a transmitter and receiver block diagram for the SERDES circuitry with the interface signals of the transmitter and receiver data paths. The figure shows a transmitter and a receiver sharing an I/O PLL as they are in the same sub-bank and using the same I/O PLL resource. In single data rate (SDR) and double data rate (DDR) modes, the data widths are 1 and 2 bits, respectively.



**Table 12. Supported Blocks and Modes for Data and Clock Path**

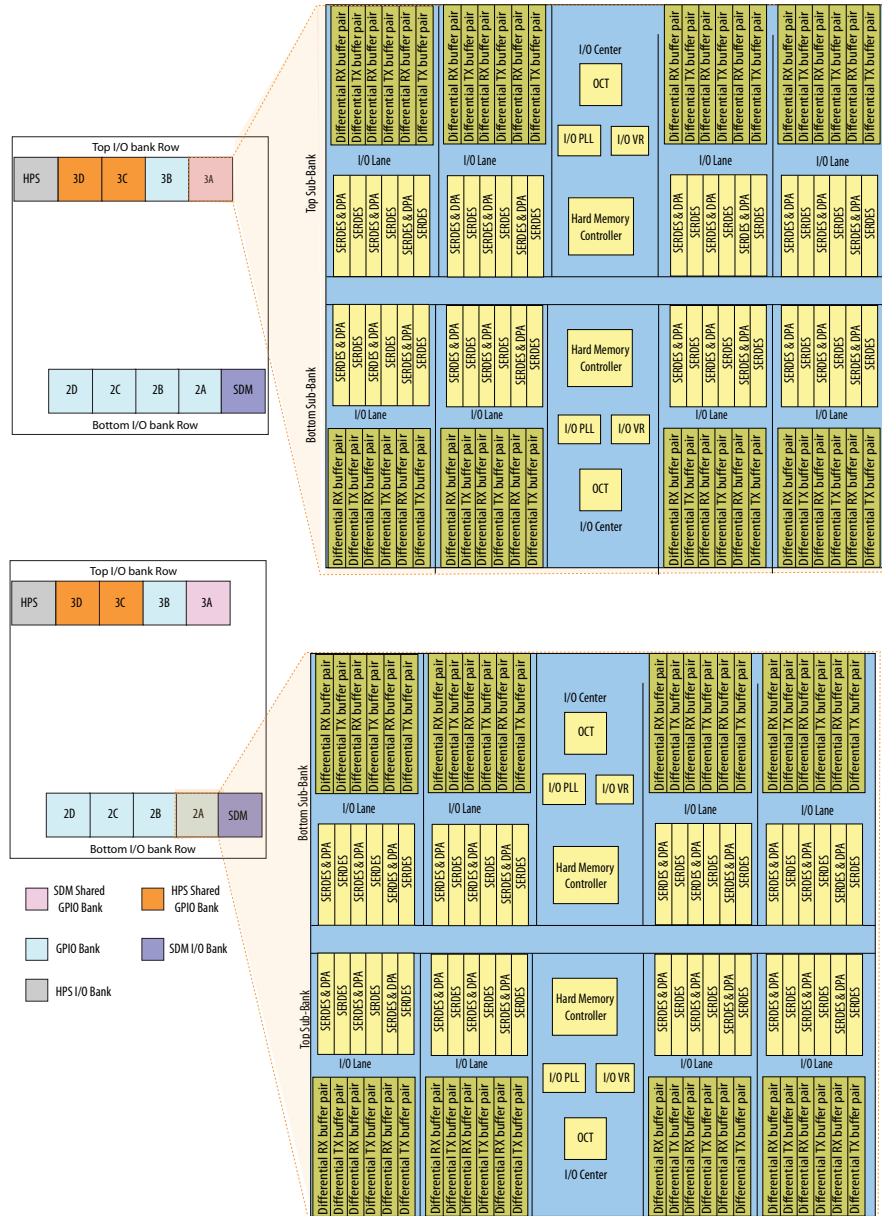
Path	Mode	Block	Clock Domain
TX Data Path	TX	Serializer	SERDES clock domain
RX Data Path	DPA-FIFO	DPA	DPA clock domain
		Synchronizer	DPA-SERDES clock domain crossing
		Bitslip	SERDES clock domain
		Deserializer	SERDES clock domain
	Soft-CDR	DPA	DPA clock domain
		Bitslip	DPA clock domain
Deserializer		DPA clock domain	

### 5.1.2. Intel Agilex GPIO Banks, SERDES, and DPA Locations

The I/O banks are located at the top and bottom I/O rows respectively. Each I/O bank contains two I/O sub-banks and each I/O sub-bank contains its own PLL, dynamic phase alignment (DPA), and SERDES circuitry blocks.

**Figure 23. I/O Bank Structure with I/O PLL, DPA, and SERDES (Bottom View)**

This figure shows an example of I/O banks in Intel Agilex AGF 012 and AGF 014 devices. The I/O banks availability and locations vary among Intel Agilex devices.



Different device packages have a different number of I/O banks. Refer to the device pin-out files for available bank location for each device package.



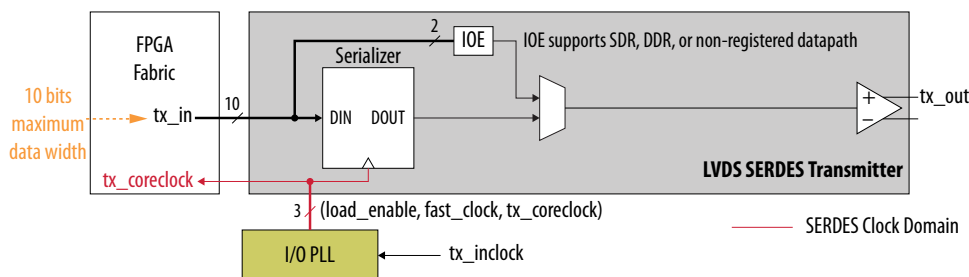
## 5.2. Intel Agilex LVDS SERDES Transmitter

### 5.2.1. LVDS SERDES Transmitter Blocks

The dedicated circuitry consists of a true differential buffer, a serializer, and I/O PLLs that you can share between the SERDES transmitter and receiver. The serializer takes up to 10 bits wide parallel data from the FPGA fabric. It clocks the data into the load registers, and serializes the data using shift registers that are clocked by the I/O PLL sending the data to the differential buffer. The MSB of the parallel data is transmitted first.

**Note:** The PLL that drives the SERDES channel must operate in integer PLL mode. You do not need a PLL if you bypass the serializer.

**Figure 24. LVDS SERDES Transmitter**



**Table 13. Dedicated Circuitry and Features of the LVDS SERDES Transmitter**

Dedicated Circuitry / Feature	Description
Differential I/O buffer	Supports 1.5 V True Differential Signaling I/O standard which is compatible with LVDS, RSDS, and Mini-LVDS.
SERDES	3 to 10-bit wide serializer
Phase-locked loops (PLLs)	Clocks the load and shift registers
Programmable $V_{OD}$	Adjusts the output voltage swing
Programmable pre-emphasis	Boosts output current

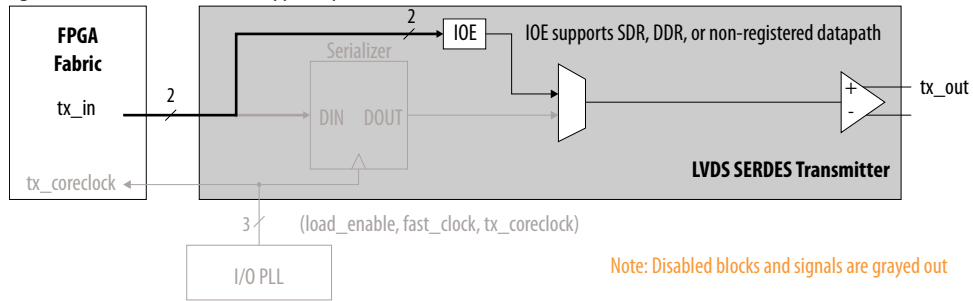
### 5.2.2. Serializer Bypass for DDR and SDR Operations

The I/O element (IOE) contains two data output registers that can each operate in either DDR or SDR mode.

You can bypass the serializer to support DDR (x2) and SDR (x1) operations to achieve a serialization factor of 2 and 1, respectively.

**Figure 25. Serializer Bypass**

This figure shows the serializer bypass path.



- In SDR mode:
  - The IOE data width is 1 bit.
  - Registered output path requires a clock.
  - Data is passed directly through the IOE.
- In DDR mode:
  - The IOE data width is 2 bits.
  - The GPIO IP core requires a clock.
  - tx\_inclock clocks the IOE register.

### 5.2.3. Serializer

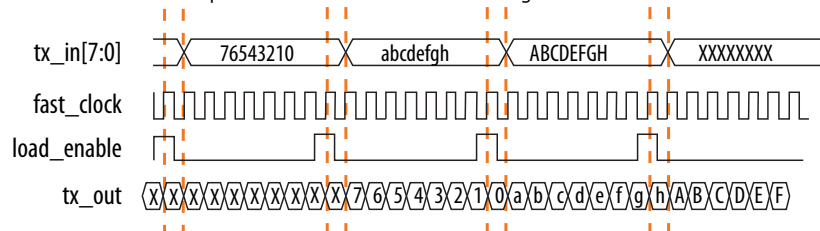
The serializer consists of two sets of registers.

The first set of registers captures the parallel data from the core using the LVDS fast clock. The load\_enable clock is provided alongside the LVDS fast clock, to enable these capture registers once in each coreclock period.

After the data is captured, it is loaded into a shift register that shifts the LSB towards the MSB at one bit per fast clock cycle. The MSB of the shift register feeds the LVDS output buffer. Therefore, higher order bits precede lower order bits in the output bitstream.

**Figure 26. LVDS SERDES x8 Serializer Bit Position**

This figure shows the waveform specific to serialization factor of eight.



**Table 14. LVDS SERDES Serializer Signals**

Signal	Description
tx_in[7:0]	Data for serialization

*continued...*





Signal	Description
	(Supported serialization factors: 3–10)
fast_clock	Clock for the transmitter
load_enable	Enable signal for serialization
tx_out	LVDS output data stream

### 5.2.4. Differential I/O Bit Position

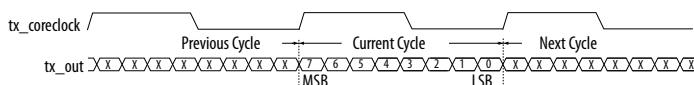
Data synchronization is necessary for successful data transmission at high frequencies.

**Figure 27. Bit-Order and Word Boundary for One Differential Channel**

This figure shows the data bit orientation for a channel operation and is based on the following conditions:

- The serialization factor is equal to the clock multiplication factor.
- The phase alignment uses edge alignment.
- The operation is implemented in hard SERDES.

**Transmitter Channel Operation (x8 Mode)**



Note: These waveforms are only functional waveforms and do not convey timing information

**Table 15. Differential Bit Naming**

This table lists the conventions for differential bit naming for 12 differential channels. The MSB and LSB positions increase with the number of channels used in a system.

Receiver Channel Data Number	Internal 8-Bit Parallel Data	
	MSB Position	LSB Position
1	7	0
2	15	8
3	23	16
4	31	24
5	39	32
6	47	40
7	55	48
8	63	56
9	71	64
10	79	72
11	87	80
12	95	88

### 5.2.5. Clocking Differential Transmitters

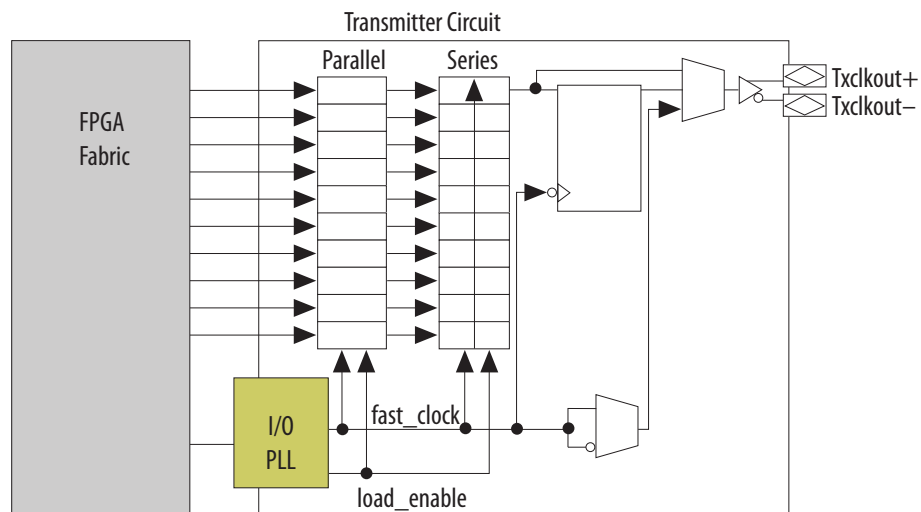
The I/O PLL generates the load enable (`load_enable`) signal and the `fast_clock` signal (the clock running at serial data rate) that clocks the load and shift registers. You can statically set the serialization factor to x3, x4, x5, x6, x7, x8, x9, or x10 using the Intel Quartus® Prime software. The load enable signal is derived from the serialization factor setting.

You can configure any Intel Agilex transmitter data channel to generate a source-synchronous transmitter clock output. This flexibility allows the placement of the output clock near the data outputs to simplify board layout and reduce clock-to-data skew.

Different applications often require specific clock-to-data alignments or specific data-rate-to-clock-rate factors. You can specify these settings statically in the Intel Quartus Prime parameter editor:

- The transmitter can output a clock signal at the same rate as the data with a maximum output clock frequency that each speed grade of the device supports.
- You can divide the output clock by a factor of 1, 2, 4, 6, 8, or 10, depending on the serialization factor.
- You can set the phase of the clock in relation to the data at 0° or 180° (edge- or center-aligned). The I/O PLLs provide additional support for other phase shifts in 45° increments.

**Figure 28. Transmitter in Clock Output Mode**



## 5.3. Intel Agilex LVDS SERDES Receiver

### 5.3.1. LVDS SERDES Receiver Blocks

The receiver has a differential buffer and I/O PLLs that you can share among the transmitter and receiver, a DPA block, a synchronizer, a data realignment block, and a deserializer. The 1.5 V True Differential Signaling buffer can receive LVDS, mini-LVDS,



RSDS, and LVPECL compatible signaling. You can statically set the I/O standard of the receiver pins to 1.5 V True Differential Signaling in the Intel Quartus Prime software Assignment Editor or .qsf file.

**Note:** The PLL that drives the SERDES channel must operate in integer PLL mode. You do not need a PLL if you bypass the deserializer

**Table 16. Dedicated Circuitry and Features of the LVDS SERDES Receiver**

Dedicated Circuitry / Feature	Description
Differential I/O buffer	Supports 1.5V True Differential Signaling compatible with LVDS, RSDS, Mini-LVDS, and LVPECL
SERDES	Up to 10-bit wide deserializer
Phase-locked loops (PLLs)	Generates different phases of a clock for data synchronizer
Data realignment (Bit slip)	Inserts bit latencies into serial data
DPA	Chooses a phase closest to the phase of the serial data
Synchronizer (FIFO buffer)	Compensate for phase differences between the data and the receiver's input reference clock
Skew adjustment	Manual
On-chip termination (OCT)	100 Ω in 1.5 V True Differential Signaling I/O standards

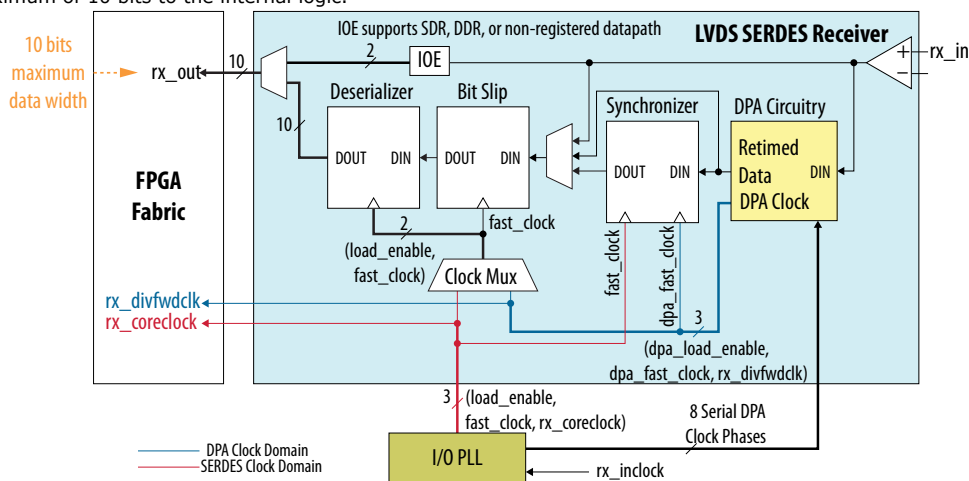
### 5.3.1.1. Receiver Blocks in Intel Agilex Devices

The Intel Agilex LVDS SERDES receiver has the following hardware blocks:

- DPA block
- Synchronizer
- Data realignment block (bit slip)
- Deserializer

**Figure 29. Receiver Block Diagram**

This figure shows the hardware blocks of the receiver. In SDR and DDR modes, the data width from the IOE is 1 and 2 bits, respectively. The deserializer includes shift registers and parallel load registers, and sends a maximum of 10 bits to the internal logic.

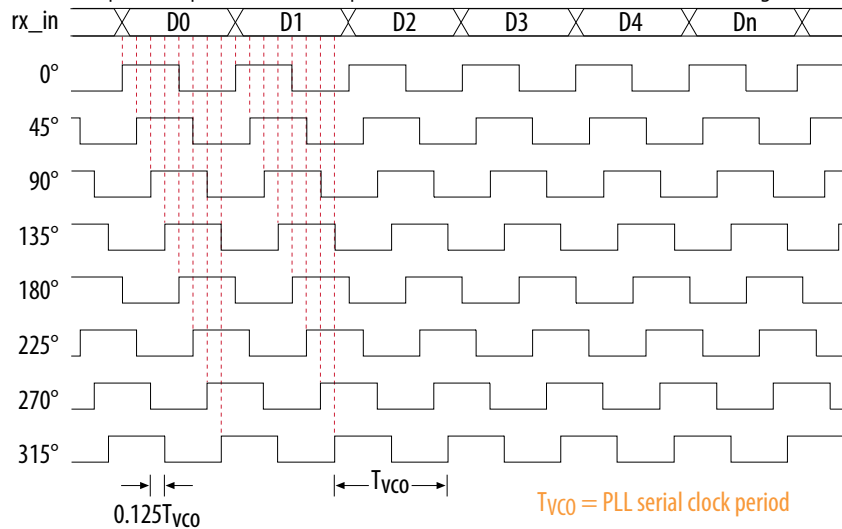


### 5.3.1.1.1. DPA Block

The DPA block takes in high-speed serial data from the differential input buffer and selects one of the eight phases that the I/O PLLs generate to sample the data. The DPA chooses a phase closest to the phase of the serial data. The maximum phase offset between the received data and the selected phase is  $1/8$  unit interval (UI)<sup>(3)</sup>, which is the maximum quantization error of the DPA. The eight phases of the clock are equally divided, offering a  $45^\circ$  resolution.

**Figure 30. DPA Clock Phase to Serial Data Timing Relationship**

This figure shows the possible phase relationships between the DPA clocks and the incoming serial data.



The DPA block continuously monitors the phase of the incoming serial data and selects a new clock phase if required. You can prevent the DPA from selecting a new clock phase by asserting the optional `rx_dpa_hold` port, which is available for each channel.

DPA circuitry does not require a fixed training pattern to lock to the optimum phase out of the eight phases. After reset or power up, the DPA circuitry requires transitions on the received data to lock to the optimum phase. An optional output port, `rx_dpa_locked`, is available to indicate an initial DPA lock condition to the optimum phase after power up or reset. Use data checkers such as a cyclic redundancy check (CRC) or diagonal interleaved parity (DIP-4) to validate the data.

An independent reset port, `rx_dpa_reset`, is available to reset the DPA circuitry. You must retrain the DPA circuitry after reset.

**Note:** The DPA block is bypassed in non-DPA mode.

(3) The unit interval is the period of the clock running at the serial data rate (fast clock).



### 5.3.1.1.2. Synchronizer (DPA FIFO)

The synchronizer is a one-bit wide and six-bit deep FIFO buffer that compensates for the phase difference between `dpa_fast_clock` from the DPA block and the `fast_clock` that the I/O PLLs produce. The synchronizer can only compensate for phase differences, not frequency differences, between the data and the receiver's input reference clock.

An optional port, `rx_fifo_reset`, is available to the internal logic to reset the synchronizer. The synchronizer is automatically reset when the DPA first locks to the incoming data. Use `rx_fifo_reset` to reset the synchronizer when the data checker indicates that the received data is corrupted.

**Note:** The synchronizer circuit is bypassed in non-DPA and soft-CDR mode.

### 5.3.1.1.3. Data Realignment Block (Bit Slip)

Skew in the transmitted data, along with skew added by the link, causes channel-to-channel skew on the received serial data streams. If you enable the DPA, the received data is captured with different clock phases on each channel. This difference may cause misalignment of the received data from channel to channel. To compensate for this channel-to-channel skew and establish the correct received word boundary at each channel, each receiver channel has a dedicated data realignment circuit that realigns the data by inserting bit latencies into the serial stream.

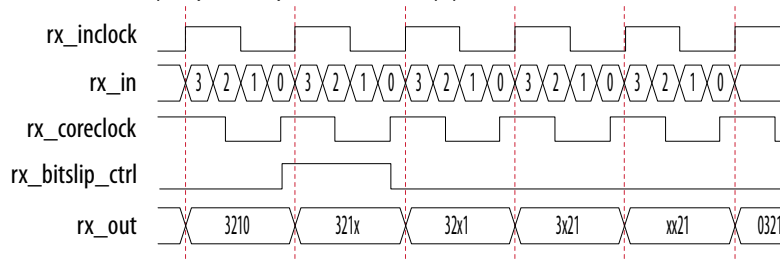
An optional `rx_bitslip_ctrl` port controls the bit insertion of each receiver independently controlled from the internal logic. The data slips one bit on the rising edge of `rx_bitslip_ctrl`. The requirements for the `rx_bitslip_ctrl` signal include the following items:

- The minimum pulse width is one period of the parallel clock in the logic array.
- The minimum low time between pulses is one period of the parallel clock.
- The signal is an edge-triggered signal.
- The valid data is available four parallel clock cycles after the rising edge of `rx_bitslip_ctrl`.

The MSB from the serial data is not the MSB of the parallel data. You can use bit slip to set the proper word boundary on the parallel data.

**Figure 31. Data Realignment Timing**

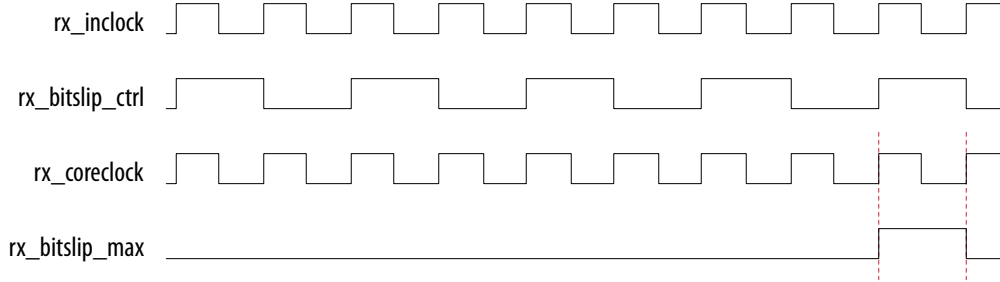
This figure shows receiver output (`rx_out`) after one bit slip pulse with the deserialization factor set to 4.



The data realignment circuit has a bit slip rollover value set to the deserialization factor. An optional status port, `rx_bitslip_max`, is available to the FPGA fabric from each channel to indicate the reaching of the preset rollover point.

**Figure 32. Receiver Data Realignment Rollover**

This figure shows a preset value of four bit cycles before rollover occurs. The rx\_bitslip\_max signal pulses for one rx\_coreclock cycle to indicate that rollover has occurred.



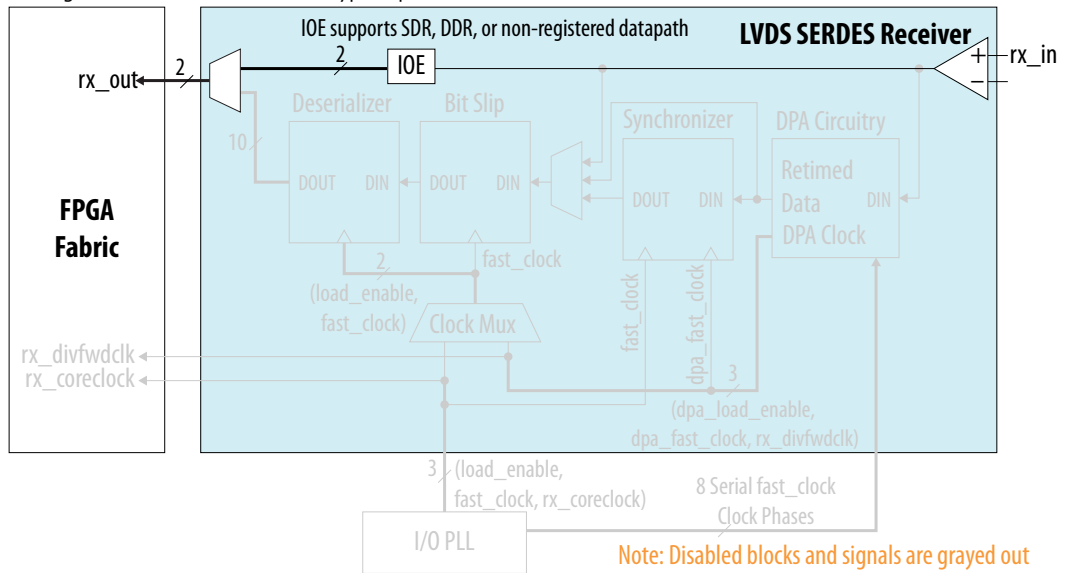
### 5.3.1.1.4. Deserializer

You can statically set the deserialization factor to x3, x4, x5, x6, x7, x8, x9, or x10 by using the Intel Quartus Prime software.

The IOE contains two data input registers that can operate in DDR or SDR mode. You can bypass the deserializer to support DDR (x2) and SDR (x1) operations.

**Figure 33. Deserializer Bypass**

This figure shows the deserializer bypass path.





- If you bypass the deserializer in SDR mode:
  - The IOE data width is 1 bit.
  - Registered input path requires a clock.
  - Data is passed directly through the IOE.
- If you bypass the deserializer in DDR mode:
  - The IOE data width is 2 bits.
  - `rx_inclock` clocks the IOE register. The clock must be synchronous to `rx_in`.
  - You must control the data-to-clock skew.

You cannot use the DPA and data realignment circuit when you bypass the deserializer.

### 5.3.2. Clocking LVDS SERDES Receivers

The I/O PLL receives the external clock input and generates different phases of the same clock. The DPA block automatically chooses one of the clocks from the I/O PLL and aligns the incoming data on each channel.

The synchronizer circuit is a 1-bit wide by 6-bit deep FIFO buffer that compensates for any phase difference between the DPA clock and the data realignment block. If necessary, the user-controlled data realignment circuitry inserts a single bit of latency in the serial bit stream to align to the word boundary. The deserializer includes shift registers and parallel load registers, and sends a maximum of 10 bits to the internal logic.

The physical medium connecting the transmitter and receiver SERDES channels may introduce skew between the serial data and the source-synchronous clock. The instantaneous skew between each SERDES channel and the clock also varies with the jitter on the data and clock signals as seen by the receiver. The three different modes—non-DPA, DPA, and soft-CDR—provide different options to overcome skew between the source synchronous clock (non-DPA, DPA) /reference clock (soft-CDR) and the serial data.

Non-DPA mode allows you to statically select the optimal phase between the source synchronous clock and the received serial data to compensate skew. In DPA mode, the DPA circuitry automatically chooses the best phase to compensate for the skew between the source synchronous clock and the received serial data. Soft-CDR mode provides opportunities for synchronous and asynchronous applications for chip-to-chip and short reach board-to-board applications for SGMII protocols.

*Note:* Only the non-DPA mode requires manual skew adjustment.

### 5.3.3. LVDS SERDES Receiver Modes

The Intel Agilex devices support the following receiver modes:

- Non-DPA mode
- DPA mode
- Soft-CDR mode

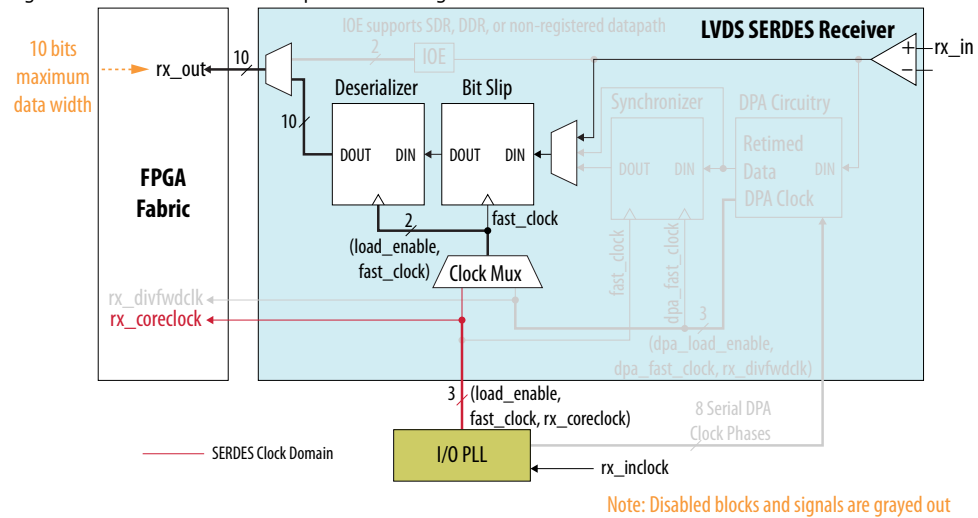
### 5.3.3.1. Non-DPA Mode

The non-DPA mode disables the DPA and synchronizer blocks. Input serial data is registered at the rising edge of the serial `fast_clock` clock that is produced by the I/O PLLs.

The `fast_clock` clock that is generated by the I/O PLLs clocks the data realignment and deserializer blocks.

**Figure 34. Receiver Datapath in Non-DPA Mode**

This figure shows the non-DPA datapath block diagram.



### 5.3.3.2. DPA Mode

The DPA block chooses the best possible clock (`dpa_fast_clock`) from the eight fast clocks produced by the I/O PLL.

This serial `dpa_fast_clock` clock is used for writing the serial data into the synchronizer. A serial `fast_clock` clock is used for reading the serial data from the synchronizer. The same `fast_clock` clock is used in data realignment and deserializer blocks.

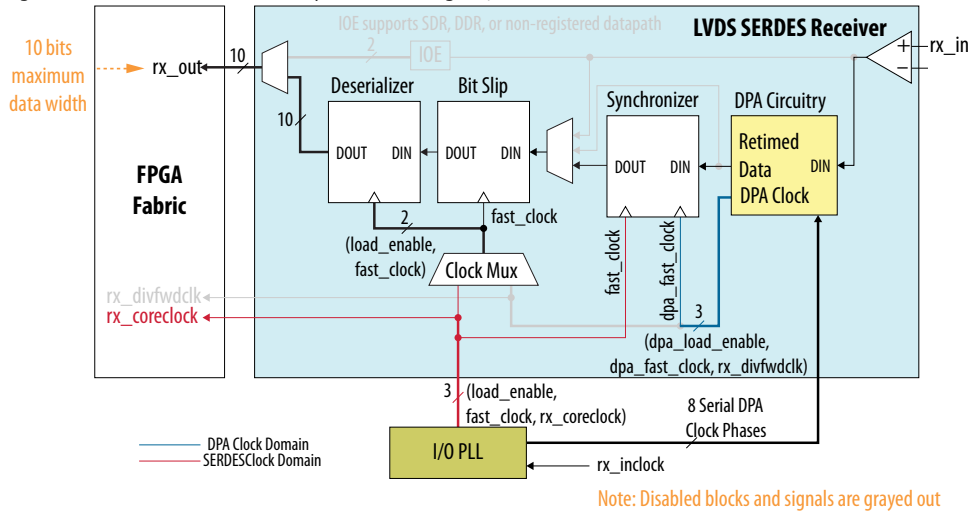
In DPA mode, the DPA FIFO synchronizes the re-timed data to the high-speed SERDES clock domain. The DPA clock may shift phase during the initial lock period. To avoid data run-through condition caused by the FIFO write pointer creeping up to the read pointer, hold the FIFO in reset state until the DPA locks.





**Figure 35. Receiver Datapath in DPA Mode**

This figure shows the DPA mode datapath. In the figure, all the receiver hardware blocks are active.



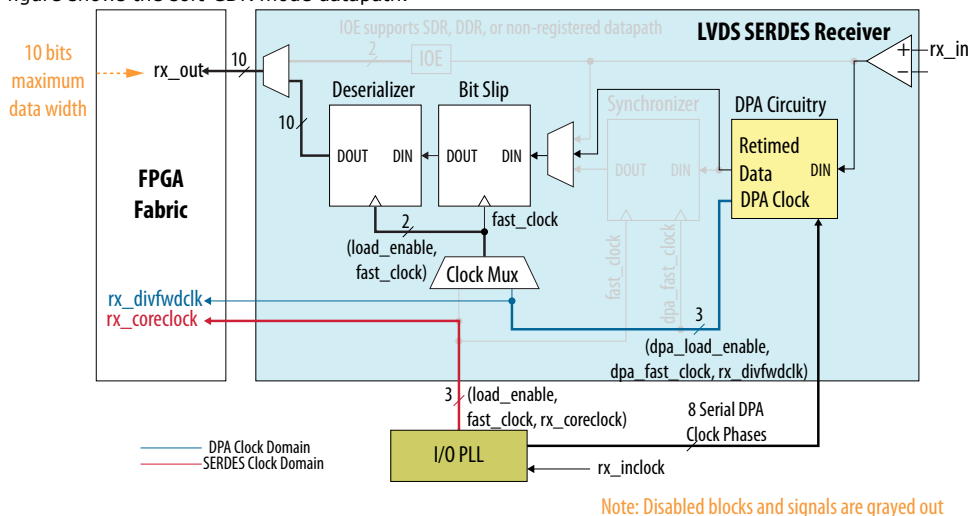
**Note:** In DPA mode, you must place all receiver channels of a SERDES instance in one I/O sub-bank. Because each I/O sub-bank has a maximum of 12 1.5 V True Signaling I/O buffer receiver pairs, each SERDES instance can support a maximum of 12 DPA channels.

### 5.3.3.3. Soft-CDR Mode

The Intel Agilex SERDES channel offers the soft-CDR mode to support the GbE and SGMII protocols. A receiver PLL uses the local clock source for reference.

**Figure 36. Receiver Datapath in Soft-CDR Mode**

This figure shows the soft-CDR mode datapath.



In soft-CDR mode, the synchronizer block is inactive. The DPA circuitry selects an optimal DPA clock phase to sample the data. This clock is used for bit slip operation and deserialization. The DPA block also forwards the selected DPA clock, divided by the deserialization factor called `rx_divfwdclk`, to the FPGA fabric, along with the deserialized data. This clock signal is put on the periphery clock (PCLK) network.

If you use the soft-CDR mode, do not assert the `rx_dpa_reset` port after the DPA has trained. The DPA continuously chooses new phase taps from the PLL to track parts per million (PPM) differences between the reference clock and incoming data.

In soft-CDR mode, the `rx_dpa_locked` signal is not valid because the DPA continuously changes its phase to track PPM differences between the upstream transmitter and the local receiver input reference clocks. However, you can use the `rx_dpa_locked` signal to determine the initial DPA locking conditions that indicate the DPA has selected the optimal phase tap to capture the data. The `rx_dpa_locked` signal is expected to deassert when operating in soft-CDR mode. The parallel clock, `rx_coreclock`, generated by the I/O PLLs, is also forwarded to the FPGA fabric.

**Note:** In soft-CDR mode, you must place all receiver channels of an SERDES instance in one I/O sub-bank. Top I/O sub-bank can support up to 4 soft-CDR channels and bottom sub-bank can support up to 8 soft-CDR channels. Refer to Intel Agilex device pin-out files to identify the pin locations that support this feature.

## 5.4. Intel Agilex LVDS SERDES Source-Synchronous Timing Budget

The topics in this section describe the timing budget, waveforms, and specifications for source-synchronous signaling in the Intel Agilex device family.

The LVDS SERDES enables high-speed transmission of data, resulting in better overall system performance. To take advantage of fast system performance, you must analyze the timing for these high-speed signals. Timing analysis for the differential block is different from traditional synchronous timing analysis techniques.

The basis of the source synchronous timing analysis is the skew between the data and the clock signals instead of the clock-to-output setup times. High-speed differential data transmission requires the use of timing parameters provided by IC vendors and is strongly influenced by board skew, cable skew, and clock jitter.

This section defines the source-synchronous differential data orientation timing parameters, the timing budget definitions for the Intel Agilex device family, and how to use these timing parameters to determine the maximum performance of a design.

### 5.4.1. Transmitter Channel-to-Channel Skew

The receiver skew margin calculation uses the transmitter channel-to-channel skew (TCCS)—an important parameter based on the Intel Agilex transmitter in a source-synchronous differential interface:

- TCCS is the difference between the fastest and slowest data output transitions, including the  $T_{CO}$  variation and clock skew.
- For SERDES transmitters, the Timing Analyzer provides the TCCS value in the TCCS report (`report_TCCS`) in the Intel Quartus Prime compilation report, which shows TCCS values for serial output ports.
- You can also get the TCCS value from the device data sheet.



For the Intel Agilex devices, perform PCB trace compensation to adjust the trace length of each SERDES channel to improve channel-to-channel skew when interfacing with non-DPA receivers at data rate above 840 Megabits per second (Mbps). The Intel Quartus Prime software Fitter Report panel reports the amount of delay you must add to each trace for the Intel Agilex device. You can use the recommended trace delay numbers shown under the Transmitter/Receiver Package Skew Compensation panel and manually compensate the skew on the PCB board trace to reduce channel-to-channel skew, thus meeting the timing budget between SERDES channels.

### 5.4.2. Receiver Skew Margin

Different modes of SERDES receivers use different specifications, which determine the ability to sample the received serial data correctly.

- In non-DPA mode, use RSKM, TCCS, and sampling window (SW) specifications for high-speed source-synchronous differential signals in the receiver data path.
- In DPA and Soft-CDR modes, use DPA jitter tolerance instead of the receiver skew margin (RSKM).

The RSKM equation expresses the relationship between RSKM, TCCS, and SW:

**Figure 37. RSKM Equation**

$$RSKM = \frac{TUI - SW - TCCS}{2}$$

The equation uses the following conventions:

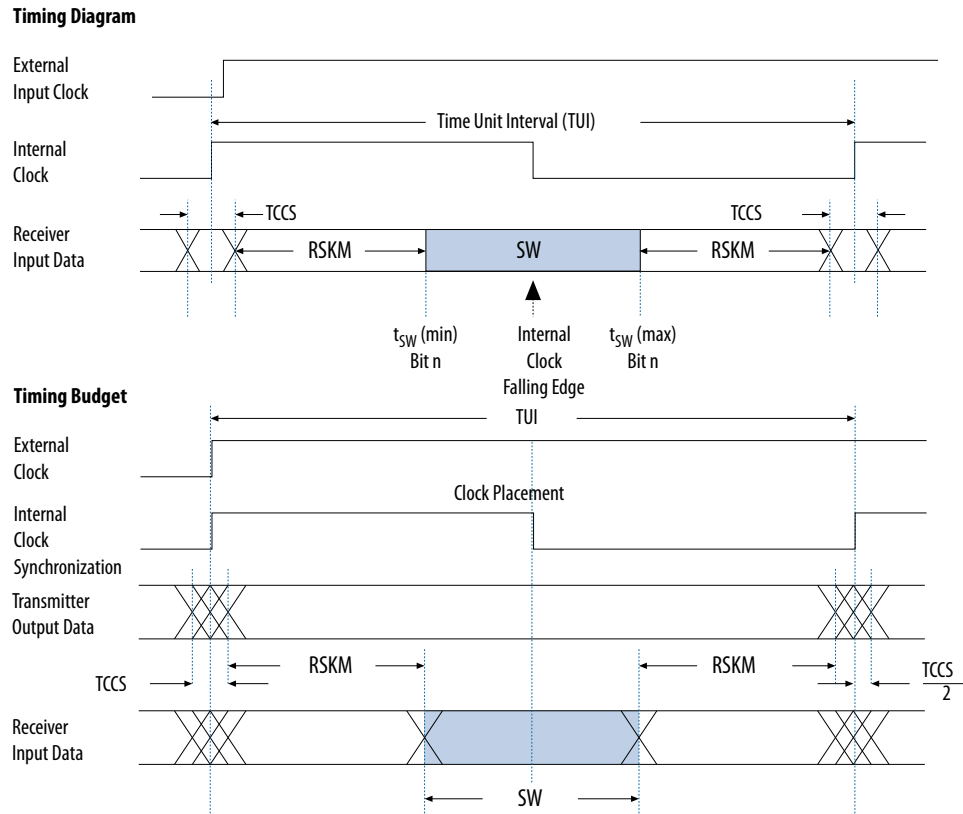
- RSKM—the timing margin between the clock input of the receiver and the data input sampling window, and the jitter induced from core noise and I/O switching noise.
- Time unit interval (TUI)—time period of the serial data.
- SW—the period of time that the input data must be stable to ensure that the LVDS receiver samples the data successfully. The SW is a device property and varies according to device speed grade.
- TCCS—the timing difference between the fastest and the slowest output edges across channels driven by the same PLL. The TCCS measurement includes the  $t_{CO}$  variation, clock, and clock skew.

**Note:** If there is additional board channel-to-channel skew, consider the total receiver channel-to-channel skew (RCCS) instead of TCCS. Total RCCS = TCCS + board channel-to-channel skew.

You must calculate the RSKM value, based on the data rate and device, to determine if the LVDS SERDES receiver can sample the data:

- A positive RSKM value, after deducting transmitter jitter, indicates that the LVDS SERDES receiver can sample the data properly.
- A negative RSKM value, after deducting transmitter jitter, indicates that the LVDS SERDES receiver cannot sample the data properly.

**Figure 38. Differential High-Speed Timing Diagram and Timing Budget**



This example shows the RSKM calculation for Intel Agilex devices at 1 Gbps data rate with a 200 ps board channel-to-channel skew.

- TCCS = 100 ps
- SW = 300 ps
- TUI = 1000 ps
- Total RCCS = TCCS + Board channel-to-channel skew = 100 ps + 200 ps = 300 ps
- $RSKM = (TUI - SW - RCCS) / 2 = (1000 \text{ ps} - 300 \text{ ps} - 300 \text{ ps}) / 2 = 200 \text{ ps}$

The non-DPA receiver works correctly if the RSKM is greater than 0 ps after deducting transmitter jitter.

## 5.5. Intel Agilex LVDS SERDES Timing

Use the Intel Quartus Prime software to generate the required timing constraint to perform proper timing analysis of the high-speed SERDES I/O in Intel Agilex devices.

**Table 17. Timing Components**

Timing Component	Description
Source Synchronous Paths	The source synchronous paths are paths where clock and data signals are passed from the transmitting devices to the receiving devices. For example:

*continued...*



Timing Component	Description
	<ul style="list-style-type: none"> <li>FPGA/SERDES/TX to external receiving device</li> <li>External transmitting device to FPGA/SERDES/RX /non-DPA mode</li> </ul>
Dynamic Phase Alignment Paths	A DPA block registers the I/O capture paths in soft-CDR and DPA-FIFO modes. The DPA block dynamically chooses the best phase from the PLL VCO clocks to latch the input data.
Internal FPGA Paths	<p>The internal FPGA paths are the paths inside the FPGA fabric:</p> <ul style="list-style-type: none"> <li>SERDES RX hardware to core registers paths</li> <li>Core registers to SERDES TX hardware paths</li> <li>Others core registers to core registers path</li> </ul> <p>The Timing Analyzer reports the corresponding timing margins.</p>

### 5.5.1. I/O Timing Analysis

The LVDS SERDES enables high-speed transmission of data, resulting in better overall system performance. To take advantage of fast system performance, you must analyze the timing for these high-speed signals. Timing analysis for the differential block is different from traditional synchronous timing analysis techniques.

#### Receiver Timing Analysis in Soft-CDR and DPA-FIFO Modes

The DPA hardware dynamically captures the received data in soft-CDR and DPA-FIFO modes. For these modes, the Timing Analyzer does not perform static I/O timing analysis.

#### Receiver Timing Analysis in Non-DPA Mode

In non-DPA mode, use RSKM, TCCS, and sampling window (SW) specifications for high-speed source-synchronous differential signals in the receiver data path.

To obtain accurate RSKM results in the Timing Analyzer, add this line of code to your `.sdc` to specify the RCCS value: `set ::RCCS <RCCS value in nanoseconds>`. For example, `set ::RCCS 0.0`.

#### Transmitter Timing Analysis

For LVDS SERDES transmitters, the Timing Analyzer provides the transmitter channel-to-channel skew (TCCS) value in the TCCS report (`report_TCCS`) in the Intel Quartus Prime compilation report, which shows TCCS values for serial output ports. You can also obtain the TCCS value from the device data sheet.

TCCS is the maximum skew observed across the channels of data and TX output clock which is the difference between the fastest and slowest data output transitions, including the  $T_{CO}$  variation and clock skew.

## 5.6. Intel Agilex LVDS SERDES Design Guidelines

### 5.6.1. Use High-Speed Clock from PLL to Clock SERDES Only

The high-speed clock generated from the PLL is intended to clock the SERDES circuitry only. Do not use the high-speed clock to drive other logic because the allowed frequency to drive the core logic is restricted by the PLL  $F_{OUT}$  specification.

For more information about the  $F_{OUT}$  specification, refer to the *Intel Agilex Device Data Sheet*.

### 5.6.2. Pin Placement for Differential Channels

Each GPIO sub-bank contains its own PLL. A PLL can drive all receiver and transmitter channels in the same sub-bank, and transmitter channels in adjacent I/O sub-banks. However, the individual PLL cannot drive receiver channels in another I/O sub-bank or transmitter channels in non-adjacent I/O sub-banks.

The pin index number 0-47 and pin index number 48-95 from device pin out files are respectively assigned to bottom sub-bank and top sub-bank in single GPIO bank. Refer to *External Memory Interface Pin Placement Requirements* for more information on the sub-bank arrangement for each I/O bank.

#### PLLs Driving DPA-Enabled Differential Receiver Channels

For differential receivers, the PLL can drive all channels in the same I/O sub-bank but cannot drive across banks.

Each differential receiver in an I/O bank has a dedicated DPA circuit to align the phase of the clock to the data phase of its associated channel.

DPA usage adds some constraints to the placement of high-speed differential receiver channels. The Intel Quartus Prime compiler automatically checks the design and issues error messages if there are placement guidelines violations. Adhere to the guidelines to ensure proper high-speed I/O operation.

#### PLLs Driving DPA-Enabled Differential Receiver and Transmitter Channels in LVDS SERDES Interface Spanning Multiple I/O Banks

If you use both differential transmitter and DPA-enabled receiver channels in a bank, the PLL can drive the transmitters at the adjacent I/O banks, but only the receivers in its own I/O sub-bank.

#### Related Information

[External Memory Interface Pin Placement Requirements](#) on page 30

### 5.6.3. SERDES Pin Pairs for Soft-CDR Mode

You can use only specific SERDES pin pairs in soft-CDR mode. Refer to the pinout file of each device to determine the SERDES pin pairs that support the soft-CDR mode.

## 6. Documentation Related to the Intel Agilex General Purpose I/O and LVDS SERDES User Guide

The following are the links to references related to Intel Agilex GPIO and LVDS SERDES system.

**Table 18. References**

Reference	Description
<a href="#">Intel Agilex Device Data Sheet</a>	This document describes the electrical characteristics, switching characteristics, configuration specifications, and timing for Intel Agilex devices.
<a href="#">Intel Agilex Device Family Pin Connection Guidelines</a>	This document describes the Intel Agilex the guidelines for all the pins in the device.
<a href="#">Intel Agilex Clocking and PLL User Guide</a>	This document describes the Intel Agilex clock and PLL specifications and guidelines.
<a href="#">Intel Agilex Configuration User Guide</a>	This document describes the Intel Agilex configuration specifications and guidelines.
<a href="#">Intel Agilex Power Management User Guide</a>	This document describes Intel Agilex power management specifications and guidelines.
<a href="#">IBIS Models for Intel Devices</a>	This link provides IBIS models for Intel Agilex devices.
<a href="#">SPICE Models for Intel Devices.</a>	This link provides HSPIC models for Intel Agilex devices.
<a href="#">AN 433: Constraining and Analyzing Source-Synchronous Interfaces</a>	This application note describes techniques for constraining and analyzing source-synchronous interfaces.



## 7. Document Revision History for the Intel Agilex General Purpose I/O and LVDS SERDES User Guide

---

Document Version	Changes
2019.04.02	Initial release.