



Intel® Agilex™ Device Data Sheet



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Intel® Agilex™ Device Data Sheet

This data sheet describes the electrical characteristics, switching characteristics, configuration specifications, and timing for Intel® Agilex™ devices.

Table 1. Intel Agilex Device Grades and Speed Grades Supported

Device Grade	Speed Grade Supported
Extended	<ul style="list-style-type: none"> • -E1V (fastest) • -E2V • -E3V • -E3E • -E4F
Industrial	<ul style="list-style-type: none"> • -I1V • -I2V • -I3V • -I3E

The suffix after the speed grade denotes the power options offered in Intel Agilex devices.

- V—standard power (VID)
- E—lower power (VID)
- F—fixed voltage

Table 2. Data Sheet Status for Intel Agilex Devices

Variant	Data Status
Intel Agilex F-series	Advance
Intel Agilex I-series	Advance

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Electrical Characteristics

The following sections describe the operating conditions and power consumption of Intel Agilex devices.

Operating Conditions

Intel Agilex devices are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Intel Agilex devices, you must consider the operating requirements described in this section.

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Intel Agilex devices.

Recommended Operating Conditions

Table 3. Recommended Operating Conditions for Intel Agilex Devices

This table lists the steady-state voltage values expected for Intel Agilex devices. Power supply ramps must all be strictly monotonic, without plateaus.

Symbol	Description	Condition	Minimum ⁽¹⁾	Typical	Maximum ⁽¹⁾	Unit
V _{CC}	Core voltage power supply	-1V, -2V, -3V, -3E ⁽²⁾	(Typical) - 3%	0.685 - 0.85 ⁽³⁾	(Typical) + 3%	V
		-4F	0.776	0.8	0.824	V
V _{CCP}	Periphery circuitry power supply	-1V, -2V, -3V, -3E ⁽²⁾	(Typical) - 3%	0.685 - 0.85 ⁽³⁾	(Typical) + 3%	V
		-4F	0.776	0.8	0.824	V

continued...

- (1) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise. Refer to power distribution network (PDN) tool for PCB power distribution network design.
- (2) The use of Power Management Bus (PMBus™) voltage regulator dedicated to Intel Agilex SmartVID devices is mandatory. The PMBus voltage regulator and Intel Agilex SmartVID devices are connected via PMBus.
- (3) The typical value is based on the SmartVID programmed value.



Symbol	Description	Condition	Minimum ⁽¹⁾	Typical	Maximum ⁽¹⁾	Unit
V _{CCPT}	Power supply for programmable power technology and I/O pre-driver	—	1.71	1.8	1.89	V
V _{CCH}	Transceiver digital power supply	E-Tile and P-Tile devices	0.87	0.9	0.93	V
V _{CCH_SDM}	Secure Device Manager (SDM) block transceiver digital power supply	E-Tile and P-Tile devices	0.87	0.9	0.93	V
V _{CCIO_PIO_SDM}	SDM block I/O bank power supply	1.5 V	1.455	1.5	1.545	V
		1.2 V	1.14	1.2	1.26	V
V _{CCIO_SDM}	SDM block configuration pins power supply	—	1.71	1.8	1.89	V
V _{CCL_SDM}	SDM block core voltage power supply	—	0.776	0.8	0.824	V
V _{CCFUSEWR_SDM}	SDM block fuse writing power supply	—	1.4	—	2.4	V
V _{CCPLLDIG_SDM}	SDM block PLL digital power supply	—	0.776	0.8	0.824	V
V _{CCPLL_SDM}	SDM block PLL analog power supply	—	1.71	1.8	1.89	V
V _{CCBAT} ⁽⁴⁾	Battery back-up power supply (For design security volatile key register)	—	1	—	1.8	V
V _{CCADC}	ADC voltage sensor power supply	—	1.71	1.8	1.89	V
V _{CCIO_PIO}	I/O bank power supply	1.5 V	1.455	1.5	1.545	V
		1.2 V	1.14	1.2	1.26	V
V _{CCA_PLL}	PLL analog power supply	—	1.71	1.8	1.89	V
V _I ⁽⁵⁾	DC input voltage	V _{CCIO_PIO} = 1.2 V	-0.3	—	1.56	V

continued...

- (1) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise. Refer to power distribution network (PDN) tool for PCB power distribution network design.
- (4) You need to always power up V_{CCBAT}. If you do not use the design security feature in Intel Agilex devices, connect V_{CCBAT} to a 1.8 V power supply. Intel Agilex power-on reset (POR) circuitry monitors V_{CCBAT}.
- (5) This value applies to both input and tri-stated output configuration. Pin voltage should not be externally pulled higher than the maximum value.



Symbol	Description	Condition	Minimum ⁽¹⁾	Typical	Maximum ⁽¹⁾	Unit
		$V_{CCIO_PIO} = 1.5\text{ V}$	-0.3	—	1.845	V
		$V_{CCIO_SDM}, V_{CCIO_HPS} = 1.8\text{ V}$	-0.3	—	2.19	V
V_O	Output voltage	—	0	—	V_{CCIO_PIO}	V
T_J	Operating junction temperature	Extended	0	—	100	°C
		Industrial	-40	—	100	°C
$t_{RAMP}^{(6)(7)(8)}$	Power supply ramp time	Standard POR	200 μs	—	100 ms	—

Transceiver Power Supply Operating Conditions

Table 5. E-Tile Transceiver Power Supply Operating Conditions

For specification status, see the *Data Sheet Status* table

Symbol	Description	Typical DC Level (V)	Recommended DC Setpoint (% of DC level)	Recommended VR Ripple (% of DC level)	Recommended AC Transient (% of DC level)	Maximum (DC Setpoint + Ripple + AC Transient) (% of DC level)
$V_{CCRT_GXE}^{(10)}$	Transceiver power supply	0.9	± 0.5%	± 2.5%		± 3%
$V_{CC_HSSL_GXE}$	E-tile digital signal power supply	0.9	± 0.5%	± 2.5%		± 3%

continued...

- (1) This value describes the required voltage measured between the PCB power and ground ball during normal device operation. The voltage ripple includes both regulator DC ripple and the dynamic noise. Refer to power distribution network (PDN) tool for PCB power distribution network design.
- (6) This is also applicable to HPS power supply. For HPS power supply, refer to t_{RAMP} specifications for standard POR when $HPS_PORSEL = 0$ and t_{RAMP} specifications for fast POR when $HPS_PORSEL = 1$.
- (7) t_{RAMP} is the ramp time of each individual power supply, not the ramp time of all combined power supplies.
- (8) To support AS fast mode, all power supplies to the Intel Agilex device must be fully ramped-up within 10 ms to the recommended operating conditions.
- (10) The difference between $V_{CCRT}/V_{CCRTPLL}$ and V_{CCH} should be no less than 200 mV.



Symbol	Description	Typical DC Level (V)	Recommended DC Setpoint (% of DC level)	Recommended VR Ripple (% of DC level)	Recommended AC Transient (% of DC level)	Maximum (DC Setpoint + Ripple + AC Transient) (% of DC level)
V _{CCRTPLL_GXE} ⁽¹⁰⁾	Transceiver PLL power supply	0.9	± 0.5%	± 2.5%		± 3%
V _{CCH_GXE}	Analog power supply	1.1	± 0.5%	± 0.5%	± 2%	± 3%
V _{CCCLK_GXE}	LVPECL REFCLK power supply	2.5	± 0.5%	± 0.5%	± 2%	± 3%

Table 6. P-Tile Transceiver Power Supply Operating Conditions

For specification status, see the *Data Sheet Status* table. The specifications below should be met at the board via direct connection to the package power balls. Place the voltage rail sense point in the FPGA pinfield (in the package shadow) as close as possible to the corresponding package power balls. For this rails, measure the output voltage at this remote sense location.

Symbol	Description	Typical DC Level (V)	Recommended DC Setpoint (% of DC level)	Recommended VR Ripple (% of DC level)	Recommended AC Transient (% of DC level)	Maximum (DC Setpoint + Ripple + AC Transient) (% of DC level)
V _{CCRT_GXP}	Transceiver power supply	0.9	± 0.5%	± 2.5%		± 3%
V _{CC_HSSI_GXP}	P-tile digital signal power supply	0.9	± 0.5%	± 2.5%		± 3%
V _{CCFUSE_GXP}	P-tile efuse power supply	0.9	± 0.5%	± 2.5%		± 3%
V _{CCCLK_GXP}	P-tile I/O buffer power supply	1.8	± 0.5%	± 0.5%	± 2%	± 3%
V _{CCH_GXP}	High voltage power for Transceiver	1.8	± 0.5%	± 0.5%	± 2%	± 3%



HPS Power Supply Operating Conditions

Table 7. HPS Power Supply Operating Conditions for Intel Agilex Devices

This table lists the steady-state voltage and current values expected for Intel Agilex system-on-a-chip (SoC) devices with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus. Refer to Recommended Operating Conditions for Intel Agilex Devices table for the steady-state voltage values expected from the FPGA portion of the Intel Agilex SoC devices.

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V _{CCL_HPS}	HPS core voltage and periphery circuitry power supply	Performance boost, fixed voltage: -1V	0.87	0.9	0.93	V
		SmartVID: -1V, -2V, -3V, -3E	0.685	—	0.85	V
		Fixed voltage: -4F	0.776	0.8	0.824	V
V _{CCPLLDIG_HPS}	HPS PLL digital power supply (can be connected to V _{CCL_HPS})	Performance boost, fixed voltage: -1V	0.87	0.9	0.93	V
		SmartVID: -1V, -2V, -3V, -3E	0.685	—	0.85	V
		Fixed voltage: -4F	0.776	0.8	0.824	V
V _{CCPLL_HPS}	HPS PLL analog power supply	1.8 V	1.71	1.8	1.89	V
V _{CCIO_HPS}	HPS I/O buffers power supply	1.8 V	1.71	1.8	1.89	V

Related Information

- [Recommended Operating Conditions](#) on page 4
Provides the steady-state voltage values for the FPGA portion of the device.
- [HPS Clock Performance](#) on page 36

DC Characteristics

Supply Current and Power Consumption

Intel offers two ways to estimate power for your design—the Excel-based Early Power Estimator (EPE) and the Intel Quartus® Prime Power Analyzer feature.

Use the Excel-based EPE before you start your design to estimate the supply current for your design. The EPE provides a magnitude estimate of the device power because these currents vary greatly with the usage of the resources.



The Intel Quartus Prime Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yield very accurate power estimates.

I/O Pin Leakage Current

Table 8. I/O Pin Leakage Current for Intel Agilex Devices

Symbol	Description	Condition	Min	Max	Unit
I_I	Input pin	$V_I = 0\text{ V to }V_{CCIO_PIO\text{ (MAX)}}$	-250	250	μA
I_{OZ}	Tri-stated I/O pin	$V_O = 0\text{ V to }V_{CCIO_PIO\text{ (MAX)}}$	-250	250	μA

Bus Hold Specifications

The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

Table 9. Bus Hold Parameters for Intel Agilex Devices

Parameter	Symbol	Condition	$V_{CCIO_PIO}\text{ (V)}$		Unit
			1.2		
			Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}\text{ (max)}$	30	—	μA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}\text{ (min)}$	-30	—	μA
Bus-hold, low, overdrive current	I_{ODL}	$0\text{ V} < V_{IN} < V_{CCIO_PIO}$	—	1,200	μA
Bus-hold, high, overdrive current	I_{ODH}	$0\text{ V} < V_{IN} < V_{CCIO_PIO}$	—	-1,200	μA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	V

OCT Calibration Accuracy Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block.



Table 10. OCT Calibration Accuracy Specifications for Intel Agilex Devices

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

These specifications require RZQ reference accuracy of $240 \Omega \pm 1\%$.

Symbol	Description	Condition (V)	Calibration Accuracy	Unit
34- Ω and 40- Ω R_S	Internal series termination with calibration (34- Ω and 40- Ω setting)	$V_{CCIO_PIO} = 1.2$	± 15	%
50- Ω and 60- Ω R_T	Internal parallel termination with calibration (50- Ω and 60- Ω setting)	SSTL-12 and HSTL-12 I/O standards	-10 to +60	%
		POD12 I/O standard	± 15	

OCT Without Calibration Resistance Tolerance Specifications

Table 11. OCT Without Calibration Resistance Tolerance Specifications for Intel Agilex Devices

This table lists the Intel Agilex OCT without calibration resistance tolerance to PVT changes.

Symbol	Description	Condition (V)	Resistance Tolerance	Unit
34- Ω and 40- Ω R_S	Internal series termination without calibration (34- Ω and 40- Ω setting)	$V_{CCIO_PIO} = 1.2$	-30 to +60	%
100- Ω R_D	Internal differential termination (100- Ω setting)	$V_{CCIO_PIO} = 1.5$	± 40	%

Pin Capacitance

Table 12. Pin Capacitance for Intel Agilex Devices

Symbol	Description	Maximum	Unit
C_{IO}	Input/output capacitance of I/O pins	2.5 ⁽¹¹⁾	pF

(11) This value refers to die-level pin capacitance without the device package.



Internal Weak Pull-Up Resistor

All I/O pins, except configuration and JTAG pins, have an option to enable weak pull-up. For SDM and HPS, the configuration I/O and peripheral I/O are supported with weak pull-up and weak pull-down options.

Table 13. Internal Weak Pull-Up Resistor Values for Intel Agilex Devices

Symbol	Description	Condition (V)	Min	Typ	Max	Unit
R _{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V _{CCIO_PIO} = 1.2 ±5%	3	10	30	kΩ

Related Information

[Intel Agilex Device Family Pin Connection Guidelines](#)

Provides more information about the pins that support internal weak pull-up and internal weak pull-down features.

I/O Standard Specifications

Tables in this section list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Intel Agilex devices.

For minimum voltage values, use the minimum V_{CCIO_PIO} values. For maximum voltage values, use the maximum V_{CCIO_PIO} values.

You must perform timing closure analysis to determine the maximum achievable frequency for general purpose I/O standards.

Related Information

[Recommended Operating Conditions](#) on page 4

Single-Ended I/O Standards Specifications

Table 14. Single-Ended I/O Standards Specifications for Intel Agilex Devices

I/O Standard	V _{CCIO_PIO} (V)			V _{IL} (V)		V _{IH} (V)	
	Min	Typ	Max	Min	Max	Min	Max
1.2 V LVCMOS	1.14	1.2	1.26	-0.3	0.35 × V _{CCIO_PIO}	0.65 × V _{CCIO_PIO}	V _{CCIO_PIO} + 0.3



Single-Ended SSTL, HSTL, HSUL, and POD I/O Reference Voltage Specifications

Table 15. Single-Ended SSTL, HSTL, HSUL, and POD I/O Reference Voltage Specifications for Intel Agilex Devices

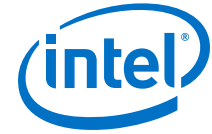
I/O Standard	V _{CCIO_PIO} (V)			V _{REF} (V)			V _{TT} (V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-12	1.14	1.2	1.26	$0.49 \times V_{CCIO_PIO}$	$0.5 \times V_{CCIO_PIO}$	$0.51 \times V_{CCIO_PIO}$	$0.475 \times V_{CCIO_PIO}$	$0.5 \times V_{CCIO_PIO}$	$0.525 \times V_{CCIO_PIO}$
HSTL-12	1.14	1.2	1.26	$0.47 \times V_{CCIO_PIO}$	$0.5 \times V_{CCIO_PIO}$	$0.53 \times V_{CCIO_PIO}$	$0.475 \times V_{CCIO_PIO}$	$0.5 \times V_{CCIO_PIO}$	$0.525 \times V_{CCIO_PIO}$
HSUL-12	1.14	1.2	1.26	$0.49 \times V_{CCIO_PIO}$	$0.5 \times V_{CCIO_PIO}$	$0.51 \times V_{CCIO_PIO}$	—	—	—
POD12	1.14	1.2	1.26	—	Internally calibrated	—	—	V _{CCIO_PIO}	—

Single-Ended SSTL, HSTL, HSUL, and POD I/O Standards Signal Specifications

Table 16. Single-Ended SSTL, HSTL, HSUL, and POD I/O Standards Signal Specifications for Intel Agilex Devices

I/O Standard	V _{IL(DC)} (V)	V _{IH(DC)} (V)	V _{IL(AC)} (V)	V _{IH(AC)} (V)
	Max	Min	Max	Min
SSTL-12	V _{REF} - 0.075	V _{REF} + 0.075	V _{REF} - 0.100	V _{REF} + 0.100
HSTL-12	V _{REF} - 0.080	V _{REF} + 0.080	V _{REF} - 0.150	V _{REF} + 0.150
HSUL-12	V _{REF} - 0.100	V _{REF} + 0.100	V _{REF} - 0.135	V _{REF} + 0.135
POD12 ⁽¹²⁾	V _{REF} - 0.055	V _{REF} + 0.055	V _{REF} - 0.070	V _{REF} + 0.070

(12) This specification is defined over internal V_{ref} range from $0.6 \times V_{CCIO_PIO}$ to $0.92 \times V_{CCIO_PIO}$.



Differential SSTL, HSTL, and HSUL I/O Standards Specifications

Table 17. Differential SSTL, HSTL, and HSUL I/O Standards Specifications for Intel Agilex Devices

I/O Standard	V _{CCIO_PIO} (V)			V _{ILdiff(DC)} (V)	V _{IHdiff(DC)} (V)	V _{ILdiff(AC)} (V)	V _{IHdiff(AC)} (V)	V _{IX(AC)} (V)			V _{Ox(AC)} (V)		
	Min	Typ	Max	Max	Min	Max	Min	Min	Typ	Max	Min	Typ	Max
SSTL-12	1.14	1.2	1.26	-0.15	0.15	-0.2	0.2	$0.5 \times V_{CCIO_PIO} - 0.12$	$0.5 \times V_{CCIO_PIO}$	$0.5 \times V_{CCIO_PIO} + 0.12$	$0.5 \times V_{CCIO_PIO} - 0.12$	$0.5 \times V_{CCIO_PIO}$	$0.5 \times V_{CCIO_PIO} + 0.12$
HSTL-12	1.14	1.2	1.26	-0.16	0.16	-0.3	0.3	$0.5 \times V_{CCIO_PIO} - 0.12$	$0.5 \times V_{CCIO_PIO}$	$0.5 \times V_{CCIO_PIO} + 0.12$	$0.5 \times V_{CCIO_PIO} - 0.12$	$0.5 \times V_{CCIO_PIO}$	$0.5 \times V_{CCIO_PIO} + 0.12$
HSUL-12	1.14	1.2	1.26	-0.2	0.2	-0.27	0.27	$0.5 \times V_{CCIO_PIO} - 0.12$	$0.5 \times V_{CCIO_PIO}$	$0.5 \times V_{CCIO_PIO} + 0.12$	$0.5 \times V_{CCIO_PIO} - 0.12$	$0.5 \times V_{CCIO_PIO}$	$0.5 \times V_{CCIO_PIO} + 0.12$

Differential POD I/O Standards Specifications

Table 18. Differential POD I/O Standards Specifications for Intel Agilex Devices

I/O Standard	V _{CCIO_PIO} (V)			V _{ILdiff(DC)} (V)	V _{IHdiff(DC)} (V)	V _{ILdiff(AC)} (V)	V _{IHdiff(AC)} (V)	V _{IX(AC)} (%) ⁽¹³⁾
	Min	Typ	Max	Max	Min	Max	Min	Max
POD12	1.14	1.2	1.26	-0.11	0.11	-0.14	0.14	25

⁽¹³⁾ Percentage of P-leg and N-leg crossing relative to the midpoint of P-leg and N-leg signal swings.



Differential I/O Standards Specifications

Table 19. Differential I/O Standards Specifications for Intel Agilex Devices

I/O Standard	V _{CCIO_PIO} (V)			V _{ID} (mV) ⁽¹⁴⁾	V _{ICM(DC)} (V)			V _{OD} (V) ⁽¹⁵⁾ ⁽¹⁶⁾			V _{OCM} (V) ⁽¹⁵⁾		
	Min	Typ	Max		Min	Condition	Max	Min	Typ	Max	Min	Typ	Max
1.5 V True Differential Signaling ⁽¹⁷⁾	1.455	1.5	1.545	100	0.3	Data rate ≤700 Mbps	1.4	0.247	—	0.454	0.99	1.1	1.21
					1	Data rate >700 Mbps	1.4						

Switching Characteristics

This section provides the performance characteristics of Intel Agilex core and periphery blocks.

Core Performance Specifications

Clock Tree Specifications

Table 20. Clock Tree Performance for Intel Agilex Devices

Parameter	Performance			Unit
	-1V	-2V	-3V, -3E, -4F	
Programmable clock routing	1,100	1,000	780	MHz

⁽¹⁴⁾ The minimum V_{ID} value is applicable over the entire common mode range, V_{CM}.

⁽¹⁵⁾ R_L range: 90 ≤ R_L ≤ 110 Ω.

⁽¹⁶⁾ The specification is only applicable to default V_{OD} setting.

⁽¹⁷⁾ For optimized true differential receiver performance, the receiver input voltage range must be lower than or equal to V_{CCIO_PIO} supply level to the buffer.



I/O PLL Specifications

Table 21. I/O PLL Specifications for Intel Agilex Devices

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f _{IN}	Input clock frequency	-1V	10	—	1,100 ⁽¹⁸⁾	MHz
		-2V	10	—	900 ⁽¹⁸⁾	MHz
		-3V, -3E, -4F	10	—	750 ⁽¹⁸⁾	MHz
f _{INPFD}	Input clock frequency to the PFD	—	10	—	325	MHz
f _{VCO}	I/O PLL VCO operating range	-1V	600	—	1,600	MHz
		-2V	600	—	1,434	MHz
		-3V, -3E, -4F	600	—	1,250	MHz
f _{CLBW}	I/O PLL closed-loop bandwidth	I/O bank I/O PLL	0.5	—	10	MHz
		Fabric-feeding I/O PLL	1	—	10	MHz
t _{EINDUTY}	Input clock or external feedback clock input duty cycle	—	40	—	60	%
f _{OUT}	Output frequency for internal clock (C counter)	-1V	—	—	1,100	MHz
		-2V	—	—	900	MHz
		-3V, -3E, -4F	—	—	750	MHz
f _{OUT_EXT}	Output frequency for external clock output	-1V	—	—	800	MHz
		-2V	—	—	720	MHz
		-3V, -3E, -4F	—	—	650	MHz
t _{OUTDUTY}	Duty cycle for dedicated external clock output (when set to 50%)	—	45	50	55	%
t _{FCOMP}	External feedback clock compensation time	—	—	—	5	ns

continued...

⁽¹⁸⁾ This specification is limited by the I/O maximum frequency. The maximum achievable I/O frequency is different for each I/O standard and is dependent on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.



Symbol	Parameter	Condition	Min	Typ	Max	Unit
f _{DYCONFIGCLK}	Dynamic configuration clock for mgmt_clk and scanclk	—	—	—	200	MHz
t _{LOCK}	Time required to lock from end-of-device configuration or deassertion of areset	—	—	—	1	ms
t _{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	—	1	ms
t _{PLL_PSERR}	Accuracy of PLL phase shift	—	—	—	±50	ps
t _{ARESET}	Minimum pulse width on the areset signal	—	10	—	—	ns
t _{INCCJ} ⁽¹⁹⁾⁽²⁰⁾	Input clock cycle-to-cycle jitter	f _{REF} < 100 MHz	—	—	±750	ps
		f _{REF} ≥ 100 MHz	—	—	0.15	UI
t _{OUTPJ_DC}	Period jitter for dedicated clock output	f _{REF} < 100 MHz	—	—	175	ps
		f _{REF} ≥ 100 MHz	—	—	17.5	mUI
t _{OUTCCJ_DC}	Cycle-to-cycle jitter for dedicated clock output	f _{REF} < 100 MHz	—	—	175	ps
		f _{REF} ≥ 100 MHz	—	—	17.5	mUI
t _{OUTPJ_IO} ⁽²¹⁾	Period jitter for clock output on the regular I/O	f _{REF} < 100 MHz	—	—	600	ps
		f _{REF} ≥ 100 MHz	—	—	60	mUI
t _{OUTCCJ_IO} ⁽²¹⁾	Cycle-to-cycle jitter for clock output on the regular I/O	f _{REF} < 100 MHz	—	—	600	ps

continued...

(19) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source with jitter < 120 ps.

(20) F_{REF} is f_{IN}/N, specification applies when N = 1.

(21) External memory interface clock output jitter specifications use a different measurement method, which are available in Memory Output Clock Jitter Specifications for Intel Agilex Devices table.



Symbol	Parameter	Condition	Min	Typ	Max	Unit
t _{CASC_OUTPJ_DC} ⁽²²⁾	Period jitter for dedicated clock output in cascaded PLLs	f _{REF} ≥ 100 MHz	—	—	60	mUI
		f _{REF} < 100 MHz	—	—	175	ps
		f _{REF} ≥ 100 MHz	—	—	17.5	mUI

Related Information

Memory Output Clock Jitter Specifications on page 28

Provides more information about the external memory interface clock output jitter specifications.

DSP Block Specifications

Table 22. DSP Block Performance Specifications for Intel Agilex Devices

Mode	Performance				Unit
	-1V	-2V	-3V, -3E	-4F	
Fixed-point 18 × 19 multiplication mode	900	771	676	600	MHz
Fixed-point 27 × 27 multiplication mode	900	771	676	600	MHz
Fixed-point 18 × 19 multiplier adder mode ⁽²³⁾	900	771	676	600	MHz
Fixed-point 18 × 19 multiplier adder summed with 36-bit input mode	900	771	676	600	MHz
Fixed-point 18 × 19 systolic mode	900	771	676	600	MHz
Fixed-point 18 × 19 complex multiplication mode	900	771	676	600	MHz

continued...

⁽²²⁾ Not applicable for fabric-feeding I/O PLL.

⁽²³⁾ When Chainout is enabled but systolic registers are not used, the performance specifications for the following speed grades are as follows:

- -1V: 675 MHz
- -2V: 578 MHz
- -3V and -3E: 507 MHz
- -4F: 450 MHz



Mode	Performance				Unit
	-1V	-2V	-3V, -3E	-4F	
Fixed-point four 9 × 9 multiplier adder mode ⁽²³⁾	900	771	676	600	MHz
FP32 floating-point multiplication mode	750	579	507	475	MHz
FP32 floating-point adder or subtract mode	750	579	507	475	MHz
FP32 floating-point multiplier adder or subtract mode	750	579	507	475	MHz
FP32 floating-point multiplier accumulate mode	750	579	507	475	MHz
Addition or subtraction of two FP16 floating-point multiplication mode	750	579	507	475	MHz
FP32 floating-point complex multiplication	750	579	507	475	MHz
FP32 floating-point direct vector dot product	750	579	507	475	MHz
FP16 floating-point complex multiplication	750	579	507	475	MHz
FP16 floating-point direct vector dot product	750	579	507	475	MHz

Memory Block Specifications

To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL and set to **50%** output duty cycle. Use the Intel Quartus Prime software to report timing for the memory block clocking schemes.

When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX} .

Table 23. Memory Block Performance Specifications for Intel Agilex Devices

Memory	Mode	Performance				Unit
		-1V	-2V	-3V, -3E	-4F	
MLAB	Single port, all supported widths (×16/×32)	1,000	782	667	600	MHz
	Simple dual-port, all supported widths (×16/×32)	1,000	782	667	600	MHz
	Simple dual-port with read-during-write option	600	500	420	360	MHz
	ROM, all supported width (×16/×32)	1,000	782	667	600	MHz

continued...



Memory	Mode	Performance				Unit
		-1V	-2V	-3V, -3E	-4F	
M20K Block	Single-port, all supported widths	1,000	782	667	600	MHz
	Simple dual-port, all supported widths	1,000	782	667	600	MHz
	Simple dual-port, coherent read enabled	1,000	782	667	600	MHz
	Simple dual-port with the read-during-write option set to Old Data , all supported widths	800	640	560	480	MHz
	Simple dual-port with ECC enabled, 512 × 32	600	500	420	310	MHz
	Simple dual-port with ECC, optional pipeline registers enabled, 512 × 32	1,000	782	667	450	MHz
	True dual port, all supported widths	600	500	420	340	MHz
	Simple quad-port, all supported widths	600	500	420	340	MHz
	ROM, all supported widths	1,000	782	667	600	MHz
eSRAM	Simple dual-port	750	640	500	500	MHz

Local Temperature Sensor Specifications

Table 24. Local Temperature Sensor Specifications for Intel Agilex Devices

Temperature Range	Accuracy	Sampling Rate	Conversion Time
-40 to 125 °C ⁽²⁴⁾	±5 °C	1 KSPS	< 1 ms

Remote Temperature Diode Specifications

Note the following for the remote temperature diode specifications:

- The typical value is at 25°C.
- Diode accuracy improves with lower injection current.
- Absolute accuracy is dependent on third-party external diode ADC and integration specifics.

⁽²⁴⁾ Temperature range refers to junction temperature.



Table 25. Remote Temperature Diode Specifications for Intel Agilex Devices (Core Fabric TSD)

Description	Min	Typ	Max	Unit
I_{bias} , diode source current	(25)	—	(25)	μ A
V_{bias} , voltage across diode	(25)	—	(25)	V
Series resistance	—	—	(25)	Ω
Diode ideality factor	—	(25)	—	—

Table 26. Remote Temperature Diode Specifications for Intel Agilex Devices (E-Tile TSD)

Description	Min	Typ	Max	Unit
I_{bias} , diode source current	100	—	170	μ A
V_{bias} , voltage across diode	0.56	—	0.8	V
Series resistance	—	—	< 2	Ω
Diode ideality factor	—	1.008	—	—

Voltage Sensor Specifications

Table 27. Voltage Sensor Specifications for Intel Agilex Devices

Parameter	Minimum	Typical	Maximum	Unit
Resolution	—	7	—	Bit
Sampling rate	—	—	1	KSPS
Differential non-linearity (DNL)	—	—	± 1	LSB
Integral non-linearity (INL)	—	—	± 1	LSB
Input capacitance	—	—	40	pF
Voltage sensor accuracy, V_{in} range: 0 V to 1.249 V	-3.5	—	3.5	%

continued...

(25) Pending silicon characterization.



Parameter		Minimum	Typical	Maximum	Unit
Unipolar Input Mode	Input signal range for Vsigp	0	—	1.49	V
	Common mode voltage on Vsign	0	—	0.25	V
	Input signal range for Vsigp – Vsign	0	—	1.24	V

Periphery Performance Specifications

This section describes the periphery performance, LVDS SERDES, and external memory interface.

Actual achievable frequency depends on design and system specific factors. Ensure proper timing closure in your design and perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

LVDS SERDES Specifications

Table 28. LVDS SERDES Specifications for Intel Agilex Devices

LVDS serializer/deserializer (SERDES) block supports SERDES factor J = 3 to 10.

DDR registers support SERDES factor J = 1 to 2.

You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.

Symbol	Condition	–1 Speed Grade			–2 Speed Grade			–3 Speed Grade			–4 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 ⁽²⁶⁾	10	—	800	10	—	700	10	—	625	10	—	625	MHz
f _{HCLK_in} (input clock frequency) Single-Ended I/O Standards	Clock boost factor W = 1 to 40 ⁽²⁶⁾	10	—	625	10	—	625	10	—	525	10	—	525	MHz

continued...

⁽²⁶⁾ Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.



Symbol		Condition	-1 Speed Grade			-2 Speed Grade			-3 Speed Grade			-4 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f _{HCLK_OUT} (output clock frequency)		—	—	—	800 ⁽²⁷⁾	—	—	700 ⁽²⁷⁾	—	—	625 ⁽²⁷⁾	—	—	625 ⁽²⁷⁾	MHz
Transmitter	True Differential I/O Standards - f _{HSDR} (data rate) ⁽²⁸⁾	SERDES factor J = 4 to 10 ⁽²⁹⁾⁽³⁰⁾⁽³¹⁾	150	—	1,600	150	—	1,434	150	—	1,250	150	—	1,000	Mbps
		SERDES factor J = 3 ⁽²⁹⁾⁽³⁰⁾⁽³¹⁾	150	—	1,200	150	—	1,076	150	—	938	150	—	600	Mbps
		SERDES factor J = 2, uses DDR registers	150	—	840 ⁽³²⁾	150	—	⁽³²⁾	150	—	⁽³²⁾	150	—	⁽³²⁾	Mbps
		SERDES factor J = 1, uses DDR registers	150	—	420 ⁽³²⁾	150	—	⁽³²⁾	150	—	⁽³²⁾	150	—	⁽³²⁾	Mbps
	t _x Jitter - True Differential I/O Standards	Total jitter for data rate, 600 Mbps - 1.6 Gbps	—	—	160	—	—	200	—	—	250	—	—	250	ps
	Total jitter for data rate, < 600 Mbps	—	—	0.1	—	—	0.12	—	—	0.15	—	—	0.15	UI	

continued...

- (27) This is achieved by using the PHY clock network.
- (28) Requires package skew compensation with PCB trace length.
- (29) The F_{max} specification is based on the fast clock used for serial data. The interface F_{max} is also dependent on the parallel clock domain which is design dependent and requires timing analysis.
- (30) The V_{CC} and V_{CCP} must be on a combined power layer and a maximum load of 5 pF for chip-to-chip interface.
- (31) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and serializer do not have a minimum toggle rate.
- (32) The maximum ideal data rate is the SERDES factor (J) × the PLL maximum output frequency (f_{OUT}) provided you can close the design timing and the signal integrity meets the interface requirements.



Symbol		Condition	-1 Speed Grade			-2 Speed Grade			-3 Speed Grade			-4 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
	$t_{DUTY}^{(33)}$	TX output clock duty cycle for Differential I/O Standards	45	50	55	45	50	55	45	50	55	45	50	55	%
	$t_{RISE} \& t_{FALL}^{(30)}$ <small>(34)</small>	True Differential I/O Standards	—	—	160	—	—	180	—	—	200	—	—	220	ps
	TCCS <small>(28)(33)</small>	True Differential I/O Standards	—	—	330	—	—	330	—	—	330	—	—	330	ps
Receiver	True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 4 to 10 <small>(29)(30)(31)</small>	150	—	1,600	150	—	1,434	150	—	1,250	150	—	1,000	Mbps
		SERDES factor J = 3 <small>(29)(30)(31)</small>	150	—	1,200	150	—	1,076	150	—	938	150	—	600	Mbps
	f_{HSDR} (data rate) (without DPA) <small>(28)</small>	SERDES factor J = 3 to 10	<small>(31)</small>	—	<small>(35)</small>	<small>(31)</small>	—	<small>(35)</small>	<small>(31)</small>	—	<small>(35)</small>	<small>(31)</small>	—	<small>(35)</small>	Mbps
		SERDES factor J = 2, uses DDR registers	<small>(31)</small>	—	<small>(32)</small>	<small>(31)</small>	—	<small>(32)</small>	<small>(31)</small>	—	<small>(32)</small>	<small>(31)</small>	—	<small>(32)</small>	Mbps
		SERDES factor J = 1, uses DDR registers	<small>(31)</small>	—	<small>(32)</small>	<small>(31)</small>	—	<small>(32)</small>	<small>(31)</small>	—	<small>(32)</small>	<small>(31)</small>	—	<small>(32)</small>	Mbps
DPA (FIFO mode)	DPA run length	—	—	10,000	—	—	10,000	—	—	10,000	—	—	10,000	UI	
DPA (soft CDR mode)	DPA run length	SGMII/GbE protocol	—	—	5	—	—	5	—	—	5	—	—	5	UI

continued...

⁽³³⁾ Not applicable for DIVCLK = 1.

⁽³⁴⁾ This applies to default pre-emphasis and V_{OD} settings only.

⁽³⁵⁾ You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.



Symbol		Condition	-1 Speed Grade			-2 Speed Grade			-3 Speed Grade			-4 Speed Grade			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
		All other protocols	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—	—	50 data transition per 208 UI	—
Soft CDR mode	Soft-CDR ppm tolerance	—	-300	—	300	-300	—	300	-300	—	300	-300	—	300	ppm
Non DPA mode	Sampling Window	—	—	—	330	—	—	330	—	—	330	—	—	330	ps

DPA Lock Time Specifications

Table 29. DPA Lock Time Specifications for Intel Agilex Devices

The specifications are applicable to both commercial and industrial grades. The DPA lock time is for one channel. One data transition is defined as a 0-to-1 or 1-to-0 transition.

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions ⁽³⁶⁾	Maximum Data Transition
SPI-4	00000000001111111111	2	128	960
Parallel Rapid I/O	00001111	2	128	960
	10010000	4	64	960
Miscellaneous	10101010	8	32	960
	01010101	8	32	960

(36) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.



LVDS SERDES Soft-CDR Sinusoidal Jitter Tolerance Specifications

Figure 1. LVDS SERDES Soft-CDR Sinusoidal Jitter Tolerance Specifications for a Data Rate Equal to 1.6 Gbps

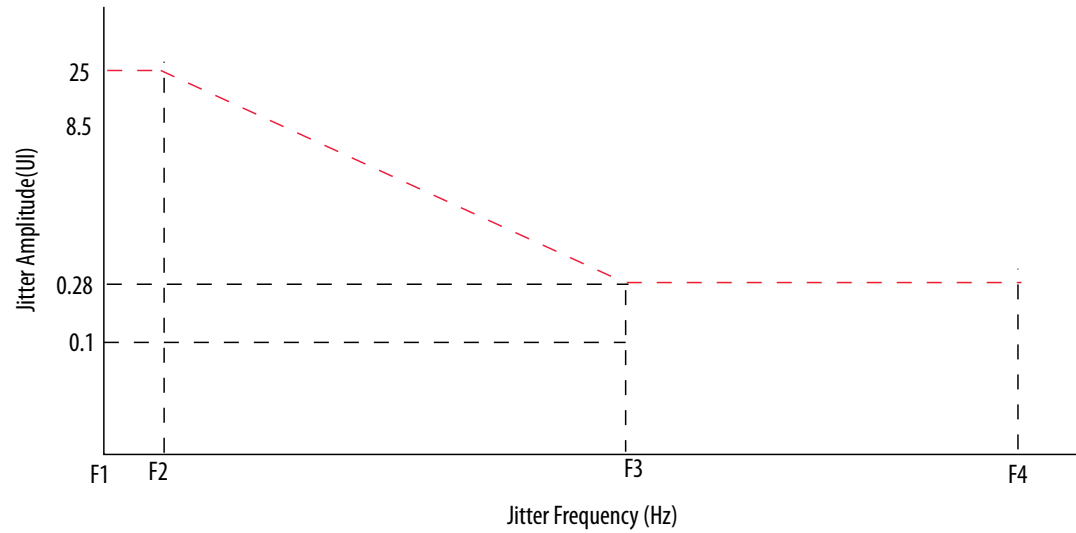
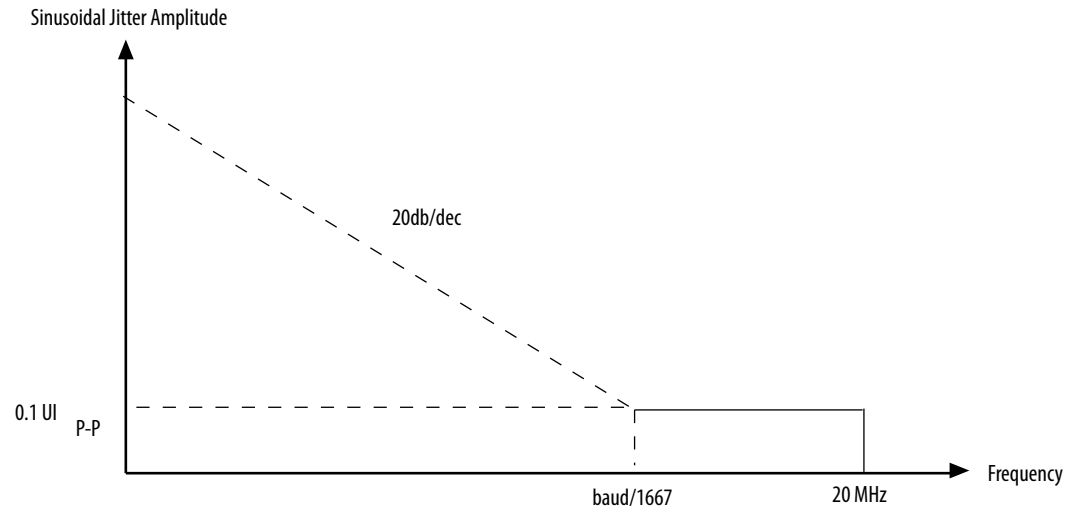


Table 30. LVDS SERDES Soft-CDR Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.6 Gbps

	Jitter Frequency (Hz)	Sinusoidal Jitter (UI)
F1	10,000	25.00
F2	17,565	25.00
F3	1,493,000	0.28
F4	50,000,000	0.28

Figure 2. LVDS SERDES Soft-CDR Sinusoidal Jitter Tolerance Specifications for a Data Rate Less than 1.6 Gbps



Memory Standards Supported by the Hard Memory Controller

Table 31. Memory Standards Supported by the Hard Memory Controller for Intel Agilex Devices

This table lists the overall capability of the hard memory controller. For specific details, refer to the *External Memory Interface Spec Estimator*.

Memory Standard	Rate Support	Maximum Frequency (MHz)
DDR4 SDRAM	Quarter rate	1,600

Related Information

[External Memory Interface Spec Estimator](#)

Provides the specific details of the memory standards supported.



Memory Standards Supported by the Soft Memory Controller

Table 32. Memory Standards Supported by the Soft Memory Controller for Intel Agilex Devices

This table lists the overall capability of the soft memory controller. For specific details, refer to the *External Memory Interface Spec Estimator*.

Memory Standard	Rate Support	Maximum Frequency (MHz)
RLDRAM 3 ⁽³⁷⁾	Quarter rate	1,200
QDR IV SRAM	Quarter rate	1,066

Related Information

[External Memory Interface Spec Estimator](#)

Provides the specific details of the memory standards supported.

Memory Standards Supported by the HPS Hard Memory Controller

Table 33. Memory Standards Supported by the HPS Hard Memory Controller for Intel Agilex Devices

This table lists the overall capability of the hard memory controller. For specific details, refer to the *External Memory Interface Spec Estimator*.

Memory Standard	Rate Support	Maximum Frequency (MHz)
DDR4 SDRAM	Quarter rate	1,600
	Half rate	1,333

Related Information

[External Memory Interface Spec Estimator](#)

Provides the specific details of the memory standards supported.

⁽³⁷⁾ For Intel Agilex RLDRAM 3, Intel only provides the PHY-only option.



DLL Range Specifications

Table 34. DLL Frequency Range Specifications for Intel Agilex Devices

Parameter	Performance (for All Speed Grades)	Unit
DLL operating frequency range	600 – 1,600	MHz
DLL reference clock input	Minimum 600	MHz

Memory Output Clock Jitter Specifications

The clock jitter specification applies to the memory output clock pins clocked by an I/O PLL, or generated using differential signal-splitter and double data I/O circuits clocked by a PLL output routed on a PHY clock network as specified. Intel recommends using PHY clock networks for better jitter performance.

The memory clock output jitter is within the JEDEC specifications with an input of 10 ps peak-to-peak jitter.

E-Tile Transceiver Performance Specifications

This section provides E-tile transceiver specifications and timing for Intel Agilex devices.

Transceiver Performance for E-Tile Devices

Table 35. E-Tile Transmitter and Receiver Data Rate Performance Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Min	Typ	Max	Unit
Supported data rate ⁽³⁸⁾	NRZ	1	—	28.9	Gbps
	PAM4	2	—	57.8 ⁽³⁹⁾	Gbps

⁽³⁸⁾ The supported data rate is for chip-to-chip and backplane links.

⁽³⁹⁾ Two channels are combined to support up to 57.8 Gbps.



Transceiver Reference Clock Specifications

Table 36. E-Tile Reference Clock LVPECL DC Electrical Characteristics

For specification status, see the *Data Sheet Status* table

Symbol	Refclk Parameter	Min	Typ	Max	Unit
V _{TT}	Termination Voltage (2.5V compliant)	0.4	0.5	0.6	V
V _{TT}	Termination Voltage (3.3V compliant)	1.04	1.3	1.56	V
R _{TT}	Termination Resistor	40	50	60	Ω
V _{DIFF}	Differential Voltage	0.4	0.8	1.2	V
V _{CM}	Input Common Mode Voltage (2.5V compliant, no internal termination resistor)	V _{DIFF} /2	—	V _{CCCLK_GXE} -V _{DIFF} /2	V
V _{CM}	Input Common Mode Voltage (2.5V compliant, internal termination resistor)	V _{CCCLK_GXE} - 1.6	V _{CCCLK_GXE} - 1.3	V _{CCCLK_GXE} - 1.0	V
V _{CM}	Input Common Mode Voltage (3.3V compliant, no internal termination resistor)	V _{DIFF} /2	—	V _{CCCLK_GXE} -V _{DIFF} /2	V
V _{CM}	Input Common Mode Voltage (3.3V compliant, internal termination resistor)	1.4	2	2.6	V

Table 37. E-Tile Reference Clock Electrical & Jitter Requirements

For specification status, see the *Data Sheet Status* table

Parameter	Condition	Min	Typ	Max	Unit
Frequency	—	125	156.25	700	MHz
Frequency Tolerance	—	-100	—	100	PPM
Clock Duty Cycle	—	45	50	55	%
<i>continued...</i>					



Parameter	Condition	Min	Typ	Max	Unit
Rise & Fall Times	20% to 80%	40	—	300	ps
Phase Jitter	12 kHz to 20 MHz	—	0.375	0.5	ps rms
Phase Noise ⁽⁴⁰⁾	10 kHz	—	—	-130	dBc/Hz
	100 kHz	—	—	-138	dBc/Hz
	500 kHz	—	—	-138	dBc/Hz
	3 MHz	—	—	-140	dBc/Hz
	10 MHz	—	—	-144	dBc/Hz
	20 MHz	—	—	-146	dBc/Hz

Transmitter Specifications for E-Tile Devices

Table 38. E-Tile Transmitter Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Min	Typ	Max	Unit
Transmitter differential output voltage peak-to-peak	No precursor/postcursor de-emphasis	—	0.97	—	V
Transmitter common mode voltage	—	$V_{CCRT_GXE}/2$			V

⁽⁴⁰⁾ The phase noise numbers in the table above are the maximum acceptable phase noise values measured at a carrier frequency of 156.25 MHz. To calculate the phase noise requirement at any other frequency, use the formula: REFCLK phase noise at f (MHz) = REFCLK phase noise at 156.25 MHz + 20*log₁₀(f/156.25)



Receiver Specifications for E-Tile Devices

Table 39. E-Tile Receiver Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Min	Typ	Max	Unit
Receiver run length ⁽⁴¹⁾	—	—	—	100 ⁽⁴²⁾	symbols
DC input impedance	—	40	—	60	Ω
DC differential input impedance	—	80	100	120	Ω
Powered down DC input impedance	Receiver pin impedance when the receiver termination is powered down	100k	—	—	Ω
Electrical Idle detection voltage	—	65	—	175	mV
Differential termination	From DC to 100 MHz	80	100	120	Ω
PPM tolerance	Allowed frequency mismatch between REFCLK and RX data	—	—	750	ppm

P-Tile Transceiver Performance Specifications

This section provides P-tile transceiver specifications and timing for Intel Agilex devices.

⁽⁴¹⁾ No additional transition density requirements apply.

⁽⁴²⁾ The incoming data must be statistically DC-balanced.



Transceiver Performance for P-Tile Devices

Table 40. P-Tile Transmitter and Receiver Data Rate Performance

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Min	Typ	Max	Unit
Supported data rate	Chip-to-chip and Backplane	2.5	—	16	Gbps

Table 41. P-Tile PLLA Performance

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Transceiver Speed Grade			Unit
		Min	Typ	Max	
VCO frequency	—	—	—	5	GHz
PLL bandwidth (BWTX-PKG_PLL1)	PCIe 2.5 GT/s	1.5	—	22	MHz
PLL peaking (PKGTX-PLL1)	PCIe 2.5 GT/s	—	—	3	dB
PLL bandwidth (BWTX-PKG_PLL2)	PCIe 5.0 GT/s	5	—	16	MHz
PLL peaking (PKGTX-PLL2)	PCIe 5.0 GT/s	—	—	1	dB

Table 42. P-Tile PLLB Performance

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	Transceiver Speed Grade			Unit
		Min	Typ	Max	
VCO frequency	—	—	—	8	GHz
PLL bandwidth (BWTX-PKG_PLL1)	PCIe 8.0 GT/s	2	—	4	MHz
	PCIe 16.0 GT/s	2	—	4	MHz
PLL peaking (PKGTX-PLL1)	PCIe 8.0 GT/s	—	—	2	dB
	PCIe 16.0 GT/s	—	—	2	dB



Transceiver Reference Clock Specifications

Table 43. P-Tile Reference Clock Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Supported I/O Standards	—	HCSL			—
Input Reference Clock Frequency ⁽⁴³⁾	—	99.97	100	100.03	MHz
Rising Edge Rate ⁽⁴⁴⁾	—	0.6	—	4	V/ns
Falling Edge Rate ⁽⁴⁴⁾	—	0.6	—	4	V/ns
Duty cycle	—	40	—	60	%
Spread-spectrum modulating clock frequency	—	30	—	33	kHz
Spread-spectrum downspread	—	—	0 to -0.5	—	%
Absolute VMAX	—	—	1.15	—	V
Absolute VMIN	—	—	-0.3	—	V
Peak-to-peak differential input voltage	—	300	—	1500	mV
VICM (DC coupled)	—	250	—	550	mV
Cycle to cycle jitter (TCCJITTER) ⁽⁴⁵⁾	—	—	—	150	ps
TSSC-MAX-PERIOD-SLEW	—	—	—	1250	ppm/us

⁽⁴³⁾ This number is with spread spectrum clocking (SSC) turned off.

⁽⁴⁴⁾ Measured from -150 mV to +150 mV on the differential waveform. The 300 mV measurement window is centered on the differential zero crossing.



Transmitter Specification for P-Tile Devices

Table 44. P-Tile Transmitter Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O			—
Differential on-chip termination resistors	—	80	—	120	Ω
Differential peak-to-peak voltage for full swing	PCIe 2.5 GT/s	800	—	1100	mV
	PCIe 5.0 GT/s	800	—	1100	mV
	PCIe 8.0 GT/s	800	—	1100	mV
	PCIe 16.0 GT/s	800	—	1100	mV
Differential peak-to-peak voltage for reduced swing	PCIe 2.5 GT/s	400	—	1100	mV
	PCIe 5.0 GT/s	400	—	1100	mV
	PCIe 8.0 GT/s	400	—	1100	mV
	PCIe 16.0 GT/s	400	—	1100	mV
Differential peak-to-peak voltage during EIEOS	PCIe 8.0 GT/s and 16.0 GT/s	250	—	—	mV
Differential peak-to-peak voltage during EIEOS for reduce swing	PCIe 8.0 GT/s and 16.0 GT/s	232	—	—	mV
VOCM (AC coupled)	—	0	—	360	mV
Lane-to-lane output skew	PCIe 2.5 GT/s	—	—	2.5	ns

continued...

(45) For common reference clock architecture, you must meet the reference clock phase jitter requirements as specified in the PCIe Express Card Electromechanical Specification for 2.5 GT/s, *Section 4.3.7 Refclk Specifications for 5.0 GT/s* and *Section 4.3.8 Refclk Specifications for 8.0 GT/s* in the *PCI Express Base Specification Revision 3.0*, and *Section 8.6 Refclk Specifications for 16.0 GT/s* in the *PCI Express Base Specification Revision 4.0*.



Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
	PCIe 5.0 GT/s	—	—	2	ns
	PCIe 8.0 GT/s	—	—	1.5	ns
	PCIe 16.0 GT/s	—	—	1.25	ns

Receiver Specifications for P-Tile Devices

Table 45. P-Tile Receiver Specifications

For specification status, see the *Data Sheet Status* table

Symbol/Description	Condition	All Transceiver Speed Grades			Unit
		Min	Typ	Max	
Supported I/O Standards	—	High Speed Differential I/O			
Peak-to-peak differential input voltage VID (diff p-p)	PCIe 2.5 GT/s ⁽⁴⁶⁾	0.175	—	1.2	V
	PCIe 5.0 GT/s ⁽⁴⁶⁾	0.1	—	1.2	V
VICM (AC coupled)	—	—	0	—	V
Differential on-chip termination resistors	—	80	—	120	Ω
RESREF	—	198	200	202	Ω

⁽⁴⁶⁾ Voltage shown for PCIe 2.5 GT/s and 5.0 GT/s are at the package pins (TP2).



HPS Performance Specifications

This section provides hard processor system (HPS) specifications and timing for Intel Agilex devices.

HPS Clock Performance

Table 46. Maximum HPS Clock Frequencies for Intel Agilex Devices

Performance	V _{CCL_HPS} (V)	MPU Frequency (MHz)	L3 Frequency (MHz) (l3_main_free_clk)	MPFE Frequency (MHz)	Rate	DDR Clock (MHz)	DDR (Mb/s per pin)
-1 speed grade	Fixed: 0.9	1,410	400	400	Quarter	1,600	3,200
				600	Half	1,200	2,400
	SmartVID	1,350	400	366.625	Quarter	1,466.5	2,933
				600	Half	1,200	2,400
-2 speed grade	SmartVID	1,200	400	300	Quarter	1,200	2,400
				600	Half	1,200	2,400
				533.25	Half	1,066.5	2,133
-3 speed grade	SmartVID	1,000	400	466.5	Half	933	1,866
				400	Half	800	1,600
-4 speed grade	Fixed: 0.8	800	400	TBD	TBD	TBD	TBD

Related Information

[External Memory Interface Spec Estimator](#)

Provides the specific details of the maximum allowed SDRAM operating frequency.

HPS Internal Oscillator Frequency

Table 47. HPS Internal Oscillator Frequency for Intel Agilex Devices

Description	Min	Typ	Max	Unit
Internal Oscillator Frequency	160	370	400	MHz



HPS PLL Specifications

HPS PLL Input Requirements

Table 48. HPS PLL Input Requirements for Intel Agilex Devices

The main HPS PLL receives its clock signals from the HPS_OSC_CLK pin. Refer to the *Intel Agilex Device Family Pin Connection Guidelines* for information about assigning this pin.

Description	Min	Typ	Max	Unit
Clock input range	25	—	125	MHz
Clock input accuracy	—	—	50	PPM
Clock input duty cycle	45	50	55	%

Related Information

[Intel Agilex Device Family Pin Connection Guidelines](#)

Provides more information about the HPS_OSC_CLK pin assignment.

HPS PLL Performance

Table 49. HPS PLL Performance for Intel Agilex Devices

Description	Min	Max	Unit
Main PLL VCO output	—	3000	MHz
Peripheral PLL VCO output	—	3000	MHz
h2f_user0_clk ⁽⁴⁷⁾	—	500	MHz
h2f_user1_clk ⁽⁴⁷⁾	—	500	MHz

(47) The HPS PLL provides this clock to the FPGA fabric.



HPS SPI Timing Characteristics

Table 50. SPI Master Timing Requirements for Intel Agilex Devices

You can adjust the input delay timing by programming the `rx_sample_dly` register.

Symbol	Description	Min	Typ	Max	Unit
$T_{spi_ref_clk}$	The period of the SPI internal reference clock, sourced from <code>l4_main_clk</code>	2.5	—	—	ns
T_{clk}	SPIM_CLK clock period	16.67	—	—	ns
$T_{dutycycle}$	SPIM_CLK duty cycle	45	50	55	%
T_{ck_jitter}	SPIM_CLK output jitter	—	—	2	%
T_{dio}	Master-out slave-in (MOSI) output skew	-3	—	2	ns
$T_{dssfrst}^{(48)}$	SPI_SS_N asserted to first SPIM_CLK edge	$(1.5 \times T_{clk}) - 2$	—	—	ns
$T_{dsslst}^{(48)}$	Last SPIM_CLK edge to SPI_SS_N deasserted	$T_{clk} - 2$	—	—	ns
$T_{su}^{(49)}$	SPIM_MISO setup time with respect to SPIM_CLK capture edge	$4.5 - (rx_sample_dly \times T_{spi_ref_clk})^{(50)}$	—	—	ns
$T_h^{(49)}$	Input hold in respect to SPIM_CLK capture edge	$1.3 + (rx_sample_dly \times T_{spi_ref_clk})$	—	—	ns

(48) SPI_SS_N behavior differs depending on Motorola SPI, TI SSP or Microwire operational mode.

(49) The capture edge differs depending on the operational mode. For Motorola SPI, the capture edge can be the rising or falling edge depending on the `scpol` register bit; for TI SSP, the capture edge is the falling edge; for Microwire, the capture edge is the rising edge.

(50) Valid values of `rx_sample_dly` range from 1 to 64 (units are in $T_{spi_ref_clk}$ steps)

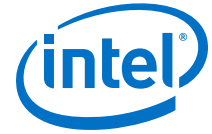
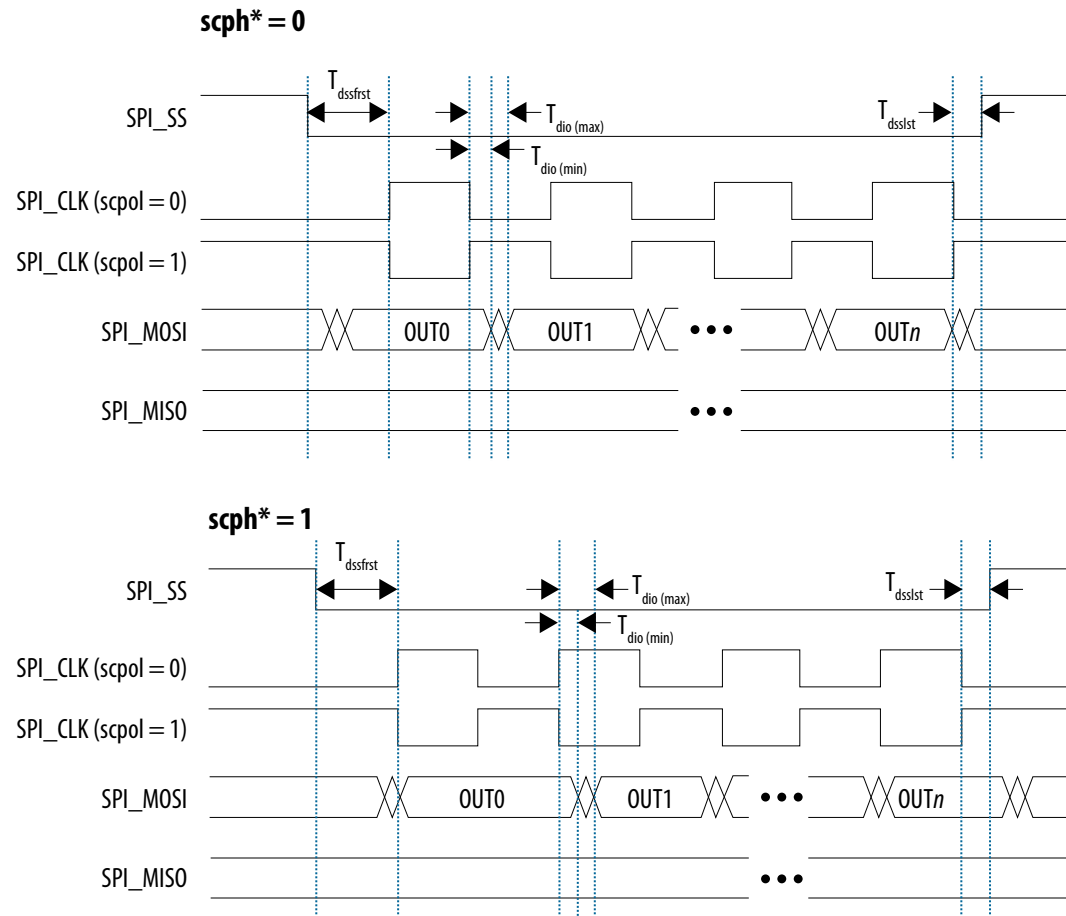
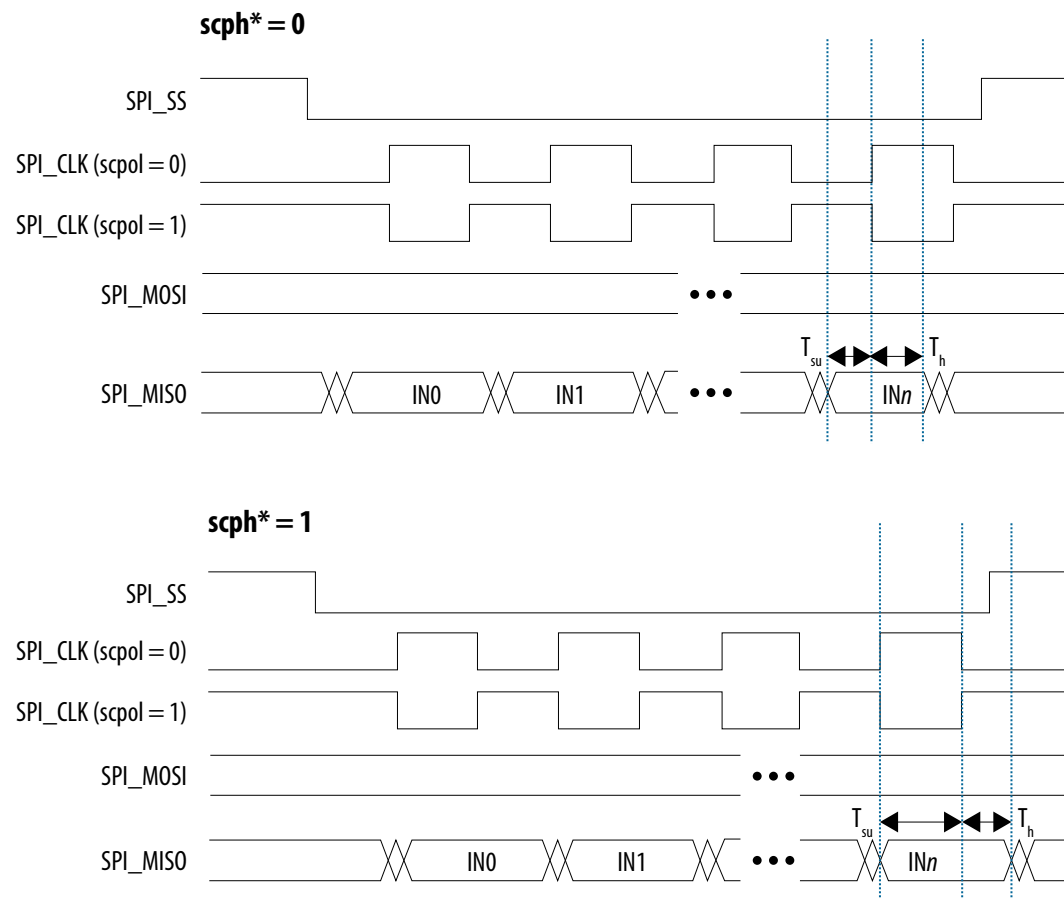


Figure 3. SPI Master Output Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRL0 register

Figure 4. SPI Master Input Timing Diagram



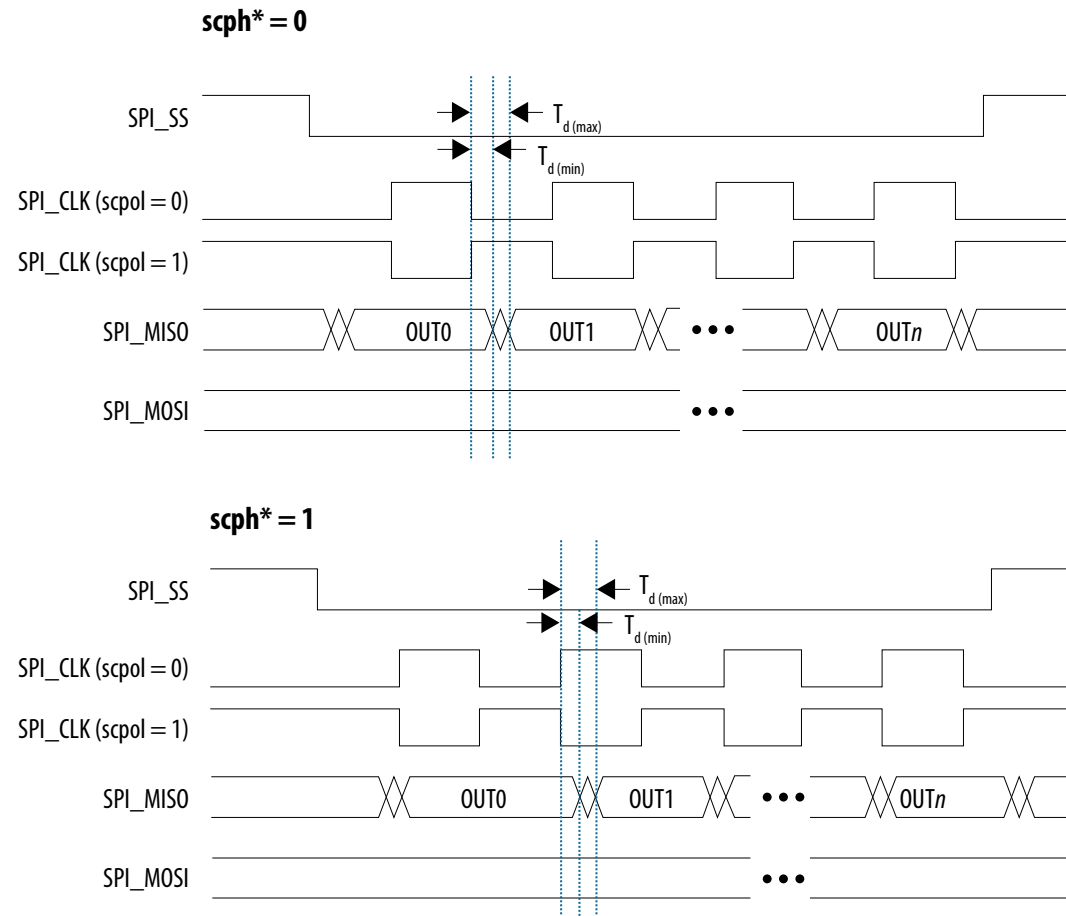
*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register



Table 51. SPI Slave Timing Requirements for Intel Agilex Devices

Symbol	Description	Min	Typ	Max	Unit
T _{spi_ref_clk}	The period of the SPI internal reference clock, sourced from 14_main_clk	2.5	—	—	ns
T _{clk}	SPIM_CLK clock period	30	—	—	ns
T _{dutycycle}	SPIM_CLK duty cycle	45	50	55	%
T _d	Master-in slave-out (MISO) output skew	$(2 \times T_{spi_ref_clk}) + \frac{3}{3}$	—	$(3 \times T_{spi_ref_clk}) + \frac{11}{11}$	ns
T _{su}	Master-out slave-in (MOSI) setup time	4	—	—	ns
T _h	Master-out slave-in (MOSI) hold time	9	—	—	ns
T _{su_{ss}}	SPI_SS_N asserted to first SPIM_CLK edge	T _{spi_ref_clk} + 4	—	—	ns
T _{h_{ss}}	Last SPIM_CLK edge to SPI_SS_N deasserted	T _{spi_ref_clk} + 4	—	—	ns

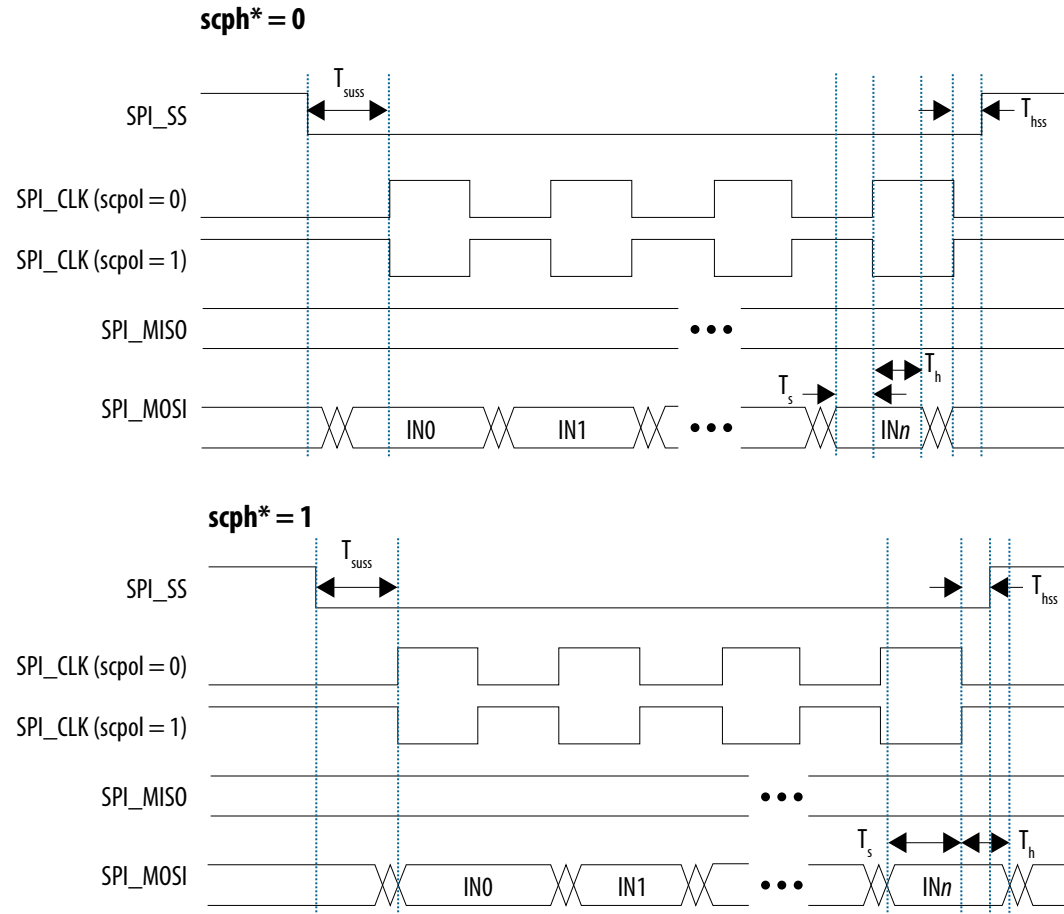
Figure 5. SPI Slave Output Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register



Figure 6. SPI Slave Input Timing Diagram



*Serial clock phase configuration bit, in the SPI controller's CTRLR0 register



HPS SD/MMC Timing Characteristics

Table 52. HPS Secure Digital (SD)/MultiMediaCard (MMC) Timing Requirements for Intel Agilex Devices

These timings apply to SD, MMC, and embedded MMC (eMMC) cards operating at 1.8 V.

Symbol	Description	Min	Typ	Max	Unit
T _{sdmmc_clk}	SDMMC_CCLK clock period (Identification mode)	2500	—	—	ns
	SDMMC_CCLK clock period (SDR12)	40	—	—	ns
	SDMMC_CCLK clock period (SDR25)	20	—	—	ns
T _{dutycycle}	SDMMC_CCLK duty cycle	45	50	55	%
T _{sdmmc_clk_jitter}	SDMMC_CCLK output jitter	—	—	2	%
T _{sdmmc_clk}	Internal reference clock before division by 4	5	—	—	ns
T _d	SDMMC_CMD/SDMMC_DATA[7:0] output delay ⁽⁵¹⁾	$T_{sdmmc_clk} \times \text{drvsel}/2$	—	$3 + (T_{sdmmc_clk} \times \text{drvsel}/2)$	ns
T _{su}	SDMMC_CMD/SDMMC_DATA[7:0] input setup ⁽⁵²⁾	$6 - (T_{sdmmc_clk} \times \text{smp1sel}/2)$	—	—	ns
T _h	SDMMC_CMD/SDMMC_DATA[7:0] input hold ⁽⁵²⁾	$0.5 + (T_{sdmmc_clk} \times \text{smp1sel}/2)$	—	—	ns

None of the HPS I/Os supports 3 V mode, while SD/MMC cards must operate at 3 V at power on. eMMC devices can operate at 1.8 V at power on.

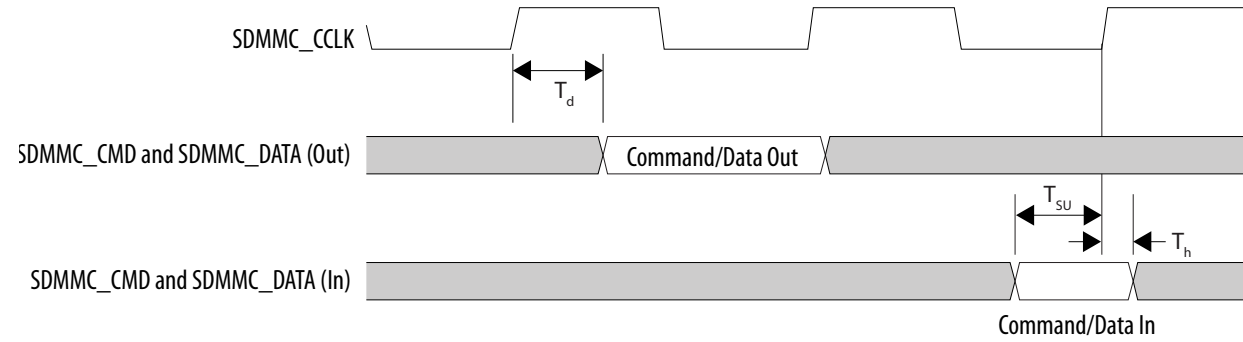
Note: SD cards power up at 3 V. To support SD, your design must include a level shifter between the SD card and the HPS SD/MMC interface.

⁽⁵¹⁾ When the `drvsel` bitfield in the `sdmmc` register is set to 3 (in the system manager) and the reference clock (`sdmmc_clk`) is 200 MHz for example, the output delay time is 7.5 to 10.5 ns.

⁽⁵²⁾ When the `smp1sel` bitfield in the `sdmmc` register is set to 2 (in the system manager) and the reference clock (`sdmmc_clk`) is 200 MHz for example, the setup time is 1 ns and the hold time is 5.5 ns.



Figure 7. SD/MMC Timing Diagram



HPS USB UPLI Timing Characteristics

Table 53. HPS USB 2.0 Transceiver Macrocell Interface Plus (UTMI+) Low Pin Interface (ULPI) Timing Requirements for Intel Agilex Devices

Symbol	Description	Min	Typ	Max	Unit
T_{usb_clk}	USB_CLK clock period	—	16.667	—	ns
T_d	Clock to USB_STP/USB_DATA[7:0] output delay	2	—	7	ns
T_{su}	Setup time for USB_DIR/USB_NXT/USB_DATA[7:0]	4	—	—	ns
T_h	Hold time for USB_DIR/USB_NXT/USB_DATA[7:0]	1	—	—	ns

Figure 8. USB ULPI Timing Diagram



Note: The USB interface supports single data rate (SDR) timing only.



HPS Ethernet Media Access Controller (EMAC) Timing Characteristics

Table 54. Reduced Gigabit Media Independent Interface (RGMII) TX Timing Requirements for Intel Agilex Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	TX_CLK clock period	—	8	—	ns
T_{clk} (100Base-T)	TX_CLK clock period	—	40	—	ns
T_{clk} (10Base-T)	TX_CLK clock period	—	400	—	ns
T_{duty} (1000Base-T)	TX_CLK duty cycle	45	50	55	%
T_{duty} (10/100Base-T)	TX_CLK duty cycle	40	50	60	%
T_d ⁽⁵³⁾ (54)	TXD/TX_CTL to TX_CLK output skew	-0.5	—	0.5	ns

Figure 9. RGMII TX and RMII TX Timing Diagram

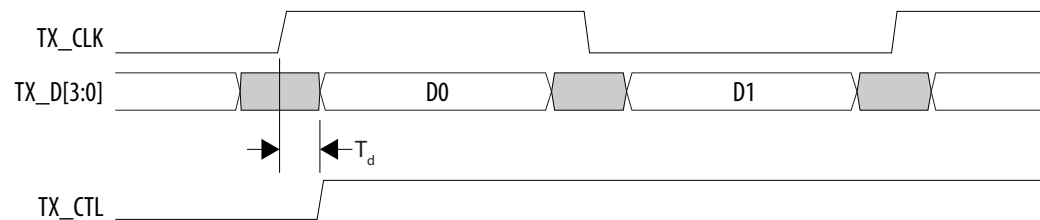


Table 55. RGMII RX Timing Requirements for Intel Agilex Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk} (1000Base-T)	RX_CLK clock period	—	8	—	ns
T_{clk} (100Base-T)	RX_CLK clock period	—	40	—	ns

continued...

⁽⁵³⁾ Rise and fall times depend on the I/O standard, drive strength, and loading. Intel recommends simulating your configuration.

⁽⁵⁴⁾ If you connect a PHY that does not implement clock-to-data skew, you can delay TX_CLK by 1.5—2.0 ns with the HPS I/O programmable delay, to meet the PHY's 1-ns data-to-clock skew requirement.



Symbol	Description	Min	Typ	Max	Unit
T_{clk} (10Base-T)	RX_CLK clock period	—	400	—	ns
$T_{dutycycle}$ (1000Base-T)	RX_CLK duty cycle	45	50	55	%
$T_{dutycycle}$ (10/100Base-T)	RX_CLK duty cycle	40	50	60	%
T_{su}	RX_D/RX_CTL to RX_CLK setup time	1	—	—	ns
T_h ⁽⁵⁵⁾	RX_CLK to RX_D/RX_CTL hold time	1	—	—	ns

Figure 10. RGMII RX and RMII RX Timing Diagram

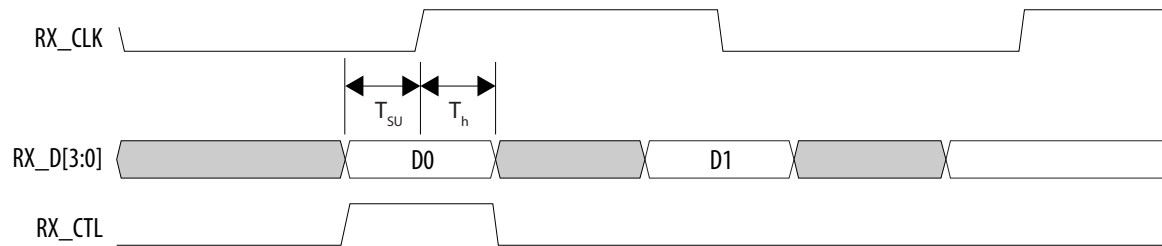


Table 56. Reduced Media Independent Interface (RMII) Clock Timing Requirements for Intel Agilex Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	REF_CLK clock period, sourced by HPS TX_CLK	—	20	—	ns
	REF_CLK clock period, sourced by external clock source	—	20	—	ns
$T_{dutycycle_int}$	Clock duty cycle, REF_CLK sourced by TX_CLK	35	50	65	%
$T_{dutycycle_ext}$	Clock duty cycle, REF_CLK sourced by external clock source	35	50	65	%

Table 57. RMII TX Timing Requirements for Intel Agilex Devices

Symbol	Description	Min	Typ	Max	Unit
T_d	TX_CLK to TXD/TX_CTL output data delay	2	—	10	ns

⁽⁵⁵⁾ If you connect a PHY that does not implement clock-to-data skew, you can meet the HPS EMAC's 1 ns setup time by delaying RX_CLK by 1.5-2 ns, using the HPS I/O programmable delay.



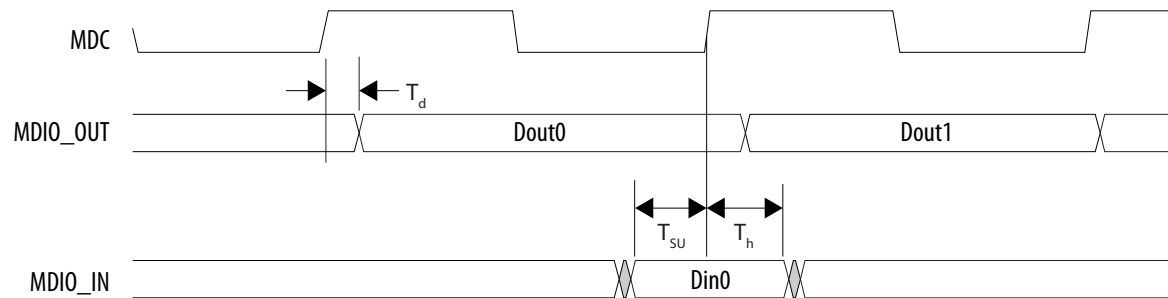
Table 58. RMIIX RX Timing Requirements for Intel Agilex Devices

Symbol	Description	Min	Typ	Max	Unit
T_{su}	RX_D/RX_CTL setup time	2	—	—	ns
T_h	RX_D/RX_CTL hold time	1	—	—	ns

Table 59. Management Data Input/Output (MDIO) Timing Requirements for Intel Agilex Devices

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	MDC clock period	400	—	—	ns
T_d	MDC to MDIO output data delay	10	—	300	ns
T_{su}	Setup time for MDIO data	10	—	—	ns
T_h	Hold time for MDIO data	0	—	—	ns

Figure 11. MDIO Timing Diagram





HPS I²C Timing Characteristics

Table 60. HPS I²C Timing Requirements for Intel Agilex Devices

Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
T _{clk}	Serial clock (SCL) clock period	10	—	2.5	—	μs
T _{clk_jitter}	I2C clock output jitter	—	2	—	2	%
T _{HIGH} ⁽⁵⁶⁾	SCL high period	4 ⁽⁵⁷⁾	—	0.6 ⁽⁵⁸⁾	—	μs
T _{LOW} ⁽⁵⁹⁾	SCL low period	4.7 ⁽⁶⁰⁾	—	1.3 ⁽⁶¹⁾	—	μs
T _{SU;DAT}	Setup time for serial data line (SDA) data to SCL	0.25	—	0.1	—	μs
T _{HD;DAT} ⁽⁶²⁾	Hold time for SCL to SDA data	0	3.15	0	0.6	μs
T _{VD;DAT} and T _{VD;ACK} ⁽⁶³⁾	SCL to SDA output data delay	—	3.45 ⁽⁶⁴⁾	—	0.9 ⁽⁶⁵⁾	μs

continued...

(56) You can adjust T_{high} using the `ic_ss_scl_hcnt` or `ic_fs_scl_hcnt` register.

(57) The recommended minimum setting for `ic_ss_scl_hcnt` is 440.

(58) The recommended minimum setting for `ic_fs_scl_hcnt` is 71.

(59) You can adjust T_{low} using the `ic_ss_scl_lcnt` or `ic_fs_scl_lcnt` register.

(60) The recommended minimum setting for `ic_ss_scl_lcnt` is 500.

(61) The recommended minimum setting for `ic_fs_scl_lcnt` is 141.

(62) T_{HD;DAT} is affected by the rise and fall time.

(63) T_{VD;DAT} and T_{VD;ACK} are affected by the rise and fall time, as well as the SDA hold time (set by adjusting the `ic_sda_hold` register).

(64) Use maximum SDA_HOLD = 240 to be within the specification.

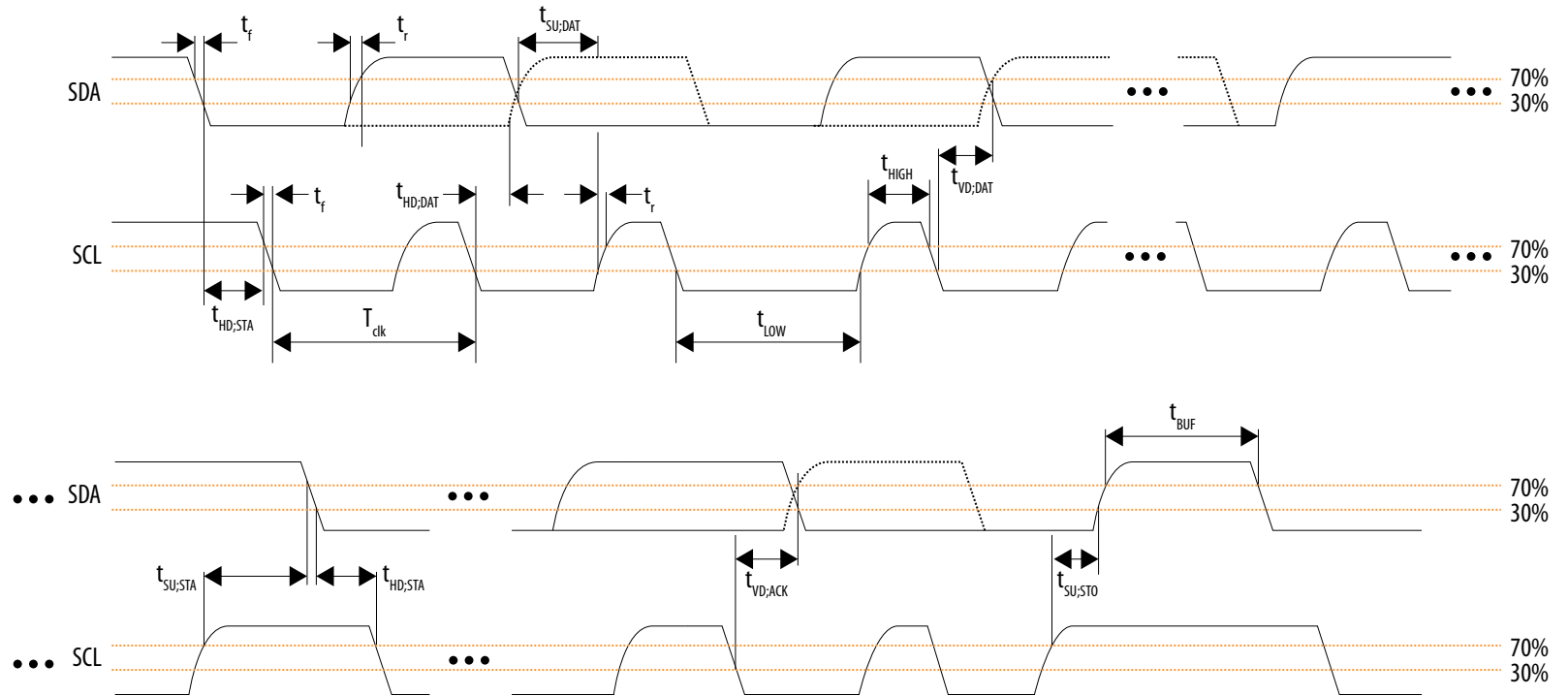
(65) Use maximum SDA_HOLD = 60 to be within the specification.



Symbol	Description	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
$T_{SU;STA}$	Setup time for a repeated start condition	4.7	—	0.6	—	μ s
$T_{HD;STA}$	Hold time for a repeated start condition	4	—	0.6	—	μ s
$T_{SU;STO}$	Setup time for a stop condition	4	—	0.6	—	μ s
T_{BUF}	SDA high pulse duration between STOP and START	4.7	—	1.3	—	μ s
$T_{scl;r}^{(66)}$	SCL rise time	—	1000	20	300	ns
$T_{scl:f}^{(66)}$	SCL fall time	—	300	6.54	300	ns
$T_{sda;r}^{(66)}$	SDA rise time	—	1000	20	300	ns
$T_{sda:f}^{(66)}$	SDA fall time	—	300	6.54	300	ns

(66) Rise and fall time parameters vary depending on external factors such as the characteristics of the IO driver, pull-up resistor value, and total capacitance on the transmission line.

Figure 12. I²C Timing Diagram





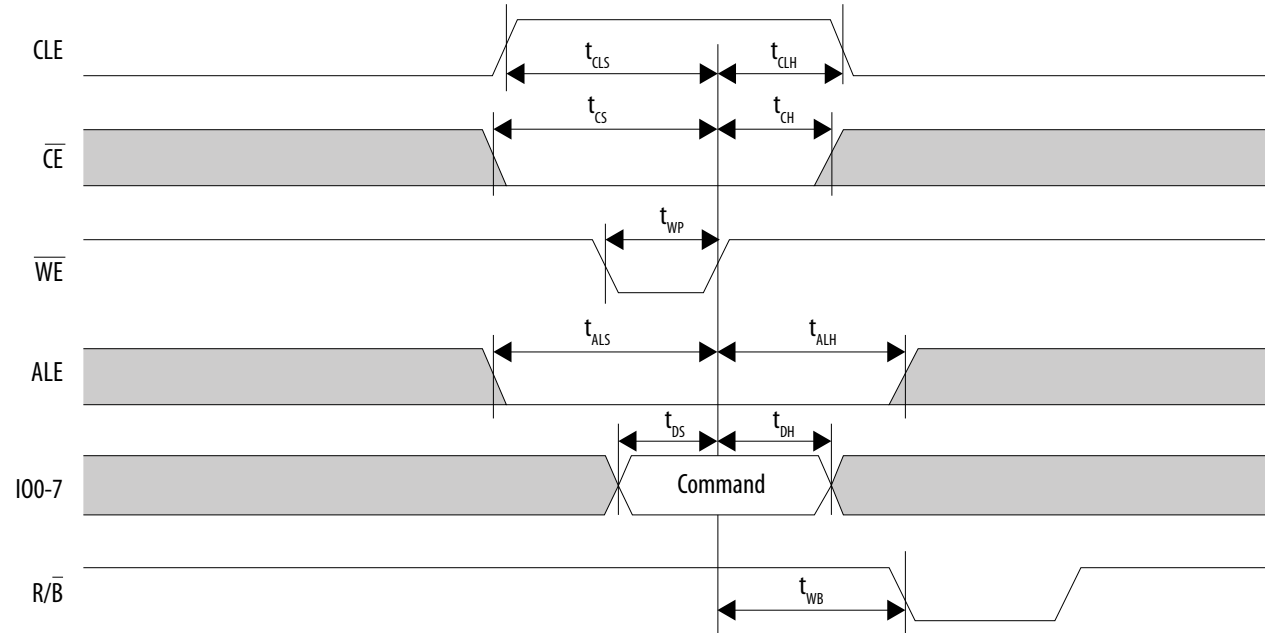
HPS NAND Timing Characteristics

Table 61. HPS NAND ONFI 1.0 Timing Requirements for Intel Agilex Devices

Symbol	Description	Min	Max	Unit
T _{WP} ⁽⁶⁷⁾	Write enable pulse width	10	—	ns
T _{WH} ⁽⁶⁷⁾	Write enable hold time	7	—	ns
T _{RP} ⁽⁶⁷⁾	Read enable pulse width	10	—	ns
T _{REH} ⁽⁶⁷⁾	Read enable hold time	7	—	ns
T _{CLS} ⁽⁶⁷⁾	Command latch enable to write enable setup time	10	—	ns
T _{CLH} ⁽⁶⁷⁾	Command latch enable to write enable hold time	5	—	ns
T _{CS} ⁽⁶⁷⁾	Chip enable to write enable setup time	15	—	ns
T _{CH} ⁽⁶⁷⁾	Chip enable to write enable hold time	5	—	ns
T _{ALS} ⁽⁶⁷⁾	Address latch enable to write enable setup time	10	—	ns
T _{ALH} ⁽⁶⁷⁾	Address latch enable to write enable hold time	5	—	ns
T _{DS} ⁽⁶⁷⁾	Data to write enable setup time	7	—	ns
T _{DH} ⁽⁶⁷⁾	Data to write enable hold time	5	—	ns
T _{WB} ⁽⁶⁷⁾	Write enable high to R/B low	—	200	ns
T _{CEA}	Chip enable to data access time	—	100	ns
T _{REA}	Read enable to data access time	—	40	ns
T _{RHZ}	Read enable to data high impedance	—	200	ns
T _{RR}	Ready to read enable low	20	—	ns

⁽⁶⁷⁾ This timing is software programmable. Refer to the *NAND Flash Controller* chapter in the *Intel Agilex Hard Processor System Technical Reference Manual* for more information about software-programmable timing in the NAND flash controller.

Figure 13. NAND Command Latch Timing Diagram



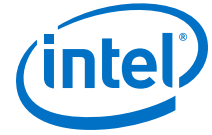


Figure 14. NAND Address Latch Timing Diagram

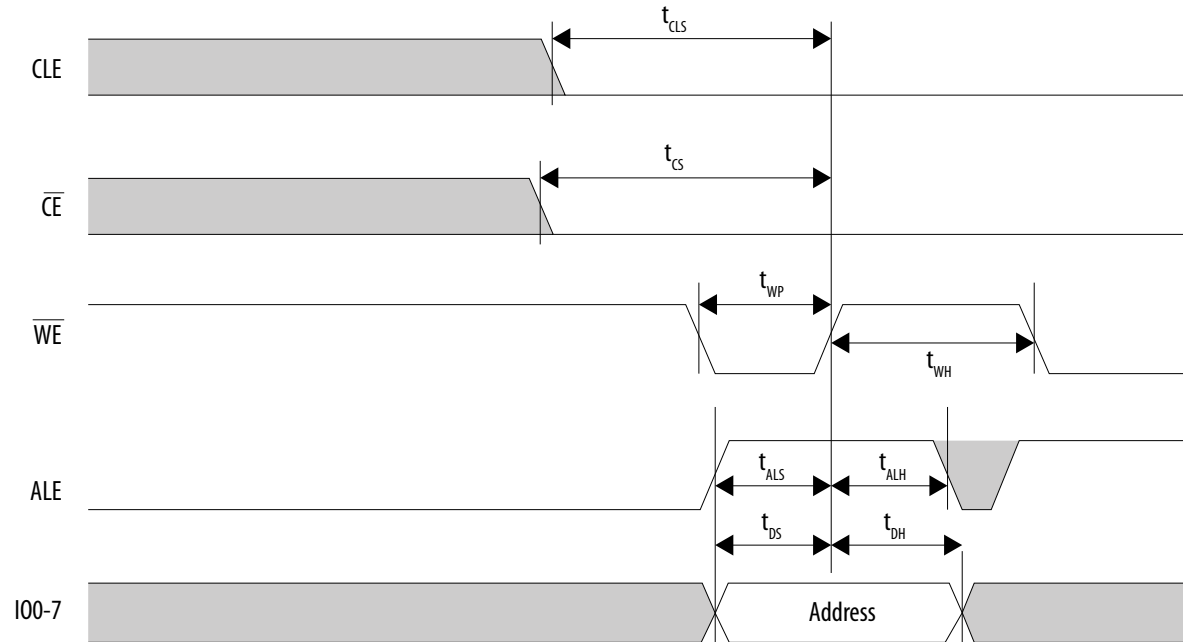
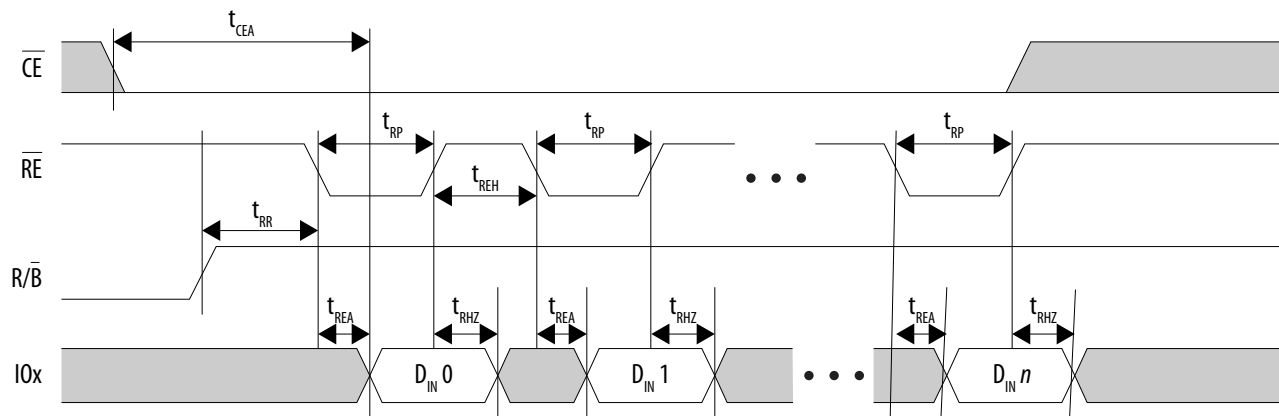


Figure 15. NAND Data Output Cycle Timing Diagram



Figure 16. NAND Data Input Cycle Timing Diagram



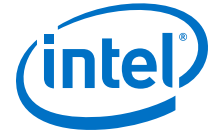


Figure 17. NAND Data Input Timing Diagram for Extended Data Output (EDO) Cycle

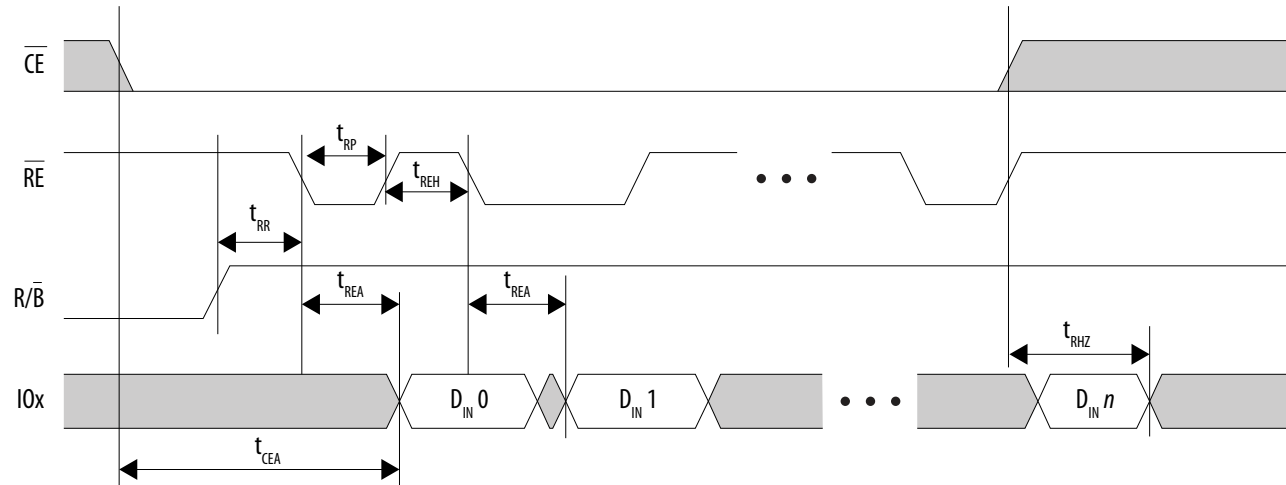
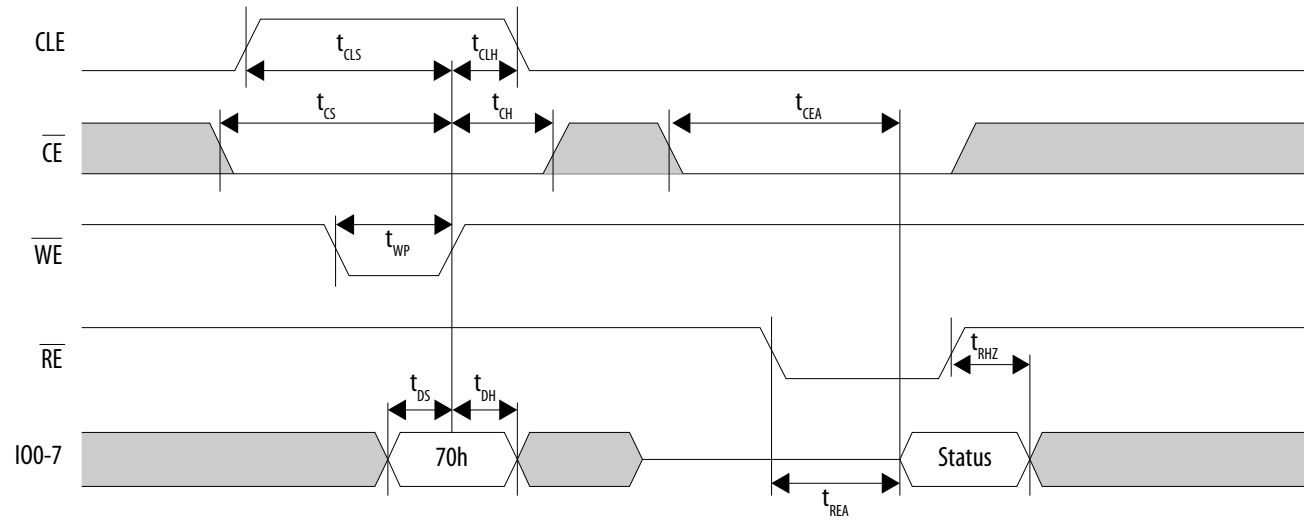


Figure 18. NAND Read Status Timing Diagram



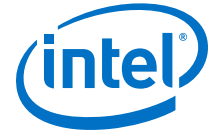
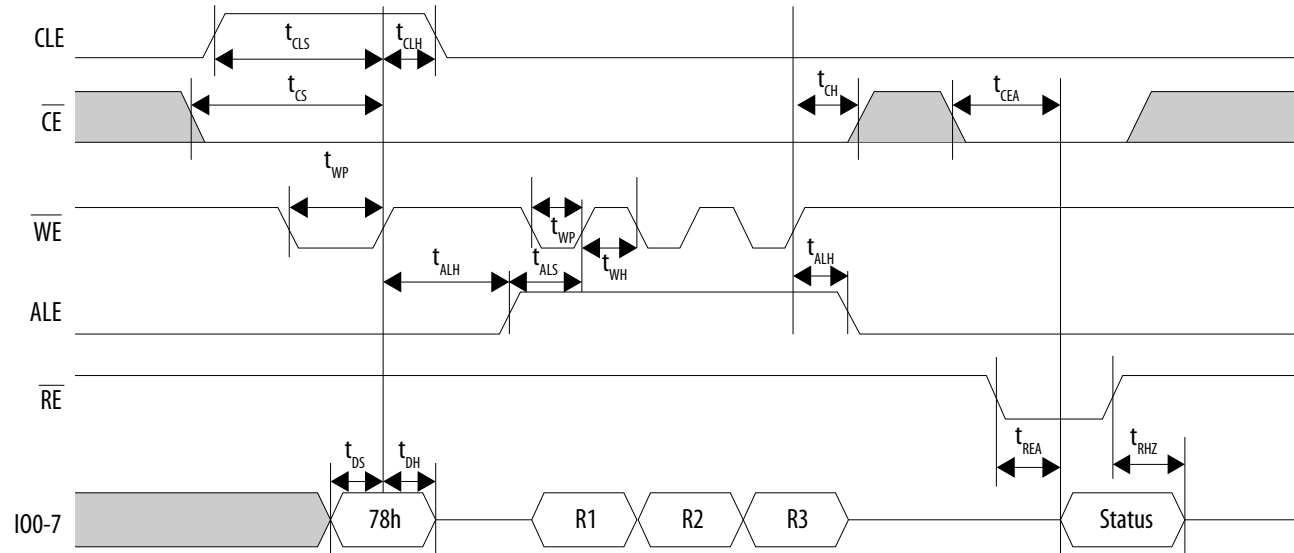


Figure 19. NAND Read Status Enhanced Timing Diagram



HPS Trace Timing Characteristics

Table 62. Trace Timing Requirements for Intel Agilex Devices

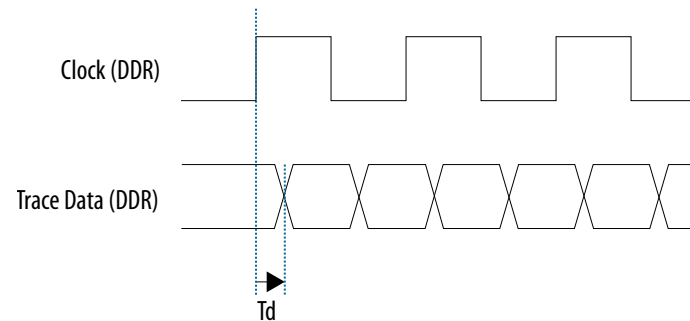
To increase the trace bandwidth, Intel recommends routing the trace interface to the FPGA in the HPS Platform Designer component. The FPGA trace interface offers a 64-bit single data rate path that can be converted to double data rate to minimize FPGA I/O usage.

Depending on the trace module that you connect to the HPS trace interface, you may need to include board termination to achieve the maximum sampling speed possible. Refer to your trace module data sheet for termination recommendations.

Most trace modules implement programmable clock and data skew, to improve trace data timing margins. Alternatively, you can change the clock-to-data timing relationship with the HPS programmable I/O delay.

Symbol	Description	Min	Typ	Max	Unit
T_{clk}	Trace clock period	6.667	—	—	ns
T_{clk_jitter}	Trace clock output jitter	—	—	2	%
$T_{dutycycle}$	Trace clock maximum duty cycle	45	50	55	%
T_d	T_{clk} to D0–D15 output data delay	0	—	1.8	ns

Figure 20. Trace Timing Diagram

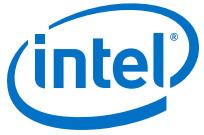




HPS GPIO Interface

The general-purpose I/O (GPIO) interface has debounce circuitry included to remove signal glitches. The debounce clock frequency ranges from 125 Hz to 32 kHz. The minimum pulse width is 1 debounce clock cycle and the minimum detectable GPIO pulse width is 62.5 μ s (at 32 kHz).

If the external signal is driven into the GPIO for less than one clock cycle, the external signal is filtered. If the external signal is between one and two clock cycles, the external signal may or may not be filtered depending on the phase of the signal. If the external signal is more than two clock cycles, the external signal is not filtered.



HPS JTAG Timing Characteristics

Table 63. HPS JTAG Timing Requirements for Intel Agilex Devices

Symbol	Description	Min	Typ	Max	Unit
t_{JCP}	TCK clock period	41.66	—	—	ns
t_{JCH}	TCK clock high time	20	—	—	ns
t_{JCL}	TCK clock low time	20	—	—	ns
t_{JPSU} (TDI)	TDI JTAG port setup time	5	—	—	ns
t_{JPSU} (TMS)	TMS JTAG port setup time	5	—	—	ns
t_{JPH}	JTAG port hold time	0	—	—	ns
t_{JPCO}	JTAG port clock to output	0	—	8	ns
t_{JPZX}	JTAG port high impedance to valid output	—	—	10	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	—	10	ns



HPS Programmable I/O Timing Characteristics

Table 64. HPS Programmable I/O Delay (Output Path) for Intel Agilex Device

output_val_en	output_val	Description	Min	Typ	Max	Unit
0	—	No I/O delay enabled	TBD	0	TBD	ps
1	[0:31]	Intrinsic I/O delay + 1×Minimum + output_val × Chain Delay	TBD	TBD	TBD	ps
2 (INVALID)	—	—	—	—	—	—
3	[0:31]	Intrinsic I/O delay + 2×Minimum + output_val × Chain Delay	TBD	TBD	TBD	ps

Table 65. HPS Programmable I/O Delay (Input Path) for Intel Agilex Device

input_val_en	input_val	Description	Min	Typ	Max	Unit
0	—	No I/O delay enabled	TBD	0	TBD	ps
1	[0:31]	Intrinsic I/O delay + 1×Minimum + input_val × Chain Delay	TBD	TBD	TBD	ps
2 (INVALID)	—	—	—	—	—	—
3	[0:31]	Intrinsic I/O delay + 2×Minimum + input_val × Chain Delay	TBD	TBD	TBD	ps

You can program the number of delay steps by adjusting the I/O Delay register (io0_delay through io47_delay for I/Os 0 through 47).



Configuration Specifications

General Configuration Timing Specifications

Table 66. General Configuration Timing Specifications for Intel Agilex Devices

Symbol	Description	Requirement		Unit
		Min	Max	
$t_{CF12ST1}$ ⁽⁶⁸⁾	nCONFIG high to nSTATUS high	—	20	ms
$t_{CF02ST0}$	nCONFIG low to nSTATUS low	—	400	ms
t_{ST0}	nSTATUS low pulse during configuration error	0.5	1.5	ms
t_{CD2UM} ⁽⁶⁹⁾	CONF_DONE high to user mode	—	2	ms

POR Specifications

Power-on reset (POR) delay is defined as the delay between the time when all the power supplies monitored by the POR circuitry reach the minimum recommended operating voltage to the time when the nSTATUS is released high and your device is ready to begin configuration.

Table 67. POR Delay Specification for Intel Agilex Devices

POR Delay	Minimum	Maximum	Unit
AS (Normal mode), AVST ×8, AVST ×16, AVST ×32, SD/MMC	11	17	ms
AS (Fast mode)	1.1	6.9	ms

⁽⁶⁸⁾ The maximum time does not exceed 2× of the typical value.

⁽⁶⁹⁾ This specification is the initialization time that indicates the time from CONF_DONE signal goes high to INIT_DONE signal goes high.



External Configuration Clock Source Requirements

Table 68. External Configuration Clock Source (OSC_CLK_1) Clock Input Requirements

Description	External Clock Source	Min	Typ	Max	Unit
Clock input frequency ⁽⁷⁰⁾	Powered by V _{CCIO_SDM}	25/100/125			MHz
Clock input jitter tolerance		—	—	2	%
Clock input duty cycle		45	50	55	%

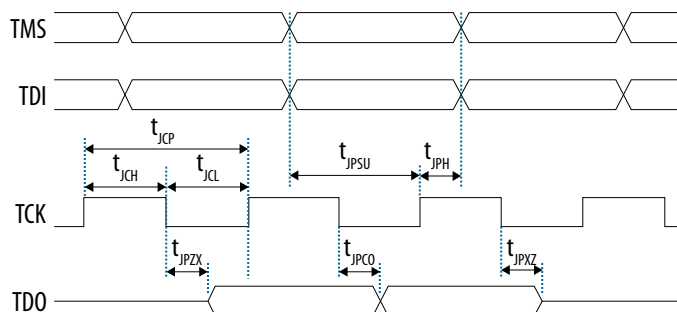
JTAG Configuration Timing

Table 69. JTAG Timing Parameters and Values for Intel Agilex Devices

Symbol	Description	Requirement		Unit
		Minimum	Maximum	
t _{JCP}	TCK clock period	30	—	ns
t _{JCH}	TCK clock high time	14	—	ns
t _{JCL}	TCK clock low time	14	—	ns
t _{JPSU (TDI)}	TDI JTAG port setup time	2	—	ns
t _{JPSU (TMS)}	TMS JTAG port setup time	3	—	ns
t _{JPH}	JTAG port hold time	5	—	ns
t _{JPCO}	JTAG port clock to output	—	7	ns
t _{JPZX}	JTAG port high impedance to valid output	—	14	ns
t _{JPXZ}	JTAG port valid output to high impedance	—	14	ns

⁽⁷⁰⁾ The acceptable clock frequencies are 25 MHz, 100 MHz, and 125 MHz only. You must match the external configuration clock frequency on the OSC_CLK_1 pin to the configuration clock source assignment in the Intel Quartus Prime software. Other frequencies in the range are not supported.

Figure 21. JTAG Timing Diagram



AS Configuration Timing

Table 70. AS Timing Parameters for Intel Agilex Devices

Intel recommends performing trace length matching for nCS0 and AS_DATA pins to AS_CLK to minimize the skew. The maximum tolerance for skew between nCS0 and AS_CLK is recommended to be less than 200 ps. The tolerance for skew between AS_CLK to AS_DATA must be within 0 ps – 400 ps.

Symbol	Description	Minimum	Typical	Maximum	Unit
T_{clk}	AS_CLK clock period	—	7.52	—	ns
T_{duty}	AS_CLK duty cycle	45	50	55	%
T_{dcsfrs}	AS_nCS0[3:0] asserted to first AS_CLK edge	4.21 ⁽⁷¹⁾	—	7.50 ⁽⁷¹⁾	ns
T_{dcslst}	Last AS_CLK edge to AS_nCS0[3:0] deasserted	5.18 ⁽⁷¹⁾	—	8 ⁽⁷¹⁾	ns

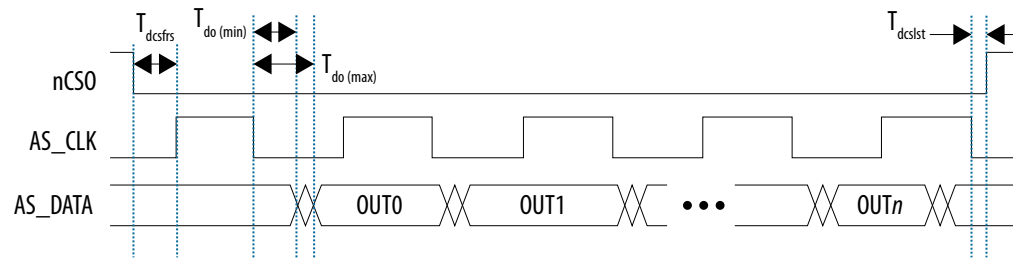
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⁽⁷¹⁾ AS operating at maximum clock frequency = 133 MHz. The delay is larger when operating at AS clock frequency lower than 133 MHz.



Symbol	Description	Minimum	Typical	Maximum	Unit
T_{do}	AS_DATA0 output delay	0	—	1.5 ⁽⁷²⁾	ns
T_{ext_delay} ⁽⁷³⁾	Total external propagation delay on AS signals	0	—	15	ns
T_{dcsb2b}	Minimum delay of slave select deassertion between two back-to-back transfers	1	—	—	AS_CLK

Figure 22. AS Configuration Serial Output Timing Diagram



(72) This specification is based on 20 pF loading.

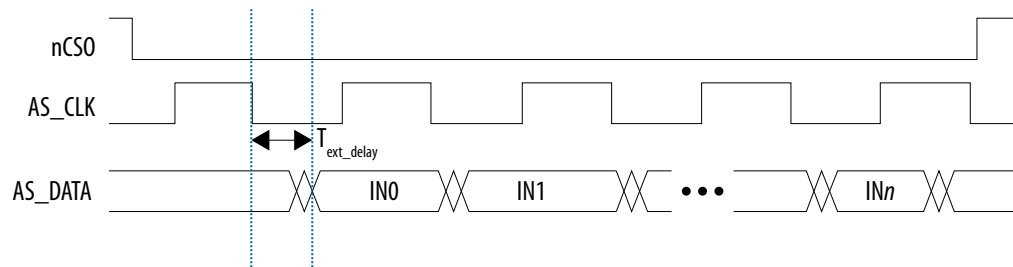
(73) $T_{ext_delay} = T_{bd_clk} + T_{co} + T_{bd_data} + T_{add}$
 T_{bd_clk} : Propagation delay for AS_CLK between FPGA and flash device.

T_{co} : Output hold time and clock low to output valid of flash device. This delay must be used to ensure T_{ext_delay} is within the minimum and maximum specification values.

T_{bd_data} : Propagation delay for AS_DATA bus between FPGA and flash device.

T_{add} : Propagation delay for active/passive components on AS_DATA interfaces.

Figure 23. AS Configuration Serial Input Timing Diagram



Avalon-ST Configuration Timing

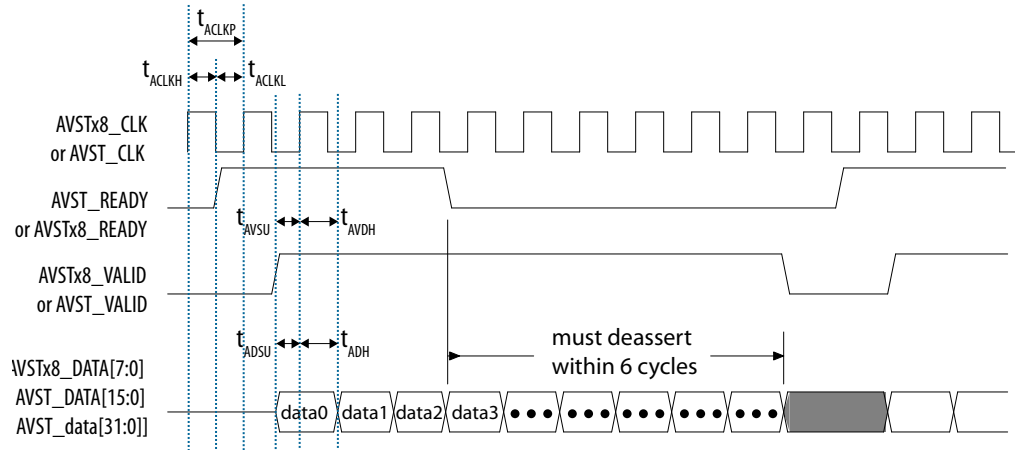
Table 71. Avalon-ST Timing Parameters for ×8, ×16, and ×32 Configurations in Intel Agilex Devices

Symbol	Description	Minimum	Unit
t_{ACKH}	AVST_CLK high time	3.6	ns
t_{ACKL}	AVST_CLK low time	3.6	ns
t_{ACKP}	AVST_CLK period	8	ns
$t_{ADSU}^{(74)}$	AVST_DATA setup time before rising edge of AVST_CLK	5.5	ns
$t_{ADH}^{(74)}$	AVST_DATA hold time after rising edge of AVST_CLK	0	ns
t_{AVSU}	AVST_VALID setup time before rising edge of AVST_CLK	5.5	ns
t_{AVDH}	AVST_VALID hold time after rising edge of AVST_CLK	0	ns

(74) Data sampled by the FPGA (sink) at the next rising clock edge.



Figure 24. Avalon-ST Configuration Timing Diagram



I/O Timing

I/O timing data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the timing analysis. You may generate the I/O timing report manually using the Timing Analyzer.

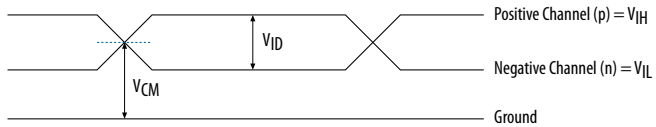

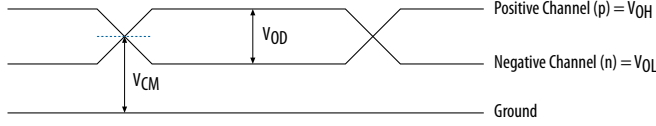
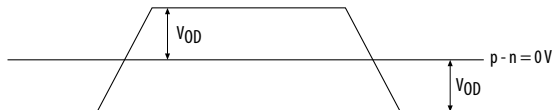
The Intel Quartus Prime Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

Glossary

Table 72. Glossary

Term	Definition
Differential I/O Standards	Receiver Input Waveforms

continued...

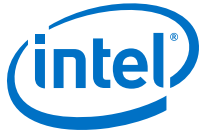
Term	Definition
	<p>Single-Ended Waveform</p>  <p>Positive Channel (p) = V_{IH} Negative Channel (n) = V_{IL} Ground</p> <p>Differential Waveform</p>  <p>p - n = 0 V</p> <p>Transmitter Output Waveforms</p> <p>Single-Ended Waveform</p>  <p>Positive Channel (p) = V_{OH} Negative Channel (n) = V_{OL} Ground</p> <p>Differential Waveform</p>  <p>p - n = 0 V</p>
f_{HSCLK}	I/O PLL input clock frequency.
f_{HSDR}	LVDS SERDES block—maximum/minimum LVDS data transfer rate ($f_{HSDR} = 1/TUI$), non-DPA.
f_{HSRDPA}	LVDS SERDES block—maximum/minimum LVDS data transfer rate ($f_{HSRDPA} = 1/TUI$), DPA.
J (SERDES factor)	LVDS SERDES block—deserialization factor (width of parallel data bus).
JTAG Timing Specifications	JTAG Timing Specifications:

continued...



Term	Definition
R_L	Receiver differential input discrete resistor (external to the Intel Agilex device).
Sampling window (SW)	<p>Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown:</p>
Single-ended voltage referenced I/O standard	<p>The JEDEC standard for the SSTL and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state.</p> <p>The new logic state is then maintained as long as the input stays beyond the DC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing.</p> <p>Single-Ended Voltage Referenced I/O Standard</p>

continued...



Term	Definition
t_c	High-speed receiver/transmitter input and output clock period.
TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the Timing Diagram figure under SW in this table).
t_{DUTY}	LVDS SERDES block—duty cycle on high-speed transmitter output clock.
t_{FALL}	Signal high-to-low transition time (80–20%).
t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input.
t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL.
t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL.
t_{RISE}	Signal low-to-high transition time (20–80%).
Timing Unit Interval (TUI)	The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = $1/(\text{Receiver Input Clock Frequency Multiplication Factor}) = t_c/w$).
$V_{CM(DC)}$	DC Common mode input voltage.
V_{ICM}	Input Common mode voltage—the common mode of the differential signal at the receiver.
$V_{ICM(DC)}$	$V_{CM(DC)}$ DC Common mode input voltage.
V_{ID}	Input differential voltage swing—the difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
$V_{DIF(AC)}$	AC differential input voltage—minimum AC input differential voltage required for switching.
$V_{DIF(DC)}$	DC differential input voltage—minimum DC input differential voltage required for switching.
<i>continued...</i>	



Term	Definition
V_{IH}	Voltage input high—the minimum positive voltage applied to the input which is accepted by the device as a logic high.
$V_{IH(AC)}$	High-level AC input voltage.
$V_{IH(DC)}$	High-level DC input voltage.
V_{IL}	Voltage input low—the maximum positive voltage applied to the input which is accepted by the device as a logic low.
$V_{IL(AC)}$	Low-level AC input voltage.
$V_{IL(DC)}$	Low-level DC input voltage.
V_{OCM}	Output Common mode voltage—the common mode of the differential signal at the transmitter.
V_{OD}	Output differential voltage swing—the difference in voltage between the positive and complementary conductors of a differential transmission line at the transmitter.
V_{SWING}	Differential input voltage.
V_{OX}	Output differential cross point voltage.
$V_{IX(AC)}$	V_{IX} Input differential cross point voltage.
W	LVDS SERDES block—Clock Boost Factor.

Document Revision History for the Intel Agilex Device Data Sheet

Document Version	Changes
2019.04.02	Initial release.