

Introduction

This errata sheet provides updated information on Stratix® II devices. This document addresses known device issues and includes methods to work around the issues.

Table 1 shows the specific issues and which Stratix II devices each issue affects.

<i>Table 1. Stratix II Family Issues (Part 1 of 2)</i>		
Issue	Affected Devices	Fixed Devices
Certain instances of PLL reconfiguration cause the scandone signal to remain in the low position. T _{RECONFIGWAIT} specification added to this section ensures proper reconfiguration.	All Stratix II devices	—
Lock signal issue at low M counter settings.	All Stratix II devices	—
Stratix II PLL Self-Reset support removed.	All Stratix II devices	—
Stratix II Device Handbook (Volume 1: version 4.1 and Volume 2: version 4.1) incorrectly indicates that the 1.2-V HSTL I/O standard is supported on I/O banks 3, 4, and 7 in all speed grade devices. However, the 1.2-V HSTL I/O standard is supported only on I/O banks 4, 7, and 8 and only in the –3 speed grade. Quartus® II software version 6.0 SP1 and earlier incorrectly supports 1.2-V HSTL on I/O bank 3 in –3 devices. Quartus II software version 6.0 SP1 with Patch 1.18 or version 6.1 and later will correctly support 1.2-V HSTL on bank 8 instead of on bank 3 in –3 devices.	All Stratix II devices	—
M-RAM blocks do not support the byte enable feature when in x128 or x144 mode and using simple dual-port mode. The ability to use byte enable with these modes within a single M-RAM block has been removed in the Quartus II software version 6.0.	All Stratix II devices	—

Table 1. Stratix II Family Issues (Part 2 of 2)		
Issue	Affected Devices	Fixed Devices
M4K blocks exhibit intermittent read failure when using dual-port mode and dual clocks. Single-port memory can be affected if Quartus II place and route packs two single-port memory functions into one M4K block. The dual-port mode with a single clock is not affected. This has been corrected in Quartus II software version 5.0 SP2 and later.	All Stratix II devices	—
The CRC error detection frequency setting for the internal oscillator divider is limited to a minimum setting of 2 (and a maximum of 50 MHz). The divide by 1 setting is removed in the Quartus II software version 5.1.	All Stratix II devices (1)	—
Clock output pins in the top and bottom PLL banks 9, 10, 11, and 12 do not meet the LVDS industry V_{OD} and V_{OCM} specifications.	All Stratix II devices	—
Clock input and clock output pins in the top and bottom I/O and PLL banks do not support HyperTransport™ technology. This feature is removed in the Quartus II software version 5.0 SP1.	All Stratix II devices	—
M-RAM block write operations on one port may fail if the read or write clock high time on the other port is greater than 5 ns.	(2)	(2)
M-RAM blocks may exhibit write enable issues.	EP2S60 ES devices	EP2S60 Production devices
M-RAM blocks do not support the byte enable feature.	EP2S60 ES devices	EP2S60 Production devices
Four user I/O pins exhibit higher than specified pin current under certain conditions.	EP2S60 ES devices	EP2S60 Production devices
The PORSEL setting of 12 ms requires a shorter maximum V_{CCINT} ramp-up time.	EP2S60 ES devices	EP2S60 Production devices

Notes to Table 1:

- (1) EP2S130 and EP2S180 devices were already limited to 50 MHz in the Quartus II software version 5.0 SP1. Further characterization results show the limit for all device densities must be 50 MHz.
- (2) See Table 4 for silicon status.

Stratix II FPGA Device Family Issues

PLL Reconfiguration Issue

Certain instances of PLL reconfiguration cause the `scandone` signal to remain in the low position. The following three cases explain when this incorrect device operation will occur. These sections also provide solutions to work around the issue.

Case 1: Reconfiguring Only the Post-Scale C[5..0] Counters

After all the `scandata` bits are loaded into the scan chain, any changes to the post-scale counters (count value) are updated automatically and correctly, but the `scandone` signal will remain low. The `busy` signal in the `ALTPLL_RECONFIG` megafunction will also be affected by this issue since the `busy` signal follows the `scandone` signal generated from the reconfiguration block.

To work around this problem, after the `scanwrite` signal is asserted high, wait for a certain time specified by $T_{\text{RECONFIGWAIT}}$. If the `ALTPLL_RECONFIG` megafunction is used, this wait time comes after the scan chain is loaded (the megafunction asserts the `scanwrite` high after loading the scan chain); make sure a minimum number of `scanclk` cycles corresponding to the PLL reconfiguration scan chain length is provided after PLL reconfiguration is asserted. If `scandone` does not go high after this wait time, then reset the PLL for at least 500 ns using the `PLLsareset` signal to ensure that the `scandone` signal goes high. When `scanwrite` is deasserted, the `scandone` signal will go low after several `scanclk` cycles. The time required for the wait after `scanwrite` goes high and when `areset` is applied can be calculated by the formula:

$$T_{\text{RECONFIGWAIT}} = (\text{Max C-counter}) / (0.8 * \text{VCO freq})$$

The maximum wait time between when `scanwrite` goes high and when the `areset` signal is asserted is 2 μs .

Case 2: Reconfiguring the N or M Counters

After all the `scandata` bits are loaded into the scan chain, any changes to the N or M (count value) are not updated and the `scandone` signal will remain low.

To work around this problem, after the `scanwrite` signal is asserted high, wait for a certain time specified by $T_{\text{RECONFIGWAIT}}$. If the `ALTPLL_RECONFIG` megafunction is used, this wait time comes after the scan chain is loaded; make sure a minimum number of `scanclk` cycles corresponding to the PLL reconfiguration scan chain length is provided. If `scandone` does not go high after this wait time, then reset the PLL for at least 500 ns using the `PLLsareset` signal to ensure that the

`scandone` signal goes high and the new (N, M) counter settings are updated successfully. The time required for the wait after `scanwrite` goes high and when the `areset` is applied can be calculated by the formula:

$$T_{\text{RECONFIGWAIT}} = (\text{Max C-counter}) / (0.8 * \text{VCO freq})$$

The maximum wait time between when `scanwrite` goes high and when the `areset` signal is asserted is 2 μs .

Case 3: Reconfiguring the Phase Shift of the M or the C[5..0] Counters Using the Phase-Shift Stepping Feature

When using the phase-shift stepping feature to reconfigure the phase shift settings, the M or C[5..0] counters are updated automatically with the new phase shift value. The `scandone` signal remains in the low position. Altera recommends against using `scandone` as a control signal when using the phase shift stepping feature.

If the PLL is reset by toggling the `areset` signal, the phase shift is set back to the original phase shift in the configuration file.

Lock Circuit Failure With Low M-Counter Values

Altera has identified an issue with the `lock` signal under certain conditions. The `lock` signal can show an out-of-lock condition although the VCO is still frequency-locked. This is due to high compensation variability when the PLL is operating at low M counter values and low charge pump currents. This issue affects both the enhanced and fast PLLs. The modes affected are shown in [Table 2](#).

Table 2. Affected Stratix II PLL Settings	
M	ICP (Charge Pump Current)
1,2	All
3, 4, 5	12 μA , 30 μA (smallest two settings)

The Quartus II software version 6.0 SP1 and prior versions supporting Stratix II are affected by this issue. Patch 1.45 for the Quartus II software version 6.0 SP1 and Quartus II version 6.1 and later will prevent the compiler from choosing these illegal M and ICP PLL setting combinations. The Quartus II software version 6.1 and later will issue a critical warning message if you force the PLL to use affected settings by defining the advanced parameter PLL settings in an HDL design file.

Stratix II PLL Self-Reset Support Removed

Altera has found the self-reset feature in Stratix II PLLs to function incorrectly. If this feature is enabled upon loss of lock, the `self_reset` signal is asserted. The PLL will regain lock after assertion of the `self_reset`, but the phase relationship between the reference clock and the output clocks and also the phase relationship between the output clocks may not be maintained.

Altera recommends using the `areset` signal upon loss of lock to reset the PLL and to maintain the phase relationship between the output clocks.

The self-reset feature will no longer be supported in future versions of the Quartus II software.

The following issues affect all Stratix II device densities. There are additional issues that affect the EP2S60 Engineering Sample (ES) device only which are detailed in the [“EP2S60 ES Device Information” on page 12](#).

1.2-V HSTL Support Issue

The 1.2-V HSTL support issue relates to both the Stratix II technical documentation and the Quartus II software.

Documentation

The Stratix II Device Handbook (Volume 1: version 4.1 and Volume 2: version 4.1) incorrectly indicates that the 1.2-V HSTL I/O standard is supported on I/O banks 3, 4, and 7 in all speed grade devices. The 1.2-V HSTL I/O standard is only supported on banks 4, 7, and 8 and only in the -3 speed grade. Version 4.2 (both Volume 1 and Volume 2) of the handbook corrects this error.

Quartus II Software Version 6.0 SP1

Quartus II software version 6.0 SP1 and earlier incorrectly supports 1.2-V HSTL on I/O banks 3, 4, and 7 in -3 speed grade devices. Quartus II software version 6.0 SP1 with Patch 1.18 or version 6.1 and later will correctly support 1.2-V HSTL on banks 4, 7, and 8 instead of banks 3, 4, and 7 in -3 speed grade devices.

Solution

Case 1: You had planned to implement 1.2-V HSTL on bank 3 of Stratix II or Stratix II GX -3 speed grade devices.

1. Install Quartus II 6.0 SP1.

2. Install Quartus II 6.0 Patch 1.18.
(http://www.altera.com/support/kdb/solutions/rd08092006_527.html)
3. Move all 1.2-V HSTL signals to bank 4, 7, or 8 and recompile.

Case 2: 1.2-V HSTL is already implemented on I/O bank 3 of Stratix II or Stratix II GX –3 speed grade devices (board layout is done).

Altera recommends re-spinning the board to move 1.2-V HSTL signals to bank 4, 7, or 8 and recompiling the design with Quartus II version 6.0 with Patch 1.18 or Quartus II version 6.1 and later. If a board re-spin is not possible, contact Altera Technical Services for support.

Case 3: You had planned to implement 1.2-V HSTL in Stratix II or Stratix II GX –4 or –5 speed grade devices.

Recompile the design to a –3 speed grade device with the Quartus II software version 6.0 with Patch 1.18 or Quartus II version 6.1 and later.

M-RAM Byte Enable Support for $\times 128$ and $\times 144$ Modes

M-RAM blocks in $\times 128$ or $\times 144$ mode only support byte enables when using single clock mode. If clock enables are being used in $\times 128$ or $\times 144$ single clock mode, you must use the same clock enable setting for both ports A and B.



For more information on how byte enables are supported for other memory widths and modes, refer to *TriMatrix Embedded Memory Blocks in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook*.

Starting with the Quartus II software version 6.0, if you implement a RAM that is in one of the affected modes and you are targeting an M-RAM block, the Quartus II software implements the RAM instance using two M-RAM blocks. This gives you the desired functionality, but uses an additional M-RAM block per instance.

M4K Intermittent Read Failure in Dual-Port Mode with Dual Clocks

Issue

All Stratix II devices are susceptible to a read failure on M4K blocks used in dual-port mode with dual clocks. When the failure occurs the failing data bit with a logic value 1 is read as 0.

Single-port memories can be affected if Quartus II place and route packs two single port memories with different clocks into one M4K block, effectively making the M4K block a dual-port RAM.



For more information, refer to Pack Mode Support section of the *TriMatrix Embedded Memory Blocks in Stratix II Devices* in Volume II of the *Stratix II Device Handbook*.

The dual-port mode with a single clock is not affected.

Root Cause

The root cause was identified to be a configuration bit settings error.

Solution

The problem is fixed by changing the bit settings for M4K blocks set by Quartus II software in the assembler step during compilation. Existing designs using M4K blocks in a mode with dual clocks requires a recompile of the Quartus II project in the updated software. Quartus II software versions 5.1 and 5.0 SP2 contain the fixed configuration bit settings.

Impact

There is a minor impact on timing for M4K blocks used in dual-port mode with dual clocks. The timing changes are reflected in Quartus II software version 5.1. Performance M4K blocks using a single clock is unaffected.

CRC Error Detection Maximum Frequency is 50 MHz

Beginning with version 5.1 of the Quartus II software, the minimum setting for the **Divide error check frequency by** option is 2 for all device densities. The **Divide by 1** setting is removed in version 5.1 of the Quartus II software. The **Divide by 1** setting has already been removed for the EP2S130 and the EP2S180 devices in version 5.0 SP1 of the Quartus II software. Characterization data shows that false errors can occur for operation at the 100-MHz setting (divider set to 1) for all device densities.



Designers who enable the CRC error detection feature in the **Device & Pin Options** dialog box and who currently use the **Divide by 1** setting must change the setting to 2. The **Divide by 1** setting will be removed beginning with version 5.1 of the Quartus II software. The default setting is **Divide by 256**.

The **Divide error check frequency by** option is located in the Assignments menu by clicking **Device > Device & Pin Options button > Error Detection CRC**.

Column Clock Pins Do Not Meet LVDS Specifications

Device characterization has shown that the clock output pins of the top and bottom PLLs in banks 9, 10, 11, and 12 do not meet the LVDS industry V_{OD} and V_{OCM} specifications. The top and bottom clock output pins support a wider range for these two specifications as shown in [Table 3](#). The row I/O pins operate within the LVDS industry specifications.



For the full list of LVDS specifications for left and right I/O banks and top and bottom I/O banks, refer to the *DC & Switching Characteristics* chapter in volume 1 of the *Stratix II Device Family Handbook*.

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OD}	Output differential voltage (single-ended)	$R_L = 100 \Omega$	250	—	550	mV
V_{OCM}	Output common mode voltage	$R_L = 100 \Omega$	840	—	1,375	mV

Column Clock Pins Do Not Support HyperTransport Technology

Device characterization has shown that the clock input pins of the top and bottom I/O banks 3, 4, 7, and 8 and the clock output pins of the top and bottom PLL banks 9, 10, 11, and 12 do not meet the HyperTransport technology specifications. Beginning with version 5.0 SP1, the Quartus II software does not support HyperTransport technology on the clock input and output pins of the top and bottom banks.

The row I/O pins and row clock pins support HyperTransport technology. These pins are used to implement a HyperTransport interface with a Stratix II device.

M-RAM Block Read & Write Issue

Altera has identified a read and write issue when using the M-RAM blocks in dual-port mode. M-RAM block write operations on one port may fail if the read or write clock high time on the other port is greater than 5 ns (less than 100-MHz clock frequency with a 50/50 duty cycle).

Table 4 shows the Stratix II silicon status.

Device	Revision A Silicon (1)	Revision B Silicon
EP2S15	Production (2)	—
EP2S30	Production	Production
EP2S60	(3) (4)	(4)
EP2S90	Production	Production
EP2S130	ES and production	Production
EP2S180	ES	Production

	Affected Silicon
	Corrected Silicon

Notes to Table 4:

- (1) Configuration files for affected silicon are forward compatible with fixed silicon except for EP2S60 ES configuration files.
- (2) EP2S15 devices are not affected because EP2S15 devices do not have M-RAM blocks.
- (3) EP2S60 ES devices have additional issues addressed in the “EP2S60 ES Device Issues” section.
- (4) All silicon revisions of EP2S60 ES devices are affected. All silicon revisions of EP2S60 production devices are corrected.

The die revision is identified by the alphanumeric character (Z) before the fab code (first two alphanumeric characters) in the date code printed on the top side of the device. Figure 1 shows a Stratix II device’s top side date code.

Figure 1. Stratix II Device Top Side Lot Number


A XβZ ## ####

 Die Revision

Table 5 highlights the effects of this issue on the M-RAM operating in its different modes for all Stratix II devices.

Table 5. M-RAM Safe Operation Modes for All Devices		
M-RAM Mode	Safe Mode	
	All Devices Except EP2S60 ES Devices	EP2S60 ES Devices
Single-port	Always safe. Use the Quartus II software version 4.2 SP1 or later to generate programming files.	Always safe. Use the Quartus II software version 4.2 SP1 or later and the INI variable shown in Table 6 to generate programming files.
Simple or true dual-port, single clock	Always safe. Use the Quartus II software version 4.2 SP1 or later to generate programming files.	Safe if read clock frequency is greater than or equal to 100 MHz (or have clock high times less than or equal to 5 ns) or the write enable is tied to V_{CC} . Use the Quartus II software version 4.2 SP1 or later and the INI variable shown in Table 6 to generate programming files.
Simple dual-port, dual-clock	Safe if read clock frequency is greater than or equal to 100 MHz (or has a clock high time less than or equal to 5 ns). In addition, if either clock needs to be stopped, you must use the clock enable port of the M-RAM block. Use the Quartus II software version 4.2 SP1 or later and the INI variable shown in Table 6 to generate programming files.	Safe if read clock frequency is greater than or equal to 100 MHz (or has a clock high time less than or equal to 5 ns). In addition, if either clock needs to be stopped, you must use the clock enable port of the M-RAM block. Use the Quartus II software version 4.2 SP1 or later and the INI variable shown in Table 6 to generate programming files.
True dual-port, dual-clock	Safe if both clock frequencies are greater than or equal to 100 MHz (or have clock high times less than or equal to 5 ns). In addition, if either clock needs to be stopped, you must use the clock enable port of the M-RAM block. Use the Quartus II software version 4.2 SP1 or later and the INI variable shown in Table 6 to generate programming files.	Safe if both clock frequencies are greater than or equal to 100 MHz (or have clock high times less than or equal to 5 ns). In addition, if either clock needs to be stopped, you must use the clock enable port of the M-RAM block. Use the Quartus II software version 4.2 SP1 or later and the INI variable shown in Table 6 to generate programming files.

Designers must ensure that their M-RAM blocks are only used in the safe modes described in [Table 5](#). If the M-RAM block cannot be placed in one of the safe modes described in [Table 5](#), the designer must contact Altera Applications at <https://mysupport.altera.com/eservice/> for a design solution. Use the INI variable shown in [Table 6](#) for the corresponding safe mode.

Device	INI Variable
All Devices (except EP2S60 ES Devices)	<code>set_global_assignment -name INI_VARS "allow_stratixii_mrams_in_dual_port_mode=on"</code>
EP2S60 ES Devices	<code>set_global_assignment -name INI_VARS "allow_ep2s60es_mram_usage=on; allow_stratixii_mrams_in_dual_port_mode=on"</code>



Make sure the INI variable is contained on a single line in the Quartus II Settings File (.qsf) file in the project directory.

[Table 7](#) lists the effects of this issue on Quartus II software features.

Feature Affected	Issue	
	All Devices Except EP2S60 ES Devices	EP2S60 ES Devices
SignalTap II feature, Quartus II software version 4.2 SP1	If the SignalTap II feature is used to target an M-RAM block, the designer must contact Altera Applications at https://mysupport.altera.com/eservice/ to download a patch to enable its use.	If the SignalTap II feature is used to target an M-RAM block, the designer must contact Altera Applications at https://mysupport.altera.com/eservice/ to download a patch to enable its use.
In-System Memory Editor, Quartus II software version 4.2 SP1	The In-System Memory Editor is not supported when targeting M-RAM blocks in affected versions of silicon. In order to use this feature you must target the corrected silicon.	The In-System Memory Editor is not supported when targeting M-RAM blocks in EP2S60 ES devices.



For specific information about how this errata affects these software features, see the Altera support solutions page at http://www.altera.com/support/kdb/solutions/rd01262005_256.html

Beginning with version 5.0, the Quartus II software supports the logic option, **Maintain Compatibility with All Stratix II M-RAM Versions**. This option is available to provide compatibility between affected and corrected silicon, and will control how Quartus II implements the M-RAM blocks. The default setting for the compatibility option is **Off**, starting with Quartus II version 5.1 and later.

When the **Maintain Compatibility with All Stratix II M-RAM versions** option is set to **Off**, Quartus II software generates programming files that are only compatible with revision B silicon for EP2S30, EP2S90, EP2S130, and EP2S180 devices. These programming files do not configure revision A silicon for these devices. The `nSTATUS` pin drives out low and the configuration fails. The Quartus II software implements all MRAM blocks, and does not check for unsafe modes.

When the **Maintain Compatibility with All Stratix II M-RAM versions** option is set to **On**, the Quartus II software generates programming files that are compatible with both silicon revisions A and B for EP2S30, EP2S90, EP2S130, and EP2S180 devices. The Quartus II software implements all RAM instances that have an auto block type as M512 or M4K blocks if they use unsafe operation modes as described in [Table 5 on page 10](#). If the RAM instance is set to use an M-RAM block in the MegaWizard Plug-In Manager and it is using an unsafe operating mode, the Quartus II Compiler issues an error and halt compilation without generating a programming file. In this case, use the appropriate INI variable in [Table 6](#) or set the **Maintain Compatibility with All Stratix II M-RAM Versions** logic option to **Off** to enable programming file generation.

EP2S60 ES Device Information

This section describes silicon issues affecting the Stratix II EP2S60 ES devices and describes additional differences between the EP2S60 ES and production silicon.



Although the configuration file sizes are the same, the configuration files for EP2S60 ES devices and EP2S60 production devices are not compatible. If a designer attempts to configure an EP2S60 production device with an EP2S60 ES configuration file, or vice versa, the `nSTATUS` pin is driven low and configuration fails. To make sure the Quartus II software generates the correct configuration file, designers must select the EP2S60 ES ordering codes when compiling for EP2S60 ES devices. Similarly, designers must select the EP2S60 production ordering codes when compiling for EP2S60 production devices.

EP2S60 ES Device Issues

Altera has identified silicon issues affecting the Stratix II EP2S60 ES devices. All of these issues will be fixed in EP2S60 production devices. The issues are:

- M-RAM blocks may have write failures in certain operation modes.
- M-RAM blocks may exhibit write enable issues.
- M-RAM blocks do not support the byte enable feature.
- Four user I/O pins exhibit higher than specified pin current under certain conditions.
- The PORSEL setting of 12 ms requires a shorter maximum V_{CCINT} ramp-up time.

M-RAM Block Read/Write Issue

M-RAM block write operations on one port may fail if the read or write clock high time on the other port is greater than 5 ns (that is, less than 100-MHz clock frequency with a 50/50 duty cycle).

See [Table 5 on page 10](#) for a list of safe operation modes for all Stratix II devices.

M-RAM Block Write Enable Support

The EP2S60 ES device M-RAM blocks may exhibit failures if the write enable is changed during the write clock high time. To ensure this does not cause a problem in your design, perform the following steps in the Quartus II software:

1. Run Timing Analyzer with Slow Timing Model (Default).
2. Run Timing Analyzer with Fast Timing Model. From the Processing menu, click **Start > Start Timing Analyzer (Fast Timing Model)**.
3. Verify that all hold time requirements are met.
4. If there are hold time violations, click **Settings > Fitter Settings** from the Assignments menu and make the following assignments:
 - a. Turn **All Paths** on in **Optimize Hold Timing**.
 - b. Turn **Optimize Fast Corner Timing** on.
 - c. Recompile the design and re-run Timing Analyzer for the Slow and Fast Models.

- If there are still hold time violations, manually add or remove delay in the design to the failing paths to meet hold time requirements.



All Stratix II production devices support the write enable feature on M-RAM blocks without need for the above steps.

M-RAM Block Byte Enable Support

The EP2S60 ES device M-RAM blocks do not support the byte enable feature. The byte enable feature is supported on the M512 and M4K RAM blocks.

For designs that require M-RAM byte enable support on EP2S60 ES devices, the designer must contact Altera Applications at <https://mysupport.altera.com/eservice/> for a design solution.



All Stratix II production devices support the byte enable feature on M-RAM blocks.

Pin Current Higher Than Specified

Four EP2S60 ES device user I/O pins have a resistive path with high current draw when the steady-state voltage applied to the pin is greater than the V_{CCIO} voltage level of the associated I/O bank. If the pin voltage is more than 0.2 V above V_{CCIO} , the pin current will increase. Therefore, designers should not drive the pins listed in [Table 8 on page 14](#) higher than the V_{CCIO} level of the I/O bank in which the pin resides. The high current draw does not occur when these four pins are used as output pins. If the voltage at the pin is greater than the V_{CCIO} level of the I/O bank due to overshoot (reflections), the increase in pin current is not excessive and will not damage the device. See [Table 8](#).

Table 8. Affected Pins in EP2S60 ES Devices

Pin Name	I/O Bank	Pin Number		
		484-Pin FineLine BGA Package	672-Pin FineLine BGA Package	1,020-Pin FineLine BGA Package
CLK0p/DIFFIO_RX_C0p	B2	L21	P25	T32
CLK0n/DIFFIO_RX_C0n	B2	L20	P24	T31
CLK10p/DIFFIO_RX_C3p	B2	L2	P2	T1
CLK10n/DIFFIO_RX_C3n	B2	L3	P3	T2

This ES device issue will be fixed in production devices. Therefore, Altera will not be characterizing this high current path across process, temperature, and voltage on the ES devices.

PORSEL Setting at 12 ms

When the `PORSEL` pin is connected to ground, the power-on reset (POR) delay time is set to 100 ms. When the `PORSEL` pin is connected to V_{CC} , the POR delay is 12 ms. If designers select the 12-ms POR delay, the V_{CCINT} supply must ramp up to 1.2 V within 12 ms. Failure to ramp up within 12ms may cause configuration failure.

If designers select the 100-ms POR delay, the V_{CCINT} supply must ramp up within 100 ms (the maximum V_{CC} rise time as specified in the *Stratix II Device Family Data Sheet*). The production devices support the maximum V_{CC} rise time of 100 ms for both `PORSEL` pin settings.

Differences Between EP2S60 ES & Production Devices

In addition to the silicon issue fixes described in the previous section, the EP2S60 production devices have additional differences from the ES silicon. The differences include the addition of on-chip series termination calibration circuitry, a slight difference in pad order, and different JTAG IDCODE values.



The pin tables for EP2S60 ES and production devices are different because of the differences in the two devices. Designers should make sure to use the appropriate pin table.

On-Chip Series Termination Calibration Circuitry

The production EP2S60 devices contain the on-chip series termination calibration circuitry, while the EP2S60 ES devices do not have this calibration circuitry. Therefore, the production pin table contains the additional dual-purpose calibration reference pins, `RUP` and `RDN`, while the ES pin table does not contain these dual-purpose pins.

If designers plan to replace EP2S60 ES devices with production devices to take advantage of the calibration circuitry, Altera recommends that designers reserve the `RUP` and `RDN` pins and place external pull-up and pull-down resistors on these reference pins when designing with the EP2S60 ES device. This eliminates the need to re-spin the board when changing from ES to production silicon. The pin numbers of the `RUP` and `RDN` pins can be found in the pin tables on www.altera.com. All other Stratix II devices support on-chip series termination with calibration in both ES and production offerings.

Pad Order

The difference between the EP2S60ES and production devices pin tables is that the RUP and RDN signals were added as secondary functions on certain I/O pins in the production pin table. This change also affected the pad order. Therefore, if you plan to migrate from the ES device to the production device, you need to turn on this migration path within the Quartus II software. The Quartus II software corrects any pin placement violations due to the current density restriction of 250 mA across any consecutive 10 pads across both devices (See the *Selectable I/O Standards in Stratix II and Stratix II Gx Devices* chapter of Volume 2 of the *Stratix II Device Handbook*). There are no differences in the pin numbering between the ES and production devices.

To assure this slight difference in pad order is not overlooked, when a user selects the ES device, the Quartus II compiler issues a warning to turn on device migration to the production device in the Quartus II software version 4.1 SP1 and later.

To turn on migration, click **Device** from the Assignments menu in the Quartus II software. Select the appropriate EP2S60 ES device and click the **Migration Devices** button. Select the appropriate production device.



Due to the difference in pad order and the different IDCODE values, EP2S60 ES and production devices require different BSDL files.

32-Bit Device IDCODE

Table 9 shows the 32-bit IDCODE values for the EP2S60 ES and production devices. The 4-bit version number was incremented from '0000' to '0001' for the production devices.

Device	IDCODE (32-Bit)			
	Version (4-Bits)	Part Number (16-Bits)	Manufacturer Identity (11-Bits)	LSB (1-Bit)
EP2S60 ES	0000	0010 0000 1001 0011	000 0110 1110	1
EP2S60 Production	0001	0010 0000 1001 0011	000 0110 1110	1



Due to the IDCODE difference and the difference in pad order, the EP2S60 ES and production devices require different BSDL files.

Revision History

Table 10 shows the revision history for this document.

Table 10. Document Revision History (Part 1 of 2)		
Date and Revision	Changes Made	Summary of Changes
October 2008, v. 2.1	<ul style="list-style-type: none"> Updated Table 1. Updated "PLL Reconfiguration Issue" and "Revision History" sections. Added Table 10. 	—
January 2007, v. 2.0	<ul style="list-style-type: none"> Updated Table 1. Updated "Stratix II FPGA Device Family Issues" on page 3. Updated "PLL Reconfiguration Issue" on page 3. Updated "Stratix II PLL Self-Reset Support Removed" on page 5. 	—
December 2006, v. 1.9	<ul style="list-style-type: none"> Updated Table 1. Added "1.2-V HSTL Support Issue" on page 5. 	—
April 2006, v. 1.8	<ul style="list-style-type: none"> Updated Table 1. Added "M-RAM Byte Enable Support for x128 and x144 Modes" on page 6. Updated "M4K Intermittent Read Failure in Dual-Port Mode with Dual Clocks" on page 6. 	—
December 2005, v. 1.7	<ul style="list-style-type: none"> Updated Table 1. Updated "M-RAM Block Read & Write Issue" on page 8. 	—
October 2005, v. 1.6	<ul style="list-style-type: none"> Updated Table 1. Added "M4K Intermittent Read Failure in Dual-Port Mode with Dual Clocks" on page 6. 	—
September 2005, v. 1.5	<ul style="list-style-type: none"> Updated Table 1. Added CRC Error Detection Maximum Frequency is 50 MHz section. Updated Column Clock Pins Do Not Support HyperTransport Technology section. 	—

Table 10. Document Revision History (Part 2 of 2)

Date and Revision	Changes Made	Summary of Changes
June 2005, v. 1.4	<ul style="list-style-type: none"> ● Added Column Clock Pins Do Not Meet LVDS Specifications section. ● Added Column Clock Pins Do Not Support HyperTransport Technology section. ● Added Stratix II FPGA Device Family Issues section. ● Updated information on Stratix II M-RAM software support. 	—
January 2005, v. 1.3	<ul style="list-style-type: none"> ● Added information on EP2S60 ES versus production devices. ● Updated information on Stratix II M-RAM issues and software support. 	—
August 2004, v. 1.2	<ul style="list-style-type: none"> ● Added information on Stratix II M-RAM issues and software support. 	—
July 2004, v. 1.1	<ul style="list-style-type: none"> ● Added information on the PORSEL setting at 12 ms. ● Added information on the configuration file differences between EP2S60 ES devices and EP2S60 production devices. 	—



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