Errata Sheet for Arria V GZ Devices

This errata sheet provides information about known device issues affecting Arria® V GZ production devices.

Production Device Issues for Arria V GZ Devices

Table 1 lists the issues and the affected Arria V GZ production devices.

Table 1. Arria V GZ Production Device Issues (Part 1 of 2)

Issue	Affected Devices	Planned Fix
"PCIe Gen2 Link Training Error When Using Hard Reset Controller"	All Arria V GZ production devices	Software will default to Soft Reset Controller in Quartus II version 13.1.
"Production Device Supply Voltage Requirements"	All Arria V GZ production devices	None
"LVDS Soft-CDR and DPA Modes" LVDS receivers in Soft-CDR or DPA mode operating between 650 Mbps to 1.22 Gbps include usage restrictions.	All Arria V GZ production devices	None
"Partial Reconfiguration (PR) with Compression Not Supported in Configuration via Protocol (CvP) when Encryption Disabled" The PR with compression feature is not supported when CvP is enabled and encryption is disabled. There is no restriction when CvP is disabled.	All Arria V GZ production devices	None
"Receiver Detect Issue in the PCIe Hard IP" The Link Training and Status State Machine (LTSSM) in the PCIe Hard IP may become stuck in the Detect.Active state after sending the `TXDetectRX` pulse.	All Arria V GZ production devices	None
"Unused Transmitter Clock Line Speed Degradation" Transceiver clock network (x1, x6, xN) performance can degrade 10% over a period of 5 years of inactivity if the devices are powered up to normal operating conditions.	All Arria V GZ production devices	Pending
"M20K Initialization in Partial Reconfiguration" M20Ks cannot be configured as ROMs or initialized RAMs using partial reconfiguration.	All Arria V GZ production devices	None

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Table 1. Arria V GZ Production Device Issues (Part 2 of 2)

Issue	Affected Devices	Planned Fix
"PCIe Configure Write Operation with Configure Retry Status (CRS) in CvP Mode" After a reset, Configuration Reads (CFGRD) must be issued until a non-CRS response is received from the PCIe core before issuing any Configuration Writes (CFGWR). This issue only affects CvP mode.	All Arria V GZ production devices	None
"JTAG Programming of 28-nm Devices"	All Arria V GZ production devices	None

PCIe Gen2 Link Training Error When Using Hard Reset Controller

An intermittent PCIe Gen2 Hard IP link-up issue may occur in Quartus II version 13.0SP1 and earlier.

When using the hard reset controller in a Gen2 native configuration, the Arria V GZ Hard IP for PCI Express MegaCore function may incorrectly transmit at 5 Gbps instead of the 2.5 Gbps data rate during link training.

Workaround

For Gen2 configurations that do not use Configuration via Protocol (CvP), follow the instructions in the Knowledge Base Solution for a workaround. For CvP Gen2 configurations, contact mySupport.

Production Device Supply Voltage Requirements

Partial Reconfiguration (PR) Power Supply Requirement

For information about speed grade and power supply requirements, contact mySupport.

LVDS Soft-CDR and DPA Modes

LVDS receivers in Soft-CDR or DPA mode operating between 650 Mbps to 1.22 Gbps include usage restrictions.

☞ For additional information, contact mySupport.

Partial Reconfiguration (PR) with Compression Not Supported in Configuration via Protocol (CvP) when Encryption Disabled

Table 2 shows the support of PR with CvP in different combinations of compression and encryption features.

Table 2. Partial Reconfiguration Support

Compression with PR	Encryption with PR	CvP mode	Support
OFF	OFF	ON	YES
OFF	ON	ON	YES

Table 2. Partial Reconfiguration Support

Compression with PR	Encryption with PR	CvP mode	Support
ON	OFF	ON	NO
ON	ON	ON	YES

There is no restriction when CvP is **Disabled**. For additional inquiries, contact mySupport.

Receiver Detect Issue in the PCIe Hard IP

The Link Training and Status State Machine (LTSSM) in the PCIe Hard IP may become stuck in the Detect.Active state after sending the `TXDetectRX` pulse. This issue may impact your system only if one of the following PCIe Gen1/Gen2 modes is used:

- Autonomous Hard IP
- Configuration via Protocol using PCIe (CvP) **Init mode** only

The CvP update mode is not affected. Other PCIe modes are not impacted by this issue. Contact mySupport. if you are using an affected device.

Unused Transmitter Clock Line Speed Degradation

Unused or idle clock dividers of the transceiver can degrade if the devices are powered up to normal operating conditions. This can result in a clock performance degradation of 10% over a period of 5 years. This issue affects designs that will enable unused clock dividers through a new configuration file at a later date. Active clock dividers are not impacted. Non-transceiver circuits are not impacted by this performance degradation.

Guidelines for Eliminating Performance Degradation

1. For unused channels, apply one of the following:
   a. Recompile with Quartus II software, version 12.1 or later to power down the unused clock dividers.
   b. For designs using Quartus II versions before 12.1, instantiate currently unused transceiver channels that may be enabled with a future programming file. This will create activity on currently unused channels.
2. For used (configured) channels, apply the following:

   For any version of the Quartus II software, do not assert the PLL and analog reset signals indefinitely.

M20K Initialization in Partial Reconfiguration

M20Ks cannot be configured as ROMs or initialized RAMs using partial reconfiguration (PR). Use MLABs as a workaround.

PCIe Configure Write Operation with Configure Retry Status (CRS) in CvP Mode

After a reset (fundamental or FLR), the core will respond to Configuration (CFG) requests with a CRS until the soft logic is ready for normal operation. In the case of Configuration Writes (CFGWR), the core will respond with a CRS, but it will still execute the register write. Therefore, after a reset, Configuration Reads (CFGRD) must be issued until a non-CRS response is received from the PCIe core before issuing any CFGWR. This issue only affects CvP mode.

JTAG Programming of 28-nm Devices

JTAG configuration of 28-nm devices does not operate correctly when you initiate a `PAUSE_DR` instruction during configuration. In this scenario, JTAG configuration fails when pausing configuration in the middle of the bit stream by entering into the PAUSE-DR state and continuing to clock the TCK input. The failure is indicated by `CONF_DONE` staying low after all of the data has been clocked into the FPGA while `nSTATUS` remains high.

The PAUSE-DR feature works correctly with normal IEEE 1149.1 JTAG test operations.

Workaround

If you require pausing in the middle of the bit stream during JTAG configuration, halt the TCK and do not enter the PAUSE-DR state. Restart the TCK when you resume the configuration.

Document Revision History

Table 3 lists the revision history for this errata sheet.

Table 3. Document Revision History

Date	Version	Changes
May 2017	1.2	Added the “JTAG Programming of 28-nm Devices” section.
December 2013	1.1	Added the “PCIe Gen2 Link Training Error When Using Hard Reset Controller” section.
October 2013	1.0	Added “Production Device Supply Voltage Requirements” Added “LVDS Soft-CDR and DPA Modes” Updated “Partial Reconfiguration (PR) with Compression Not Supported in Configuration via Protocol (CvP) when Encryption Disabled” Updated “Receiver Detect Issue in the PCIe Hard IP” Updated “Unused Transmitter Clock Line Speed Degradation” Updated “M20K Initialization in Partial Reconfiguration” Updated “PCIe Configure Write Operation with Configure Retry Status (CRS) in CvP Mode”
December 2012	0.1	Preliminary draft.