1. About this Document

This document lists known device errata for Intel® Stratix® 10 DX production devices.
# 2. Device Errata Summary

This section lists the errata that apply to the Intel Stratix 10 DX devices. Each listed erratum has an associated status that identifies any planned fixes.

<table>
<thead>
<tr>
<th>Table 1. Device Issues</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Issue</strong></td>
</tr>
<tr>
<td>FPGA</td>
</tr>
<tr>
<td>P-Tile</td>
</tr>
<tr>
<td>Root Port Legacy Interrupt Status register INTx is stuck HIGH on page 5</td>
</tr>
<tr>
<td>TLP Bypass Error Status Register may Report Receiver Errors on page 6</td>
</tr>
<tr>
<td>PCIe CV and PTC Tests in the PCI-SIG Compliance Test Suite may Fail on page 7</td>
</tr>
<tr>
<td>Returning Incorrect Function Number on page 8</td>
</tr>
<tr>
<td>Incorrect Return Value for Power Management Register on page 9</td>
</tr>
<tr>
<td>Register Implementation while using the Multi-function and SR-IOV Features on page 10</td>
</tr>
</tbody>
</table>
2.1. FPGA

2.1.1. P-Tile

2.1.1.1. Root Port Legacy Interrupt Status register INTx is stuck HIGH

Description

During root port implementation in the Intel FPGA P-Tile Hard IP for PCIe, the Root Port Legacy Interrupt status register INT_status of the port configuration and status register space (address: 0x10414C[3:0]) is stuck HIGH (it can be any bit of INT_status) when the AssertINTx message is received but the DeassertINTx is not received. This may occur when a warm reset or PERST is issued before the endpoint sends the DeassertINTx message. As a result, the root port interrupt handling does not operate correctly.

Subsequent warm reset or PERST does not clear the stuck interrupt bits.

Impacted Modes

- Intel FPGA P-Tile Avalon® Streaming Interface Hard IP for PCIe in Root Port mode

Workaround

When using the Intel FPGA P-Tile Hard IP for PCIe in root port mode, Intel recommends you to use the MSI/MSI-X interrupt messages.

To avoid this event when using the Root Port Legacy Interrupt, ensure that an AssertINTx message is followed by a DeassertINTx message before a warm reset or PERST is issued. Otherwise, to clear the stuck interrupt bits, you must re-program the device.

Status

Affects:

- Intel Stratix 10 DX 2800
- Intel Stratix 10 DX 2100
- Intel Stratix 10 DX 1100

Status: No planned fix.
2.1.1.2. TLP Bypass Error Status Register may Report Receiver Errors

**Description**

During the TLP Bypass implementation using the Intel FPGA P-Tile Avalon Streaming Interface Hard IP for PCIe, the `tlpbypass_err_status` register of port configuration and status registers (address: 0x104190[8]) may report receiver errors after the PERST is released. Therefore, if the user logic implements the Advanced Error Reporting (AER) capability based on the `tlpbypass_err_status` register, the correctable error status register of the AER capability indicates receiver errors.

**Impacted Modes**

- Intel FPGA P-Tile Avalon Streaming Interface Hard IP for PCIe in TLP Bypass mode

**Workaround**

While using the Intel FPGA P-Tile Avalon Streaming Interface Hard IP for PCIe, the user logic must clear the `tlpbypass_err_status` register’s receiver error status bit (0x104190[8]) of the port configuration and status registers before the PERST is released.

**Status**

Affects:
- Intel Stratix 10 DX 2800
- Intel Stratix 10 DX 2100
- Intel Stratix 10 DX 1100

Status: No planned fix.
2.1.1.3. PCIe CV and PTC Tests in the PCI-SIG Compliance Test Suite may Fail

Description
While using the Intel FPGA P-Tile Hard IP for PCIe, the following PCIe Configuration Verifier (CV) and Protocol Test Card (PTC) tests in the PCI-SIG Compliance Test Suite may fail:

• TD_1_4
• TD_1_7
• TD_1_13
• TD_1_27
• TD_1_73
• Link Layer Transaction test (Data Link Feature Exchange)

Note: The current Intel Quartus Prime Pro Edition software version does not enable every feature that is required to demonstrate compliance.

Impacted Modes
• Intel FPGA P-Tile Avalon Streaming Interface Hard IP for PCIe in Endpoint mode
• Intel FPGA P-Tile Avalon Memory-Mapped Interface IP for PCIe in Endpoint mode

Workaround
None.

Status
Affects:
• Intel Stratix 10 DX 2800
• Intel Stratix 10 DX 2100
• Intel Stratix 10 DX 1100

2.1.1.4. Returning Incorrect Function Number

**Description**

While using the Intel FPGA P-Tile Hard IP for PCIe, the last Physical Function (PF) indicates incorrect next function number if the following conditions are true:

- Alternative Routing-ID Interpretation (ARI) capability is enabled
- Number of Physical Functions (PFs) is less than 8

The next function number incorrectly shows a value of PF+1. As a result, the correctable error status register in the Advanced Error Reporting (AER) capability structure of the root port may report a non-fatal error.

**Impacted Modes**

- Intel FPGA P-Tile Avalon Streaming Interface Hard IP for PCIe in Endpoint mode
- Intel FPGA P-Tile Avalon Memory-Mapped Interface IP for PCIe in Endpoint mode

**Workaround**

To avoid this issue, the user logic must use the Configuration Intercept Interface (CII) to override the read data for the next function number when the above conditions are true.

The user logic must clear the correctable error status register of the AER capability using the Hard IP Reconfiguration interface.

**Status**

Affects:

- Intel Stratix 10 DX 2800
- Intel Stratix 10 DX 2100
- Intel Stratix 10 DX 1100

Status: No planned fix.
2.1.1.5. Incorrect Return Value for Power Management Register

**Description**
While using the Intel FPGA P-Tile Hard IP for PCIe, the Power Management Control and Status Register (offset 0x04Ch bit [3]: No_Soft_Reset) returns a value of 1'b0 instead of value of 1'b1. As a result, the software expects the Intel FPGA P-Tile Hard IP for PCIe to reset the configuration space during transition from D3HOT state to D0 state.

**Impacted Modes**
- Intel FPGA P-Tile Avalon Streaming Interface Hard IP for PCIe in Endpoint, Root Port, and TLP Bypass modes
- Intel FPGA P-Tile Avalon Memory-Mapped Interface IP for PCIe in Endpoint and Root Port modes

**Workaround**
None.

**Status**
Affects:
- Intel Stratix 10 DX 2800
- Intel Stratix 10 DX 2100
- Intel Stratix 10 DX 1100

2.1.1.6. Register Implementation while using the Multi-function and SR-IOV Features

Description

While using the Intel FPGA P-Tile Hard IP for PCIe:

- When the SR-IOV feature is enabled:
  - The PCIe capability link status register (offset 0x082h bits [15:0]) returns the parent PF link status register values when accessed by virtual functions. According to the PCIe Base specification revision 4.0 version 1.0, when SR-IOV feature is enabled, this register must be implemented as Reserved and Zero (RsvdZ) and accessed by virtual functions.
  - The PCIe device control2 register (offset 0x098h bit [12]: 10-bit tag requested enable bit) returns the parent PF device control2 register values when accessed by virtual functions. According to the PCIe Base specification revision 4.0 version 1.0, when SR-IOV feature is enabled, this register must be implemented as Reserved and Preserved (RsvdP) and accessed by virtual functions.
  - The PCIe Address Translation Service (ATS) control register (ATS base address + offset 0x006h bit [4:0]: smallest translation unit (STU) bits) is implemented as read-only (RO) register but returns the value of the parent PF when accessed by virtual functions. According to the PCIe Base specification revision 4.0 version 1.0, this register must be implemented as a read-only (RO) register and hard-wired to 0 when accessed by virtual functions.

- When the multi-function feature is enabled:
  - the PCIe device status register (offset 0x07Ah bit [5]: Transactions pending bit) is implemented as a Write-1-to-Clear status register (RW1C). According to the PCIe Base specification revision 4.0 version 1.0, this register must be implemented as read-only (RO) when multi-function feature is enabled.

These issues do not cause functional failure.

Impacted Modes

- Intel FPGA P-Tile Avalon Streaming Interface Hard IP for PCIe in Endpoint mode
- Intel FPGA P-Tile Avalon Memory-Mapped Interface IP for PCIe in Endpoint mode

Workaround

Your logic must use the Configuration Intercept Interface (CII) to modify the configuration accesses to these registers.

Status

Affects:

- Intel Stratix 10 DX 2800
- Intel Stratix 10 DX 2100
- Intel Stratix 10 DX 1100

# 3. Intel Stratix 10 DX Device Errata Revision History

<table>
<thead>
<tr>
<th>Document Version</th>
<th>Changes</th>
</tr>
</thead>
<tbody>
<tr>
<td>2020.05.06</td>
<td>Corrected the offset value for PCIe ATS control register in Register Implementation while using the Multi-function and SR-IOV Features on page 10.</td>
</tr>
<tr>
<td>2020.04.08</td>
<td>Removed the following erratum:</td>
</tr>
<tr>
<td></td>
<td>• Lecroy LTSSM Arc Test may fail</td>
</tr>
<tr>
<td></td>
<td>• Access Control Service Support for Root Port</td>
</tr>
<tr>
<td>2020.02.05</td>
<td>Initial release.</td>
</tr>
</tbody>
</table>