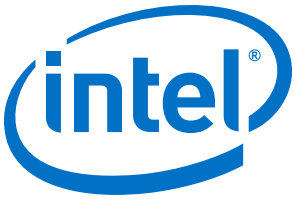

Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs Version 1.2 Errata

Updated for Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs: **1.2**

ES-1067 | 2018.12.04
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Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs Version 1.2 Errata

This document provides information about errata affecting the Intel® Acceleration Stack for Intel Xeon® CPU with FPGAs.

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The table below can be used as a reference to identify the FPGA Interface Manager (FIM), Open Programmable Acceleration Engine (OPAE) and Intel Quartus® Prime Pro Edition version that corresponds to your software stack release.

Table 1. Intel Acceleration Stack Reference Table

Note: When the image in the user partition cannot be loaded, a flash failover occurs and the factory image is loaded instead. After a flash failover occurs, the PR ID reads as d4a76277-07da-528d-b623-8b9301feaffe.

Intel Acceleration Stack Version	Platform	FPGA Interface Manager (FIM) Version: Partial Reconfiguration (PR) Interface ID	Open Programmable Acceleration Engine (OPAE) Version	Intel Quartus Prime Pro Edition
1.2	Intel PAC with Intel Arria® 10 GX FPGA	69528db6-eb31-577a-8c36-68f9faa081f6	1.1.2	17.1.1
1.1	Intel PAC with Intel Arria 10 GX FPGA	9926ab6d-6c92-5a68-aabc-a7d84c545738	1.0.2	17.1.1
1.0	Intel PAC with Intel Arria 10 GX FPGA	ce489693-98f0-5f33-946d-560708be108a	0.13.1	17.0.0

Flash Fallback Does Not Meet PCIe Timeout

Description

The host may hang or report a PCIe failure after a flash failover has occurred. This issue can be seen when the user image in flash is corrupted and the configuration subsystem loads the factory image into the FPGA.

Workaround

Follow the instructions in the *Updating Flash Using the Intel Quartus Prime Pro Edition Programmer* section in the *Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA*. If the issue persists, contact your local field representative.

Status

No planned fix

Related Information

Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA

Unsupported Transaction Layer Packet Types

Description

The Acceleration Stack FPGA Interface Manager (FIM) does not support PCIe* Memory Read Lock, Configuration Read Type 1, and Configuration Write Type 1 transaction layer packets (TLPs). If the device receives a PCIe packet of this type, it does not respond with a Completion packet as expected.

Workaround

No workaround available.

Status

No planned fix

`fpgainfo errors -c` Does Not Clear the Error Response When Non-Fatal Errors Occur

Description

If an fpga non-fatal errors occurs, `fpgainfo errors fme -b 0x5e` displays the error on bus 0x5e. If you attempt to clear the error by using `fpgainfo errors -c all -b 0x5e`, it does not clear.

Workaround

To clear the error, type: `ras <BDF> -c`

Status

No planned fix

Board management controller does not verify the CRC in a PLDM request.

Description

The board management controller responds to PLDM packets that have an incorrect CRC value.

Workaround

No workaround available.

Status

No planned fix

The 1.2 V current and 1.8 V voltage upper non-recoverable (UNR) limits for the board management controller and the pacd are set to the same value.

Description

Because the 1.2 V current and 1.8 V voltage upper non-recoverable (UNR) limits for the board management controller and the pacd are the same, the board management controller may shutdown before pacd can perform graceful shutdown. The possibility of encountering this issue is low.

Workaround

No workaround available.

Status

No planned fix

Intel Acceleration Stack for Intel Xeon CPU with FPGAs v1.2 Errata Revision History

Date	Intel Acceleration Stack Version	Changes
2018.12.04	1.2 (compatible with Intel Quartus Prime Pro Edition 17.1.1)	Initial release.