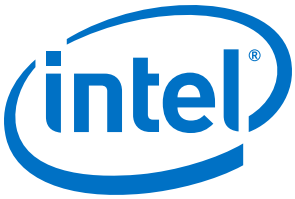

Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs 1.1 Errata

Updated for Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs: **1.1 Production**

ES-1065 | 2018.08.06
Latest document on the web: PDF | HTML

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Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs 1.1 Errata

This document provides information about errata affecting the Intel® Acceleration Stack for Intel Xeon® CPU with FPGAs.

Issue	Affected Versions	Planned Fix
Flash Fallback Does Not Meet PCIe Timeout on page 4	Acceleration Stack 1.0 Production and 1.1 Production	No Planned Fix
Unsupported Transaction Layer Packet Types on page 5	Acceleration Stack 1.0 Production and 1.1 Production	No Planned Fix

The table below can be used as a reference to identify the FPGA Interface Manager (FIM), Open Programmable Acceleration Engine (OPAE) and Intel Quartus® Prime Pro Edition version that corresponds to your software stack release.

Table 1. Intel Acceleration Stack 1.1 Reference Table

Intel Acceleration Stack Version	Platform	FPGA Interface Manager (FIM) Version: Partial Reconfiguration (PR) Interface ID	Open Programmable Acceleration Engine (OPAE) Version	Intel Quartus Prime Pro Edition
1.1 Production(1)	Intel PAC with Intel Arria® 10 GX FPGA	9926ab6d-6c92-5a68-aabc-a7d84c545738	1.0.2	17.1.1
1.1 Beta	Intel PAC with Intel Arria 10 GX FPGA	0f17997f-199b-5f75-9713-2653d3ce0176	1.0.1	17.1.1
1.1 Alpha	Intel PAC with Intel Arria 10 GX FPGA	8fd6574f-8f82-5164-9336-69c4bdaba437	0.14.0	17.1.1
1.0 Production(1)	Intel PAC with Intel Arria 10 GX FPGA	ce489693-98f0-5f33-946d-560708be108a	0.13.1	17.0.0

(1) When the image in the user partition cannot be loaded, a flash failover occurs and the factory image is loaded instead. After a flash failover occurs, the PR ID reads as d4a76277-07da-528d-b623-8b9301feaffe.

Flash Fallback Does Not Meet PCIe Timeout

Description

The host may hang or report a PCIe failure after a flash failover has occurred. This issue can be seen when the user image in flash is corrupted and the configuration subsystem loads the factory image into the FPGA.

Workaround

Follow the instructions in the *Updating Flash Using the Intel Quartus Prime Pro Edition Programmer* section in the *Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA*. If the issue persists, contact your local field representative.

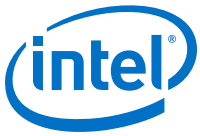
Status

Affects: Intel Acceleration Stack 1.0 Production and 1.1 Production

Status: No planned fix

Related Information

Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA



Unsupported Transaction Layer Packet Types

Description

The Acceleration Stack FPGA Interface Manager (FIM) does not support PCIe* Memory Read Lock, Configuration Read Type 1, and Configuration Write Type 1 transaction layer packets (TLPs). If the device receives a PCIe packet of this type, it does not respond with a Completion packet as expected.

Workaround

No workaround available.

Status

Affects: Intel Acceleration Stack 1.0 Production and 1.1 Production

Status: No planned fix

Intel Acceleration Stack for Intel Xeon CPU with FPGAs 1.1 Errata Revision History

Date	Intel Acceleration Stack Version	Changes
2018.08.06	1.1 Production (compatible with Intel Quartus Prime Pro Edition 17.1.1)	Initial release.