Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs 1.1 Errata

Updated for Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs: 1.1 Production
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Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs 1.1 Errata

This document provides information about errata affecting the Intel® Acceleration Stack for Intel Xeon® CPU with FPGAs.

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The table below can be used as a reference to identify the FPGA Interface Manager (FIM), Open Programmable Acceleration Engine (OPAE) and Intel Quartus® Prime Pro Edition version that corresponds to your software stack release.

Table 1. Intel Acceleration Stack 1.1 Reference Table

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<td>1.1 Production (1)</td>
<td>Intel PAC with Intel Arria® 10 GX FPGA</td>
<td>9926ab6d-6c92-5a68-aabc-a7d84c545738</td>
<td>1.0.2</td>
<td>17.1.1</td>
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<tr>
<td>1.1 Beta</td>
<td>Intel PAC with Intel Arria 10 GX FPGA</td>
<td>0f17997f-199b-5f75-9f73-2653d3ce0176</td>
<td>1.0.1</td>
<td>17.1.1</td>
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<tr>
<td>1.1 Alpha</td>
<td>Intel PAC with Intel Arria 10 GX FPGA</td>
<td>8fd6574f-8f82-5164-9336-69c4bda4b37</td>
<td>0.14.0</td>
<td>17.1.1</td>
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<tr>
<td>1.0 Production (1)</td>
<td>Intel PAC with Intel Arria 10 GX FPGA</td>
<td>cc489693-98f0-5f33-946d-560708be108a</td>
<td>0.13.1</td>
<td>17.0.0</td>
</tr>
</tbody>
</table>

(1) When the image in the user partition cannot be loaded, a flash failover occurs and the factory image is loaded instead. After a flash failover occurs, the PR ID reads as d4a76277-07da-528d-b623-8b9301feaffe.
Flash Fallback Does Not Meet PCIe Timeout

**Description**

The host may hang or report a PCIe failure after a flash failover has occurred. This issue can be seen when the user image in flash is corrupted and the configuration subsystem loads the factory image into the FPGA.

**Workaround**

Follow the instructions in the *Updating Flash Using the Intel Quartus Prime Pro Edition Programmer* section in the *Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA*. If the issue persists, contact your local field representative.

**Status**

Affects: Intel Acceleration Stack 1.0 Production and 1.1 Production

Status: No planned fix

**Related Information**

*Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA*
Unsupported Transaction Layer Packet Types

**Description**

The Acceleration Stack FPGA Interface Manager (FIM) does not support PCIe* Memory Read Lock, Configuration Read Type 1, and Configuration Write Type 1 transaction layer packets (TLPs). If the device receives a PCIe packet of this type, it does not respond with a Completion packet as expected.

**Workaround**

No workaround available.

**Status**

Affects: Intel Acceleration Stack 1.0 Production and 1.1 Production

Status: No planned fix
## Intel Acceleration Stack for Intel Xeon CPU with FPGAs 1.1 Errata

### Revision History

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<thead>
<tr>
<th>Date</th>
<th>Intel Acceleration Stack Version</th>
<th>Changes</th>
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<tr>
<td>2018.08.06</td>
<td>1.1 Production (compatible with Intel Quartus Prime Pro Edition 17.1.1)</td>
<td>Initial release.</td>
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