Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs 1.0 Errata

Updated for Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs: 1.0 Production
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Intel® Acceleration Stack for Intel® Xeon® CPU with FPGAs 1.0 Errata

This document provides information about errata affecting the Intel® Acceleration Stack for Intel Xeon® CPU with FPGAs.

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<td>No planned fix</td>
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The table below can be used as a reference to identify the FPGA Interface Manager (FIM), Open Programmable Acceleration Engine (OPAE) and Intel Quartus® Prime Pro Edition version that corresponds to your software stack release.

Table 1. Intel Acceleration Stack 1.0 Reference Table

<table>
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<tr>
<td>1.0 Production&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>Intel PAC with Intel Arria® 10 GX FPGA</td>
<td>ce489693-98f0-5f33-946d-560708be108a</td>
<td>0.13.1</td>
<td>17.0.0</td>
</tr>
</tbody>
</table>

Related Information

Intel Acceleration Stack for Intel Xeon CPU with FPGAs Release Notes
Refer to the release notes for more information about known issues and enhancements for Intel Acceleration Stack 1.0

<sup>(1)</sup> The factory partition of the configuration flash contains the Acceleration Stack 1.0 Alpha version. When the image in the user partition cannot be loaded, a flash failover occurs and the factory image is loaded instead. After a flash failover occurs, the PR ID reads as d4a76277-07da-528d-b623-8b9301feaff.

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Flash Fallback Does Not Meet PCIe Timeout

Description
The host may hang or report a PCIe failure after a flash failover has occurred. This issue can be seen when the user image in flash is corrupted and the configuration subsystem loads the factory image into the FPGA.

Workaround
Follow the instructions in the "Updating Flash with FPGA Interface Manager (FIM) Image using Intel Quartus Prime Programmer" section in the Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA. If the issue persists, contact your local field representative.

Status
Affects: Intel Acceleration Stack 1.0 Production
Status: No planned fix

Related Information
Intel Acceleration Stack Quick Start Guide for Intel Programmable Acceleration Card with Intel Arria 10 GX FPGA
Unsupported Transaction Layer Packet Types

**Description**

The Acceleration Stack FPGA Interface Manager (FIM) does not support PCIe* Memory Read Lock, Configuration Read Type 1, and Configuration Write Type 1 transaction layer packets (TLPs). If the device receives a PCIe packet of this type, it does not respond with a Completion packet as expected.

**Workaround**

No workaround available.

**Status**

Affects: Intel Acceleration Stack 1.0 Production

Status: No planned fix
JTAG Timing Failures May Be Reported in the FPGA Interface Manager

Description
The Intel Quartus Prime Pro Edition Timing Analyzer may report unconstrained JTAG I/O paths in the FIM.

Workaround
These unconstrained paths can be safely ignored because the JTAG I/O paths are not used in the FIM.

Status
Affects: Intel Acceleration Stack 1.0 Production
Status: Planned fix in Intel Acceleration Stack 1.1
fpgabist Tool Does Not Pass Hexadecimal Bus Numbers Properly

Description

The Open Programmable Acceleration Engine (OPAE) fpgabist tool does not pass valid bus numbers if the PCIe bus number is any character above F. If any of these characters are included, you may encounter the following error message:

Running mode: nlb_3

Attempting Partial Reconfiguration:

invalid bus: d4

Failed to load gbs file: /home/lab/workspace/DCP/PRC/hw/samples/nlb_mode_3/bin/nlb_mode_3.gbs

Please try a different gbs

Workaround

Change /usr/bin/bist_common.py line 83 from

```python
    cmd = "{} -b {} -v "\".format('fpgaconf', bus_num, gbs_file)
```

to

```python
    cmd = "{} -b 0x{} -v "\".format('fpgaconf', bus_num, gbs_file)
```

Status

Affects: Intel Acceleration Stack 1.0 Production

Status: Planned fix in Intel Acceleration Stack 1.1
Possible Low dma_afu Bandwidth Due to memcpy Function

Description
fpgabist may report lower bandwidth for the dma_afu but not the native loopback 3 (NLB3) due to the use of the memcpy function in the dma_afu driver.

Workaround
You can workaround this erratum by removing memcpy from the dma_afu driver code and adding code to accept buffers from the user that have been pre-pinned. For use with OpenCL®, there is no current workaround.

Status
Affects: Intel Acceleration Stack 1.0 Beta and Production
Status: Planned fix in Intel Acceleration Stack 1.1
**regress.sh –r Option Does Not Work With dma_afu**

**Description**
When using the –r option with regress.sh, the script does not work with the dma_afu example. Using the –r option results in a fatal gcc error.

**Workaround**
Do not use the –r option when running the regress.sh script. Running the script without the –r option places the output simulation in $OPAE_LOC/ase/rtl_sim instead of a user-specified directory.

**Status**
Affects: Intel Acceleration Stack 1.0 Production

Status: No planned fix
### Intel Acceleration Stack for Intel Xeon CPU with FPGAs 1.0 Errata

#### Revision History

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<thead>
<tr>
<th>Date</th>
<th>Intel Acceleration Stack Version</th>
<th>Changes</th>
</tr>
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<tr>
<td>2018.06.22</td>
<td>1.0 Production (compatible with Intel Quartus Prime Pro Edition 17.0.0)</td>
<td>Updated the path of the <code>bist_common.py</code> file in the <code>fpgabist Tool Does Not Pass Hexadecimal Bus Numbers Properly</code> erratum.</td>
</tr>
<tr>
<td>2018.04.11</td>
<td>1.0 Production (compatible with Intel Quartus Prime Pro Edition 17.0.0)</td>
<td>Initial release.</td>
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